12-Bit, 1-GSPS Analog-to-Digital Converter

1 Features

- 1-GSPS sample rate
- 12-Bit resolution
- 2.1 GHz input bandwidth
- SFDR = 65 dBc at 1.2 GHz
- SNR = 57 dBFS at 1.2 GHZ
- 7 Clock cycle latency
- Interleave friendly: internal adjustments for gain, phase and offset
- 1.5 - 2 V_{PP} Differential input voltage, programmable
- LVDS-compatible outputs, 1 or 2 bus options
- Total power dissipation: 2.2 W
- On-chip analog buffer
- 100-pin ceramic nonconductive tie-bar package
- Military temperature range (–55°C to 125°C T_{case})
- Processed per internal QML class V assembly/test flow
- QML class V qualified, SMD 5962-09240

2 Applications

- Test and measurement instrumentation
- Ultra-wide band software-defined radio
- Data acquisition
- Power amplifier linearization
- Signal intelligence and jamming
- Radar
- Engineering Evaluation (/EM) Samples are Available (1)

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. no burn-in, etc.) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of -55°C to 125°C or operating life.

3 Description

The ADS5400 is a 12-bit, 1-GSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs. The analog input buffer isolates the internal switching of the track and hold from disturbing the signal source. The simple 3-stage pipeline provides extremely low latency for time critical applications. Designed for the conversion of signals up to 2 GHz of input frequency at 1 GSPS, the ADS5400 has outstanding low noise performance and spurious-free dynamic range over a large input frequency range.

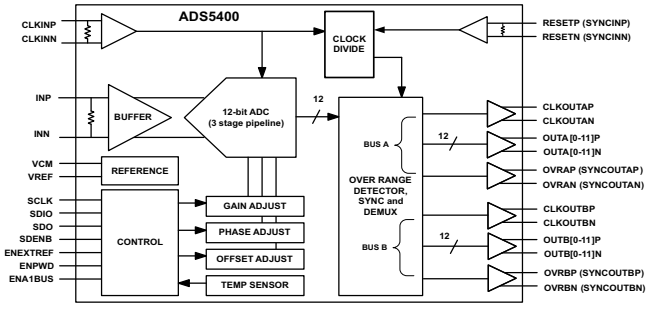
The ADS5400 is available in a 100-Pin Ceramic Nonconductive Tie-Bar Package. The combination of the ceramic package and moderate power consumption of the ADS5400 allows for operation without an external heatsink. The ADS5400 is built on Texas Instrument's complementary bipolar process (BiCom3) and is specified over the full military temperature range (–55°C to 125°C T_{case}).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS5400-SP	HSF (100)	19.05 mm x 19.05 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2014) to Revision E **Page**

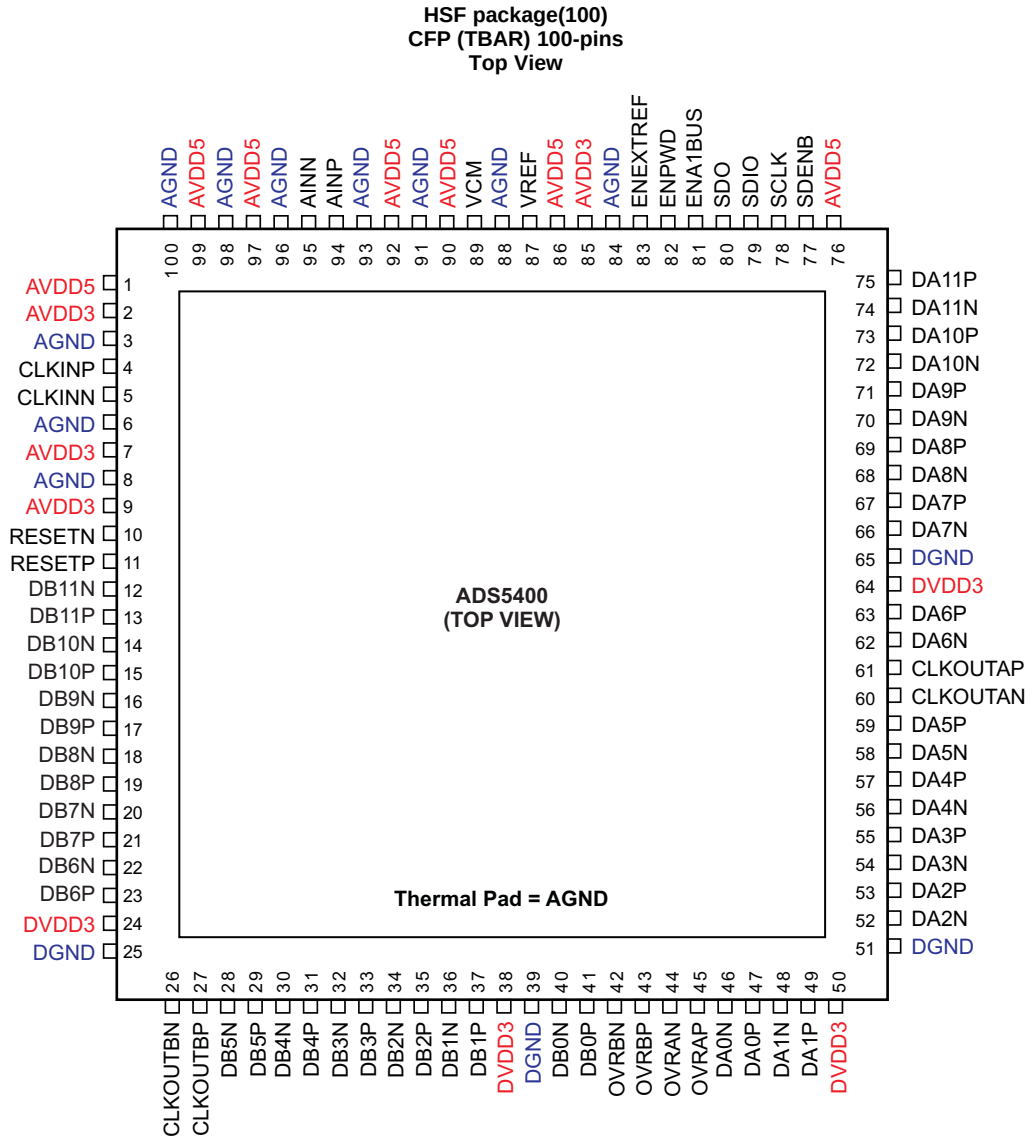
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added table note 1 to the *Recommended Operating Conditions* ... 6
- Changed the *Thermal Information* table ... 6
- Changed the *Layout* section ... 45

Changes from Revision C (August 2012) to Revision D **Page**

- Added /EM bullet to *Features* ... 1
- Deleted PACKAGE/ORDERING INFORMATION table ... 1

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5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AINP, AINN	94, 95	Analog differential input signal (positive, negative). Includes 100-Ω differential load on-chip.
AVDD5	1, 76, 86, 90, 92, 97, 99	Analog power supply (5 V)
AVDD3	2, 7, 9, 85	Analog power supply (3.3 V)
DVDD3	24, 38, 50, 64	Output driver power supply (3.3 V)
AGND	3, 6, 8, 84, 88, 91, 93, 96, 98, 100	Analog Ground
DGND	25, 39, 51, 65	Digital Ground
CLKINP, CLKINN	4, 5	Differential input clock (positive, negative). Includes 160-Ω differential load on-chip.
DA0N, DA0P	46, 47	Bus A, LVDS digital output pair, least-significant bit (LSB) (P = positive output, N = negative output)
DA1N–DA10N, DA1P-DA10P	48-49, 52-59, 62-63, 66-73	Bus A, LVDS digital output pairs (bits 1- 10)
DA11N, DA11P	74, 75	Bus A, LVDS digital output pair, most-significant bit (MSB)
CLKOUTAN, CLKOUTAP	60, 61	Bus A, Clock Output (Data ready), LVDS output pair
DB0N, DB0P	40, 41	Bus B, LVDS digital output pair, least-significant bit (LSB) (P = positive output, N = negative output)
DB1N–DB10N, DB1P-DB10P	14-23, 28-37	Bus B, LVDS digital output pairs (bits 1- 10)
DB11N, DB11P	12, 13	Bus B, LVDS digital output pair, most-significant bit (MSB)
CLKOUTBN, CLKOUTBP	26, 27	Bus B, Clock Output (Data ready), LVDS output pair
OVRAN, OVRAP	44, 45	Bus A, Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range. Becomes SYNCOUTA when SYNC mode is enabled in register 0x05.
OVRBN, OVRBP	42, 43	Bus B, Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range. Becomes SYNCOUTB when SYNC mode is enabled in register 0x05.
RESETN, RESETP	10, 11	Digital Reset Input, LVDS input pair. Inactive if logic low. When clocked in a high state, this is used for resetting the polarity of CLKOUT signal pair(s). If SYNC mode is enabled in register 0x05, this input also provides a SYNC time-stamp with the data sample present when RESET is clocked by the ADC, as well as CLKOUT polarity reset. Includes 100-Ω differential load on-chip.
SCLK	78	Serial interface clock.
SDIO	79	Bi-directional serial interface data in 3-pin mode (default) for programming/reading internal registers. In 4-pin interface mode (reg 0x01), the SDIO pin is an input only.
SDO	80	Uni-directional serial interface data in 4-pin mode (reg 0x01) provides internal register settings. The SDO pin is in high-impedance state in 3-pin interface mode (default).
SDENB	77	Active low serial data enable, always an input. Use to enable the serial interface. Internal 100kΩ pull-up resistor.
VREF	87	Reference voltage input (2V nominal). A 0.1μF capacitor to AGND is recommended, but not required.
ENA1BUS	81(1)	Enable single output bus mode (2-bus mode is default), active high. This pin is logic OR'd with addr 0x02h bit<0>.
ENPWD	82(1)	Enable Powerdown, active high. Places the converter into power-saving sleep mode when high. This pin is logic OR'd with addr 0x05h bit<6>.
ENEXTREF	83(1)	Enable External Reference Mode, active high. Device uses an external voltage reference when high. This pin is logic OR'd with addr 0x05h bit<2>.
VCM	89	Analog input common mode voltage, Output (for DC-coupled applications, nominally 2.5V). A 0.1μF capacitor to AGND is recommended, but not required.

(1) This pin contains an internal ~40kΩ pull-down resistor, to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
Supply voltage	AVDD5 to GND				6	V
	AVDD3 to GND				5	V
	DVDD3 to GND				5	V
	AINP, AINN to GND(2)	voltage difference between pin and ground		0.5	4.5	V
	AINP to AINN (2)	voltage difference between pins, common mode at AVDD5/2	short duration	–0.3	(AVDD5 + 0.3)	V
			continuous AC signal	1.25	3.75	V
			continuous DC signal	1.75	3.25	V
	CLKINP, CLKINN to GND (2)	voltage difference between pin and ground		0.5	4.5	V
	CLKINP to CLKINN (2)	voltage difference between pins, common mode at AVDD5/2	continuous AC signal	1.1	3.9	V
			continuous DC signal	2	3	V
	RESETP, RESETN to GND (2)	voltage difference between pin and ground		–0.3	(AVDD5 + 0.3)	V
	RESETP to RESETN (2)	voltage difference between pins	continuous AC signal	1.1	3.9	V
			continuous DC signal	2	3	V
	Data/OVR Outputs to GND (2)	voltage difference between pin and ground		–0.3	(DVDD3 + 0.3)	V
	SDENB, SDIO, SCLK to GND(2)			–0.3	(AVDD3 + 0.3)	
	ENA1BUS, ENPWD, ENEXTREF to GND(2)			–0.3	(AVDD5 + 0.3)	
Operating case temperature range				–55	125	°C
Maximum junction temperature, T_J					150	°C
Storage temperature range				–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. Kirkendall voidings and current density information for calculation of expected lifetime is available upon request.
(2) Valid when supplies are within recommended operating range.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
SUPPLIES					
	Analog supply voltage, AVDD5	4.75	5	5.25	V
	Analog supply voltage, AVDD3	3.135	3.3	3.465	V
	Digital supply voltage, DVDD3	3.135	3.3	3.465	V
ANALOG INPUT					
	Full-scale differential input range	1.52		2	V_{pp}
V_{CM}	Input common mode		AVDD5/2		V
DIGITAL OUTPUT					
	Differential output load			5	pF
CLOCK INPUT (1)					
	CLK input sample rate (sine wave)	100		1000	MSPS
	Clock amplitude, differential	0.6		1.5	V_{pp}
	Clock duty cycle	45%	50%	55%	
T_C	Operating case temperature	–55		125	°C

(1) Device is functional across the specified operating case temperature; however, electrical characteristics are only ensured at sampling rate = 1 GSPS.

6.4 Thermal Information

THERMAL METRIC(1)		ADS5400-SP HSF (CFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	14.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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6.5 Electrical Characteristics

Typical values at T_A = 25°C, minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
Analog Inputs						
	Full-scale differential input range	Programmable	1.52		2	V_{PP}
V_{CM}	Common-mode input	Self-biased to AVDD5 / 2		AVDD5/2		V
R_{IN}	Input resistance, differential (dc)			100		Ω
C_{IN}	Input capacitance	Estimated to ground from each AIN pin, excluding soldered package		4.3		pF
CMRR	Common-mode rejection ratio	Common mode signal = 125 MHz		40		dB
Internal Reference Voltage						
V_{REF}	Reference voltage		1.98	2	2.02	V
Dynamic Accuracy						
	Resolution	No missing codes	12			Bits
DNL	Differential linearity error	f_{IN} = 125 MHz	-1	±0.4	2.5	LSB
INL	Integral non- linearity error	f_{IN} = 125 MHz	-4.5	±1.5	4.5	LSB
	Offset error	default is trimmed near 0mV	–2.5	0	2.5	mV
	Offset temperature coefficient			0.02		mV/°C
	Gain error			±5		%FS
	Gain temperature coefficient			0.03		%FS/°C
Power Supply(1)						
$I_{(AVDD5)}$	5-V analog supply current (Bus A and B active)	f_{IN} = 125 MHz, f_S = 1 GSPS		220	245	mA
	5-V analog supply current (Bus A active)			225	255	mA
$I_{(AVDD3)}$	3.3-V analog supply current (Bus A and B active)			205	234	mA
	3.3-V analog supply current (Bus A active)			226	242	mA
$I_{(DVDD3)}$	3.3-V digital supply current (Bus A and B active)			136	154	mA
	3.3-V digital supply current (Bus A active)			72	85	mA
	Total power dissipation (BUS A and B active)			2.2	2.5	W
	Total power dissipation (Bus A active)			2	2.3	W
	Total power dissipation	ENPWD = logic High (sleep enabled)		13	50	mW
	Wake-up time from sleep			1.8		ms
PSRR	Power-supply rejection ratio	1MHz injected to each supply, measured without external decoupling		50		dB
Dynamic AC Characteristics						
SNR	Signal-to-noise ratio	f_{IN} = 125 MHz	54	58.5		dBFS
		f_{IN} = 600 MHz	53.5	58.3		
		f_{IN} = 850 MHz	53	58		
		f_{IN} = 1200 MHz		57.6		
		f_{IN} = 1700 MHz		55.7		

(1) All power values assume LVDS output current is set to 3.5 mA.

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Electrical Characteristics (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	f_{IN} = 125 MHz	62	72		dBc
		f_{IN} = 600 MHz	60	70		
		f_{IN} = 850 MHz	56	62.7		
		f_{IN} = 1200 MHz		65.7		
		f_{IN} = 1700 MHz		56		
HD2	Second harmonic	f_{IN} = 125 MHz	62	78		dBc
		f_{IN} = 600 MHz	60	75		
		f_{IN} = 850 MHz	56	62.5		
		f_{IN} = 1200 MHz		66		
		f_{IN} = 1700 MHz		56		
HD3	Third harmonic	f_{IN} = 125 MHz	62	78		dBc
		f_{IN} = 600 MHz	60	72		
		f_{IN} = 850 MHz	56	75		
		f_{IN} = 1200 MHz		70		
		f_{IN} = 1700 MHz		63		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 125 MHz	62	80		dBc
		f_{IN} = 600 MHz	60	79		
		f_{IN} = 850 MHz	56	79		
		f_{IN} = 1200 MHz		66		
		f_{IN} = 1700 MHz		64		
THD	Total Harmonic Distortion	f_{IN} = 125 MHz	60	71.7		dBc
		f_{IN} = 600 MHz	58	67		
		f_{IN} = 850 MHz	55	66.5		
		f_{IN} = 1200 MHz		63.8		
		f_{IN} = 1700 MHz		55.7		
SINAD	Signal-to-noise and distortion	f_{IN} = 125 MHz	53	57		dBFS
		f_{IN} = 600 MHz	52.4	56.8		
		f_{IN} = 850 MHz	50.8	55.8		
		f_{IN} = 1200 MHz		56.6		
		f_{IN} = 1700 MHz		52.7		
	Two-tone SFDR	f_{IN1} = 247.5 MHz, f_{IN2} = 252.5 MHz, each tone at –7 dBFS		74.6		dBFS
		f_{IN1} = 247.5 MHz, f_{IN2} = 252.5 MHz, each tone at –11 dBFS		77.9		
		f_{IN1} = 1197.5 MHz, f_{IN2} = 1202.5 MHz, each tone at –7 dBFS		68.3		
		f_{IN1} = 1197.5 MHz, f_{IN2} = 1202.5 MHz, each tone at –11 dBFS		73.7		
ENOB	Effective number of bits (using SINAD in dBFS)	f_{IN} = 125 MHz	8.52	9.55		Bits
		f_{IN} = 600 MHz	8.42	9.29		
		f_{IN} = 850 MHz	8.16	9.23		
	RMS idle-channel noise	Inputs tied to common-mode		1.41		LSB rms
				60.2		dBFS

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6.6 Switching Characteristics

Typical values at T_A = 25°C, Min and Max values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
LVDS Digital Outputs (DATA, OVR/SYNCOUT, CLKOUT)						
V_{OD}	Differential output voltage (±)	Terminated 100 Ω differential	247	350	454	mV
V_{OC}	Common mode output voltage		1.125	1.25	1.375	V
LVDS Digital Inputs (RESET)						
V_{ID}	Differential input voltage (±)	Each input pin	175	350		mV
V_{IC}	Common mode input voltage		0.1	1.25	2.4	V
R_{IN}	Input resistance			100		Ω
C_{IN}	Input capacitance	Each pin to ground		3.7		pF
Digital Inputs (SCLK, SDIO, SDENB)						
V_{IH}	High level input voltage		2		AVDD3 + 0.3	V
V_{IL}	Low level input voltage		0		0.8	V
I_{IH}	High level input current			±1		µA
I_{IL}	Low level input current			±1		µA
C_{IN}	Input capacitance			2.9		pF
Digital Inputs (ENEXTREF, ENPWD, ENA1BUS)						
V_{IH}	High level input voltage		2		AVDD5 + 0.3	V
V_{IL}	Low level input voltage		0		0.8	V
I_{IH}	High level input current	~40kΩ internal pull-down		125		µA
I_{IL}	Low level input current			20		µA
C_{IN}	Input capacitance			2.9		pF
Digital OutputS (SDIO, SDO)						
V_{OH}	High level output voltage	I_{OH} = 250 µA	2.8			V
V_{OL}	Low level output voltage	I_{OL} = 250 µA			0.4	V
Clock Inputs						
R_{IN}	Differential input resistance	CLKINP, CLKINN	100	130	190	Ω
C_{IN}	Input capacitance	Estimated to ground from each CLKIN pin, excluding soldered packaged		4.8		pF

6.7 Timing Characteristics(1)

Typical values at T_A = 25°C, Min and Max values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
t_a	Aperture delay			250		ps
	Aperture jitter, rms	Uncertainty of sample point due to internal jitter sources		125		fs
	Latency	Bus A, using Single Bus Mode		7		Cycles
		Bus A, using Dual Bus Mode Aligned		7.5		
		Bus B, using Dual Bus Mode Aligned		8.5		
		Bus A and B, using Dual Bus Mode Staggered		7.5		

(1) Timing parameters are specified by design or characterization, but not production tested.

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Timing Characteristics[1] (continued)

Typical values at T_A = 25°C, Min and Max values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS/NOTES	MIN	TYP	MAX	UNIT
LVDS Output Timing (DATA, CLKOUT, OVR/SYNCOUT)[2]						
t_{CLK}	Clock period		1		10	ns
t_{CLKH}	Clock pulse duration, high	Assuming worst case 45/55 duty cycle	0.45			ns
t_{CLKL}	Clock pulse duration, low	Assuming worst case 55/45 duty cycle	0.45			ns
$t_{PD-CLKDIV2}$	Clock propagation delay	CLKIN rising to CLKOUT rising in divide by 2 mode		1200		ps
$t_{PD-CLKDIV4}$	Clock propagation delay	CLKIN rising to CLKOUT rising in divide by 4 mode		1200		ps
$t_{PD-ADATA}$	Bus A data propagation delay	CLKIN falling to Data Output transition		1400		ps
$t_{PD-BDATA}$	Bus B data propagation delay			1400		ps
t_{SU-SBM} [3]	Setup time, single bus mode	Data valid to CLKOUT edge, 50% CLKIN duty cycle	290	(t_{CLK}/2) - 185		ps
t_{H-SBM}	Hold time, single bus mode	CLKOUT edge to Data invalid, 50% CLKIN duty cycle	410	(t_{CLK}/2) - 65		ps
t_{SU-DBM}	Setup time, dual bus mode	Data valid to CLKOUT edge, 50% CLKIN duty cycle	550	t_{CLK} - 425		ps
t_{H-DBM}	Hold time, dual bus mode	CLKOUT edge to Data invalid, 50% CLKIN duty cycle	1150	t_{CLK} + 175		ps
t_r	LVDS output rise time	Measured 20% to 80%		400		ps
t_f	LVDS output fall time			400		ps
LVDS Input Timing (RESETIN)						
t_{RSU}	RESET setup time	RESETP going HIGH to CLKINP going LOW	325			ps
t_{RH}	RESET hold time	CLKINP going LOW to RESETP going LOW	325			ps
	RESET input capacitance	Differential		1		pF
	RESET input current			±1		µA
SeriaL Interface Timing						
$t_{S-SDENB}$	Setup time, serial enable	SDENB falling to SCLK rising	20			ns
$t_{H-SDENB}$	Hold time, serial enable	SCLK falling to SENDB rising	25			ns
t_{S-SDIO}	Setup time, SDIO	SDIO valid to SCLK rising	10			ns
t_{H-SDIO}	Hold time, SDIO	SCLK rising to SDIO transition	10			ns
f_{SCLK}	Frequency				10	MHz
t_{SCLK}	SCLK period		100			ns
t_{SCLKH}	Minimum SCLK high time		40			ns
t_{SCLKL}	Minimum SCLK low time		40			ns
t_r	Rise time	10pF		10		ns
t_f	Fall time	10pF		10		ns
t_{DDATA}	Data output delay	Data output (SDO/SDIO) delay after SCLK falling, 10pF load	75			ns

(2) LVDS output timing measured with a differential 100Ω load placed ~4 inches from the ADS5400. Measured differential load capacitance is 3.5 pF. Measurement probes and other parasitics add ~1pF. Total approximate capacitive load is 4.5 pF differential. All timing parameters are relative to the device pins, with the loading as stated.

(3) In single bus mode at 1 GSPS (1ns clock), the minimum output setup/hold times over process and temperature provide a minimum 700 ps of data valid window, with 300 ps of uncertainity.

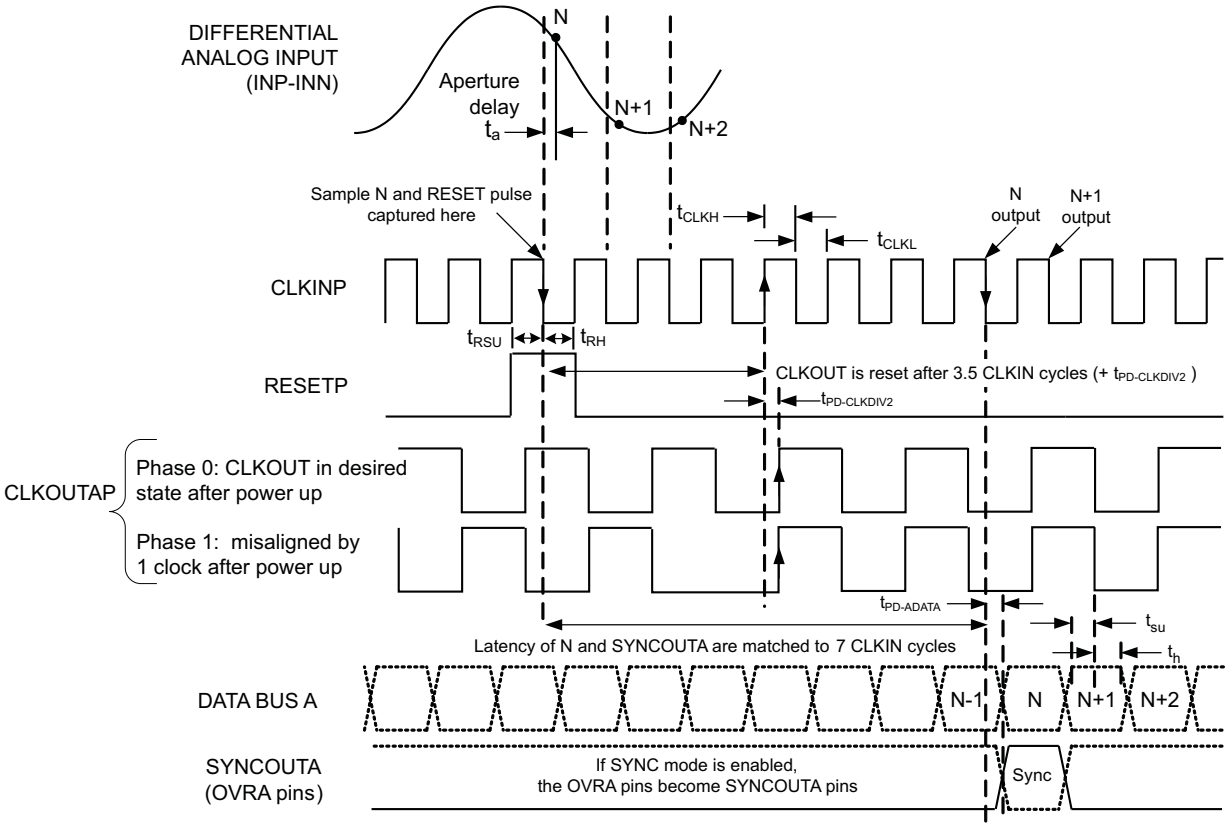
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6.8 Interleaving Adjustments

Typical values at T_A = 25°C, Min and Max values over full temperature range T_{MIN} = –55°C to T_{MAX} = 125°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Adjustments						
	Resolution		9			Bits
	LSB magnitude	at full scale range of $2V_{PP}$		120		µV
DNL	Differential linearity error		-2.5		2.5	LSB
INL	Integral Non-Linearity error		-3		3	LSB
	Recommended Min Offset Setting	from default offset value, to maintain AC performance		-8		mV
	Recommended Max Offset Setting			8		mV
Gain Adjustments						
	Resolution		12			Bits
	LSB magnitude			120		µV
DNL	Differential linearity error		-4	-1.2, +0.5	4	LSB
INL	Integral Non-Linearity error		-8	-2, +1	8	LSB
	Min Gain Setting			1.52		V_{PP}
	Max Gain Setting			2		V_{PP}
Input Clock Fine Phase Adjustment						
	Resolution		6			Bits
	LSB magnitude			116		fs
DNL	Differential linearity error		-2		2.5	LSB
INL	Integral Non-Linearity error		-2.5		4	LSB
	Max Fine Clock Skew setting			7.4		ps
Input Clock Coarse Phase Adjustment						
	Resolution		5			Bits
	LSB magnitude			2.4		ps
DNL	Differential linearity error		-1		1	LSB
INL	Integral Non-Linearity error		-1		5	LSB
	Max Coarse Clock Skew setting			73		ps

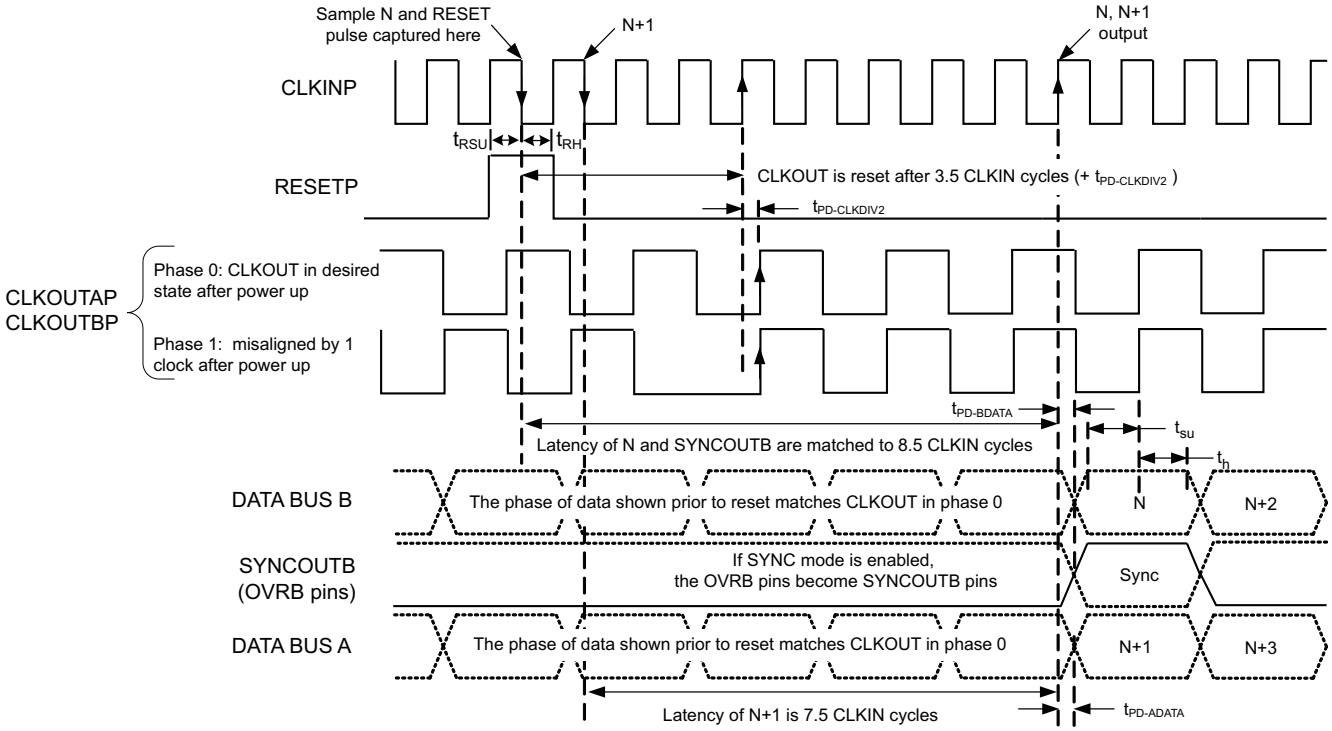
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Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTA transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit. Bus B is not active in single bus mode.

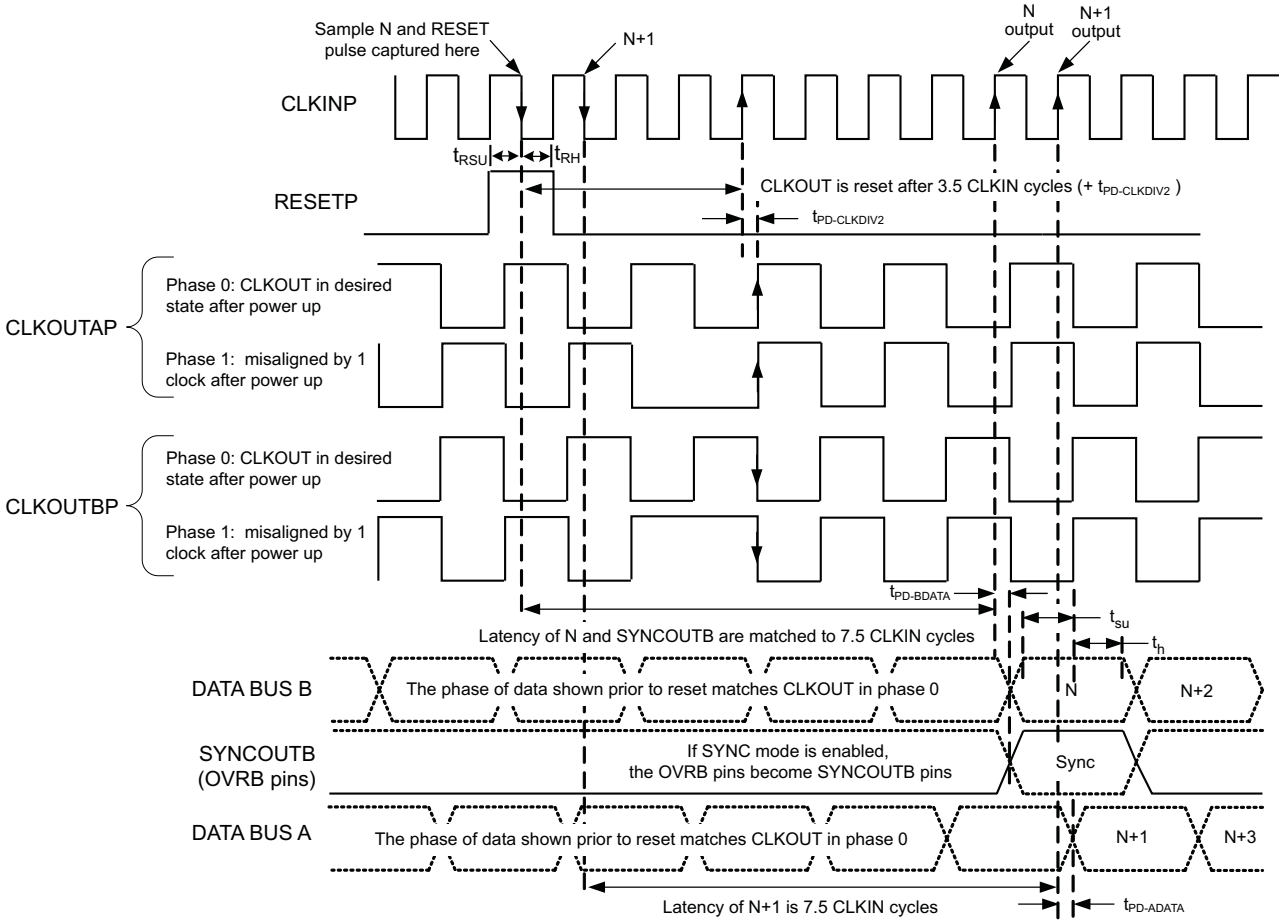
Figure 1. Single Bus Mode

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Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

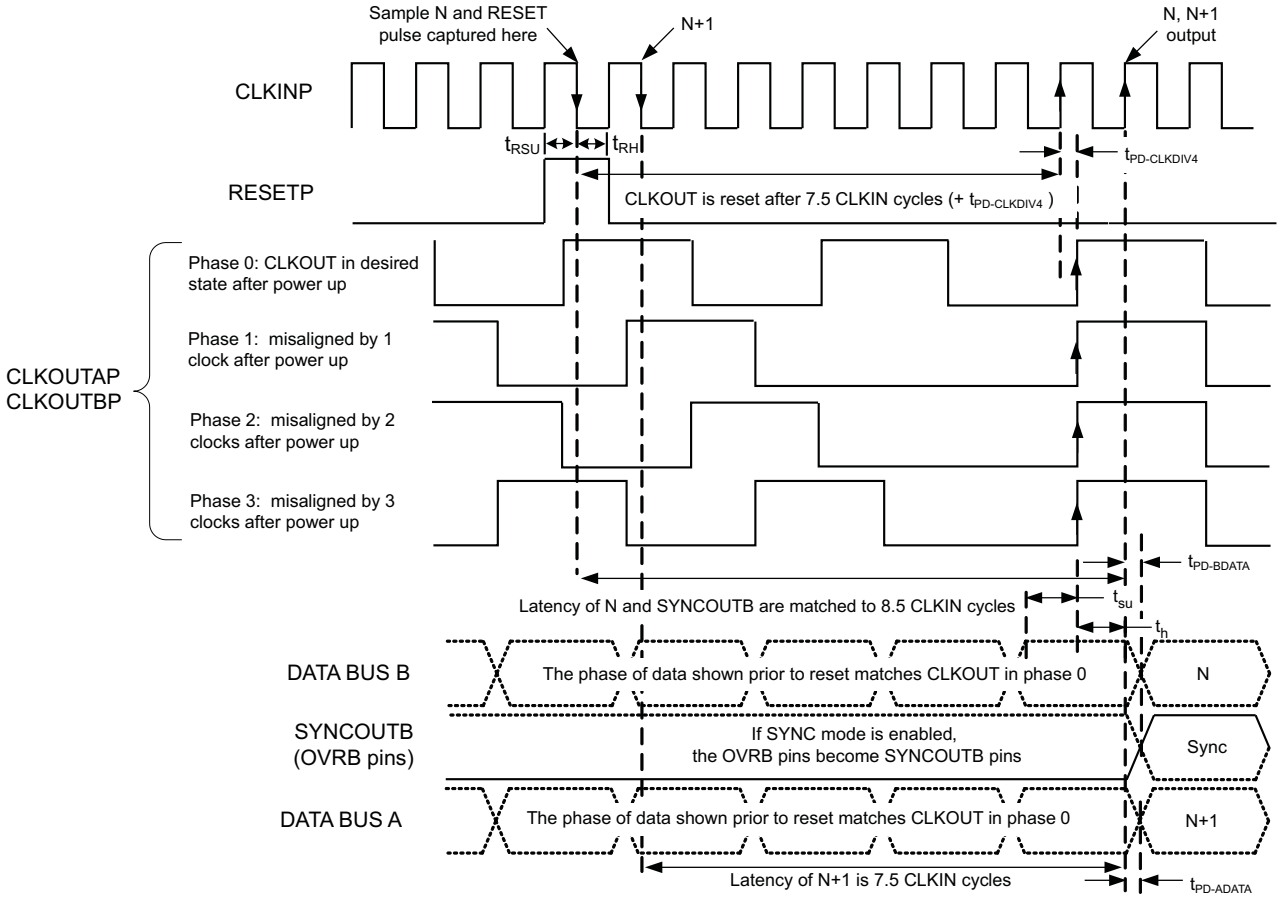
Figure 2. Dual Bus Mode - Aligned, CLKOUT Divide By 2



Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/2, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

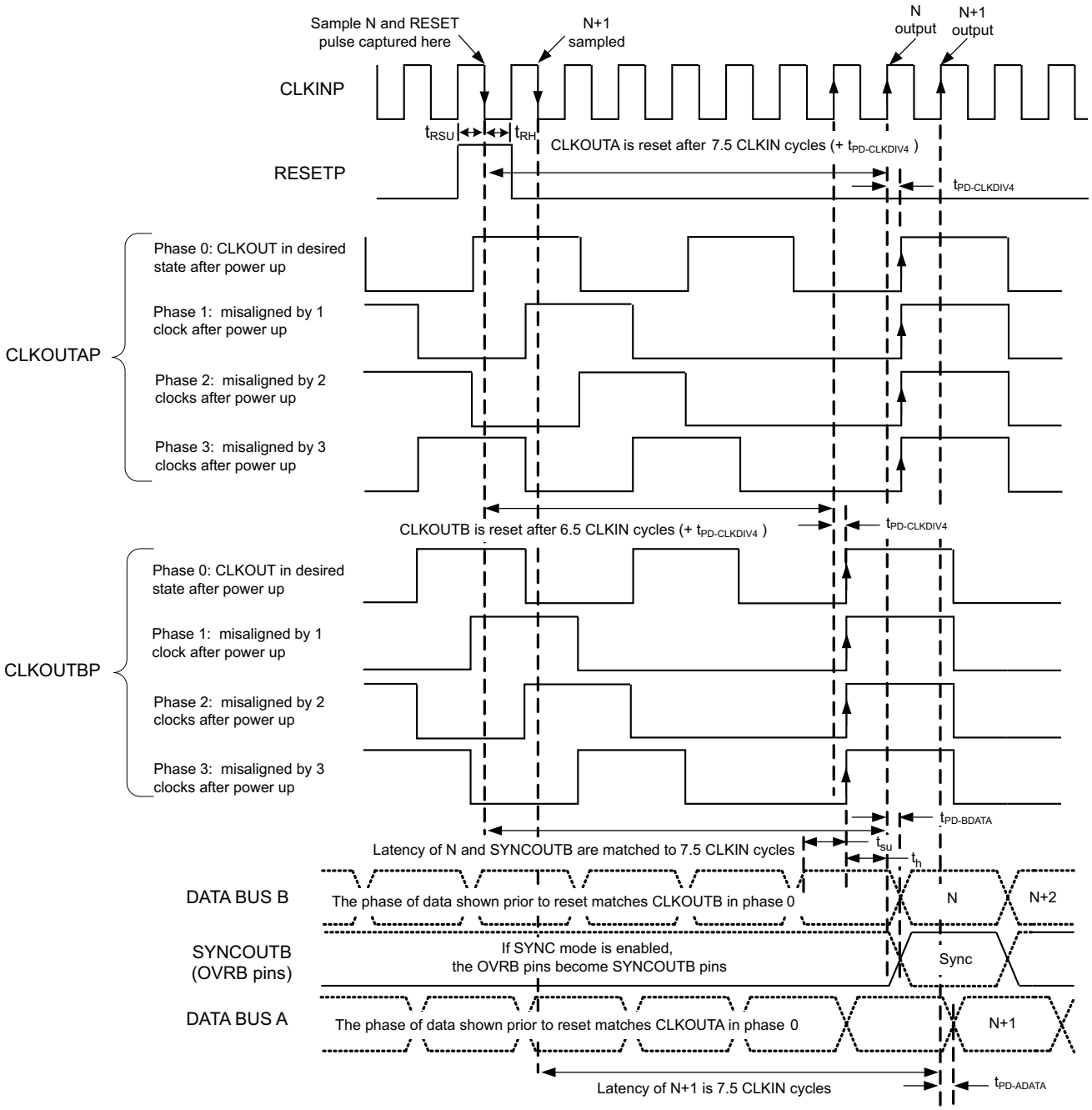
Figure 3. Dual Bus Mode - Staggered, CLKOUT Divide By 2

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Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/4, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

Figure 4. Dual Bus Mode - Aligned, CLKOUT Divide By 4



Propagation delays and setup/hold times not drawn to scale. RESET and SYNCOUT are optional. Any clock phase will work properly, but makes synchronization of data capture across multiple ADCs difficult without a known CLKOUT phase. RESET can be a single pulse (as shown), low-to-high step or repetitive pulse input signal. The frequency of repetitive RESET pulses should not exceed CLKIN/4, and should be an even divisor of CLKIN, in order to keep the CLKOUT phase the same with each RESET event. SYNCOUTB transitions with the same latency as the sample that is present when the RESET pulse is captured, shown here as sample N. Each RESET captured generates a SYNCOUT pulse, which behaves as a data bit.

Figure 5. Dual Bus Mode - Staggered, CLKOUT Divide By 4

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6.9 Typical Characteristics

Typical plots at T_A = 25°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5-V_{PP} differential clock, (unless otherwise noted)

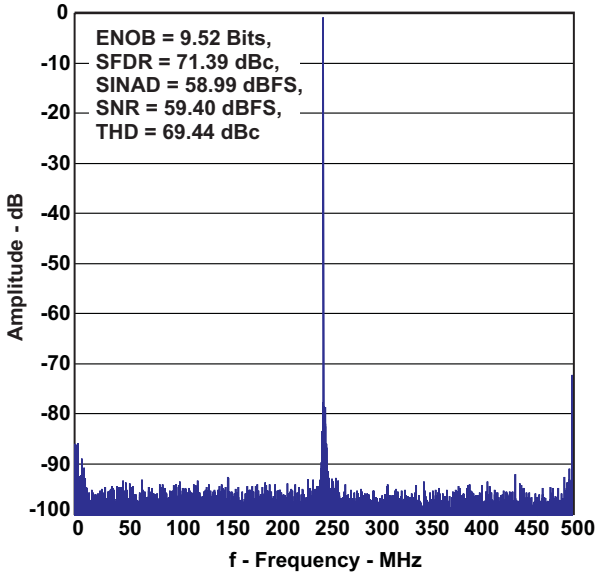


Figure 6. Spectral Performance v FFT for 250-MHz Input Signal

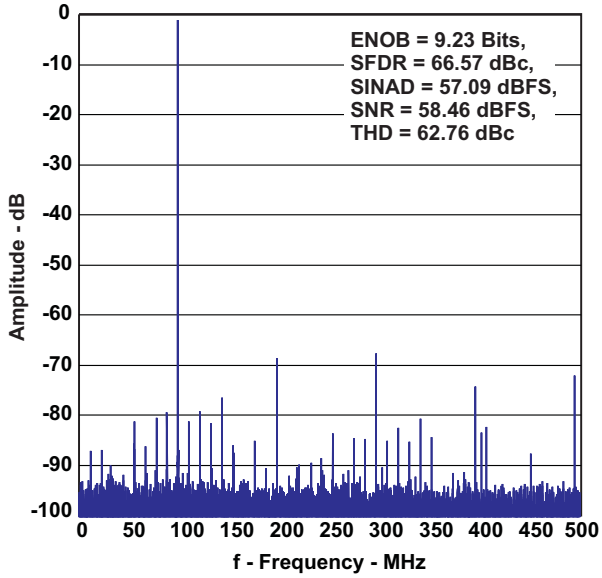


Figure 7. Spectral Performance v FFT for 0.9-GHz Input Signal

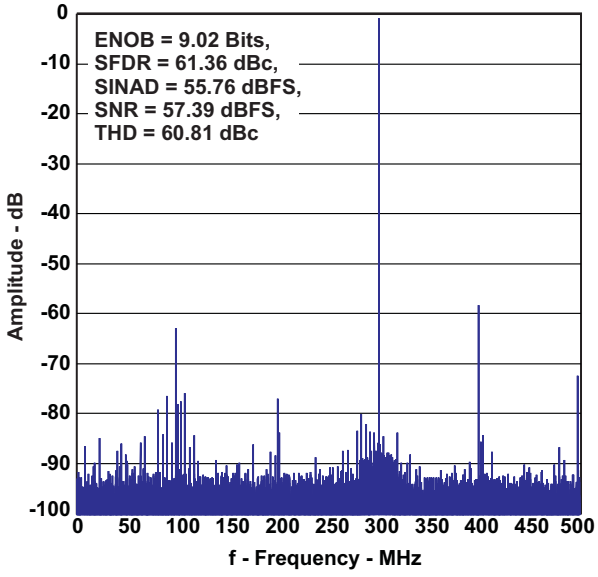


Figure 8. Spectral Performance v FFT for 1.3-GHz Input signal

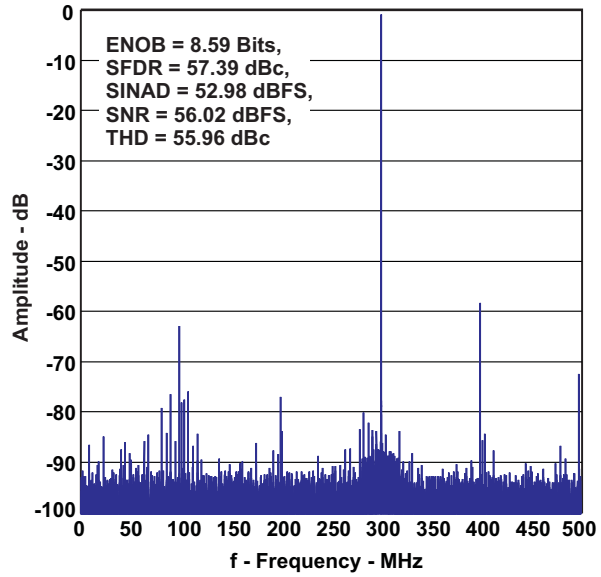


Figure 9. Spectral Performance v FFT for 1.7-GHz Input Signal

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Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5-V_{PP} differential clock, (unless otherwise noted)

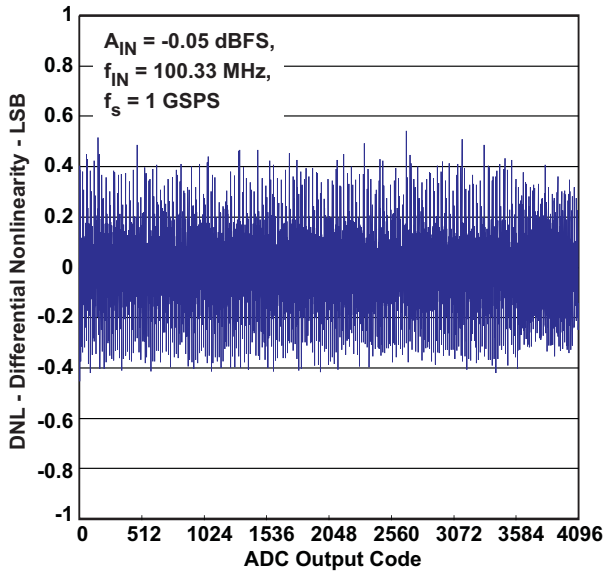


Figure 10. Differential Nonlinearity

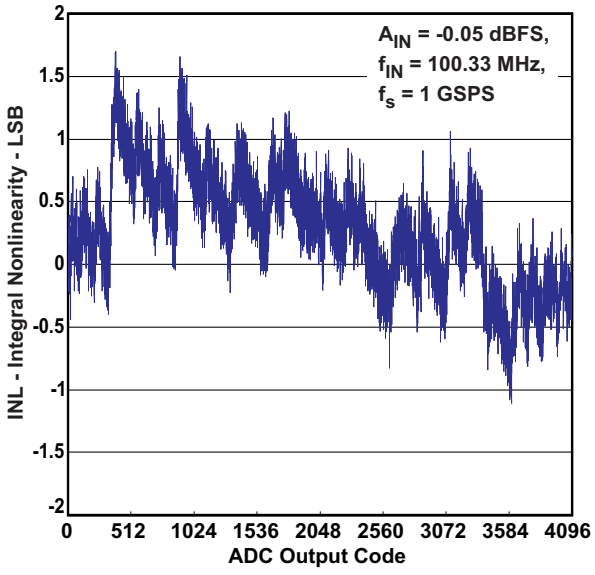


Figure 11. Integral Nonlinearity

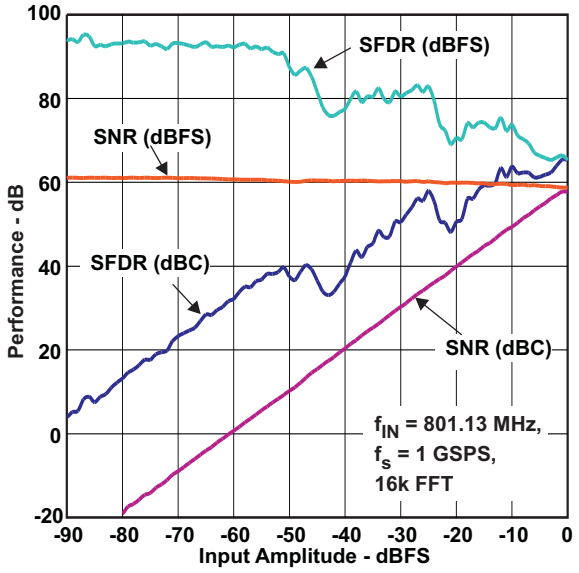


Figure 12. AC Performance vs Input Amplitude (801.13-MHz Input signal)

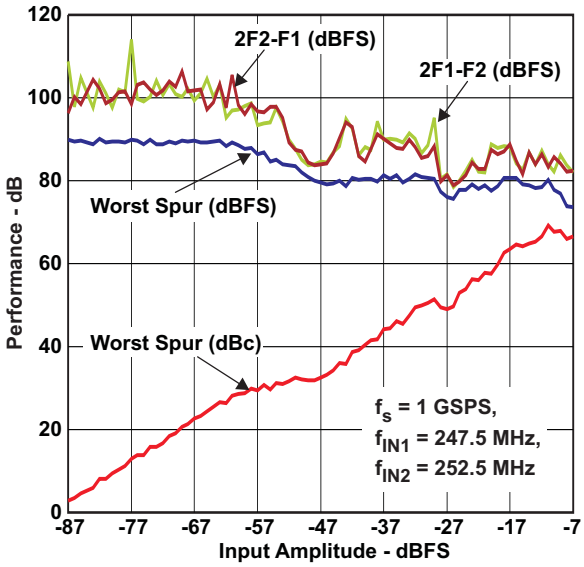


Figure 13. AC Performance vs Input Amplitude (247.5-MHz and 252.5-MHz Two-tone Input Signal)

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Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5-V_{PP} differential clock, (unless otherwise noted)

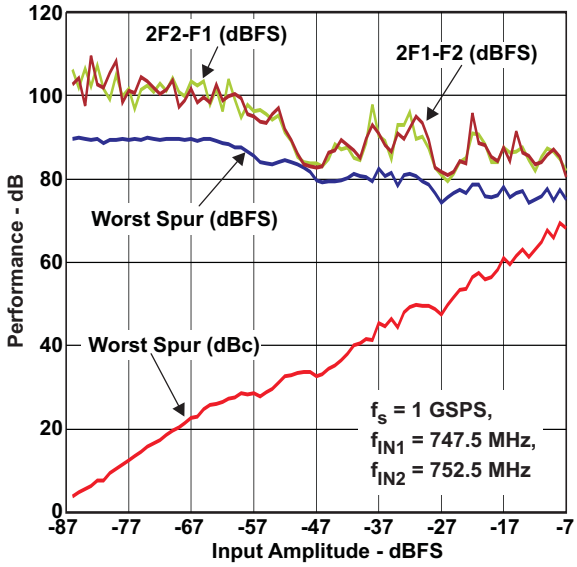


Figure 14. AC Performance vs Input Amplitude (747.5-MHz and 752.5-MHz Two-tone Input Signal)

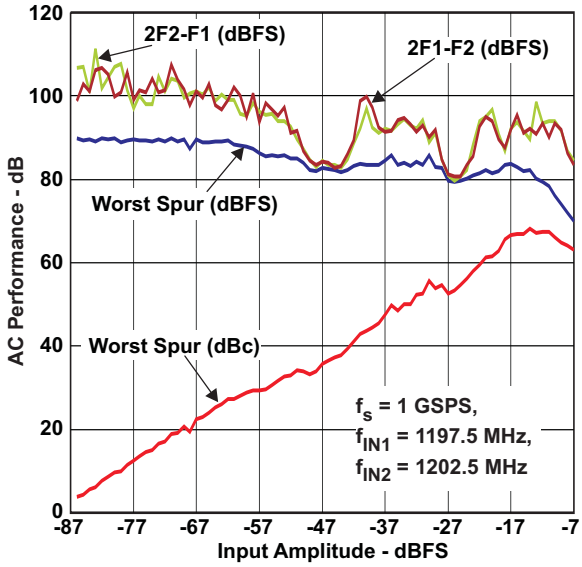


Figure 15. AC Performance vs Input Amplitude (1197.5-MHz and 1202.5-MHz Two-tone Input Signal)

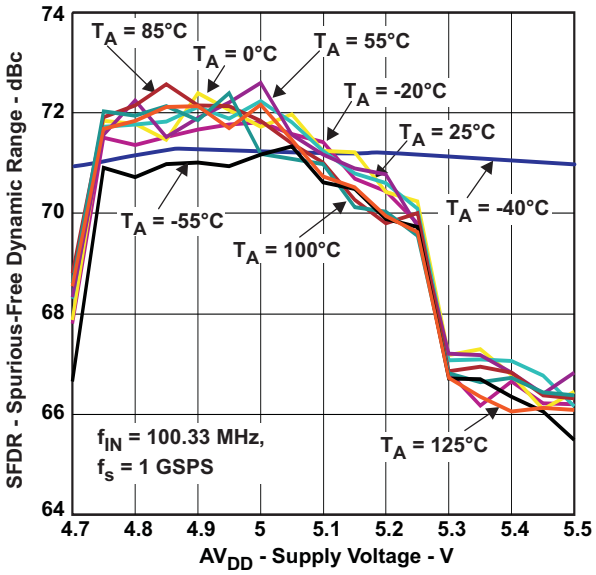


Figure 16. SFDR vs AVDD5 Across Temperature

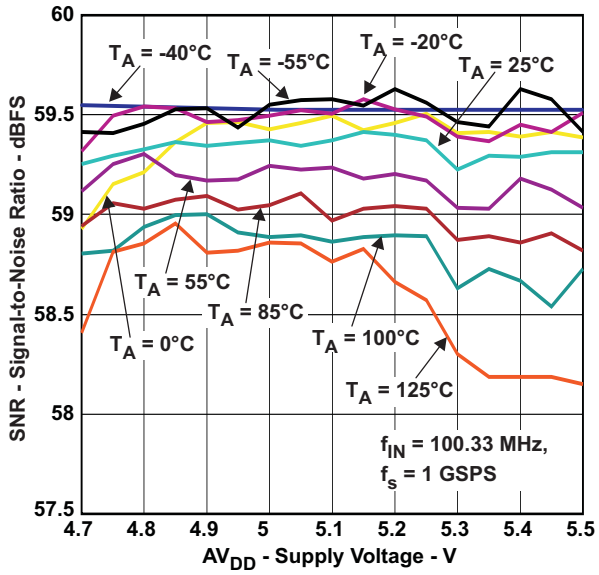


Figure 17. SNR vs AVDD5 Across Temperature

Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5-V_{PP} differential clock, (unless otherwise noted)

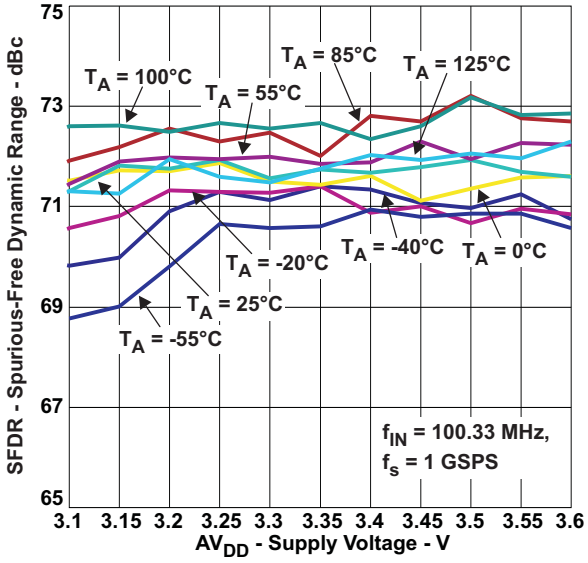


Figure 18. SFDR vs AVDD3 Across Temperature

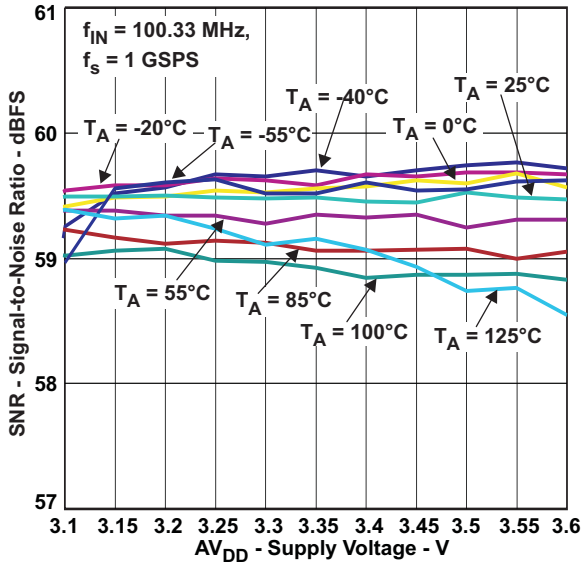


Figure 19. SNR vs AVDD3 Across Temperature

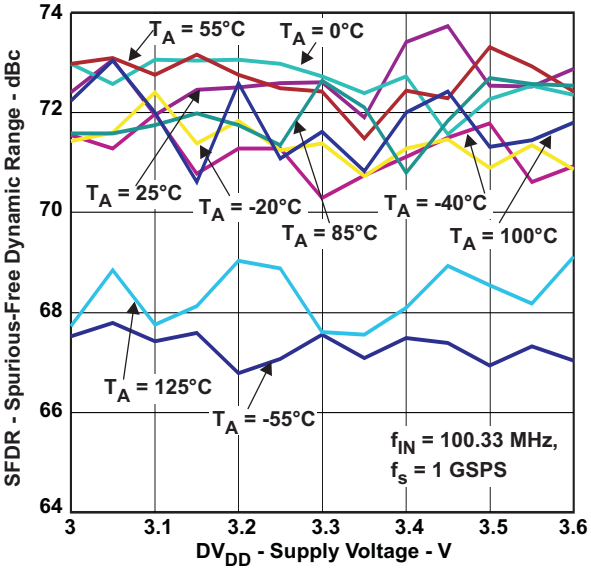


Figure 20. SFDR vs DVDD3 Across Temperature

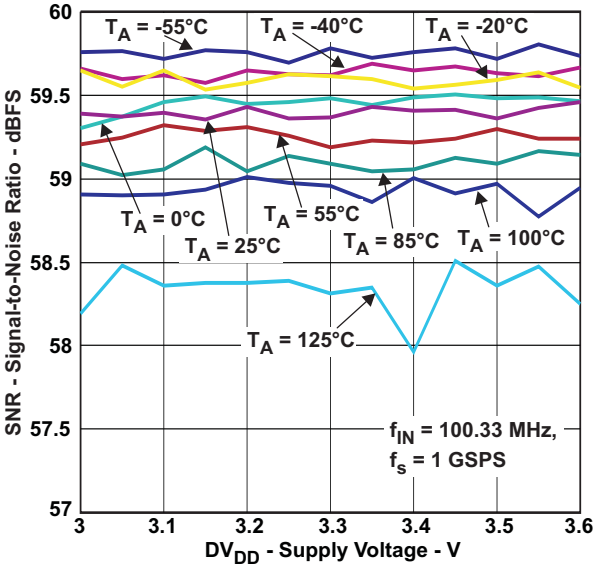


Figure 21. SNR vs DVDD3 Across Temperature

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Typical Characteristics (continued)

Typical plots at T_A = 25°C, sampling rate = 1 GSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 1.5-V_{PP} differential clock, (unless otherwise noted)

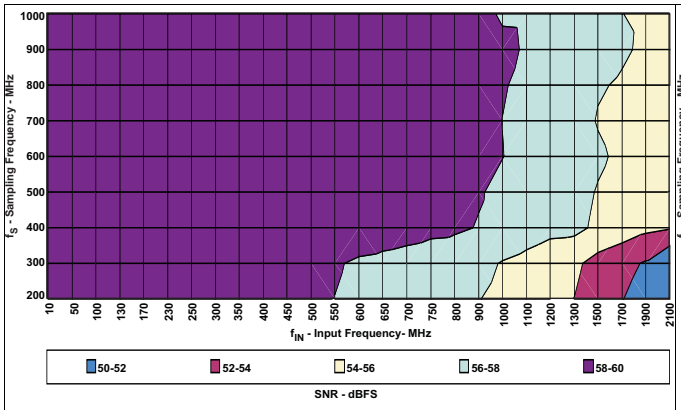


Figure 22. SNR vs Input Frequency and Sampling Frequency

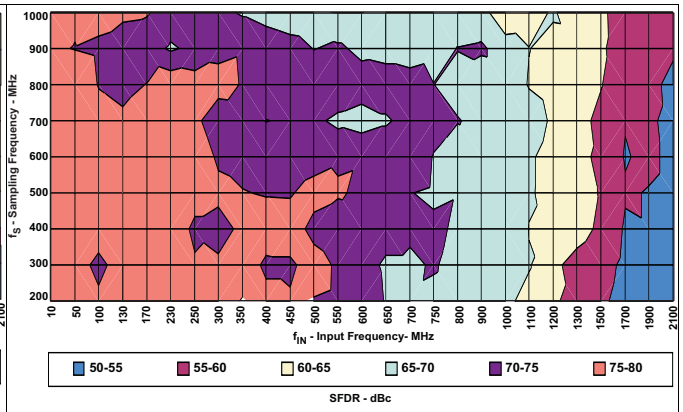


Figure 23. SFDR vs Input Frequency and Sampling Frequency

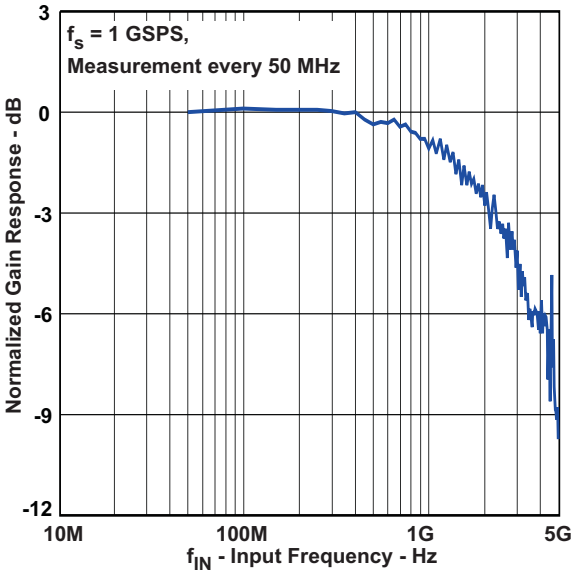


Figure 24. Normalized Gain Response vs Input Frequency

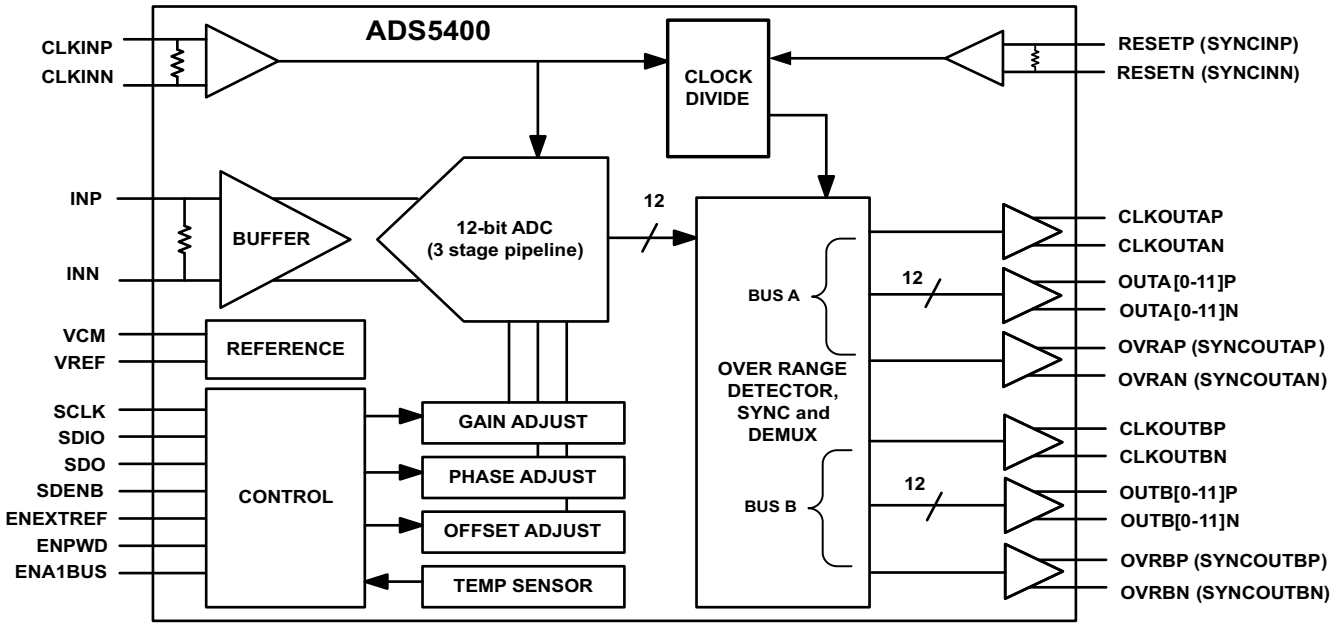
7 Detailed Description

7.1 Overview

The ADS5400-SP is a 12-bit, 1-GSPS, monolithic pipeline ADC. Its bipolar transistor analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible digital outputs. The conversion process is initiated by the falling edge of the external input clock. At the sampling instant, the differential input signal is captured by the input track-and-hold (T&H), and the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 7 - 8.5 clock cycles (output mode dependent), after which the output data is available as a 12-bit parallel word, coded in offset binary or two's complement format.

The user can select to accept the data at the full sample rate using one bus (bus A, latency 7 cycles), or demultiplex the data into two buses (bus A and B, latency 7.5 or 8.5 cycles) at half rate. A serial peripheral interface (SPI) is provided for adjusting operational modes, as well as for calibrations of analog gain, analog offset and clock phase for inter-leaving multiple ADS5400-SP. Die temperature readout using the SPI is provided. SYNC and RESET modes exist for synchronizing output data across multiple ADS5400-SP.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Configuration

The analog input for the ADS5400-SP consists of an analog pseudo-differential buffer followed by a bipolar transistor track-and-hold (see Figure 25). The integrated analog buffer isolates the source driving the input of the ADC from sampling glitches on the T&H and allows for the integration of a 100-Ω differential input resistor. The input common mode is set internally through a 500-Ω resistor connected from half of the AVDD5 supply voltage to each of the inputs. The parasitic package capacitance shown is with the package unsoldered. Once soldered, depending on the board characteristics, one can expect another ~1pF at the analog input pins, which is board dependent.

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Feature Description (continued)

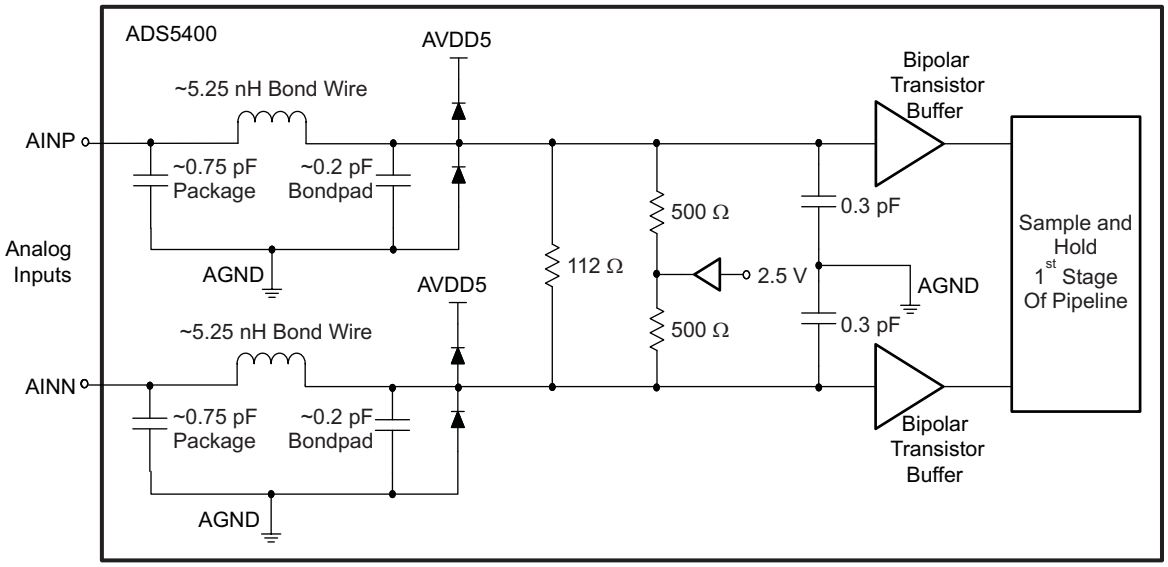


Figure 25. Analog Input Equivalent Circuit

For a full-scale differential input, each of the differential lines of the input signal swing symmetrically between 2.5 V + 0.5 V and 2.5 V – 0.5 V. This means that each input has a maximum signal swing of 1 V_{PP} for a total differential input signal swing of 2 V_{PP}. The maximum fullscale range can be programmed from 1.5-2Vpp using the SPI. The maximum swing is determined by the internal reference voltage generator and the fullscale range set using the SPI, eliminating the need for any external circuitry for this purpose. The analog gain adjustment has a resolution of 12-bits across the 1.5-2V_{PP} range, providing for fine calibration of analog gain mismatches across multiple ADS5400-SP signal chains, primarily for interleaving.

The ADS5400-SP obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 26 shows one possible configuration using an RF transformer. Datasheet performance, especially at >1GHz input frequency, can only be obtained with a carefully designed differential drive path to the ADC.

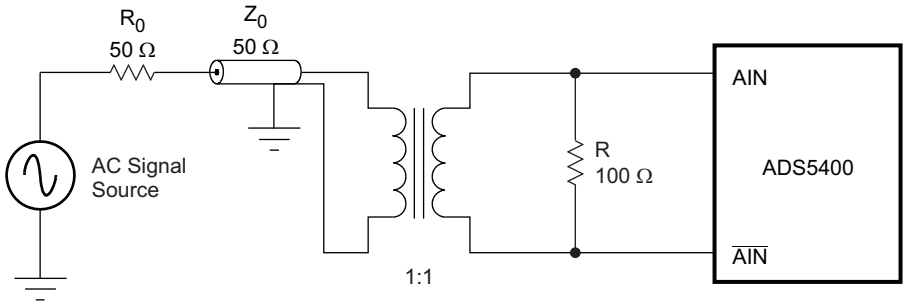


Figure 26. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

7.3.2 Voltage Reference

The 2 V voltage reference is provided internal to the ADS5400-SP. A VCM (voltage common mode) pin is provided as an output for use in dc-coupled applications, equal to the AVDD5 supply divided by 2. This provides the analog input common mode voltage to a driving circuit so that the common mode is setup properly. Some systems may prefer the use of an external voltage reference. This mode can be enabled by pulling the ENEXTREF pin high. In this mode, an external reference can be driven onto the VREF pin, which is normally expecting 2V.

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Feature Description (continued)

7.3.3 Analog Input Over-Range Recovery Error

An over-range condition occurs if the analog input voltage exceeds the full-scale range of the converter (0dBFS). To test recovery from an over-range, the ADC analog input is injected with a sinusoidal input frequency exactly at CLKIN/4 (a four-point sinusoid at the digital outputs). The four sample points of each period occur at the top, mid-scale, bottom and mid-scale of the sinusoid (clipped by the ADC when over-ranged to all 0s or all 1s). Once the amplitude exceeds 0dBFS, the top and bottom of the sinusoidal input becomes out of range, while the mid-scale point is always in-range and measureable with ADC output codes. The graph in Figure 27 indicates the amount of error from the expected mid-scale value of 2048 that occurs after negative over-range (bottom of sinusoid) and positive over-range (top of sinusoid). This equates to the amount of error in a valid sample 1 clock cycle after an over-range occurs, as a function of input amplitude.

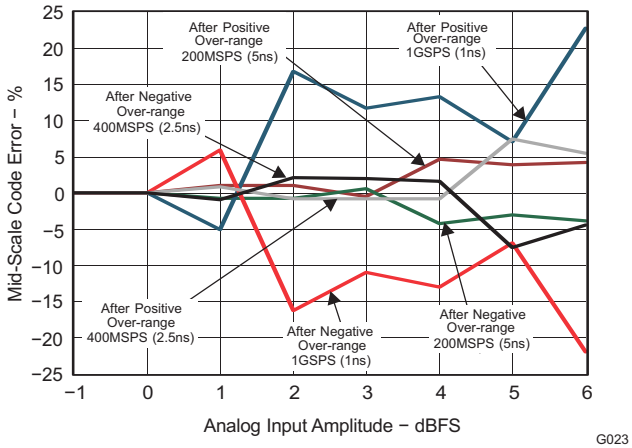


Figure 27. Recovery Error 1 Clock Cycle After Over-Range vs Input Amplitude

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Feature Description (continued)

7.3.4 Clock Inputs

The ADS5400-SP clock input can be driven with either a differential clock signal or a single-ended clock input. The equivalent clock input circuit can be seen in Figure 28. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock (as shown in Figure 29) could save cost and board space without much performance tradeoff. When clocked with this configuration, it is best to connect $\overline{CLK}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 29.

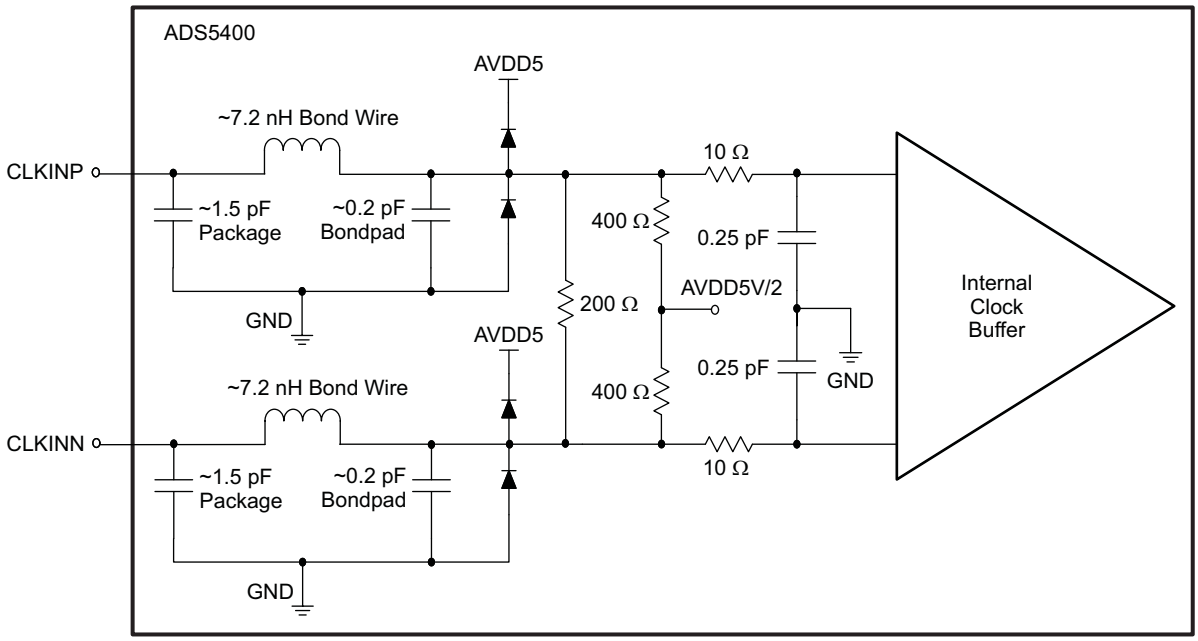


Figure 28. Clock Input Circuit

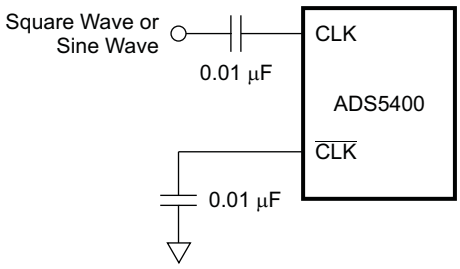


Figure 29. Single-Ended Clock

Feature Description (continued)

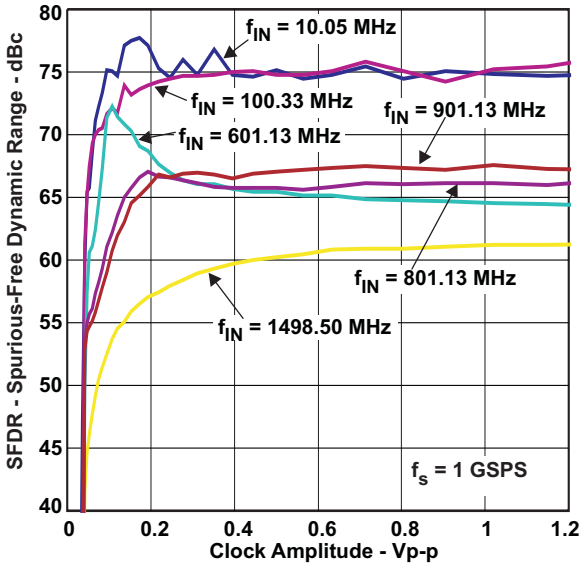


Figure 30. ADS5400 SFDR vs Differential Clock Level

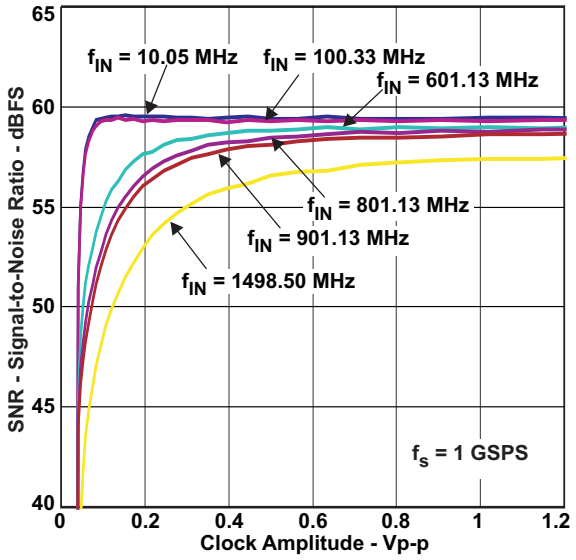


Figure 31. ADS5400 SNR vs Differential Clock Level

The characterization of the ADS5400-SP is typically performed with a 1.5 V_{PP} differential clock, but the ADC performs well with a differential clock amplitude down to ~400 mV_{PP} (200mV swing on both CLK and $\overline{CLK}$), as shown in Figure 30 and Figure 31. For jitter-sensitive applications, the use of a differential clock has some advantages at the system level and is strongly recommended. The differential clock allows for common-mode noise rejection at the printed circuit board (PCB) level. With a differential clock, the signal-to-noise ratio of the ADC is better for jitter-sensitive, high-frequency applications because the board level clock jitter is superior.

Larger clock amplitude levels are recommended for high analog input frequencies or slow clock frequencies. At high analog input frequencies, the sampling process is sensitive to jitter. At slow clock frequencies, a small amplitude sinusoidal clock has a lower slew rate and can create jitter-related SNR degradation due to the uncertainty in the sampling point associated with a slow slew rate. Figure 32 demonstrates a recommended method for converting a single-ended clock source into a differential clock; it is similar to the configuration found on the evaluation board and was used for much of the characterization. See also *Clocking High Speed Data Converters* (SLYT075) for more details.

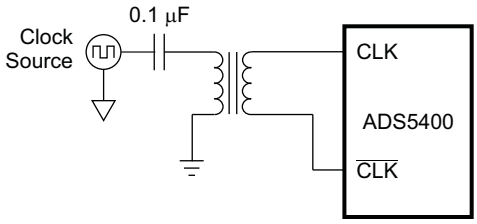


Figure 32. Differential Clock

The common-mode voltage of the clock inputs is set internally to 2.5 V using internal 400 Ω resistors (see Figure 28). It is recommended to use ac coupling in the clock path, but if this scheme is not possible, the ADS5400-SP features good tolerance to clock common-mode variation, as shown in Figure 33 and Figure 34. The internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided.

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Feature Description (continued)

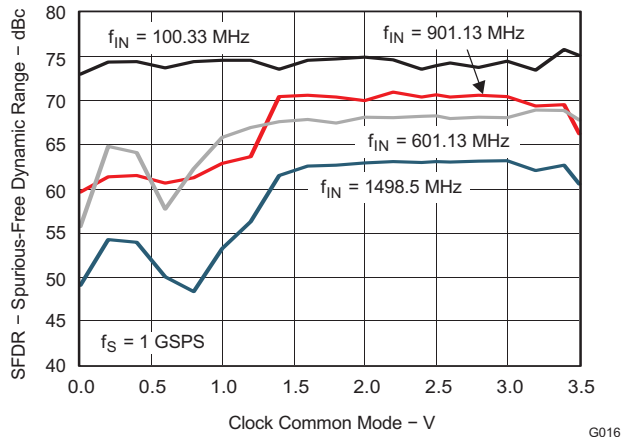


Figure 33. ADS5400-SP SFDR vs Clock Common Mode

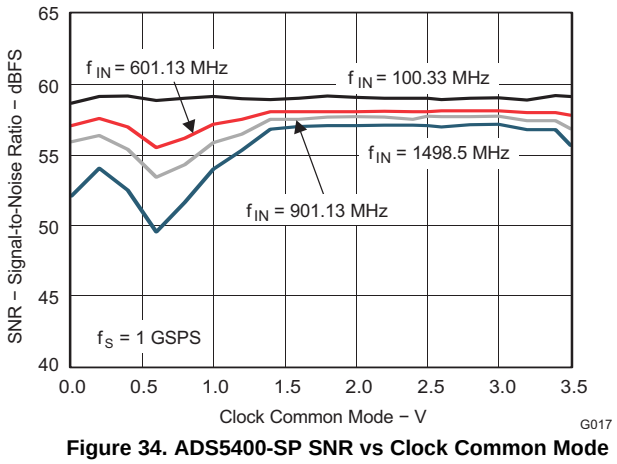


Figure 34. ADS5400-SP SNR vs Clock Common Mode

To understand how to determine the required clock jitter, an example is useful. The ADS5400 is capable of achieving 58.7 dBFS SNR at 850 MHz of analog input frequency. To achieve SNR at 850 MHz, the external clock source rms jitter must be at least 210fs when combined with the 125fs of internal aperture jitter in order for the total rms jitter to be 244fs. A summary of maximum recommended rms clock jitter as a function of analog input frequency is provided in Table 1 (using 125fs of internal aperture jitter). The equations used to create the table are also presented.

Table 1. Recommended RMS Clock Jitter

INPUT FREQUENCY (MHz)	MEASURED SNR (dBc)	TOTAL JITTER (fs rms)	MAXIMUM EXT CLOCK JITTER (fs rms)
125	58.1	1585	1580
600	57.8	318	342
850	57.7	244	210
1200	56.6	196	151
1700	54.7	172	119

Equation 1 and Equation 2 are used to estimate the required clock source jitter.

$$SNR\ (dBc) = -20 \times LOG10\ (2 \times \pi \times f_{IN} \times j_{TOTAL}) \quad (1)$$

$$j_{TOTAL} = (j_{ADC}^{2} + j_{CLOCK}^{2})^{1/2} \quad (2)$$

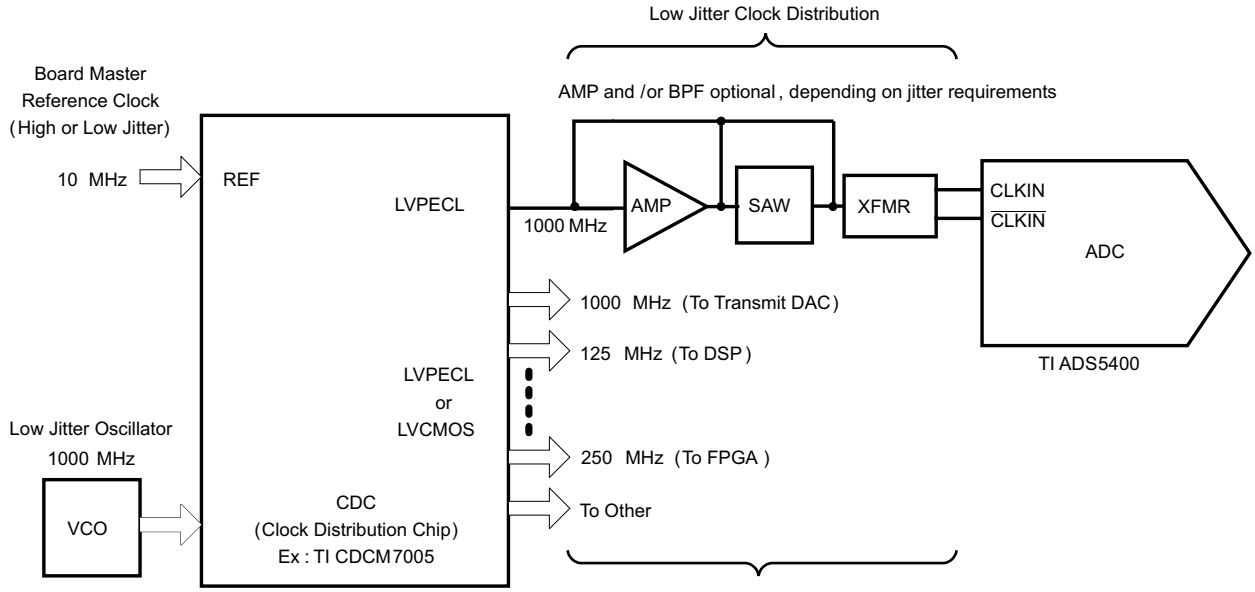
where:

j_{TOTAL} = the rms summation of the clock and ADC aperture jitter;
j_{ADC} = the ADC internal aperture jitter which is located in the data sheet;
j_{CLOCK} = the rms jitter of the clock at the clock input pins to the ADC; and
f_{IN} = the analog input frequency.

Notice that the SNR is a strong function of the analog input frequency, not the clock frequency. The slope of the clock source edges can have a mild impact on SNR as well and is not taken into account for these estimates. For this reason, maximizing clock source amplitudes at the ADC clock inputs is recommended, though not required (faster slope is desirable for jitter-related SNR). For more information on clocking high-speed ADCs, see Application Note SLWA034, *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices*. Recommended clock distribution chips (CDCs) are the TI CDC7005 and CDCM7005. Depending on the jitter requirements, a band pass filter (BPF) is sometimes required between the CDC and the ADC. If the insertion loss of the BPF causes the clock amplitude to be too low for the ADC, or the clock source amplitude is too low to begin with, an inexpensive amplifier can be placed between the CDC and the BPF.

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Figure 35 represents a scenario where an LVPECL output is used from a TI CDCM7005 with the clock signal path optimized for maximum amplitude and minimum jitter. The jitter of this setup is difficult to estimate and requires a careful phase noise analysis of the clock path. The BPF (and possibly a low-cost amplifier because of insertion loss in the BPF) can improve the jitter between the CDC and ADC when the jitter provided by the CDC is still not adequate. The total jitter at the CDCM7005 output depends heavily on the phase noise of the VCXO selected. If it is determined that the jitter from the CDCM7005 with a VCXO is sufficient without further conditioning, it is possible to clock the device directly from the CDCM7005 using differential LVPECL outputs (see the CDCM7005 data sheet for the exact schematic). A careful analysis of the required jitter and of the components involved is recommended before determining the proper approach.



This is a general block diagram example: Consult the datasheet of the CDCM7005 for proper schematic and for specifications regarding allowable input and output frequency and amplitude ranges.

Figure 35. Clock Source Diagram

7.3.5 Over Range

The OVR output equals a logic high when the 12-bit output word attempts to exceed either all 0s or all 1s. This flag is provided as an indicator that the analog input signal exceeded the full-scale input limit set in register 0x00 and 0x01 (± gain error). The OVR indicator is provided for systems that use gain control to keep the analog input signal within acceptable limits. The OVR pins are not available when the sychronization mode is enabled, as they become the SYNCOUT indicator.

7.3.6 Data Scramble

In normal operation, with this mode disabled, the MSBs have similar energy to the analog input fundamental frequency and can in some instances cause board interference. A data scramble mode is available in register 0x06. In this mode, bits 11-1 are XOR'd with bit 0 (the LSB). Because of the random nature of the LSB, this has the effect of randomizing the data pattern. To de-scramble, perform the opposite operation in the digital chip after receiving the scrambled data.

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7.3.7 Test Patterns

Determining the closure of timing or validating the digital interface can be difficult in normal operation. Therefore, test patterns are available in register 0x06. One pattern toggles the outputs between all 1s and all 0s. Another pattern generates a 7-bit PRBS (pseudo-random bit sequence).

In dual bus mode, the toggle mode could be in the same phase on bus A and B (bus A and B outputting 1s or 0s together), or could be out of phase (bus A outputting 1s while bus B outputs 0s). The start phase cannot be controlled.

The PRBS output sequence is a standard 2^7-1 pseudo-random sequence generated by a feedback shift register where the two last bits of the shift register are exclusive-OR'ed and fed back to the first bit of the shift register. The standard notation for the polynomial is $x^7 + x^6 + 1$. The PRBS generator is not reset, so there is no initial position in the sequence. The pattern may start at any position in the repeating 127-bit long pattern and the pattern repeats as long as the PRBS mode is enabled. The data pattern from the PRBS generator is used for all of the LVDS parallel outputs, so when the pattern is '1' then all of the LVDS outputs are outputting '1' and when the pattern is '0' then all of the LVDS drivers output '0'. To determine if the digital interface is operating properly with the PRBS sequence, the user must generate the same sequence in the receiving device, and do a shift-and-compare until a matching sequence is confirmed.

7.3.8 Die Identification and Revision

A unique 64-bit die indentifier code can be read from registers 0x17 through 0x1E. An 8-bit die revision code is available in register 0x1F.

7.3.9 Die Temperature Sensor

In register 0x05, the die temperature sensor can be enabled. The sensor is power controlled independently of global powerdown, so that it and the SPI can be used to monitor the die temperature even when the remainder of the ADC is in sleep mode. Register 0x08 is used to read values which can be mapped to the die temperature. The exact mapping is detailed in the register map. Care should be taken not to exceed a maximum die temperature of 150°C for prolonged periods of time in order to maintain the life of the device.

7.3.10 Interleaving

7.3.10.1 Gain Adjustment

A signal gain adjustment is available in registers 0x00 and 0x01. The allowable fullscale range for the ADC is 1.52 - $2V_{PP}$ and can be set with 12-bit adjustment resolution across this range. For equal up/down gain adjustment of the system and ADC gain mismatches, a nominal starting point of $1.75V_{PP}$ could be programmed, in which case ±250mV of adjustment range would be provided.

7.3.10.2 Offset Adjustment

Analog offset adjustment is available in register 0x03 and 0x04. This provides ±30mV of adjustment range with 9-bit adjustment resolution of 120uV per step. At production test, the default code for this register setting is set to a value that provides 0mV of ADC offset. For optimum spectral performance, it is not recommended to use more than ±8mV adjustment from the default setting

7.3.10.3 Input Clock Coarse Phase Adjustment

Coarse adjustment is available in register 0x02. The typical range is approximately 73 ps with a resolution of 2.4ps.

7.3.10.4 Input Clock Fine Phase Adjustment

Fine adjustment is available in register 0x03. The typical range is approximately 7.4 ps with a resolution of 116fs.

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7.4 Device Functional Modes

7.4.1 Output Bus and Clock Options

The ADS5400-SP has two buses, A and B. Using register 0x02, a single or dual bus output can be selected. In single-bus mode, bus A is used at the full clock rate, while in two-bus mode, data is multiplexed at half the clock rate on A and B. While in single bus mode, CLKOUTA is at frequency CLKIN/2 and a DDR interface is achieved. In two-bus mode, CLKOUTA/CLKOUTB can be either at frequency CLKIN/2 or CLKIN/4, providing options for an SDR or DDR interface. The ADC provides 12 LVDS-compatible data outputs (D11 to D0; D11 is the MSB and D0 is the LSB), a data-ready signal (CLKOUT), and an over-range indicator (OVR) on each bus. It is recommended to use the CLKOUT signal to capture the output data of the ADS5400. Both two's complement and offset binary are available output formats, in register 0x05.

The capacitive loading on the digital outputs should be minimized. Higher capacitance shortens the data-valid timing window. The values given for timing were obtained with an estimated 3.5-pF of differential parasitic board capacitance on each LVDS pair.

7.4.2 Reset and Synchronization

Referencing the timing diagrams starting in Figure 1, the polarity of CLKOUT with respect to the sample N data output transition is undetermined because of the unknown startup logic level of the clock divider that generates the CLKOUT signal, whether in frequency CLKIN/2 or CLKIN/4 mode. The polarity of CLKOUT could invert when power is cycled off/on. If a defined CLKOUT polarity is required, the RESET input pins are used to reset the clock divider to a known state after power on with a reset pulse. A RESET is not commonly required when using only one ADS5400 because a one sample uncertainty at startup is not usually a problem.

NOTE: initial samples capture RESET = HIGH on the rising edge of CLKINP. This is being corrected for final samples and will reflect the diagram as drawn, with RESET = HIGH captured on falling edge of CLKINP.

In addition to CLKOUT alignment using RESET, a synchronization mode is provided in register 0x05. In this mode, the OVR output becomes the SYNCOUT. The SYNCOUT will indicate which sample was present when the RESET input pulse was captured in a HIGH state. The OVR indicator is not available when sync mode is enabled. In single bus mode, only SYNCOUTA is used. In dual bus mode, only SYNCOUTB is used.

7.4.3 LVDS

Differential source loads of 100 Ω and 200 Ω are provided internal to the device and can be implemented using register 0x06 (as well as no internal load). Normal LVDS operation expects 3.5 mA of current, but alternate values of 2.5, 4.5, and 5.5 mA are provided to save power or improve the LVDS signal quality when the environment provides excessive loading.

7.5 Programming

7.5.1 Serial Interface

The serial port of the ADS5400-SP is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of ADS5400. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface in register **0x01h**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and **SDO** is data out only.

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. Table 2 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

Table 2. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

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R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from ADS5400 and a low indicates a write operation to the ADS5400.

[N1:N0] Identifies the number of data bytes to be transferred per Table 3 below. Data is transferred MSB first.

Table 3. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4:A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the ADS5400 MSB first and counts down for each byte.

Figure 36 shows the serial interface timing diagram for a device write operation. **SCLK** is the serial interface clock input to ADS5400-SP. Serial data enable **SDENB** is an active low input to ADS5400-SP. **SDIO** is serial data in. Input data to the device is clocked on the rising edges of **SCLK**.

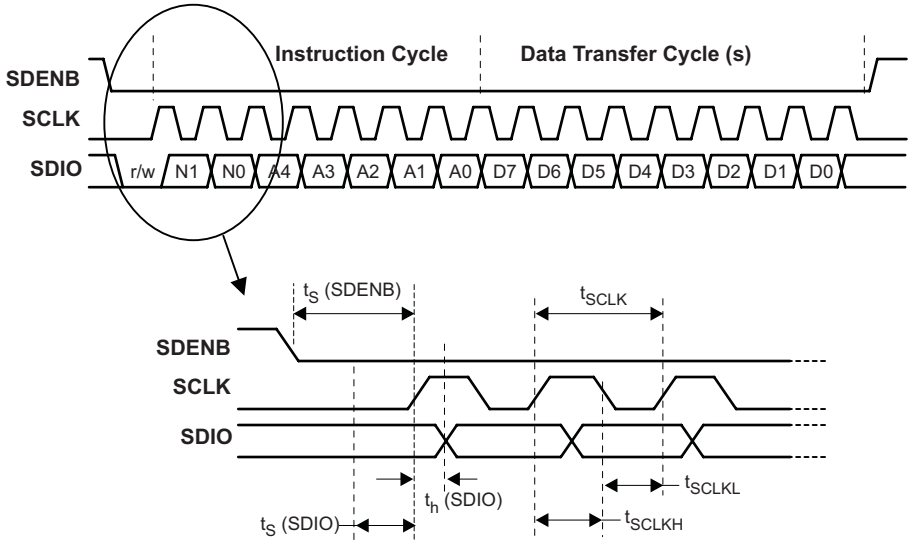


Figure 36. Serial Interface Write Timing Diagram

Figure 37 shows the serial interface timing diagram for a device read operation. **SCLK** is the serial interface clock input to the device. Serial data enable **SDENB** is an active low input to the device. **SDIO** is serial data in during the instruction cycle. In 3 pin configuration, **SDIO** is data out from the device during the data transfer cycle(s), while **SDO** is in a high-impedance state. In 4 pin configuration, **SDO** is data out from the device during the data transfer cycle(s). At the end of the data transfer, SDO outputs low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

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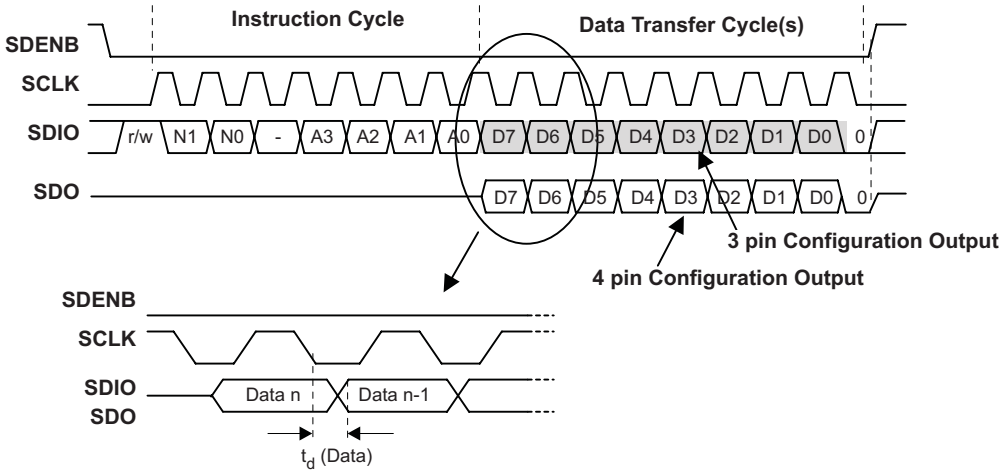


Figure 37. Serial Interface Read Timing Diagram

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7.6 Serial Register Map

Table 4 gives a summary of all the modes that can be programmed through the serial interface.

Table 4. Summary of Functions Supported by Serial Interface

REGISTER ADDRESS IN HEX	REGISTER FUNCTIONS							
Address	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
00	Analog Gain Adjustment bits<11:4>							
01	continued...Analog Gain Adjustment bits<3:0>				3 or 4-pin SPI	SPI Reset	0	0
02	Coarse Clock Phase Adjustment bits<4:0>					0	Clock Divider	Single or Dual Bus
03	Fine Clock Phase Adjustment bits<5:0>						0	Analog Offset bit<8>
04	continued...Analog Offset Control bits<7:0>							
05	Temp Sensor	Powerdown	1	Sync Mode	Data Format	Reference	Stagger Output	0
06	Data output mode		LVDS termination		LVDS current		Force LVDS outputs	
07	0000 0000							
08	Die temperature bits<7:0>							
09	000 0000							Memory error
0A	0000 0000							
0B-16	addresses not implemented, writes have no effect, reads return 0x00							
17	DIE ID<7:0>							
18	DIE ID<15:8>							
19	DIE ID<23:16>							
1A	DIE ID<31:24>							
1B	DIE ID<39:32>							
1C	DIE ID<47:40>							
1D	DIE ID<55:48>							
1E	DIE ID<63:56>							
1F	Die revision indicator<7:0>							

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7.6.1 Description of Serial Registers

Each register function is explained in detail below.

Table 5. Serial Register 0x00 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	Analog Gain Adjustment bits<11:4>							
Defaults	0	0	0	0	0	0	0	0

BIT <7:0>	Analog gain adjustment (most significant 8 bits of a 12 bit word)
	All 12-bits in this adjustment in address 0x00 and 0x01 set to 0000 0000 0000 = fullscale analog input 2.0V_{PP}
	All 12-bits in this adjustment in address 0x00 and 0x01 set to 1111 1111 1111 = fullscale analog input 1.52V_{PP}
	Step adjustment resolution is 120µV.
	Can be used for one-time setting or continual calibration of analog signal path gain.

Table 6. Serial Register 0x01 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x01	Analog Gain Adjustment bits<3:0>				3 or 4-pin SPI	SPI Reset	0	0
Defaults	0	0	0	0	0	0	0	0

BIT <0:1>	RESERVED
0	set to 0 if writing this register
1	do not set to 1

BIT <2>	SPI Register Reset
0	altered register settings are kept
1	resets all SPI registers to defaults (self clearing)

BIT <3>	Set SPI mode to 3- or 4-pin
0	3-pin SPI (read/write on SDIO, SDO not used)
1	4-pin SPI (SDIO is write, SDO is read)

BIT <7:4>	Analog gain adjustment continued (least significant 4 bits of a 12-bit word)
	All 12-bits in this adjustment in address 0x00 and 0x01 set to 0000 0000 0000 = fullscale analog input 2V_{PP}
	All 12-bits in this adjustment in address 0x00 and 0x01 set to 1111 1111 1111 = fullscale analog input 1.52V_{PP}
	Step adjustment resolution is 120µV.
	Can be used for one-time setting or continual calibration of analog signal path gain.

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Table 7. Serial Register 0x02 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x02	Coarse Clock Phase Adjustment bits<4:0>					0	Clock Divider	Single or Dual Bus
Defaults	0	0	0	0	0	0	0	0

BIT <0>	Single or Dual Bus Output Selection
0	dual bus output (A and B)
1	single bus output (A)

BIT <1>	Output Clock Divider
0	CLKOUT equals CLKIN divide by 4 (not available in single bus mode)
1	CLKOUT equals CLKIN divide by 2

BIT <2>	RESERVED
0	set to 0 if writing this register
1	do not set to 1

BIT <7:3> **Input Clock Coarse Phase Adjustment**

Use as a coarse adjustment of input clock phase. The 5-bit adjustment provides a step size of ~2.4ps across a range from code 00000 = 0 ps to code 11111 = 73ps.

Table 8. Serial Register 0x03 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x03	Fine Clock Phase Adjustment bits<5:0>						0	Analog Offset bit<8>
Defaults	0	0	0	0	0	0	0	factory set

BIT <0> **Analog Offset control (most significant bit of 9-bit word)**

All 9-bits in this adjustment in address 0x03 and 0x04 set to 0 0000 0000 = -30mV (TBD)

All 9-bits in this adjustment in address 0x03 and 0x04 set to 1 1111 1111 = +30mV (TBD)

Step adjustment resolution is 120µV (or 1/4 LSB). Adjustments can be used for calibration of analog signal path offset (for instance offset error induced outside of the ADC) or to match multiple ADC offsets.

The default setting for this register is factory set to provide ~0mV of ADC offset in the output codes and is unique for each device.

BIT <1>	RESERVED
0	set to 0 if writing this register
1	do not set to 1

BIT <7:2> **Fine Clock Phase Adjustment**

Use as a fine adjustment of the input clock phase. The 6-bit adjustment provides a step resolution of ~116fs across a range from code 000000 = 0ps to code 111111 = 7.4ps. Can be used in conjuction with Coarse Clock Phase Adjustment in address 0x02.

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Table 9. Serial Register 0x04 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x04	Analog Offset Control bits<7:0>							
Defaults	factory set							

BIT <7:0>	Analog Offset control continued (least significant bits of 9-bit word)
	All 9-bits in this adjustment in address 0x03 and 0x04 set to 0 0000 0000 = -30mV (TBD)
	All 9-bits in this adjustment in address 0x03 and 0x04 set to 1 1111 1111 = +30mV (TBD)
	Step adjustment resolution is 120uV (or 1/4 LSB). Adjustments can be used for calibration of analog signal path offset (for instance offset error induced outside of the ADC) or to match multiple ADC offsets.
	The default setting for this register is factory set to provide ~0mV of ADC offset in the output codes and is unique for each device.
	Performance of the ADC is not specified across the entire offset control range. Some performance degradation is expected as larger offsets are programmed.

Table 10. Serial Register 0x05 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x05	Temp Sensor	Powerdown	reserved	Sync Mode	Data Format	Reference	Stagger Output	0
Defaults	0	0	1	0	0	0	0	0

BIT <0>	RESERVED
0	set to 0 if writing this register
1	do not set to 1
BIT <1>	**Stagger Output Bus**
0	Output bus A and B aligned
1	Output bus A and B staggered (see timing diagrams)
BIT <2>	**Enable External Reference**
0	Enable internal reference
1	Enable external reference
BIT <3>	**Set Data Output Format**
0	Enable offset binary
1	Enable two's complement
BIT <4>	**Set Sync Mode**
0	Disable data synchronization mode
1	Enable data synchronization mode
	When enabled, the OVR pin(s) are replaced with SYNC output signal(s). The SYNC output signal is time-aligned with the output data matching the corresponding input sample and RESET input pulse

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BIT <5>	RESERVED
0	
1	set to 1 if writing this register

BIT <6>	Powerdown
0	device active
1	device in low power mode (sleep mode)

BIT <7>	Temperature Sensor
0	temperature sensor inactive
1	temperature sensor active, independent of powerdown bit in Bit<6>, allows reading of temp sensor while the rest of the ADC is in sleep mode

Table 11. Serial Register 0x06 (Read or Write)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x06	Data output mode		LVDS termination		LVDS current		Force LVDS outputs	
Defaults	0	0	0	0	0	1	0	0

BIT <0:1>	Force LVDS outputs
00 and 01	normal operating mode (LVDS is outputting sampled data bits)
10	forces the LVDS outputs to all logic zeros (data and clock out) - for level check
11	forces the LVDS outputs to all logic ones (data and clock out) - for level check

BIT <3:2>	Set LVDS output current
00	2.5mA
01	3.5mA (default)
10	4.5mA
11	5.5mA

BIT <5:4>	Set Internal LVDS termination differential resistor (for LVDS outputs only)
00 and 01	no internal termination
10	internal 200Ω resistor selected
11	internal 100Ω resistor selected

BIT <7:6>	Control Data Output Mode
00	normal mode (LVDS is outputting sampled data bits)
01	scrambled output mode (D11:D1 is XOR'd with D0)
10	output data is replaced with PRBS test pattern (7-bit sequence)
11	output data is replaced with toggling test pattern (all 1s, then all 0s, then all 1s, etc.....on all bits)

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Table 12. Serial Register 0x08 (Read only)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x08	Die temperature bits<7:0>							
Defaults	depends on reading from temperature sensor							

BIT <7:0> **Die temperature readout**

if enabled in register 0x05. To obtain the die temperature in Celsius, convert the 8-bit word to decimal and subtract 78.

<7:0> = 0x00 = 00000000, measured temperature is 0-78 = -78°C

<7:0> = 0x73 = 01110011, measured temperature is 115 - 78 = 37°C

<7:0> = 0xAF, measured temperature is 175 - 78 = 97°C

Table 13. Serial Register 0x09 (Read only)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x09	000 0000							Memory error
Defaults	000 0000							0

BIT <7:1> **RESERVED**

set to 0 if writing this register

do not set to 1

BIT <0> **Memory Error Indicator**

Registers 0x00 through 0x07 have multiple redundancy. If any copy disagrees with the others, an error is flagged in this bit. This is for systems that require the highest level of assurance that the device remains programmed in the proper state and indication of an error if something changes unexpectedly.

Table 14. Serial Register 0x0A (Read only)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0A	0000 0000							
Defaults	0000 0000							

BIT <7:0> **RESERVED**

set to 0 if writing this register

do not set to 1

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Table 15. Serial Register 0x17 through 0x1E (Read only)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x17 - 0x1E	Die ID							
Defaults	factory set							

BIT <7:0> **Die Identification Bits**

Each of these eight registers contains 8-bits of a 64-bit unique die identifier.

Table 16. Serial Register 0x1F (Read only)

Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x1F	Die Revision Number							
Defaults	factory set							

BIT <7:0> **Die revision**

Provides design revision information.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In the design of any application involving a high-speed data converter, particular attention should be paid to the design of the analog input, the clocking solution, and careful layout of the clock and analog signals. The device evaluation module (EVM) is one practical example of the design of the analog input circuit and clocking solution, as well as a practical example of good circuit board layout practices around the ADC.

8.2 Typical Application

The analog inputs of the ADS5400-SP must be fully differential and biased to an appropriate common mode voltage, VCM. It is rare that the end equipment has a signal that already meets the requisite amplitude and common mode and is fully differential. Therefore, there is a signal conditioning circuit for the analog input. If the amplitude of the input circuit is such that no gain is needed to make full use of the full-scale range of the ADC, then a transformer coupled circuit as used on the EVM may be used with good results. The transformer coupling is inherently low-noise, and inherently AC-coupled so that the signal may be biased to VCM after the transformer coupling.

If signal gain is required, or the input bandwidth is to include the spectrum all the way down to DC such that AC coupling is not possible, then an amplifier-based signal conditioning circuit would be required. shows LMH3401 interfaced with ADS5400-SP. LMH3401 is configured to have to Single-Ended input with a differential outputs follow by 1st Nyquist based low pass filter with 400 MHz bandwidth. Figure 38 also shows the power supply recommendations for the amplifier.

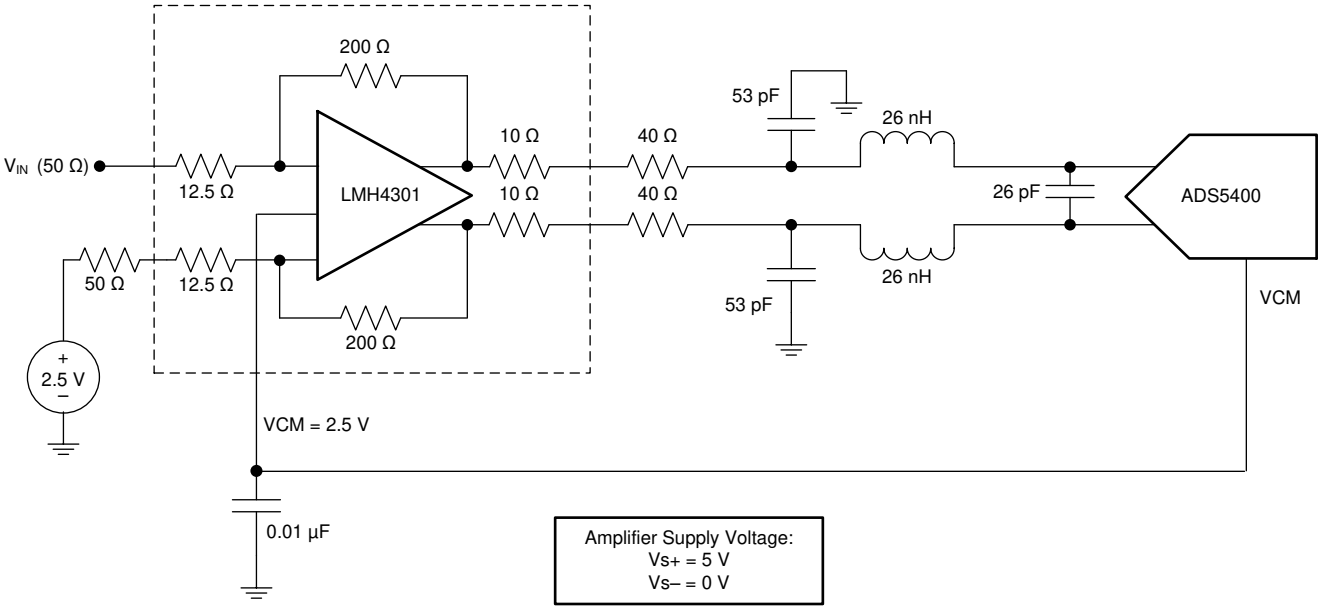


Figure 38. ADS5400-SP Input Circuit Using an LMH3401 Fully Differential Amplifier

Clocking a High Speed ADC such as the ADS5400-SP requires a fully differential clock signal from a clean, low-jitter clock source and driven by an appropriate clock buffer, often with LVPECL or LVDS signaling levels. The sample clock must be biased up to the appropriate common-mode voltage, and the device will internally bias the clock to the appropriate common-mode voltage if the clock signal is AC-coupled as shown in Figure 39.

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Typical Application (continued)

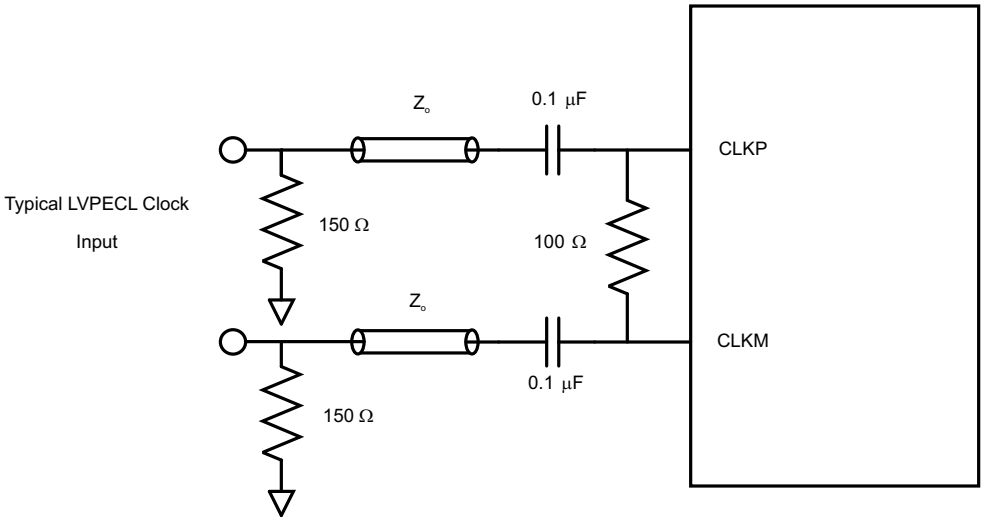


Figure 39. Recommended Differential Clock Driving Circuit

8.2.1 Design Requirements

The ADS5400-SP requires a fully differential analog input with a full-scale range not to exceed 2 V peak to peak differential, biased to a common mode voltage of 2.5 V. In addition the input circuit must provide proper transmission line termination (or proper load resistors in an amplifier-based solution) so the input of the impedance of the ADC analog inputs should be considered as well.

The device is capable of a typical SNR of 58.5 dBFS for input frequencies of about 125 MHz, which is well under the Nyquist limit for this ADC operating at 1000 Msps. The amplifier and clocking solution will have a direct impact on performance in terms of SNR, so the amplifier and clocking solution should be selected such that the SNR performance of at least 58 dBFS is preserved.

8.2.2 Detailed Design Procedure

8.2.2.1 Clocking Source for ADS5400-SP

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise, the thermal noise, and the total jitter of the sample clock. Quantization noise is driven by the resolution of the ADC, which is 12 bits for the ADS5400. Thermal noise is typically not noticeable in high speed pipelined converters such as the ADS5400-SP, but may be estimated by looking at the signal to noise ratio of the ADC with very low input frequencies and using Equation 4 to solve for thermal noise. (For this estimation, we will take thermal noise to be zero. The lowest frequency for which SNR is specified is 125 MHz. If we had an SNR specification for input frequencies around 5 MHz then that SNR would be a good approximation for SNR due to thermal noise. This would be just an approximation, and the lower the input frequency that has an SNR specification the better this approximation would be.) The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies. For ADCs with higher resolution and typical SNR of 75 dBFS or so, thermal noise would be more of a factor in overall performance. Quantization noise is also a limiting factor for SNR, as the theoretical maximum achievable SNR as a function of the number of bits of resolution is set by Equation 3.

$$SNR_{max} = 1.76 + (6.02 \times N) \quad (3)$$

where

- N = number of bits resolution.

For a 12-bit ADC, the maximum SNR = 1.76 + (6.02 × 12) = 74 dB. This is the number that we shall enter into Equation 4 for quantization noise as we solve for total SNR for different amounts of clock jitter using Equation 4.

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Typical Application (continued)

$$SNR_{ADC}\ [dBc] = -20 \times Log\sqrt{\left(10^{\frac{SNR_{Quantization_Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Thermal_Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Jitter}}{20}}\right)^2} \quad (4)$$

The SNR limitation due to sample clock jitter can be calculated by Equation 5.

$$SNR_{Jitter}\left[dBc\right] = -20 \times \log\left(2\pi \times f_{IN} \times t_{Jitter}\right) \quad (5)$$

It is important to note that the clock jitter in Equation 5 is the total amount of clock jitter, whether the jitter source is internal to the ADC itself or external due to the clocking source. The total clock jitter (TJitter) has two components – the internal aperture jitter (125 fs for ADS5400-SP) which is set by the noise of the clock input buffer, and the external clock jitter from the clocking source and all associated buffering of the clock signal. Total clock jitter can be calculated from the aperture jitter and the external clock jitter as in Equation 6.

$$T_{Jitter} = \sqrt{\left(T_{Jitter,Ext.Clock_Input}\right)^2 + \left(T_{Aperture_ADC}\right)^2} \quad (6)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate may at times also improve the ADC aperture jitter slightly.

The device has an internal aperture jitter of 125 fs, which is largely fixed. The SNR depending on amount of external jitter for different input frequencies is shown in Figure 40. Often the design requirements will list a target SNR for a system, and Equation 4 through Equation 6 are then used to calculate the external clock jitter needed from the clocking solution to meet the system objectives.

Figure 40 shows that with an external clock jitter of 200 fs rms, the expected SNR of the device would be greater than 58 dBFS at an input tone of 400 MHz, which is the assumed bandwidth for this design example. Having less external clock jitter such as 150 fs rms or even 100 fs rms would result in an SNR that would exceed our design target, but at possibly the expense of a more costly clocking solution. Having external clock jitter of much greater than 200 fs rms or more would fail to meet our design target.

8.2.2.2 Amplifier Selection

The amplifier and any input filtering will have its own SNR performance, and the SNR performance of the amplifier front end will combine with the SNR of the ADC itself to yield a system SNR that is less than that of the ADC itself. System SNR can be calculated from the SNR of the amplifier conditioning circuit and the overall ADC SNR as in Equation 7. In Equation 7, the SNR of the ADC would be the value derived from the datasheet specifications and the clocking derivation presented in the previous section.

$$SNR_{System} = -20 \cdot \log\sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{Amp+Filter}}{20}}\right)^2} \quad (7)$$

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the noise specifications in the datasheet for the amplifier, the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter and the rolloff of the filter will depend on the order of the filter, so it is convenient to replace the filter rolloff with an equivalent brick-wall filter bandwidth. For example, a 1st order filter may be approximated by a brick-wall filter with bandwidth of 1.57 times the bandwidth of the 1st order filter. Assume a 1st order filter for this design. The amplifier and filter noise can be calculated using Equation 8.

$$SNR_{Amp+Filter} = 10 \times \log\left(\frac{V_O{}^2}{E^2_{FILTEROUT}}\right) = 20 \times \log\left(\frac{V_O}{E_{FILTEROUT}}\right)$$

where

- V_O= the amplifier output signal (which will be full scale input of the ADC expressed in rms)
- $E_{FILTEROUT} = E_{NAMPOUT} \times \sqrt{ENB}$
  - $E_{NAMPOUT}$ = the output noise density of the LMH3401 (3.4 nV/$\sqrt{Hz}$)
  - E_{NB} = the brick-wall equivalent noise bandwidth of the filter (8)

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Typical Application (continued)

In Equation 8, the parameters of the equation may be seen to be in terms of signal amplitude in the numerator and amplifier noise in the denominator, or SNR. For the numerator, use the full scale voltage specification of the ADS5400-SP, or 2 V peal to peak differential. Because Equation 8 requires the signal voltage to be in rms, convert 2 V_{PP} to 0.706 V rms.

The noise specification for the LMH3401 is listed as 3.4 nV/$\sqrt{Hz}$, therefore, use this value to integrate the noise component from DC out to the filter cutoff, using the equivalent brick wall filter of 400 MHz × 1.57, or 628 MHz. 3.4 nV/$\sqrt{Hz}$ integrated over 628 MHz yields 85204 nV, or 85.204 µV.

Using 0.706 V rms for V_O and 85.204 µV for $E_{FILTEROUT,}$ (see Equation 8) the SNR of the amplifier and filter as given by Equation 8 is approximately 78.4 dB.

Taking the SNR of the ADC as 58.8 dB from Figure 40, and SNR of the amplifier and filter as 78.4 dB, Equation 7 predicts the system SNR to be 58.75 dB. In other words, the SNR of the ADC and the SNR of the front end combine as the square root of the sum of squares, and because the SNR of the amplifier front end is much greater than the SNR of the ADC in this example, the SNR of the ADC dominates Equation 7 and the system SNR is almost the same as the SNR of the ADC. The assumed design requirement is 58 dB, and after a clocking solution was selected and an amplifier or filter solution was selected, the predicted SNR is 58.75 dBFS.

8.2.3 Application Curve

Figure 40 shows the SNR of the ADC as a function of clock jitter and input frequency for the device. This plot of curves take into account the aperture jitter of the ADC, the number of bits of resolution, and the thermal noise estimation so that Figure 40 may be used to predict SNR for a given input frequency and external clock jitter. Figure 40 then may be used to set the jitter requirement for the clocking solution for a given input bandwidth and given design goal for SNR.

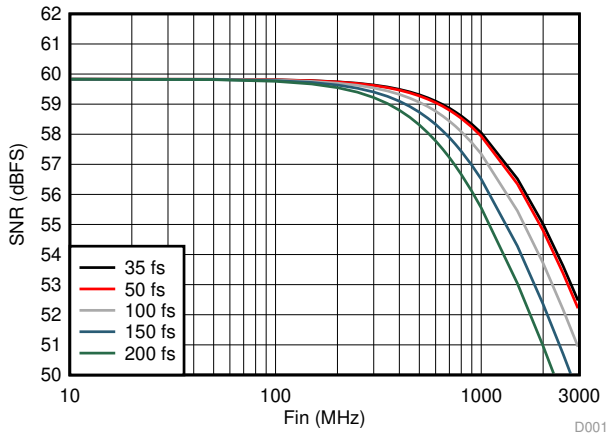


Figure 40. SNR vs Input Frequency and External Clock Jitter

9 Power Supply Recommendations

The ADS5400-SP uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies generate more noise components that can be coupled to the ADS5400-SP. The PSRR value and the plot shown in Figure 41 were obtained without bulk supply decoupling capacitors. When bulk (0.1 μF) decoupling capacitors are used, the board-level PSRR is much higher than the stated value for the ADC. The power consumption of the device does not change substantially over clock rate or input frequency as a result of the architecture and process.

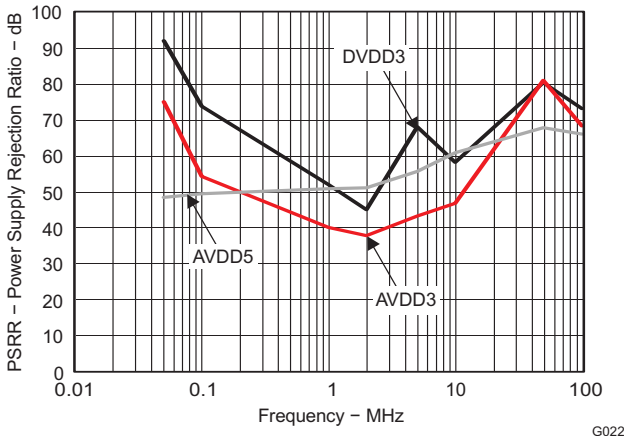


Figure 41. PSRR versus Supply Injected Frequency

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10 Layout

10.1 Layout Guidelines

The evaluation board provides a guideline of how to lay out the board to obtain the maximum performance from the ADS5400-SP. General design rules, such as the use of multilayer boards, single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors, should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications where low jitter is required like high IF sampling. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device. The thermal heat sink should be soldered to the board as described in the section.

Figure 42 is a section of the layout of the ADS5400-SP that illustrates good layout practices for the clocking, analog input, and digital outputs. In this example, the analog input enters from the top left while the clocking enters from the left center, keeping the clock signal away from the analog signals so as to not allow coupling between the analog signal and the clock signal. One thing to notice on the layout of the differential traces is the symmetry of the trace routing between the two sides of the differential signals.

The digital outputs are routed off to the right, so as to keep the digital signals away from the analog inputs and away from the clock. Notice the circuitous routing added to some of the LVDS differential traces but not to others; this is the equalize the lengths of the routing across all of the LVDS traces so as to preserve the setup/hold timing at the end of the digital signal routings. If the timing closure in the receiving device (such as an FPGA or ASIC) has enough timing margin, then the circuitous routing to equalize trace lengths may not be necessary.

10.2 Layout Example

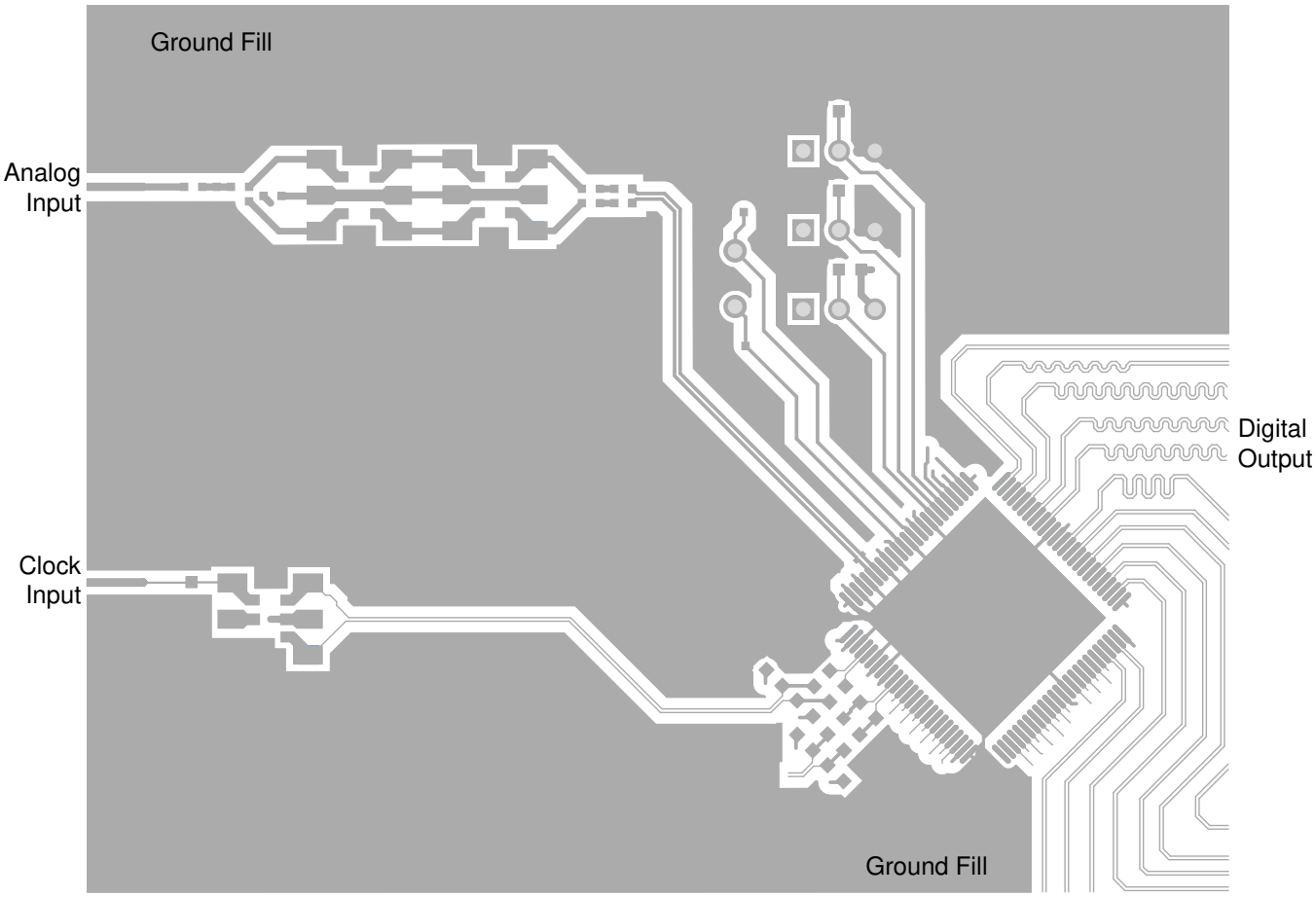


Figure 42. Example Layout of AS5400-SP

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Definition of Specifications

Analog Bandwidth
The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Delay
The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay

Clock Pulse Duration/Duty Cycle
The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR)
CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB)
ENOB is a measure in units of bits of a converter's performance as compared to the theoretical limit based on quantization noise

$$\text{ENOB} = (\text{SINAD} - 1.76)/6.02 \tag{9}$$

Gain Error
Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL)
INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error
Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR)
PSRR is a measure of the ability to reject frequencies present on the power supply. The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$\text{SNR} = 10\text{Log}_{10}\frac{P_S}{P_N} \tag{10}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

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Device Support (continued)

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10} \frac{P_S}{P_N + P_D} \quad (11)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10Log_{10} \frac{P_s}{P_N} \quad (12)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

11.2 Documentation Support

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0924001VXC	Active	Production	CFP (HFS) | 100	1 | OTHER	ROHS Exempt	AU	N/A for Pkg Type	-55 to 125	(5962-, ADS5400MHFSV) 0924001VXC ADS5400MHFS-V
ADS5400HFS/EM	Active	Production	CFP (HFS) | 100	1 | OTHER	ROHS Exempt	AU	N/A for Pkg Type	25 to 25	ADS5400HFS/EM EVAL ONLY
ADS5400MHFSV	Active	Production	CFP (HFS) | 100	1 | OTHER	ROHS Exempt	AU	N/A for Pkg Type	-55 to 125	(5962-, ADS5400MHFSV) 0924001VXC ADS5400MHFS-V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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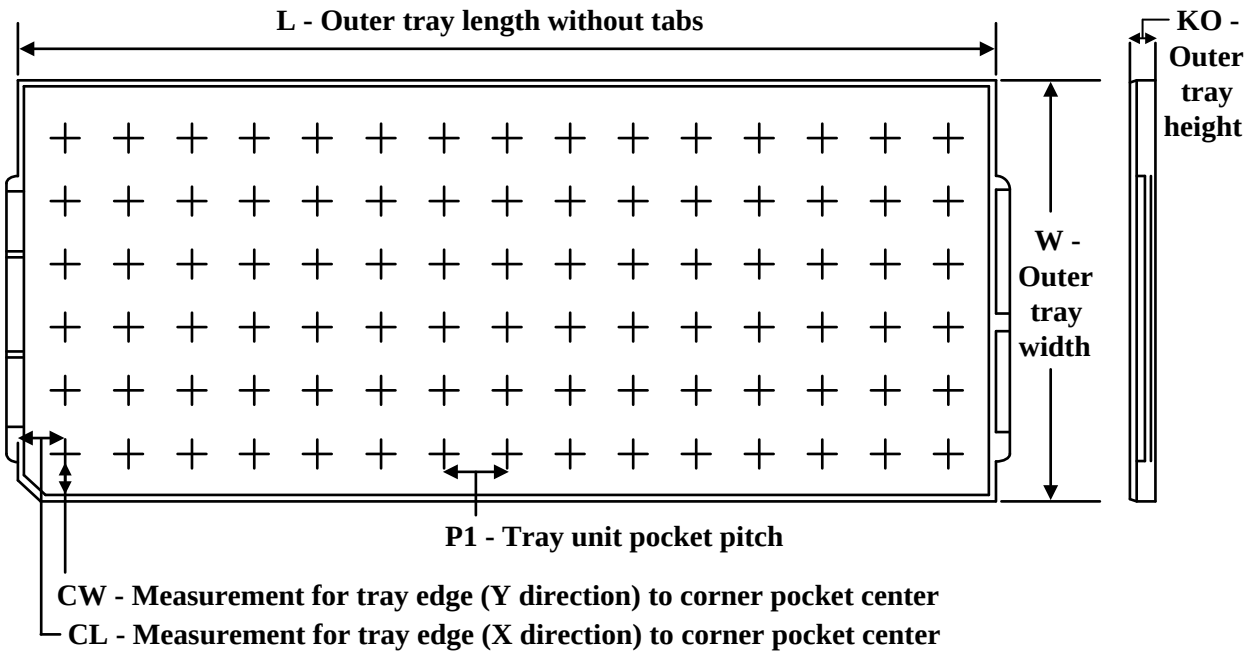
OTHER QUALIFIED VERSIONS OF ADS5400-SP :

- Catalog : ADS5400

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TRAY

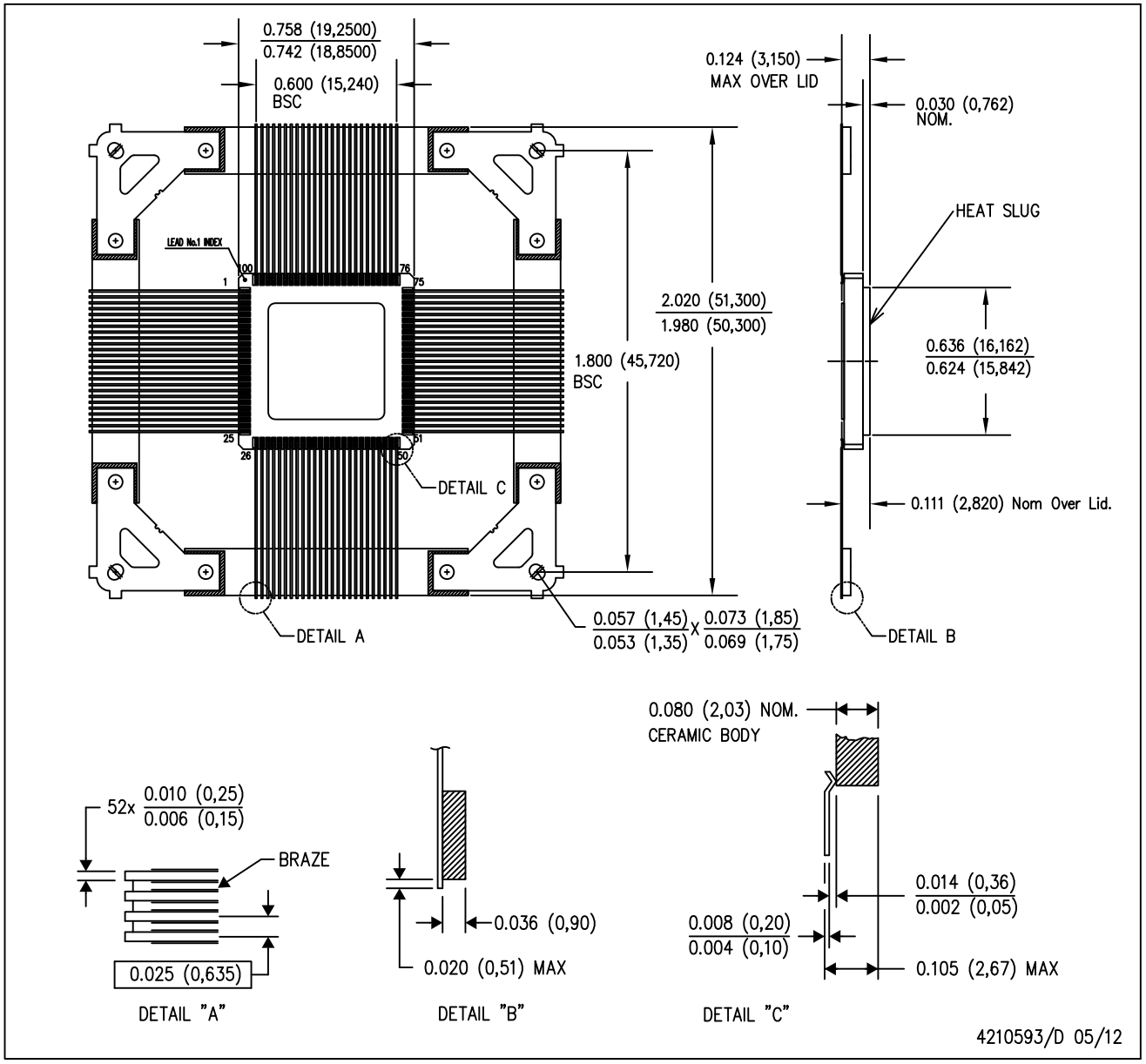


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-0924001VXC	HFS	CFP (TBAR)	100	1	2 x 5	150	315	135.9	7620	57	43.5	39.45
ADS5400HFS/EM	HFS	CFP (TBAR)	100	1	2 x 5	150	315	135.9	7620	57	43.5	39.45
ADS5400MHFSV	HFS	CFP (TBAR)	100	1	2 x 5	150	315	135.9	7620	57	43.5	39.45

HFS (S–CQFP–F100) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

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