ADS5263 四通道、16 位、100MSPS 高 SNR ADC

1 特性

- 最大采样率：100MSPS
- 可编程器件分辨率
  - 四通道，16 位，高 SNR 模式
  - 四通道，14 位，低功耗模式
- 16 位高 SNR 模式
  - 100MSPS 时总体功耗为 1.4W
    - 每通道 355mW
  - 4 Vpp 满量程输入
  - $f_{输入}$= 3MHz，100MSPS 时，85dBFS SNR
- 14 位低功耗模式
  - 100MSPS 下总体功耗 785mW
    - 每通道 195mW
  - 2 Vpp 满量程输入
  - $f_{输入}$= 10MHz，74dBFS SNR
  - 集成钳位（用于与电荷耦合元件 (CCD) 传感器对接）
- 低频噪声抑制
- 数字处理块
  - 可编程 FIR 抽取滤波器
  - 可编程数字增益：0dB 至 12dB
  - 平均 2 或 4 通道
- ADC 输入通道与低压差分信令 (LVDS) 输出引脚间的可编程映射 - 简化了电路板设计
- 多种测试模式以验证现场可编程栅极阵列 (FPGA) / 接收器的数据捕捉
- 已串化 LVDS 输出
- 内部和外部基准
- 3.3V 模拟电源
- 1.8V 数字电源
- 在 1 个时钟周期内从 6dB 过载内恢复
- 封装：
  - 9mm × 9mm 64 引脚四方扁平无引线 (QFN)
  - 针对磁共振成像 (MRI) 系统的非磁性封装选项
- CMOS 技术

2 应用

- 医疗成像 - MRI
- 光谱分析
- CCD 成像

3 说明

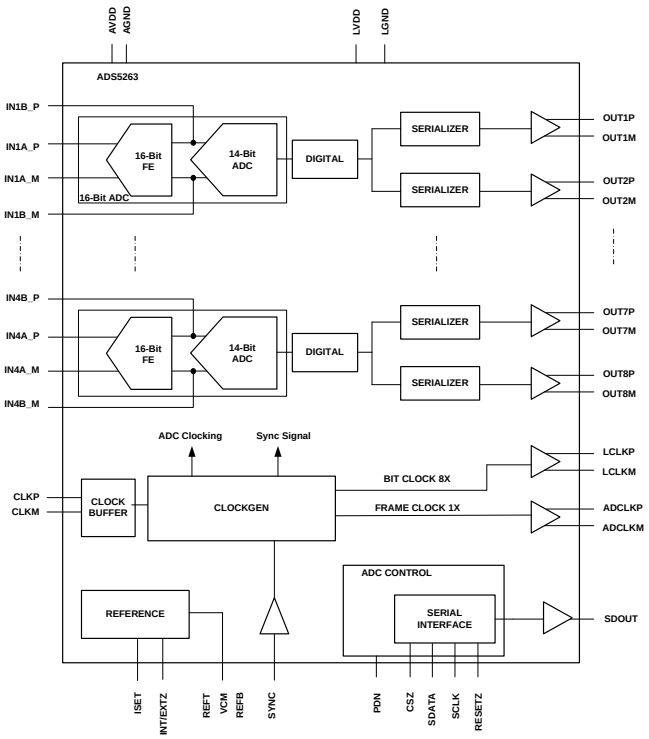
通过使用 CMOS 工艺技术和创新型电路技术，ADS5263 被设计用来在低功耗下运行，并且在 4 Vpp 满量程输入时提供极高的 SNR 性能。通过使用一个低噪声 16 位模拟前端级，之后是一个 14 位 ADC，此器件提供高达 10MHz 的 85dBFS SNR，以及高达 30MHz，优于 80dBFS 的 SNR。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS5263	VQFN (64)	9.00mm x 9.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

ADS5263 框图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 说明 （续） ... 5
6 **Pin Configuration and Functions** ... 6
7 **Specifications** ... 8
7.1 Absolute Maximum Ratings ... 8
7.2 ESD Ratings ... 8
7.3 Recommended Operating Conditions ... 8
7.4 Thermal Information ... 9
7.5 Electrical Characteristics, Dynamic Performance – 16-Bit ADC ... 9
7.6 Electrical Characteristics, General – 16-Bit ADC Mode ... 10
7.7 Electrical Characteristics, Dynamic Performance – 14-Bit ADC ... 11
7.8 Digital Characteristics ... 12
7.9 Timing Requirements ... 12
7.10 LVDS Timing at Lower Sampling Frequencies - 2 Wire, 8× Serialization ... 13
7.11 LVDS Timing for 1 Wire 16× Serialization ... 13
7.12 LVDS Timing for 2 Wire, 7× Serialization ... 13
7.13 LVDS Timing for 1 Wire, 14× Serialization ... 13
7.14 Serial Interface Timing Requirements ... 14
7.15 Reset Switching Characteristics ... 14
7.16 Typical Characteristics ... 17
8 **Detailed Description** ... 25
8.1 Overview ... 25
8.2 Functional Block Diagram ... 26
8.3 Feature Description ... 27
8.4 Device Functional Modes ... 41
8.5 Programming ... 43
8.6 Register Maps ... 44
9 **Application and Implementation** ... 62
9.1 Application Information ... 62
9.2 Typical Applications ... 70
10 **Power Supply Recommendations** ... 71
11 **Layout** ... 72
11.1 Layout Guidelines ... 72
11.2 Layout Example ... 73
12 器件和文档支持 ... 74
12.1 器件支持 ... 74
12.2 社区资源 ... 75
12.3 商标 ... 75
12.4 静电放电警告 ... 75
12.5 Glossary ... 76
13 机械、封装和可订购信息 ... 76
13.1 封装 ... 76

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (January 2013) to Revision D **Page**

- Added Register 57 in *Register Maps* ... 45
- Added Register CB in *Register Maps* ... 45
- Added Typical Applications section ... 70
- Added Layout section ... 72
- Deleted Ordering Information table. See POA at the end of the data sheet. ... 73

Changes from Revision B (October 2011) to Revision C **Page**

- Changed Pin 54 From: REFB To: NC ... 7
- Changed Pin 55 From: REFC To: NC ... 7
- Changed the VCM Pin description To: "Internal reference mode: Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input External reference mode: Apply voltage input that sets the reference for ADC operation." From: "Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input pins." ... 7
- Added "Idle channel noise" To SNR ... 9
- Added "Idle channel noise" To LSB ... 9
- Changed the INL values- 100 MSPS From: TYP = ±2.2 To: ±5, Added MAX = ±12 ... 9
- to Changed the INL values- 80 MSPS From: TYP = ±2.2 To: ±5 ... 9
- Added From: VCM common-mode output voltage To: VCM common-mode output voltage, Internal reference mode ... 10
- Added From: VCM output current capability To: VCM output current capability, Internal reference mode ... 10
- Added From: VCM input voltage To: VCM input current, external reference mode ... 10

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- Added VCM input current, external reference mode Typical value - 80 MSPS of 0.5 10
- Changed E_{GREF} - 100 MSPS MIN value From: ±2.5 To: ±1 10
- Added Temperature Coefficient to E_{GREF} 10
- Added Temperature Coefficient to E_{GCHAN} 10
- Changed SNR f_{in} = 5 MHz MIN value From: 68.8 To: to 67.5 11
- Added t_A Aperture delay to the Timing Requirements Table 12
- Changed From: 2 WIRE, 16× SERIALIZATION To: 2 WIRE, 8× SERIALIZATION 12
- Added 100 MSPS to the SAMPLING FREQUENCY, MSPS column of LVDS Timing at Lower Sampling Frequencies - 2 Wire, 8× Serialization 13
- Changed to 8x from 16x 13
- Changed LVDS Timing for 2 Wire, 7× Serialization title From: LVDS Timing for 2 Wire, 14× Serialization To: LVDS Timing for 2 Wire, 7× Serialization 13
- Changed the Digital Filter Section 28
- Changed Table 9 Description From: Reference voltage must be forced on REFT and REFB pins To: Apply voltage on VCM pin to set the references for ADC operation 41
- Table 10 Added: <EN_HIGH_ADDRS> as bit D4. Added: Register 0x09 to Serial Register Ma; 44
- Table 10 Added: Register bit EXT_REF_VCM. Added: D12 <18x SERIALIZATION> 44
- Table 10 Added: new register entries from Address 5A to 89. Added: new register F0 44
- Added D4 <EN_HIGH_ADDRS> 46
- Added Added register description table (D10 <EN_CLAMP>) for register 0x09 47
- Added description for register EXT_REF_VCM 54
- Added Description for <EN_REG_42>, <PHASE_DDR> and EXT_REF_VCM 54
- Added Decsription for 18b SERIALIZATION 56
- Changed D11, D10, and D5 To: SERIALIZATION From: SERIAL'N 56
- Changed the register for A7-A0 IN HEX 59
- Added description for register F0 for A7–A0 IN HEX 60
- Replaced the Clamp Function section with the Clamp Functon for CCD Signals section 64
- Deleted Figure - CCD Sensor Connections 67
- Added External Reference Mode 68

Changes from Revision A (August 2011) to Revision B **Page**

- Added new Figure below Figure 16 18
- Added new Figure below Figure 22 (now Figure 24) 19
- Added new section below Digital Averaging titled: Performance with Didgital Processing Blocks 34
- Added listitem 6. to the OUTPUT LVDS INTERFACE section 36
- Added Added new figure in section Output LVDS Interface (Figure 55) 38
- Added new section after Output LVDS Interface titled: Programmable LCLK Phase, also 2 new figures added. 40
- Added register 42 between register 38 and register 45 54
- Added new figure 52 in Large and Smll Signal Input Bandwidth section 64

Changes from Original (May 2011) to Revision A **Page**

- 已添加“针对磁共振成像 (MRI) 系统的非磁性封装选项”至 特性 1
- 已更改 特性 列表项 - 由“100MSPS 时的总功耗为 1.35W”改为“100MSPS 时的总功耗为 1.4W” 1
- 已更改 特性 列表项 - 由“每通道 338mW”改为“每通道 355mW” 1
- Changed the CLOCK INPUT values in the ROC table 8
- Changed the ELECTRICAL CHARACTERISTICS, DYNAMIC PERFORMANCE – 16-BIT ADC table 9

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- Changed the ELECTRICAL CHARACTERISTICS, GENERAL – 16-BIT ADC MODE table 10
- Added the ELECTRICAL CHARACTERISTICS, DYNAMIC PERFORMANCE – 14-BIT ADC table 11
- Changed the values in DIGITAL OUTPUTS – LVDS INTERFACE 12
- Added LVDS Timing for 1 Wire 16× Serialization, LVDS Timing for 2 Wire, 7× Serialization, and LVDS Timing for 1 Wire, 14× Serialization 13
- Added Figure 25, Figure 26, and Figure 27 20
- Added section - Large and Small Signal Input Bandwidth 63
- Added Section - Board Design Considerations 73
- Added Package Marking ADS5263NM and Ordering Number ADS5263IRGC-NM 73
- 已添加“技术规范定义”部分 74
- 已添加“封装”部分 76

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5 说明（续）

ADS5263 具有 14 位低功耗模式，其在此模式下作为一个四通道 14 位 ADC 运行。16 位前端级被断电，与 16 位模式相比，此部件的能耗大约为一半。14 位模式支持一个 2 Vpp 满量程输入信号，此时 SNR 典型值为 74dBFS。ADS5263 可在两个分辨率模式间自动切换。这使得系统能够使用高分辨率、高功耗模式或者一个低分辨率、低功耗模式中的同一部件。

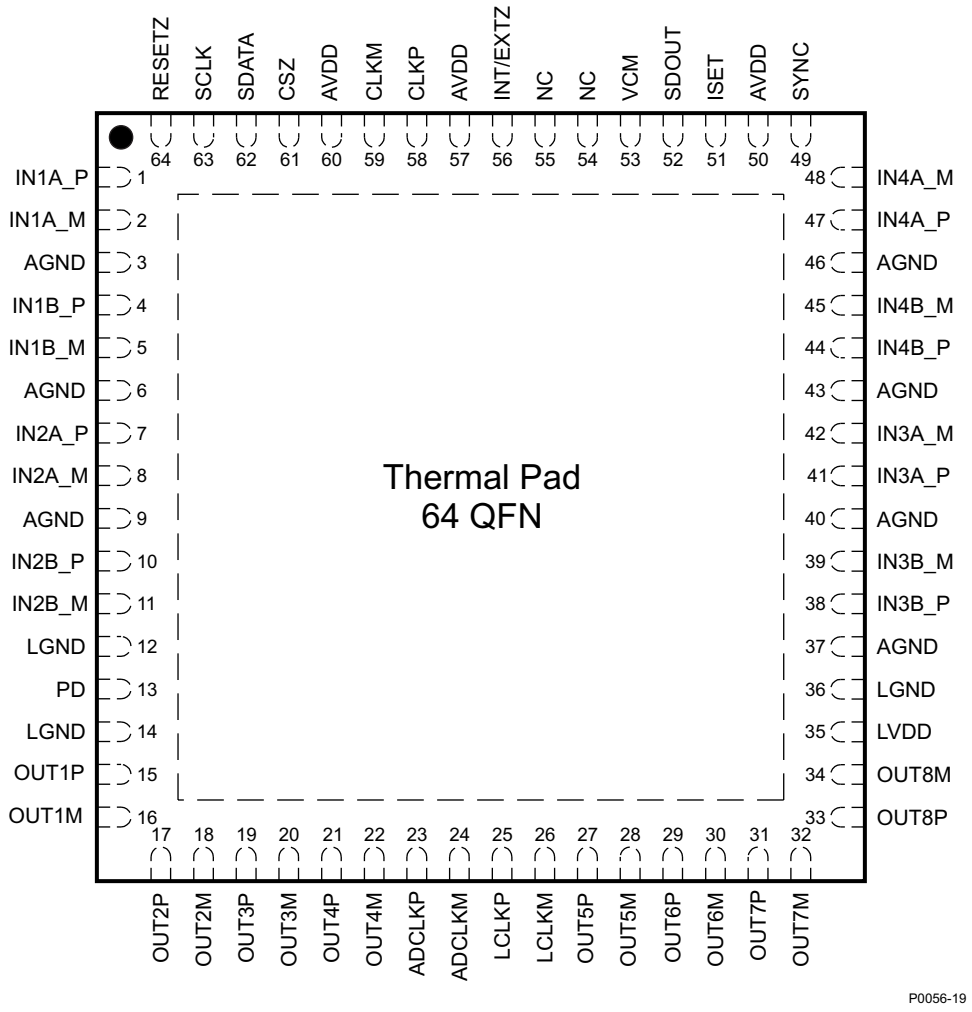
该器件还配有一个数字处理模块，其中集成数字增益（最高可达 12dB）等多种常用数字功能。它包括一个数字滤波器模块，此模块具有内置的抽取滤波器（具有低通、高通和带通特点）。此抽取率也是可编程的（2 倍，4 倍或 8 倍）。这使得该器件非常适用于窄带 应用，因为滤波器可为此类应用提高 SNR 并滤除谐波，同时降低输出数据速率。

此器件包括一个平均模式，在此模式中，可将两个通道（或四个通道）平均来改进 SNR。一个非常独特的特性是可以实现输入通道和 LVDS 输出引脚间灵活映射的可编程映射器模块。这有助于大大减少 LVDS 输出路径选择的复杂程度，并且有可能通过减少印刷电路板 (PCB) 的层数来获得更加廉价的系统电路板。该器件在 -40°C 至 85°C 的工业级温度范围内运行。

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6 Pin Configuration and Functions

QFN Package
64-Pin With Thermal Pad
Top View



P0056-19

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADCLKM	24	O	LVDS frame clock (1X) – negative output
ADCLKP	23	O	LVDS frame clock (1X) – positive output
AGND	3, 6, 9, 37, 40, 43, 46	I	Analog ground
AVDD	50, 57, 60	I	Analog power supply, 3.3 V
CLKM	59	I	Negative differential clock input. For single-ended clock, tie CLKM to ground.
CLKP	58	I	Positive differential clock input
$\overline{CS}$	61	I	Serial interface enable input, active LOW. The pin has an internal 300-kΩ pulldown resistor to ground
IN1A_P, IN1A_M	1, 2	I	Differential analog input for channel 1, 16 bit ADC
IN1B_P, IN1B_M	4, 5	I	Differential analog input for channel 1, 14 bit ADC
IN2A_P, IN2A_M	7, 8	I	Differential analog input for channel 2, 16 bit ADC
IN2B_P, IN2B_M	10, 11	I	Differential analog input for channel 2, 14 bit ADC
IN3A_P, IN3A_M	41, 42	I	Differential analog input for channel 3, 16 bit ADC
IN3B_P, IN3B_M	38, 39	I	Differential analog input for channel 3, 14 bit ADC

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN4A_P, IN4A_M	47, 48	I	Differential analog input for channel 4, 16 bit ADC
IN4B_P, IN4B_M	44, 45	I	Differential analog input for channel 4, 14 bit ADC
$\overline{\text{INT/EXT}}$	56	I	Internal/external reference mode select input Logic HIGH –internal reference Logic LOW – external reference
ISET	51	I	Bias pin – 56.2 kΩ resistor (1% tolerance value) to ground
LCLKM	26	O	LVDS bit clock (8X) – negative output
LCLKP	25	O	LVDS bit clock (8X) – positive output
LGND	12, 14, 36	I	Digital ground
LVDD	35	I	Digital and I/O power supply, 1.8 V
OUT1P, OUT1M	15, 16	O	Wire 1, channel 1 LVDS differential output
OUT2P, OUT2M	17, 18	O	Wire 2, channel 1 LVDS differential output
OUT3P, OUT3M	19, 20	O	Wire 1, channel 2, LVDS differential output
OUT4P, OUT4M	21, 22	O	Wire 2, channel 2 LVDS differential output
OUT5P, OUT5M	27, 28	O	Wire 1, channel 3 LVDS differential output
OUT6P, OUT6M	29, 30	O	Wire 2, channel 3 LVDS differential output
OUT7P, OUT7M	31, 32	O	Wire 1, channel 4 LVDS differential output
OUT8P, OUT8M	33, 34	O	Wire 2, channel 4 LVDS differential output
PD	13	I	Power-down input
NC	54, 55		Do not connect
$\overline{\text{RESET}}$	64	I	Serial interface RESET input, active LOW. When using the serial interface mode, the user ***must*** initialize internal registers through hardware RESET by applying a low-going pulse on this pin or by using software reset option. See the *Serial Interface* section.
SCLK	63	I	Serial interface clock input. The pin has an internal 300-kΩ pulldown resistor.
SDATA	62	I	Serial interface data input. The pin has an internal 300-kΩ pulldown resistor.
SDOUT	52	O	Serial register readout This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOUT pin becomes active. This is a CMOS digital output running from the AVDD supply.
SYNC	49	I	Input signal to synchronize channels and chips when used with reduced output data rates **Alternate function:** Clamp signal input (14-bit ADC mode only)
VCM	53	IO	**Internal reference mode:** Outputs the common-mode voltage (1.5 V) that can be used externally to bias the analog input. **External reference mode:** Apply voltage input that sets the reference for ADC operation.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, AVDD	–0.3	3.9	V
Supply voltage, LVDD	–0.3	2.2	V
Voltage between AGND and DRGND	–0.3	0.3	V
Voltage applied to analog input pins – INP_A, INM_A, INP_B, INM_B	–0.3	minimum (3.6, AVDD + 0.3 V)	V
Voltage applied to input pins – CLKP, CLKM, RESET, SCLK, SDATA, CSZ	–0.3	AVDD + 0.3	V
Voltage applied to reference input pins	–0.3	2.8	V
Operating free-air temperature, T_A	–40	85	°C
Operating junction temperature, T_J		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3	3.3	3.6	V
LVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage	16-bit ADC mode		4		V_{PP}
		14-bit ADC mode		2		V_{PP}
	Input common-mode voltage			1.5 ±0.1		V
	Maximum analog input frequency	4-Vpp input amplitude, 16-bit ADC mode		70		MHz
		2-Vpp input amplitude, 16-bit ADC mode		140		
CLOCK INPUT						
	Input clock sample rate		10		100	MSPS
	Input clock amplitude differential (VCLKP-VCLKM)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled	0.2	1.6		V_{PP}
		LVDS, ac-coupled	0.2	0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
	Operating free-air temperature, T_A		–40		85	°C

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7.4 Thermal Information

THERMAL METRIC[1]		ADS5263 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, Dynamic Performance – 16-Bit ADC

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted); MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, LVDD = 1.8 V

PARAMETERS	TEST CONDITIONS	100 MSPS			80 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SNR Idle channel noise	With inputs tied to common-mode VCM		87.5			87.5		dBFS
LSB Idle channel noise	With inputs tied to common-mode VCM		0.98			0.98		rms
SNR Signal-to-noise ratio	f_{in} = 5 MHz at 25°C	81	84.5			85.5		dBFS
	f_{in} = 5 MHz across temperature	80						
	f_{in} = 10 MHz		84.6			85.3		
	f_{in} = 30 MHz		82.7			83.1		
	f_{in} = 65 MHz		78.9			79.4		
SINAD Signal-to-noise and distortion ratio	f_{in} = 5 MHz	76.6	78.2			78.8		dBFS
	f_{in} = 10 MHz		77.5			79		
	f_{in}n = 30 MHz		74.8			76		
	f_{in} = 65 MHz		71.6			72.5		
ENOB Effective number of bits	f_{in} = 5 MHz		12.7			12.8		LSB
DNL Differential non-linearity	f_{in} = 5 MHz		±0.1			±0.1		LSB
INL Integrated non-linearity	f_{in} = 5 MHz Changed the INL values 100 MSPS From: TYP = ±2.2 To: ±5, Added MAX = ±12		±5	±12		±5		LSB
SFDR Spurious-free dynamic range	f_{in} = 5 MHz	73.5	80			80		dBc
	f_{in} = 10 MHz		80			81		
	f_{in} = 30 MHz		76			77		
	f_{in} = 65 MHz		74			75		
THD Total harominc distortion	f_{in} = 5 MHz	72.5	78			78.8		dBc
	f_{in} = 10 MHz		77.4			79.2		
	f_{in} = 30 MHz		74.5			76		
	f_{in} = 65 MHz		71.4			72.4		
HD2 Second harmonic Distortion	f_{in} = 5 MHz	73.5	83.5			85		dBc
	f_{in} = 10 MHz		81			84		
	f_{in} = 30 MHz		80			83		
	f_{in} = 65 MHz		75			76		

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Electrical Characteristics, Dynamic Performance – 16-Bit ADC (continued)

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted); MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, LVDD = 1.8 V

PARAMETERS	TEST CONDITIONS	100 MSPS			80 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
HD3 Third harmonic distortion	f_{in} = 5 MHz	73.5	80			80		dBc
	f_{in} = 10 MHz		80			81		
	f_{in} = 30 MHz		75			77		
	f_{in} = 65 MHz		74			75		
Worst Spur Excluding HD2, HD3	f_{in} = 5 MHz		80			90		dBc
	f_{in} = 10 MHz		85			90		
	f_{in}n = 30 MHz		85			88		
	f_{in} = 65 MHz		82			86		
IMD 2-tone intermodulation distortion	f_1 = 8 MHz, f_2 = 10 MHZ, each tone at –7 dBFS		92			92		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1		clock cyles
PSRR AC power supply rejection ratio	For 50 mV signal on AVDD supply, up to 1 MHz ripple frequency		30			30		dB

7.6 Electrical Characteristics, General – 16-Bit ADC Mode

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input (unless otherwise noted); MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, LVDD = 1.8V

PARAMETERS		100 MSPS			80 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
	Differential input voltage range (0-dB gain)		4			4		Vpp
	Differential input resistance (at dc)		2.5			2.5		kΩ
	Differential input capacitance		12			12		pF
	Analog input bandwidth		700			700		MHz
	Analog input common-mode current (per input pin)		8			8		µA/MSPS
	VCM common-mode output voltage, Internal reference mode		1.5			1.5		V
	VCM output current capability, Internal reference mode		3			3		mA
	VCM input voltage, external reference mode	1.45	1.5	1.55	1.45	1.5	1.55	V
	VCM input current, external reference mode		0.5			0.5		mA
DC ACCURACY								
	Offset error		±10	±30		±10		mV
E_{GREF}	Gain error due to internal reference inaccuracy alone	±1	±0.5	1		±0.5		% FS
E_{GREF} Temperature Coefficient	Internal reference mode		0.002			0.002		Δ%/°C
	External l reference mode		0.001			0.001		Δ%/°C
E_{GCHAN}	Gain error of channel alone		1			1		% FS
E_{GCHAN} Temperature Coefficient			0.002			0.002		Δ%/°C
	Gain matching		0.5%			0.5%		

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Electrical Characteristics, General – 16-Bit ADC Mode (continued)

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input (unless otherwise noted); MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, LVDD = 1.8V

PARAMETERS		100 MSPS			80 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
IAVDD	Analog supply current		370	390		290		mA
ILVDD	Digital and output buffer supply current with 100-Ω external LVDS termination		110	150		100		mA
	Analog power		1.22			0.96		W
	Digital power		0.2			0.18		W
	Global power down		63	110		63		mW
	Standby		208	250		208		mW

7.7 Electrical Characteristics, Dynamic Performance – 14-Bit ADC

Typical values are at 25°C, AVDD = 3.3V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input (unless otherwise noted); MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, LVDD = 1.8 V

PARAMETERS	TEST CONDITIONS	100 MSPS			UNIT
		MIN	TYP	MAX	
SNR Signal-to-noise ratio	f_{in} = 5 MHz	67.5	74		dBFS
	f_{in}v = 30 MHz		73		
	f_{in} = 65 MHz		71.3		
SINAD Signal-to-noise and distortion ratio	f_{in} = 5 MHz	65.8	73.5		dBFS
	f_{in} = 30 MHz		71.9		
	f_{in}n = 65 MHz		70.3		
SFDR Spurious-free dynamic range	f_{in} = 5 MHz	71.8	85		dBc
	f_{in} = 30 MHz		81		
	f_{in} = 65 MHz		78		
THD Total harmonic distortion	f_{in} = 5 MHz	69	83.5		dBc
	f_{in} = 30 MHz		78		
	f_{in} = 65 MHz		76.5		
HD2 Second harmonic Distortion	f_{in} = 5 MHz	71.8	92		dBc
	f_{in} = 30 MHz		84		
	f_{in} = 65 MHz		80		
HD3 Third harmonic distortion	f_{in} = 5 MHz	71.8	85		dBc
	f_{in} = 30 MHz		81		
	f_{in} = 65 MHz		78		

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7.8 Digital Characteristics

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3V, LVDD = 1.8V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS – $\overline{\text{RESET}}$, SCLK, SDATA, $\overline{\text{CS}}$, PDN, SYNC, $\overline{\text{INT/EXT}}$							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels.	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	SDATA, SCLK, $\overline{\text{CS}}$ (1)	V_{HIGH} = 1.8 V		5		µA
I_{IL}	Low-level input current	SDATA, SCLK, $\overline{\text{CS}}$	V_{LOW} = 0 V		0		µA
DIGITAL CMOS OUTPUT – SDOUT							
V_{OH}	High-level output voltage		I_{OH} = 100 µA		AVDD – 0.05		V
V_{OL}	Low-level output voltage		I_{OL} = 100 µA		0.05		V
DIGITAL OUTPUTS – LVDS INTERFACE (OUT1P/M TO OUT8P/M, ADCLKP/M, LCLKP/M)							
V_{ODH}	High-level output differential voltage		With external 100-Ω termination	275	370	465	mV
V_{ODL}	Low-level output differential voltage		With external 100-Ω termination	–465	–370	–275	mV
V_{OCM}	Output common-mode voltage			1000	1200	1400	mV

(1) $\overline{\text{CS}}$, SDATA, SCLK have internal 300-kΩ pulldown resistor.

7.9 Timing Requirements(1)

Typical values are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, sampling frequency = 100 MSPS, sine wave input clock = 1.5 Vpp clock amplitude, C_{LOAD} = 5 pF(2), R_{LOAD} = 100 Ω(3), unless otherwise noted. MIN and MAX values are across the full temperature range, T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, LVDD = 1.7 V to 1.9 V

			MIN	TYP	MAX	UNIT
t_j	Aperture jitter			220		fs rms
t_A	Aperture delay	Time delay between rising edge of input clock and the actual sampling instant		3		ns
	Wake-up time	Time to valid data after coming out of STANDBY mode		10		µs
		Time to valid data after coming out of global power down		60		
	ADC latency	Latency of ADC alone, excludes the delay from input clock to output clock (t_{PDI}), Figure 3		16		Clock cycles
2 WIRE, 8× SERIALIZATION (4)						
t_{su}	Data setup time	Data valid (5) to zero-crossing of LCLKP	0.23			ns
t_h	Data hold time	Zero-crossing of LCLKP to data becoming invalid(5)	0.31			ns
t_{PDI}	Clock propagation delay	Input clock rising edge crossover to output frame clock ADCLKP rising edge crossover, $t_{PDI} = (t_s/4) + t_{delay}$	6.8	8.8	10.8	ns
	Variation of t_{PDI}	Between two devices at same temperature and LVDD supply		±0.6		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (LCLKP-LCLKM)		50%		
t_{RISE} t_{FALL}	Data rise time, Data fall time	Rise time measured from –100 mV to 100 mV, Fall time measured from 100 mV to –100 mV *10 MSPS ≤ Sampling frequency ≤ 100 MSPS*		0.17		ns
$t_{CLKRISE}$ $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV *10 MSPS ≤ Sampling frequency ≤ 100 MSPS*		0.2		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(5) Data valid refers to logic HIGH of 100 mV and logic LOW of –100 mV.

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7.10 LVDS Timing at Lower Sampling Frequencies - 2 Wire, 8× Serialization

SAMPLING FREQUENCY, MSPS	SETUP TIME			HOLD TIME			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
100	0.23			0.31			ns
80	0.47			0.47			ns
65	0.56			0.7			ns
50	0.66			1			ns
20	2.7			2.8			ns

7.11 LVDS Timing for 1 Wire 16× Serialization

SAMPLING FREQUENCY, MSPS	SETUP TIME			HOLD TIME			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
65	0.15			0.31			ns
50	0.27			0.35			ns
40	0.45			0.55			ns
20	1.1			1.4			ns
Clock Propagation Delay $t_{PDI} = (t_s/8) + t_{delay}$ 10 MSPS < Sampling Frequency < 65 MSPS	t_{delay}						ns
	MIN	TYP	MAX				ns
	6.8	8.8	10.8				ns

7.12 LVDS Timing for 2 Wire, 7× Serialization

SAMPLING FREQUENCY, MSPS	SETUP TIME			HOLD TIME			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
100	0.29			0.39			ns
80	0.51			0.60			ns
65	0.58			0.82			ns
50	0.85			1.20			ns
20	3.2			3.3			ns
Clock Propagation Delay $t_{PDI} = (t_s/3.5) + t_{delay}$ 10 MSPS < Sampling Frequency < 100 MSPS	t_{delay}						ns
	MIN	TYP	MAX				ns
	6.8	8.8	10.8				ns

7.13 LVDS Timing for 1 Wire, 14× Serialization

SAMPLING FREQUENCY, MSPS	SETUP TIME			HOLD TIME			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
65	0.19			0.28			ns
50	0.37			0.42			ns
30	0.70			1.0			ns
20	1.3			1.5			ns
Clock Propagation Delay $t_{PDI} = (t_s/7) + t_{delay}$ 10 MSPS < Sampling Frequency < 65 MSPS	t_{delay}						ns
	MIN	TYP	MAX				ns
	6.8	8.8	10.8				ns

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7.14 Serial Interface Timing Requirements

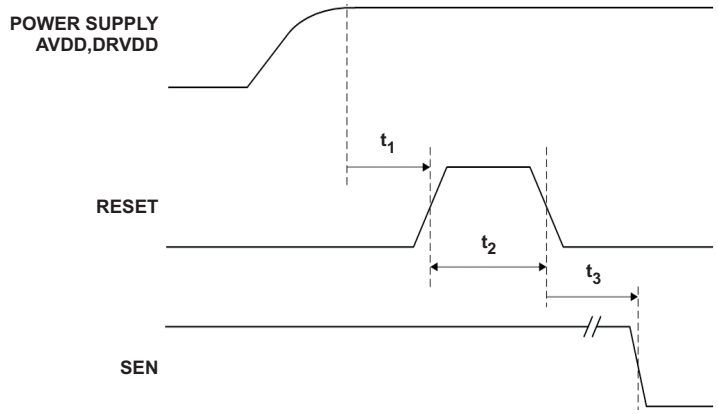
Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, LVDD = 1.8 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		20	MHz
t_{SLOADS}	$\overline{CS}$ to SCLK setup time	25			ns
t_{SLOADH}	SCLK to $\overline{CS}$ hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

7.15 Reset Switching Characteristics

Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up of AVDD and LVDD to RESET pulse active		1		ms
t_2	Reset pulse duration	Pulse duration of active RESET signal	50			ns
t_3	Register write delay	Delay from RESET disable to $\overline{CS}$ active		100		ns



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 1. Reset Timing Diagram

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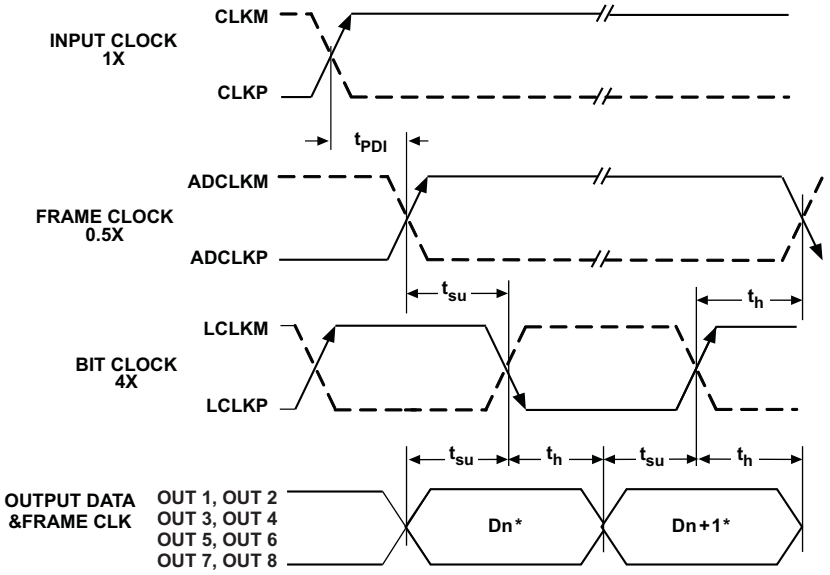


Figure 2. LVDS Timing

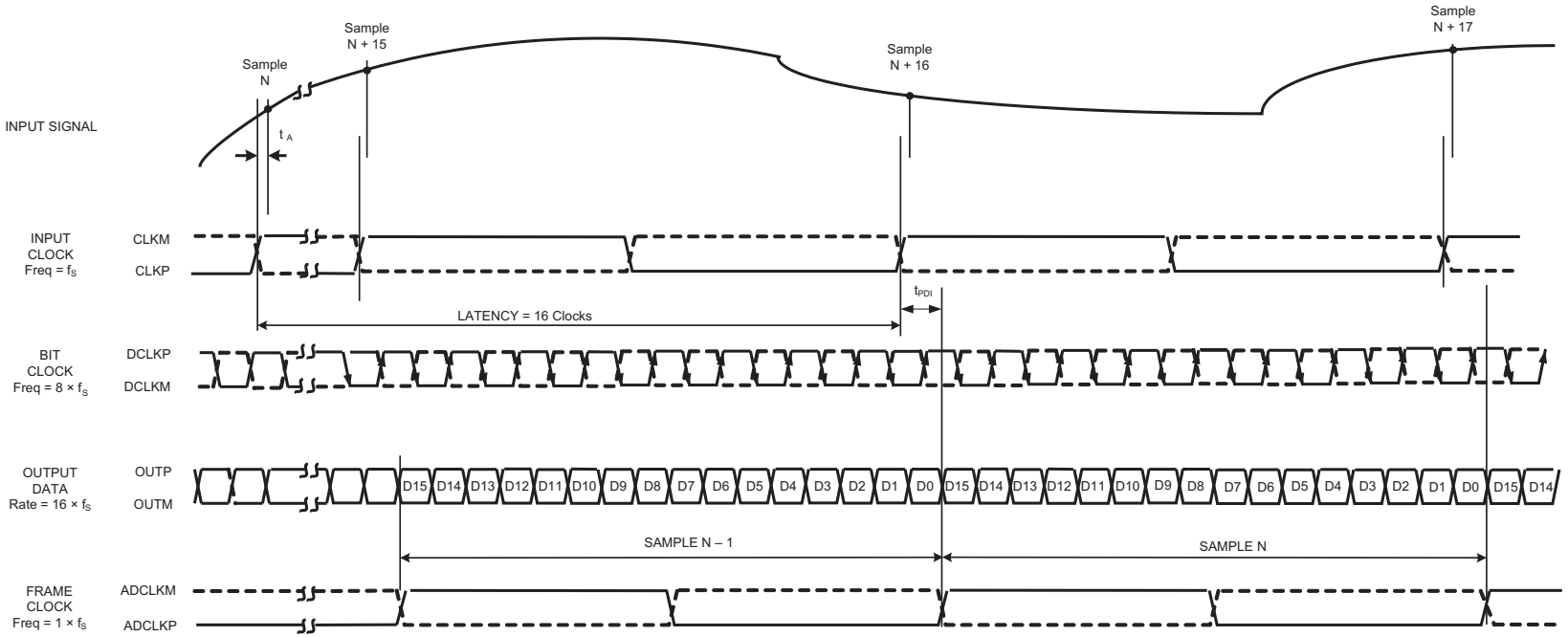


Figure 3. Latency Diagram

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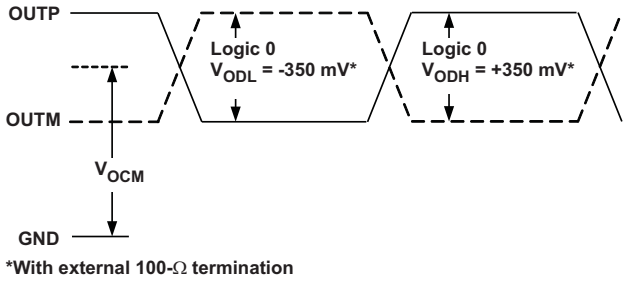


Figure 4. LVDS Output Voltage Levels

7.16 Typical Characteristics

7.16.1 Typical Characteristic – 16-Bit ADC Mode

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

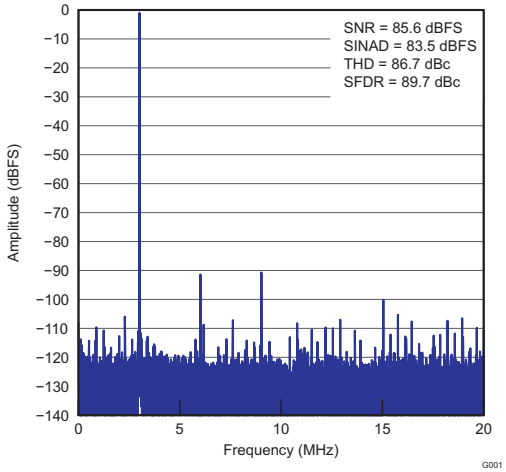


Figure 5. FFT for 3-MHz Input Signal, f_S = 40 MSPS

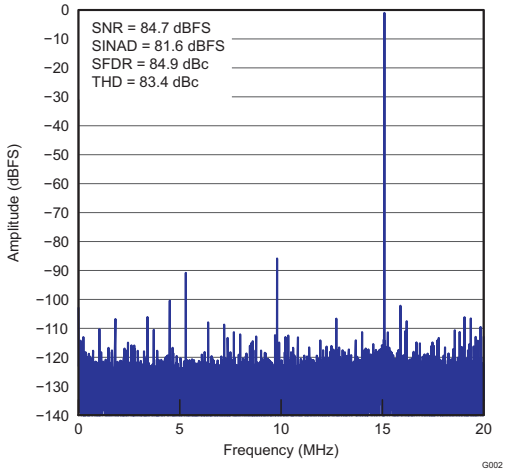


Figure 6. FFT for 15-MHz Input Signal, f_S = 40 MSPS

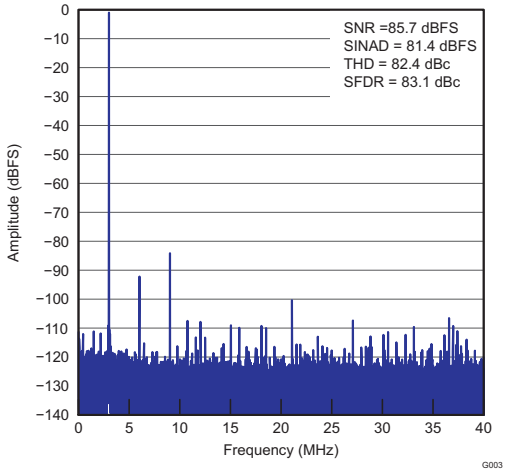


Figure 7. FFT for 3-MHz Input Signal, f_S = 80 MSPS

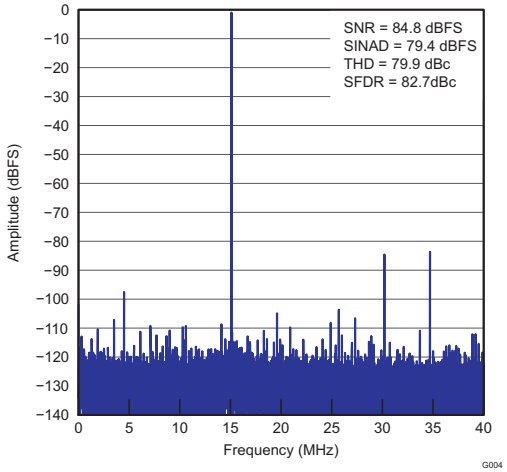


Figure 8. FFT for 15-MHz Input Signal, f_S = 80 MSPS

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Typical Characteristic – 16-Bit ADC Mode (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

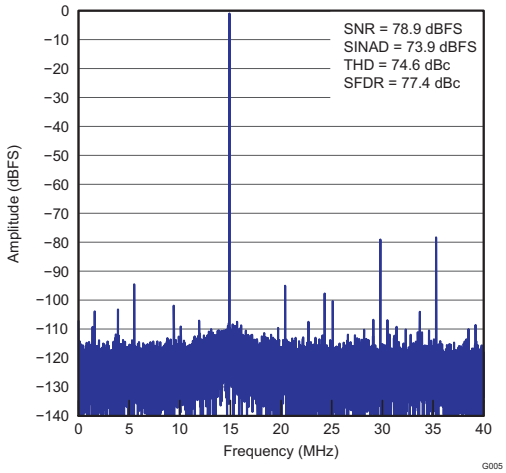


Figure 9. FFT for 65-MHz Input Signal, f_S = 80 MSPS

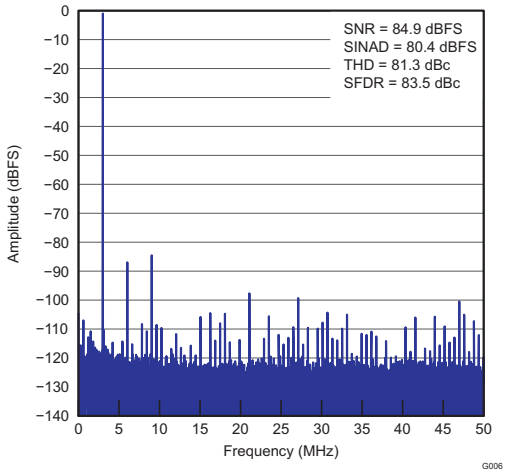


Figure 10. FFT for 3-MHz Input Signal, f_S = 100 MSPS

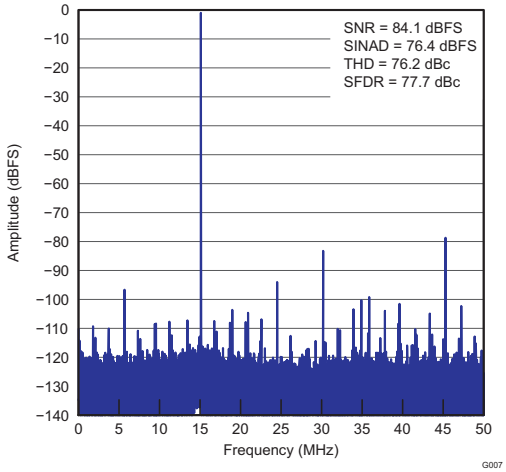


Figure 11. FFT for 15-MHz Input Signal, f_S = 100 MSPS

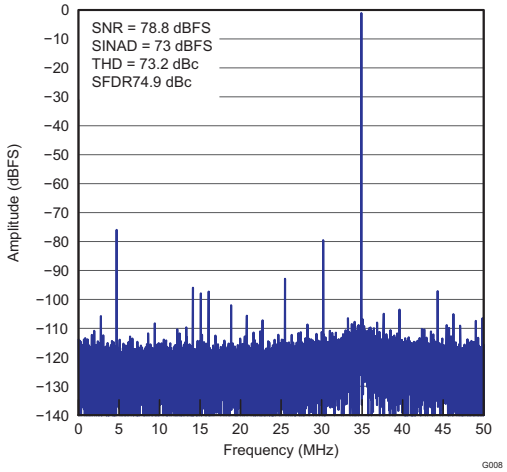


Figure 12. FFT for 65-MHz Input Signal, f_S = 100 MSPS

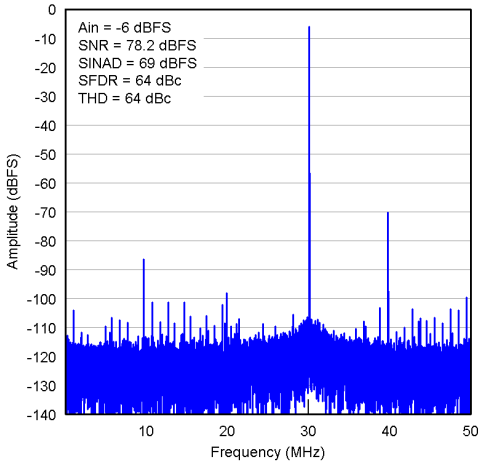


Figure 13. FFT for 130-MHz Input Signal, f_S = 100 MSPS

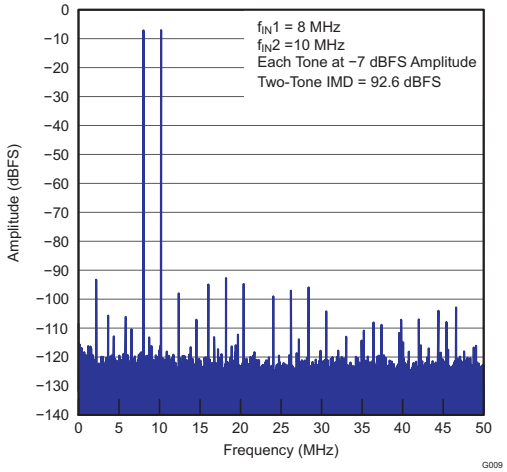


Figure 14. FFT for 2-Tone Input Signal

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Typical Characteristic – 16-Bit ADC Mode (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

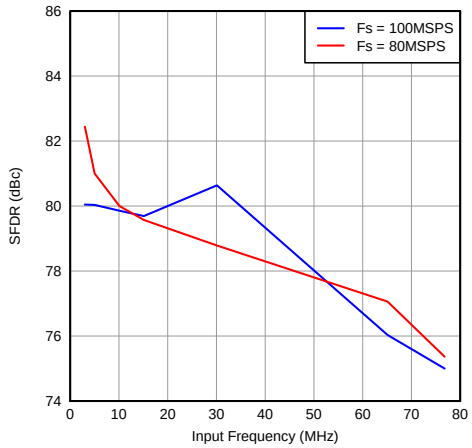


Figure 15. SFDR vs Input Frequency

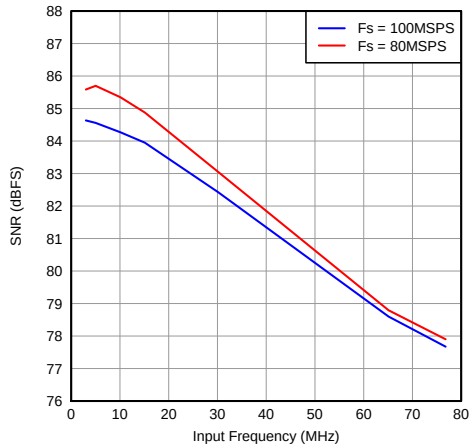


Figure 16. SNR vs Input Frequency

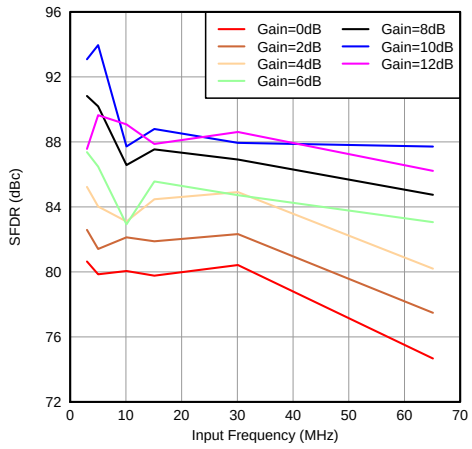


Figure 17. SFDR Across Gain

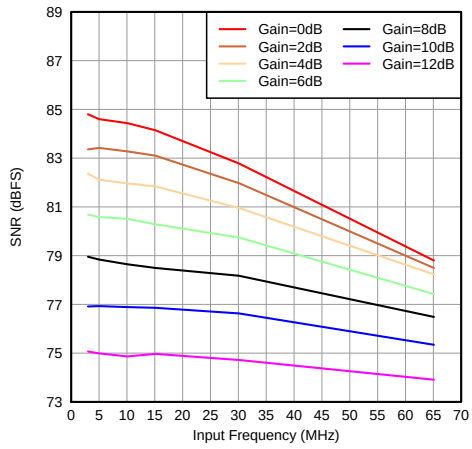


Figure 18. SNR Across Gain

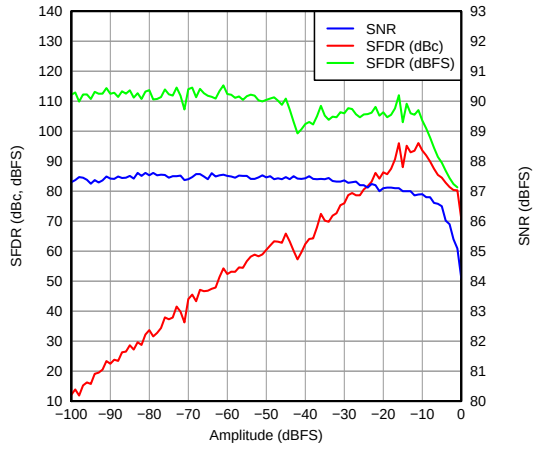


Figure 19. Performance Across Input Amplitude, Single Tone

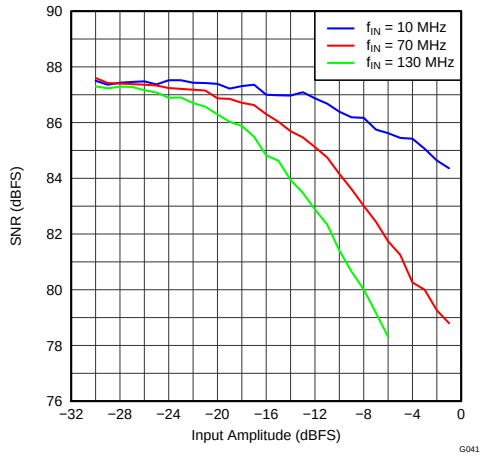


Figure 20. SNR Across Input Amplitude vs Input Frequency

Typical Characteristic – 16-Bit ADC Mode (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

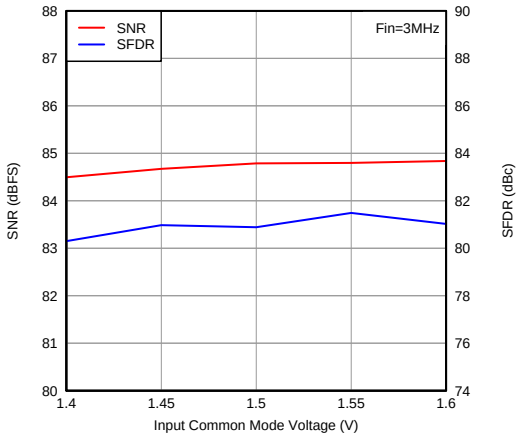


Figure 21. Performance vs Input Common-Mode Voltage

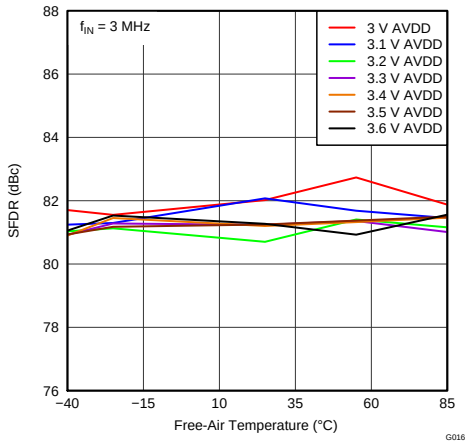


Figure 22. SFDR Across Temperature vs AVDD Supply, Sample Rate = 80 MSPS

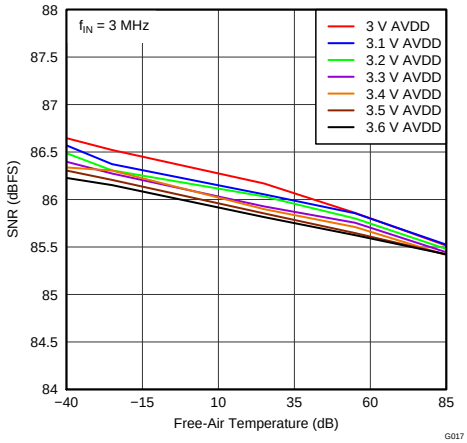


Figure 23. SNR Across Temperature vs AVDD Supply, Sample Rate = 80 MSPS

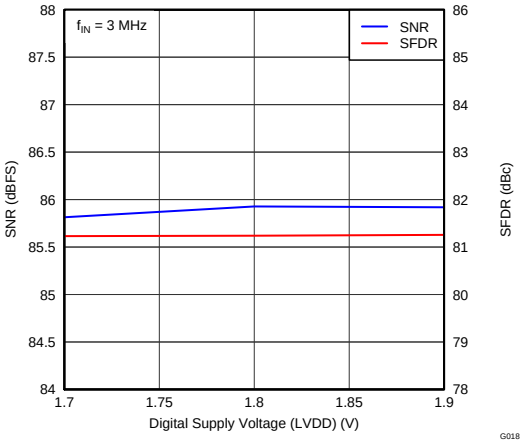


Figure 24. Performance Across LVDD Supply Voltage, Sample Rate = 80 MSPS

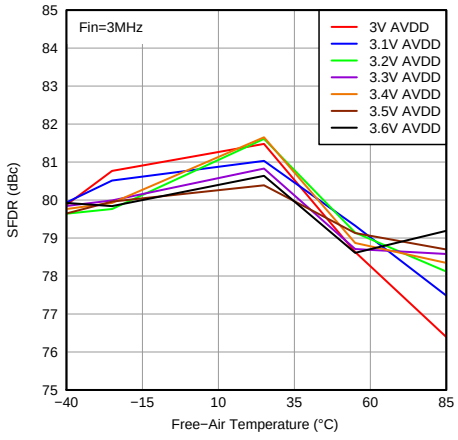


Figure 25. SFDR Across Temperature Sample Rate = 100 MSPS

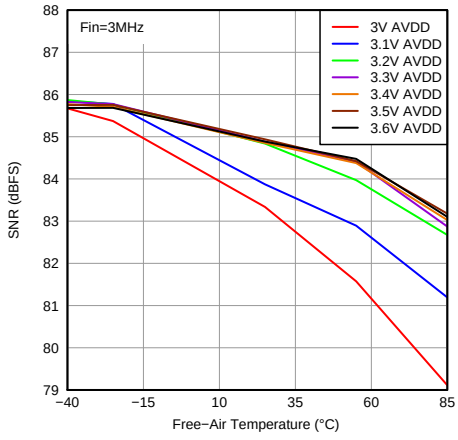


Figure 26. SNR Across Temperature Sample Rate = 100 MSPS

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Typical Characteristic – 16-Bit ADC Mode (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

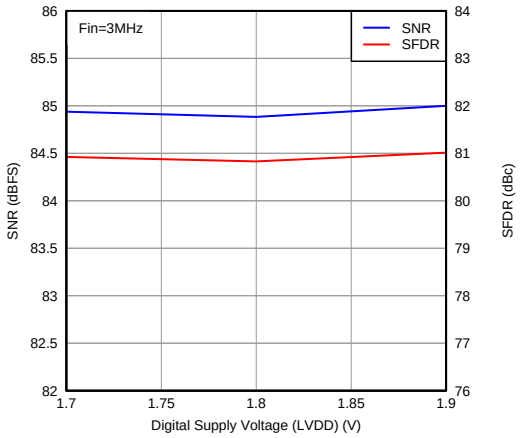


Figure 27. Performance Across LVDD Supply Sample Rate = 100 MSPS

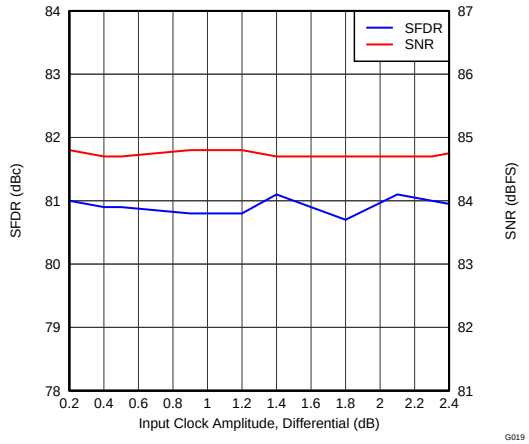


Figure 28. Performance Across Input Clock Amplitude, Sample Rate = 100 MSPS

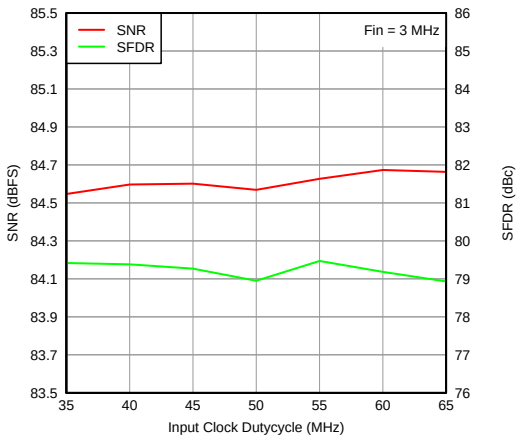


Figure 29. Performance Across Input Clock Duty Cycle, Sample Rate = 100 MSPS

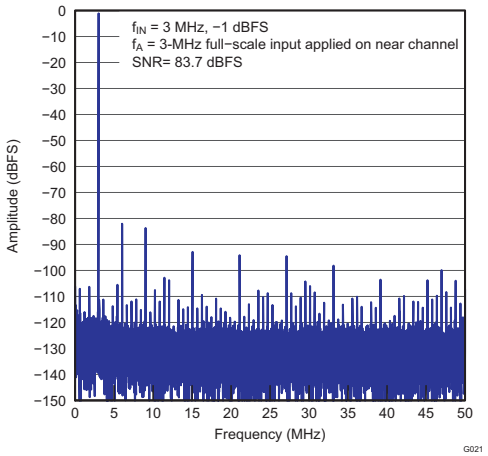


Figure 30. Near-Channel Crosstalk Spectrum, Sample Rate = 100 MSPS

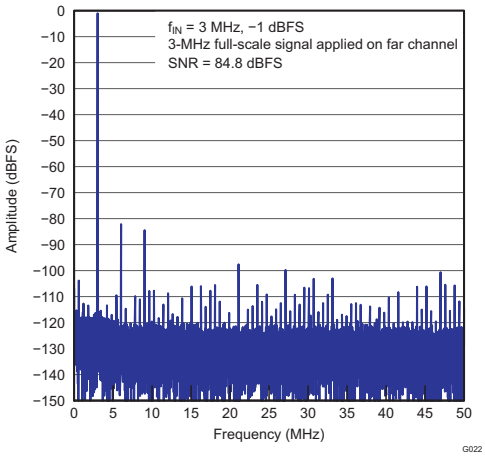


Figure 31. Far-Channel Crosstalk Spectrum

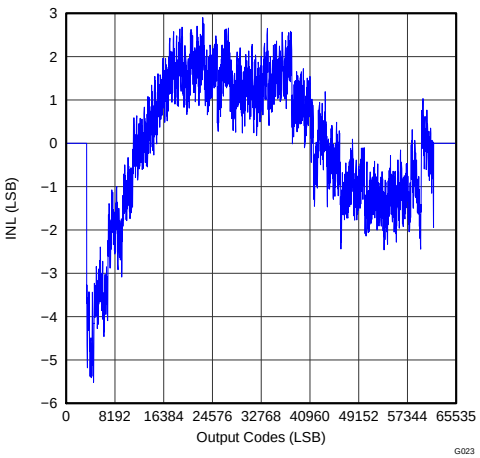


Figure 32. Integral Non-Linearity

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Typical Characteristic – 16-Bit ADC Mode (continued)

All plots are at 25°C, AVDD = 3.3 V, LVDD = 1.8 V, maximum-rated sampling frequency, sine-wave input clock = 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, 32k point FFT (unless otherwise noted).

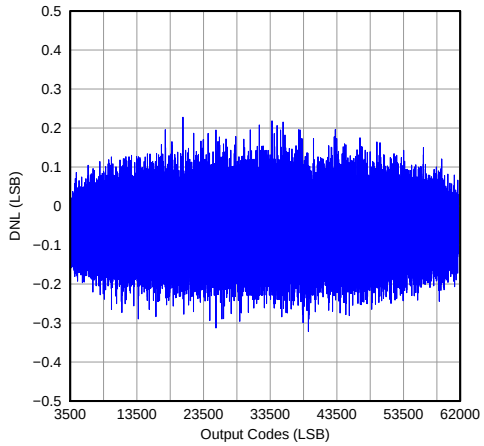


Figure 33. Differential Non-Linearity

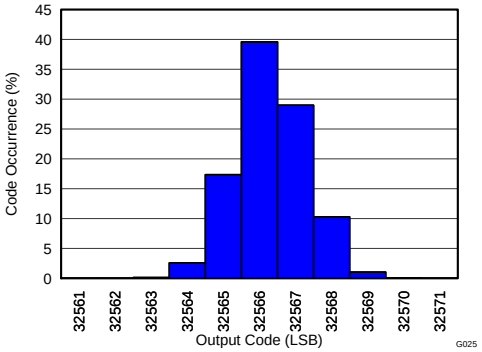


Figure 34. Histogram of Output Code with Analog Inputs Shorted

7.16.2 Typical Characteristic – 14-Bit ADC Mode

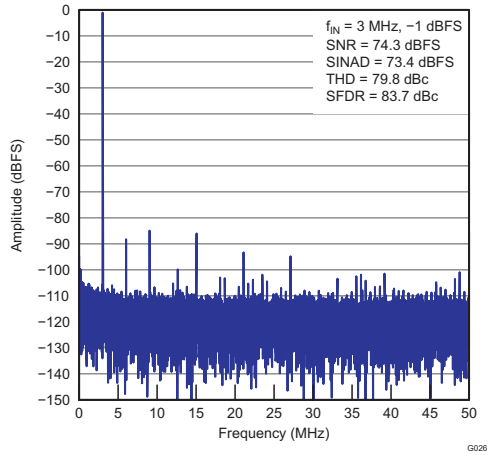


Figure 35. FFT for 3-MHz Input Signal, f_S = 100 MSPS

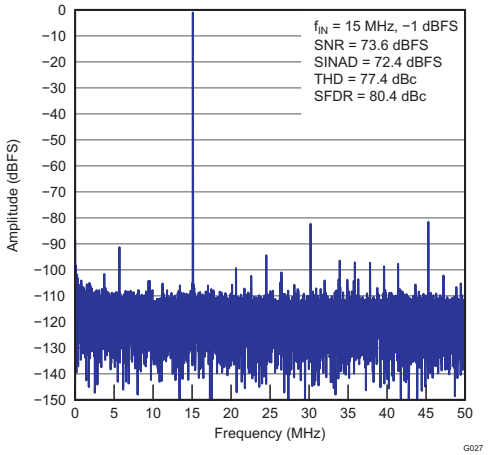


Figure 36. FFT for 15-MHz Input Signal, f_S = 100 MSPS

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Typical Characteristic – 14-Bit ADC Mode (continued)

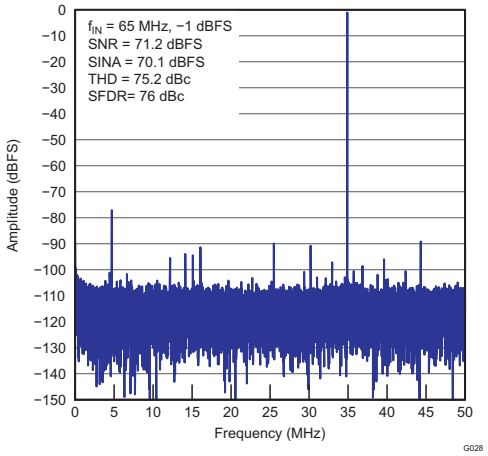


Figure 37. FFT for 65-MHz Input Signal, f_S = 100 MSPS

7.16.3 Typical Characteristics – Common Plots

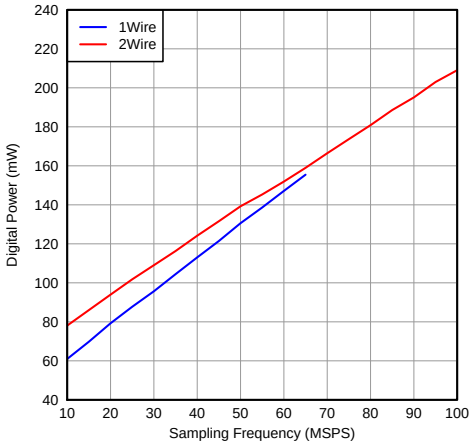


Figure 38. 16-Bit Digital Power Across Sampling Frequencies

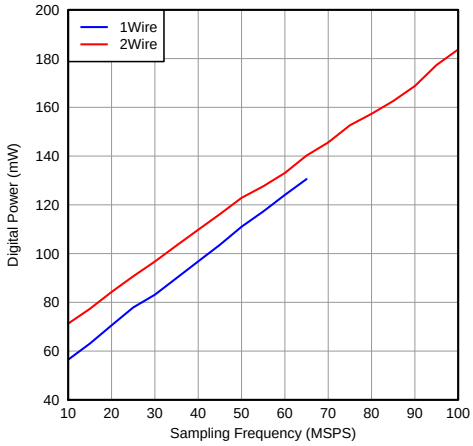


Figure 39. 14-Bit Digital Power Across Sampling Frequencies

Typical Characteristics – Common Plots (continued)

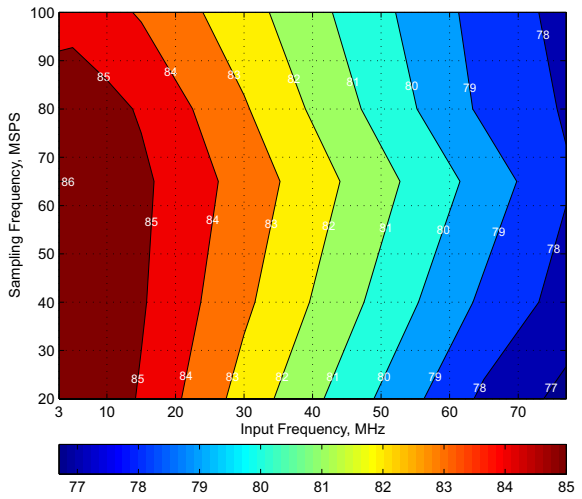


Figure 40. SNR Contour Across Sampling and Input Frequencies, 16-Bit ADC

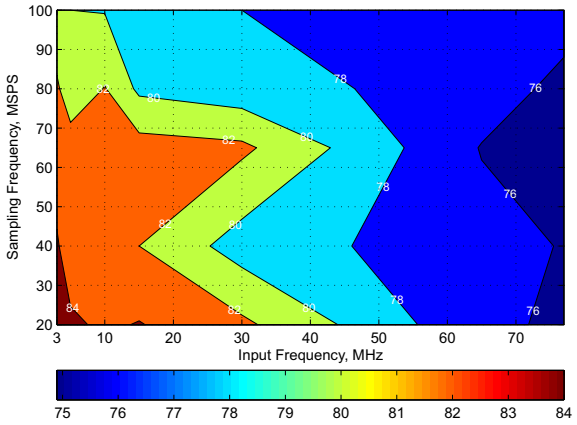


Figure 41. SFDR Contour Across Sampling and Input Frequencies, 16-Bit ADC

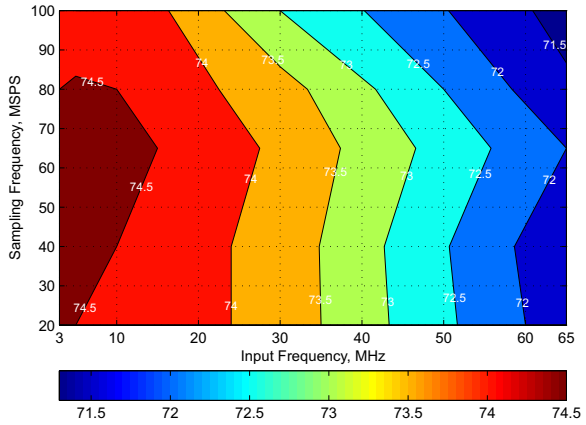


Figure 42. SNR Contour Across Sampling and Input Frequencies, 14-Bit ADC

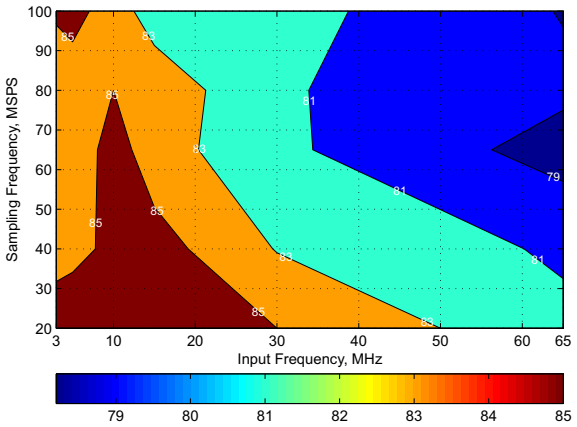


Figure 43. SFDR Contour Across Sampling and Input Frequencies, 14-Bit ADC

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8 Detailed Description

8.1 Overview

The ADS5263 is a high-SNR 16-bit, quad-channel, 100-MSPS ADC using serial LVDS interface to reduce pin connections from ADC to FPGA. For low power applications, the part can be progammed into 14-bit, Low-power mode saving 615 m-W at 100-MSPS

The ADS5263 has a digital processing block that integrates several commonly used digital functions, such as digital gain (up to 12 dB). It includes a digital filter module that has built-in decimation filters (with low-pass, high-pass and band-pass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8). This makes it very useful for narrow-band applications, where the filters can be used to improve SNR and knock-off harmonics, while at the same time reducing the output data rate.

The device includes an averaging mode where two channels (or even four channels) can be averaged to improve SNR. A very unique feature is the programmable mapper module that allows flexible mapping between the input channels and the LVDS output pins. This helps to greatly reduce the complexity of LVDS output routing and can potentially result in cheaper system boards by reducing the number of PCB layers.

The data from each channel ADC is serialized and output on two pairs of LVDS output lines, along with a bit clock and a frame clock. Serial LVDS outputs reduce the number of interface lines. This, together with the low-power design, enables four channels to be packaged in a compact 9-mm × 9-mm QFN, allowing high system integration densities.

In order to ease interfacing to CCD sensors, a clamp function is integrated in the device. Using this feature, the analog input pins can be clamped to an internal voltage, based on a SYNC signal. With this, the CCD sensor output can be easily ac-coupled to the ADS5263 analog inputs. The clamp feature and quad channels in a compact package make the ADS5263 attractive for industrial CCD imaging applications.

The device integrates an internal reference trimmed to accurately match across devices. Additionally, the device supports an external reference mode for applications that require very low temperature drift of reference. The ADS5263 is available in a non-magnetic QFN package that does not create any MRI signature. The device is specified over the full industrial temperature range.

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8.2 Functional Block Diagram

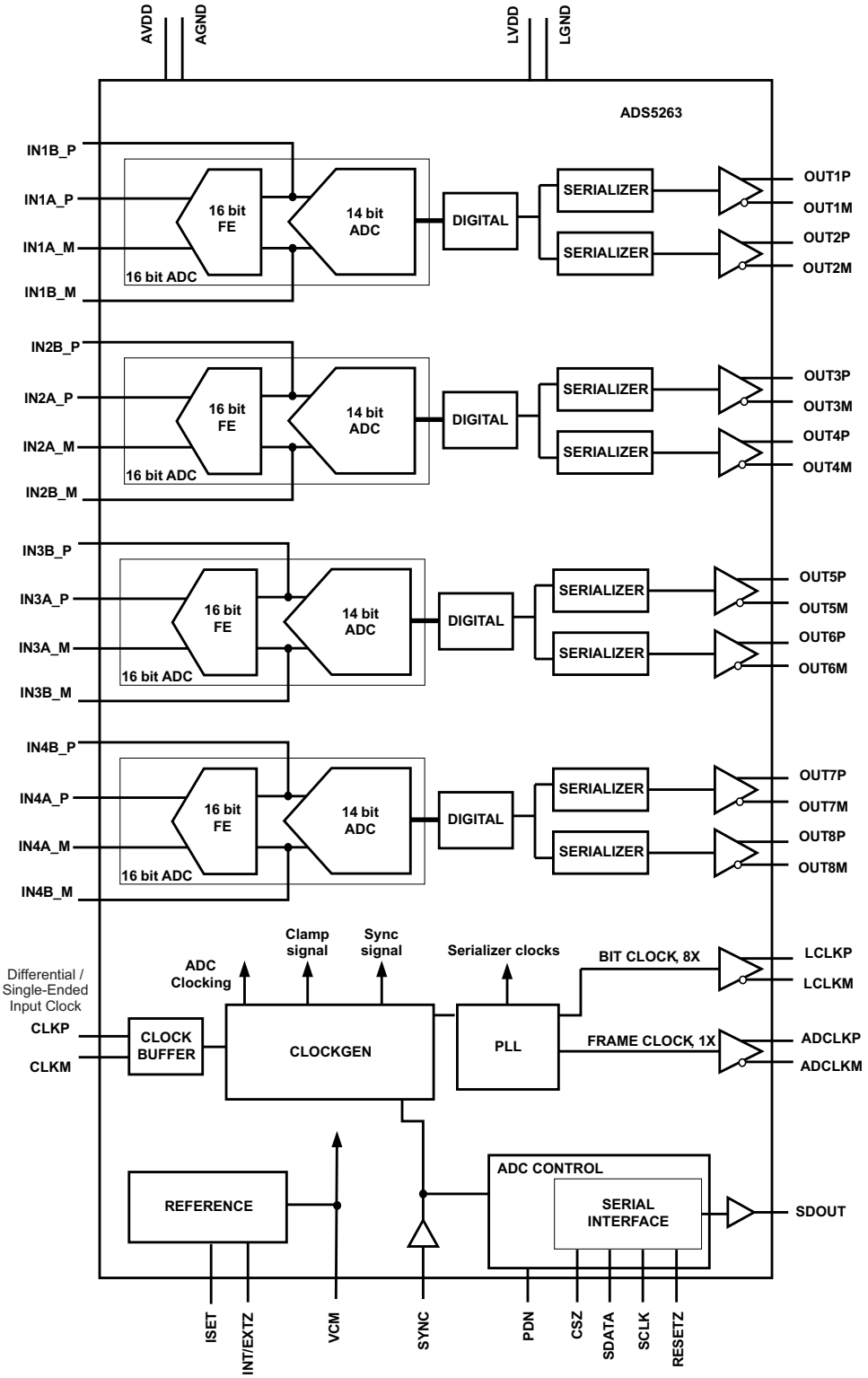


Figure 44. ADS5263 Block Diagram

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8.3 Feature Description

8.3.1 Digital Processing Blocks

The ADS5263 integrates a set of commonly useful digital functions that can be used to ease system design. These functions are shown in the digital block diagram of Figure 45 and described in the following sections.

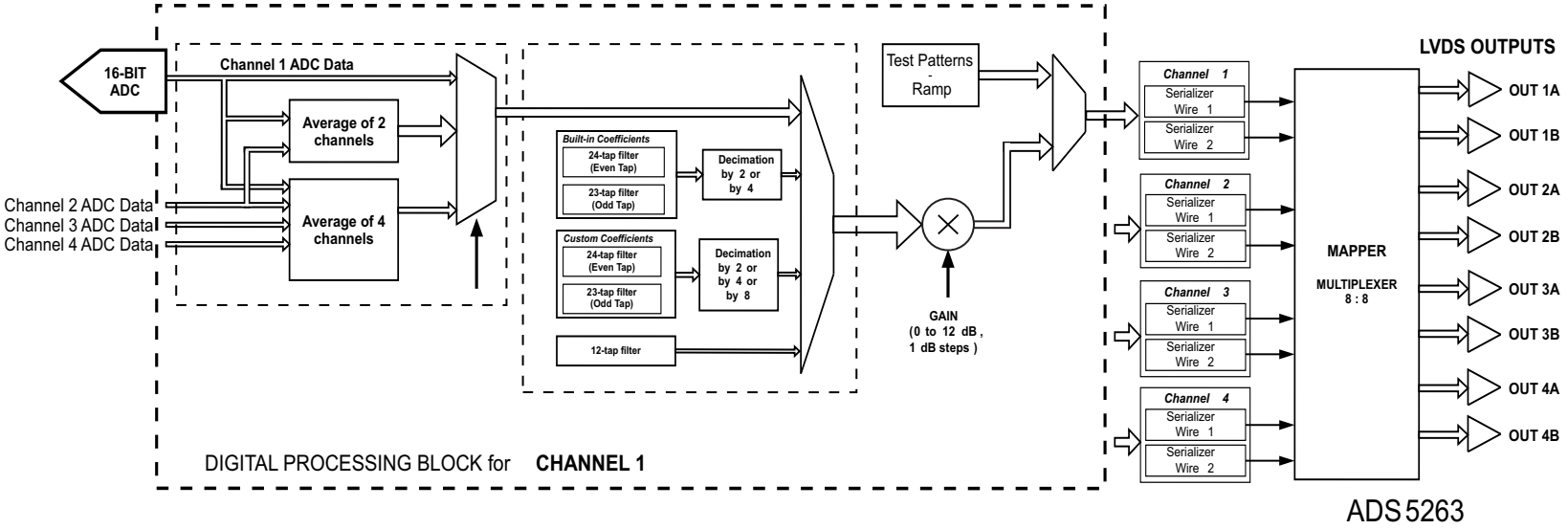


Figure 45. Block Diagram – Digital Processing

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8.3.2 Digital Gain

ADS5263 includes programmable digital gain settings from 0 dB to 12 dB in steps of 1 dB. The benefit of digital gain is to get improved SFDR performance. The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades by about 1 dB. So, the gain can be used to trade off between SFDR and SNR.

For each gain setting, the analog supported input full-scale range scales proportionally, as shown in Table 1. The full-scale range depends on the ADC mode used (16-bit or 14-bit).

After a reset, the device comes up in the 0-dB gain mode. To use other gain settings, program the **<GAIN CH x>** register bits.

Table 1. Analog Full-Scale Range Across Gains

DIGITAL GAIN, dB	16-BIT ADC MODE	14-BIT ADC MODE
	ANALOG FULL-SCALE INPUT, Vpp	ANALOG FULL-SCALE INPUT, Vpp
0	4.00	2
1	3.57	1.78
2	3.18	1.59
3	2.83	1.42
4	2.52	1.26
5	2.25	1.12
6	2.00	1.00
7	1.79	0.89
8	1.59	0.80
9	1.42	0.71
10	1.26	0.63
11	1.13	0.56
12	1.00	0.50

8.3.3 Digital Filter

The digital processing block includes the option to filter and decimate the ADC data outputs digitally. Various filters and decimation rates are supported – decimation rates of 2, 4, and 8 and low-pass, high-pass, and band-pass filters are available. The filters are internally implemented as a 24-tap *asymmetric* FIR (even-tap) using pre-defined coefficients following the equation which is described in Figure 46.

Alternatively, some of the filters can be configured as a 23-tap *asymmetric* FIR (or odd-tap filters) following the equation which is described in Figure 47.

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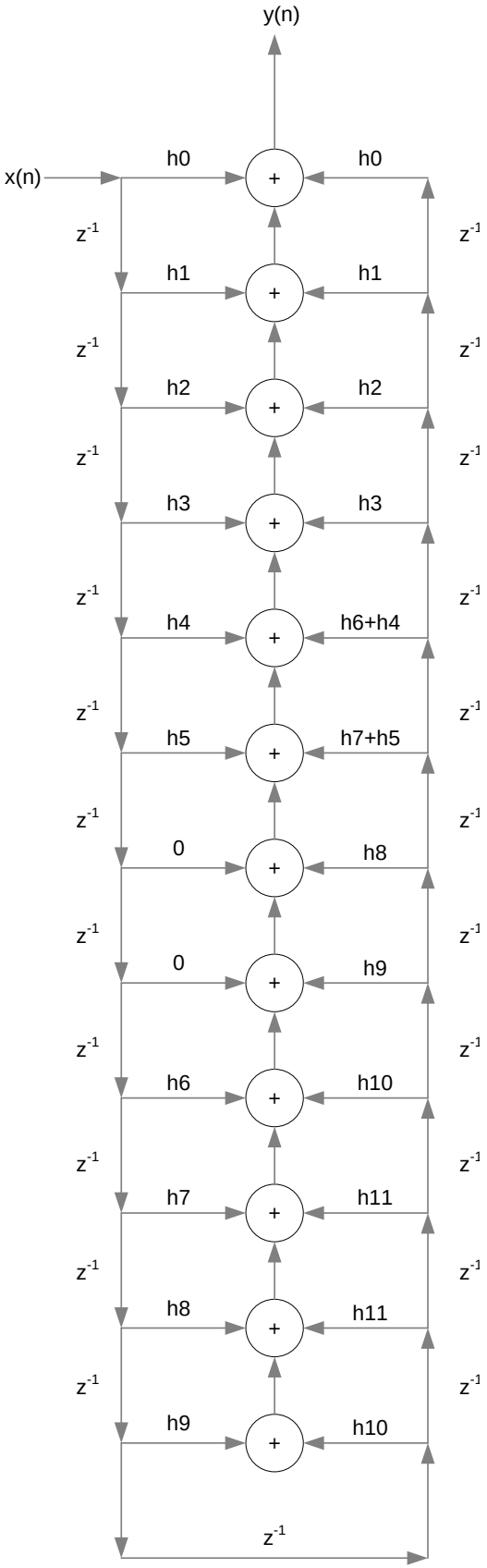


Figure 46. 24-tap Filter Equation

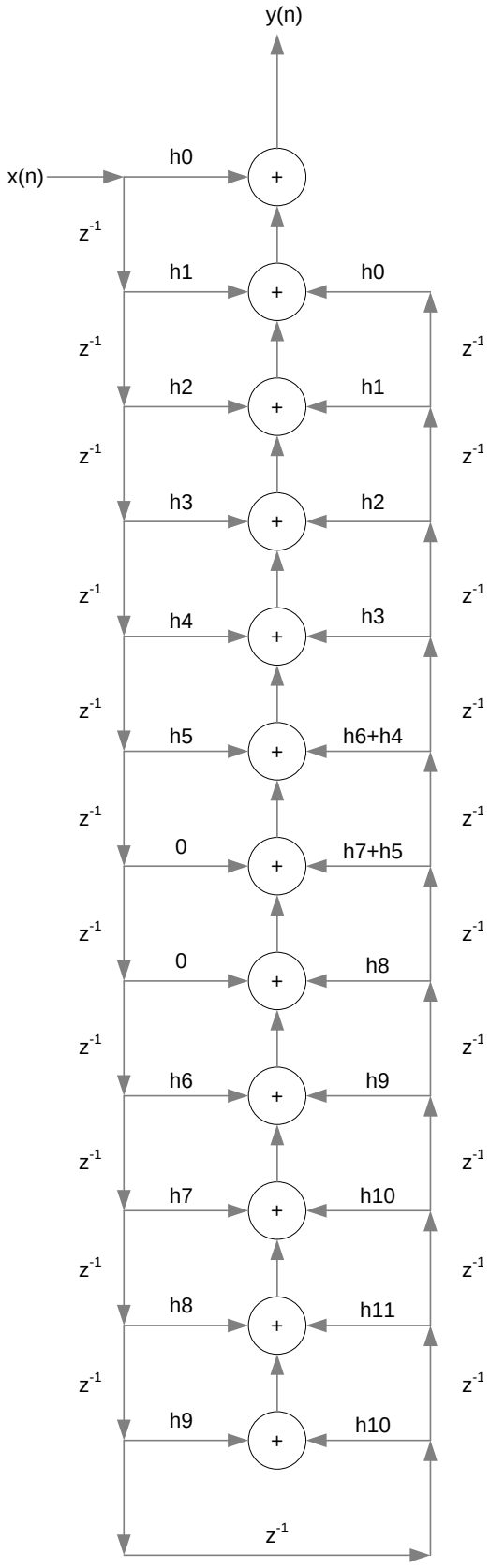


Figure 47. 23-tap Filter Equation

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In the equations,

h0, h1 …h11 are 12-bit signed 2s complement representation of the coefficients (-2048 to +2047)

x(n) is the input data sequence to the filter

y(n) is the filter output sequence

Details of the registers used for configuring the digital filters are show in Table 2 and Table 3.

Table 2. Digital Filter Registers

BIT	NAME	DESCRIPTION
ADDR: 2E, 2F, 30, 31 Default = 0		
D9-D7	FILTER TYPE CHn<2:0>	Selects low-pass, high-pass or band-pass filters
D6-D4	DEC by RATE CHn<2:0>	Selects the decimation rate
D2	ODD TAP CHn	Even tap or odd tap
D0	USE FILTER CHn	Enables the filter
ADDR: 38, Default = 0		
D1-D0	OUTPUT RATE<1:0>	Select output data rate depending on the type of filter
ADDR: 29, Default = 0		
D1	EN DIG FILTER	Enables digital filter – global control

See Table 3 for choosing the right combination of decimation rate and filter types.

Table 3. Digital Filters

DECIMATION	TYPE OF FILTER	<OUTPUT RATE>	DEC by RATE CHx>	<FILTER TYPE CHx>	<SEL ODD TAP>	<USE FILTER CHx>	<EN CUSTOM FILT>	<EN DIG FILTER>
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to $f_S/4$)	001	000	000	1	1	0	1
	Built-in **high-pass odd-tap** filter (pass band = 0 to $f_S/4$)	001	000	001	1	1	0	1
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to $f_S/8$)	010	001	010	0	1	0	1
	Built-in first **band pass even tap** filter(pass band = $f_S/8$ to $f_S/4$)	010	001	011	0	1	0	1
	Built-in second **band pass even tap** filter(pass band = $f_S/4$ to 3 $f_S/8$)	010	001	100	0	1	0	1
	Built-in **high pass odd tap** filter (pass band = 3 $f_S/8$ to $f_S/2$)	010	001	101	1	1	0	1
Decimate by 2	Custom filter (user programmablecoefficients)	001	000	000	0 or 1	1	1	1
Decimate by 4	Custom filter (user programmablecoefficients)	010	001	000	0 or 1	1	1	1
Decimate by 8	Custom filter (user programmablecoefficients)	011	100	000	0 or 1	1	1	1
12-tap filter without decimation	Custom filter (user programmablecoefficients)	000	011	000	0	1	1	1

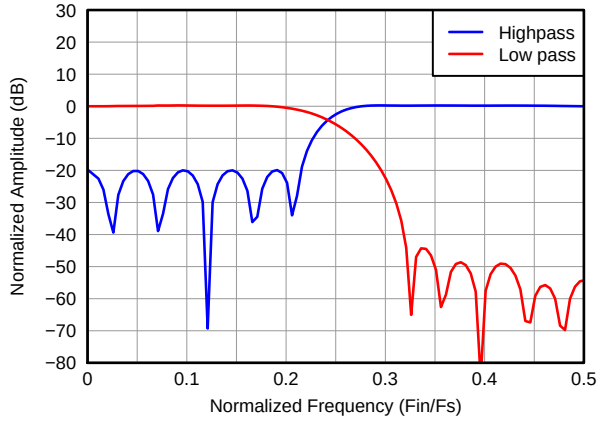


Figure 48. Filter Response – Decimate by 2

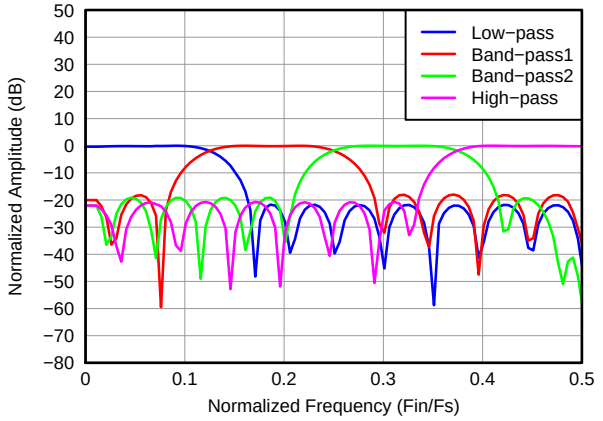


Figure 49. Filter Response – Decimate by 4

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8.3.4 Custom Filter Coefficients

In addition to these built-in filters, customers also have the option of using their own custom 12-bit signed coefficients. Only 12 coefficients can be specified according to Figure 48 or Figure 49. These coefficients (h0 to h11) must be configured in the custom coefficient registers as:

Register content = 12-bit signed representation of [real coefficient value × 2^{11}]

The 12 custom coefficients must be loaded into 12 separate registers for each channel (refer Table 4). The MSB bit of each coefficient register decides if the built in filters or custom filters are used. If the MSB bit <EN CUSTOM FILT> is reset to 0, then built in filter coefficients are used. Else, the custom coefficients are used.

Table 4. Custom Coefficient Registers (1)

BIT	NAME	DESCRIPTION
ADDR: 5A to 65, Default = 0 Set value of h0 in register 0x5A, h1 in 0x5B & so on till h11 in register 0x65		
D11-D0	COEFFn SET CH1<11:0>	Custom coefficient for digital filter of channel 1
D15	<EN CUSTOM FILT CH1>	1: Enables custom coefficients to be used 0: Built in coefficients are used
ADDR: 66 to 71, Default = 0 Set value of h0 in register 0x66, h1 in 0x67 & so on till h11 in register 0x71		
D11-D0	COEFFn SET CH2<11:0>	Custom coefficient for digital filter of channel 2
D15	<EN CUSTOM FILT CH2>	1: Enables custom coefficients to be used 0: Built in coefficients are used
ADDR: 72 to 7D, Default = 0 Set value of h0 in register 0x72, h1 in 0x73 & so on till h11 in register 0x7D		
D11-D0	COEFFn SET CH3<11:0>	Custom coefficient for digital filter of channel 3
D15	<EN CUSTOM FILT CH3>	1: Enables custom coefficients to be used 0: Built in coefficients are used
ADDR: 7E to 89, Default = 0 Set value of h0 in register 0x7E, h1 in 0x7F & so on till h11 in register 0x89		
D11-D0	COEFFn SET CH4<11:0>	Custom coefficient for digital filter of channel 4
D15	<EN CUSTOM FILT CH4>	1: Enables custom coefficients to be used 0: Built in coefficients are used

(1) Where n = 0 to 11

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8.3.4.1 Custom Filter Without Decimation

Another mode exists to use the digital filter without decimation. In this mode, the filter behaves like a 12-tap *symmetric* FIR filter as per the equation described by Figure 50

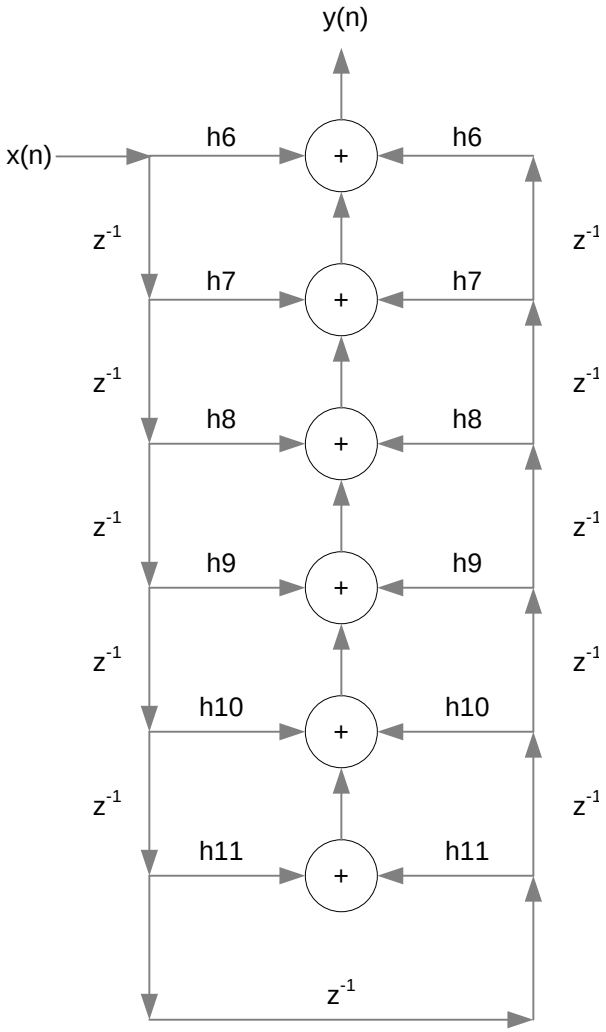


Figure 50. 12-tap Symmetric Filter Equation

Where,

h6, h7 …h11 are 12-bit signed 2s complement representation of the coefficients (-2048 to +2047)

x(n) is the input data sequence to the filter

y(n) is the filter output sequence

In this mode, as the filter is implemented as a 12-tap symmetric FIR, only 6 custom coefficients need to be specified and must be loaded in registers h6 to h11. Table 4

To enable this mode, use the register setting specified in the last row of Table 3

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8.3.5 Digital Averaging

The ADS5263 includes an averaging function where the ADC digital data from two (or four) channels can be averaged. The averaged data is output on specific LVDS channels. Table 5 shows the combinations of the input channels that can be averaged and the LVDS channels on which averaged data is available

Table 5. Using Channel Averaging

Averaged Channels	Output on Which Averaged Data Is Available	Register Settings
Channel 1, Channel 2	OUT1A, OUT1B	Set **<AVG OUT 1>** = **10** and **<EN AVG GLO>** = **1**
Channel 1, Channel 2	OUT3A, OUT3B	Set **<AVG OUT 3>** = **11** and **<EN AVG GLO>** = **1**
Channel 3, Channel 4	OUT4A, OUT4B	Set **<AVG OUT 4>** = **10** and **<EN AVG GLO>** = **1**
Channel 3, Channel 4	OUT2A, OUT2B	Set **<AVG OUT 2>** = **11** and **<EN AVG GLO>** = **1**
Channel 1, Channel 2, Channel 3, Channel 4	OUT1A, OUT1B	Set <**AVG OUT 1>** = **11** and **<EN AVG GLO>** = **1**
Channel 1, Channel 2, Channel 3, Channel 4	OUT1A, OUT1B	Set **<AVG OUT 4>** = **11** and **<EN AVG GLO>** = **1**

8.3.6 Performance with Digital Processing Blocks

The ADS5263 provides very high SNR along with high sampling rates. In applications where even higher SNR performance is desired, digital processing blocks such as averaging and decimation filters can be used advantageously to achieve this. Table 6 shows the improvement in SNR that can be achieved compared to the default value, using these modes.

Table 6. SNR Improvement Using Digital Processing (1)

MODE	TYPICAL SNR, dBFS	TYPICAL IMPROVEMENT in SNR, dB
Default	84.5	
With decimation-by-2 filter enabled	86.7	2.2
With decimation-by-4 filter enabled	87.7	3.2
With decimation-by-8 filter enabled	88.6	4.1
With two channels averaged and decimation-by-8 filter enabled	91.3	6.8
With four channels averaged	89.6	5.1
With four channels averaged and decimation-by-8 filter enabled	93	8.5

(1) Custom coefficients used for decimation-by-8 filter.

8.3.6.1 18-Bit Data Output with Digital Processing

As shown in Table 6, very high SNR can be achieved using the digital blocks. Now, the overall SNR is limited by the quantization noise of the 16-bit output data. (16-bit quantization SNR = 6n + 1.76 = 16 × 6 + 1.76 = 97.76 dBFS.) To overcome this, the digital processing blocks (averaging and digital filters) automatically output 18-bit data. With the two additional bits, the quantization SNR improves by 12 dB and no longer limits the maximum SNR that can be achieved using the ADS5263. For example, with four channels averaged and the decimation-by-8 filter, the typical SNR improves to about 94.5 dBFS using 18-bit data (an improvement of 1.5 dB over the SNR with 16-bit data).

The 18-bit data can be output using the special 18× serialization mode (see *Output LVDS Interface*). Note that the user can choose either the default 16× serialization (which takes the upper 16 bits of the 18-bit data) or the 18× serialization mode (that outputs all 18 bits).

8.3.7 Flexible Mapping o Channel Data to LVDS Outputs

ADS5263 has a mapping function by the use of which the digital data for any channel can be routed to any LVDS output. So, as an example, in the 1-wire interface, the channel-1 ADC output can be output either on OUT1 pins or on OUT2 or OUT3 or OUT4 pins.

This flexibility in mapping simplifies board designs by avoiding complex routing that would be caused by a rigid mapping of input channels and output pins. This can also lead to potential saving in PCB layers and hence cost. The mapping is programmable using the register bits **<MAP_Ch1234_OUTn>** as shown in Figure 51 and Figure 52.

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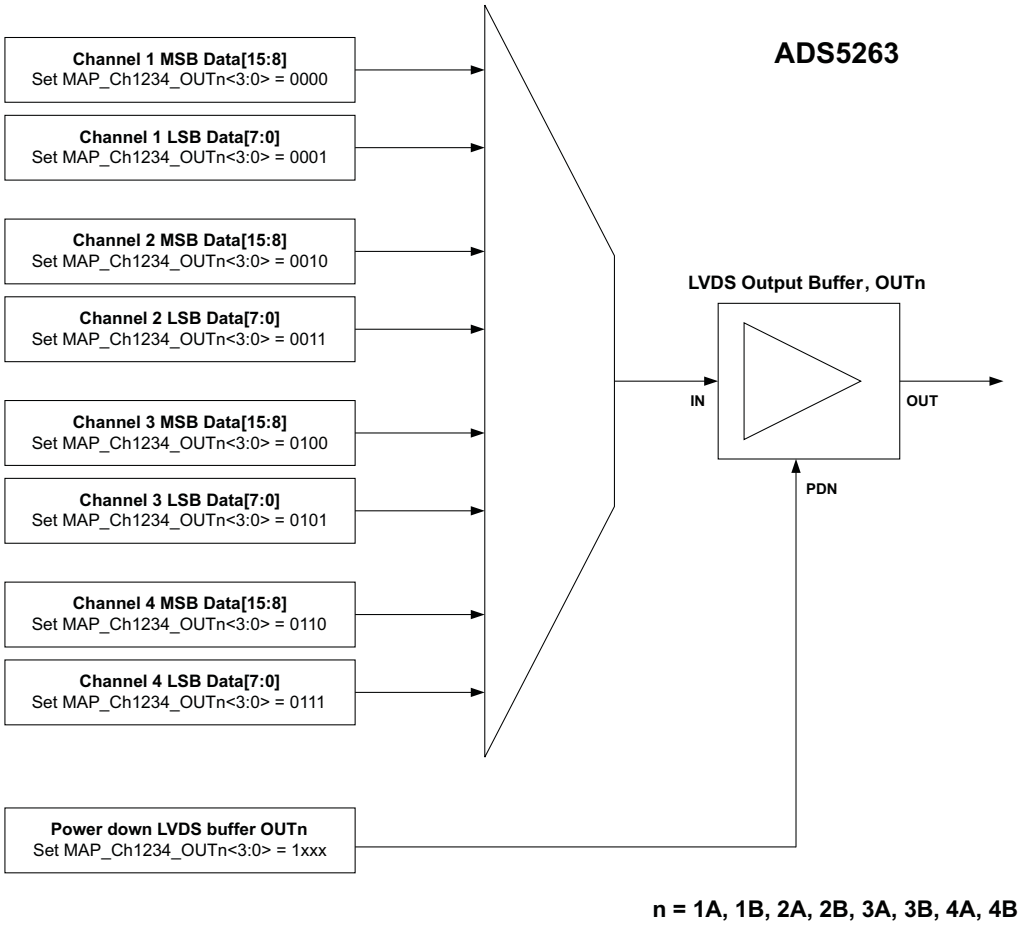


Figure 51. Mapping in 2-Wire Interface

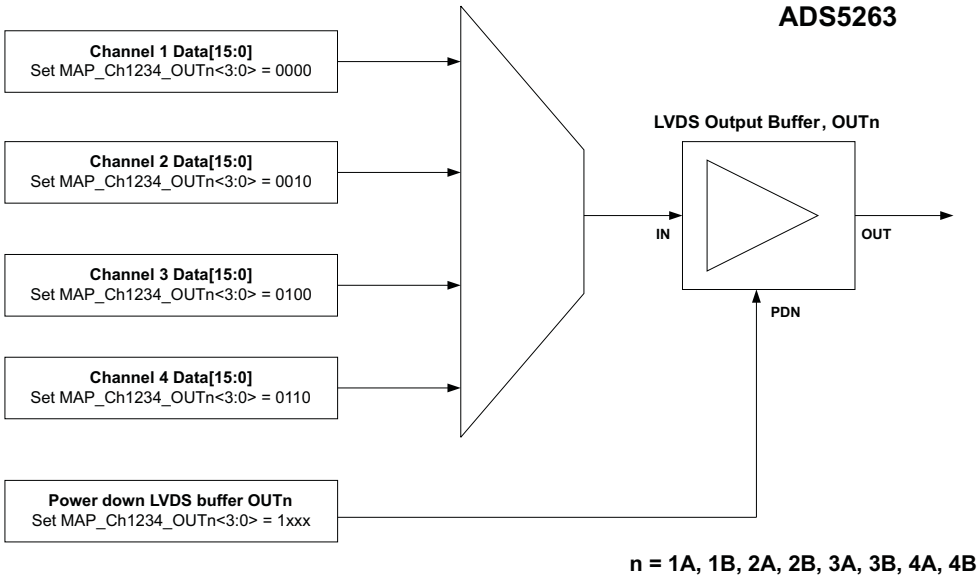


Figure 52. Mapping in 1-Wire Interface

8.3.8 Output LVDS Interface

The ADS5263 offers several flexible output options, making it easy to interface to an ASIC or an FPGA. Each of these options can be easily programmed using the serial interface. A summary of all the options is presented in Table 7, along with the default values after power up and reset. Following this, each option is described in detail.

The output interface options are:

1. 1-wire, 16× serialization with DDR bit clock and 1× frame clock
   - The 16-bit ADC data is serialized and output over one LVDS pair per channel together with an 8× bit clock and 1× frame clock. The output data rate is 16× sample rate; hence, it is suited for low sample rates, typically up to 50 MSPS.
2. 2-wire, 8× serialization with DDR bit clock and 0.5× frame clock (16 bit ADC mode, Figure 54 and Figure 55)
   - Here, the 16 bit ADC data is serialized and output over two LVDS pairs per channel. The output data rate is 8x sample rate, with a 4x bit clock and 0.5x frame clock.
     Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
3. 2-wire, 8× serialization with DDR bit clock and 0.5× frame clock (14-bit ADC mode)
   - Here, the 14-bit ADC data is padded with two zero bits. The combined 16-bit data is then serialized and output over two LVDS pairs per channel. The output data rate is 8× sample rate, with a 4× bit clock and 0.5× frame clock Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
4. 1-wire, 14× serialization with DDR bit clock and 1× frame clock (14-bit ADC mode)
   - The 14-bit ADC data is serialized and output over one LVDS pair per channel together with a 7× bit clock and 1× frame clock. The output data rate is 14× sample rate; hence, it is suited for low sample rates, typically up to 50 MSPS.
5. 2-wire, 7× serialization with DDR bit clock and 0.5× frame clock (14-bit ADC mode, Figure 57 and Figure 58)
   - Here, the 14-bit ADC data is serialized and output over two LVDS pairs per channel. The output data rate is 7× sample rate, with a 3.5× bit clock and 0.5× frame clock. Because the output data rate is half compared to the 1-wire case, this interface can be used up to the maximum sample rate of the device.
6. 1-wire, 18× serialization with DDR bit clock and 1× frame clock – Here, the 18-bit data from the digital processing block is serialized and output over one LVDS pair per channel, together with a 9× bit clock and 1x frame clock. The output data rate is 18× sample rate; hence, it is suited for low sample rates, typically up to 40 MSPS. This interface is primarily intended to be used when the averaging and digital filters are enabled.

Table 7. Summary of Output Interface Options

FEATURE	OPTIONS	AVAILABLE IN		DEFAULT AFTER POWER UP AND RESET	BRIEF DESCRIPTION
		1 wire	2 wire		
Wire interface	1 wire and 2 wire			1 wire	1 wire – ADC data is sent serially over one pair of LVDS pins 2 wire – ADC data is split and sent serially over two pairs of LVDS pins
Serialization factor	16×	X	X	16×	For 16-bit ADC mode Can also be used with 14-bit ADC mode – the 14-bit ADC data is padded with two zeros and the combined 16-bit data is serialized.
	18×	X			18-bit data is available when 16-bit ADC mode is used with averaging and decimation filters enabled.
	14×	X	X		For 14-bit ADC mode only
DDR bit-clock frequency	8×	X		8×	16× serialization
	4×		X		16× serialization Only with 2-wire interface
	9×	X			18× serialization
	7×	X			14× serialization
	3.5×		X		14× serialization Only with 2-wire interface

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Table 7. Summary of Output Interface Options (continued)

FEATURE	OPTIONS	AVAILABLE IN		DEFAULT AFTER POWER UP AND RESET	BRIEF DESCRIPTION
		1 wire	2 wire		
Frame-clock frequency	1× sample rate	X		1×	
	1/2× sample rate		X		
Bit sequence	Bytewise		X	—	Bytewise – The ADC data is split into upper and lower bytes, which are output on separate wires. Bitwise – The ADC data is split into even and odd bits, which are output on separate wires. Wordwise – Successive ADC data samples are sent over separate wires. These options are available only with 2-wire interface.
	Bitwise		X		
	Wordwise		X		

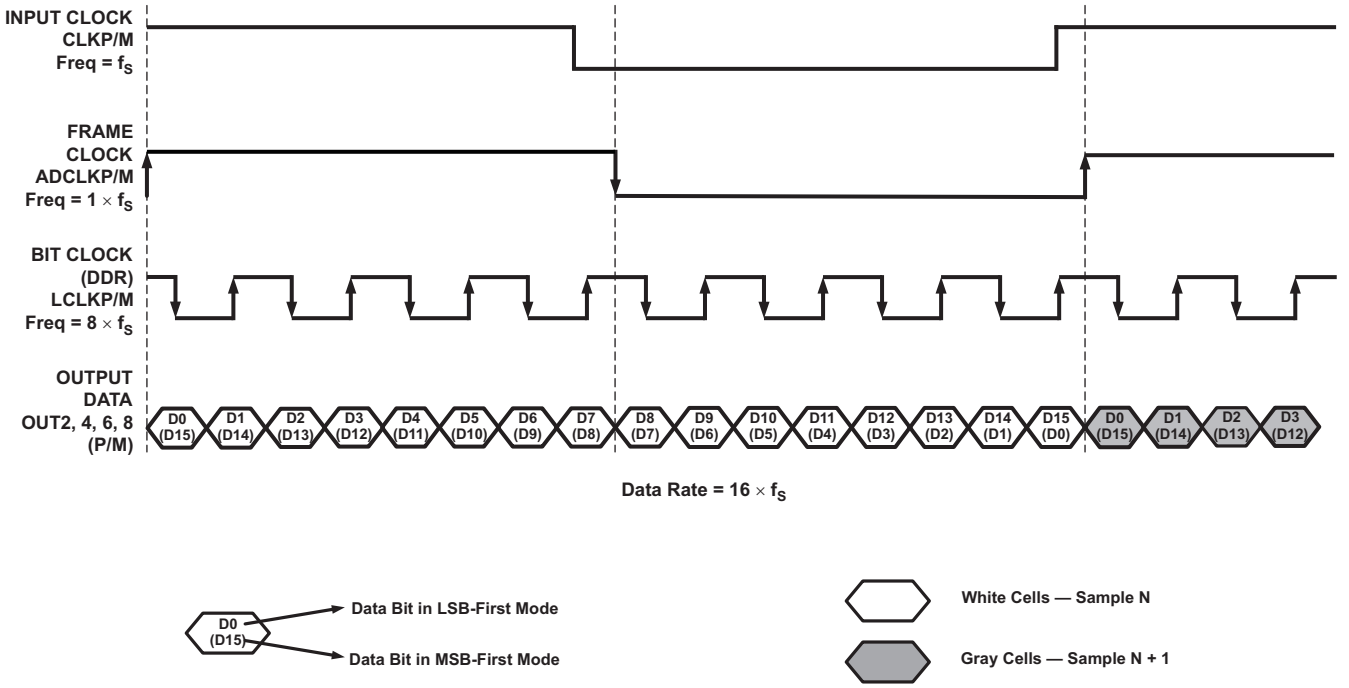


Figure 53. Output LVDS Interface, 1-Wire, 16× Serialization

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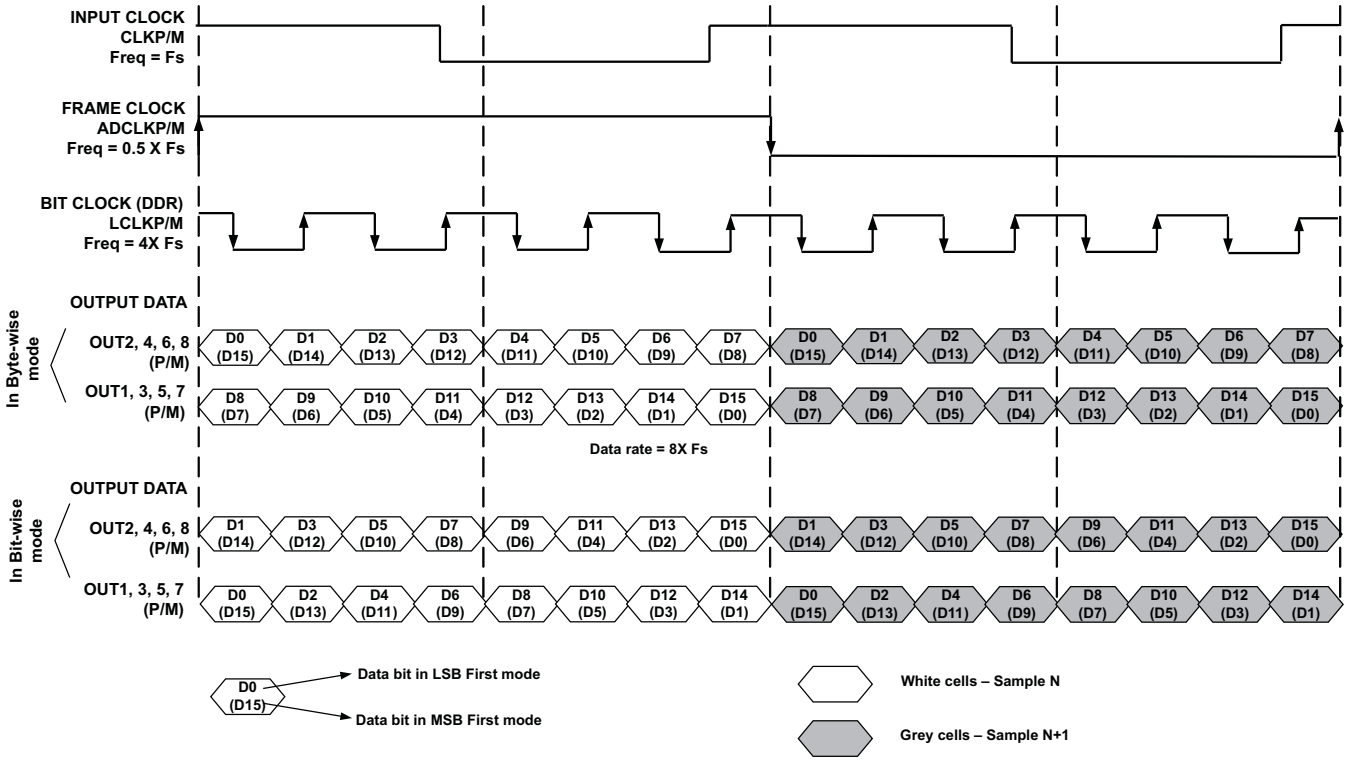


Figure 54. LVDS Output Interface, 2-Wire, 8× Serialization, Bytewise and Bitwise Modes

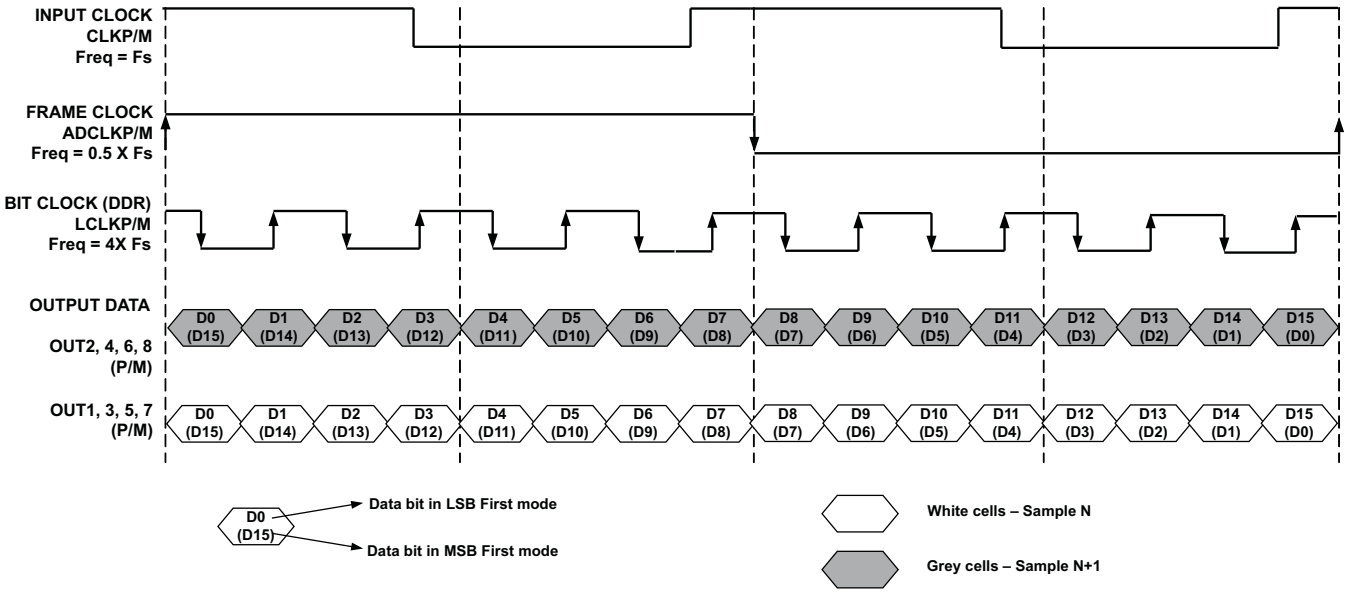


Figure 55. LVDS Output Interface, 2-Wire, 8× Serialization, Wordwise Mode

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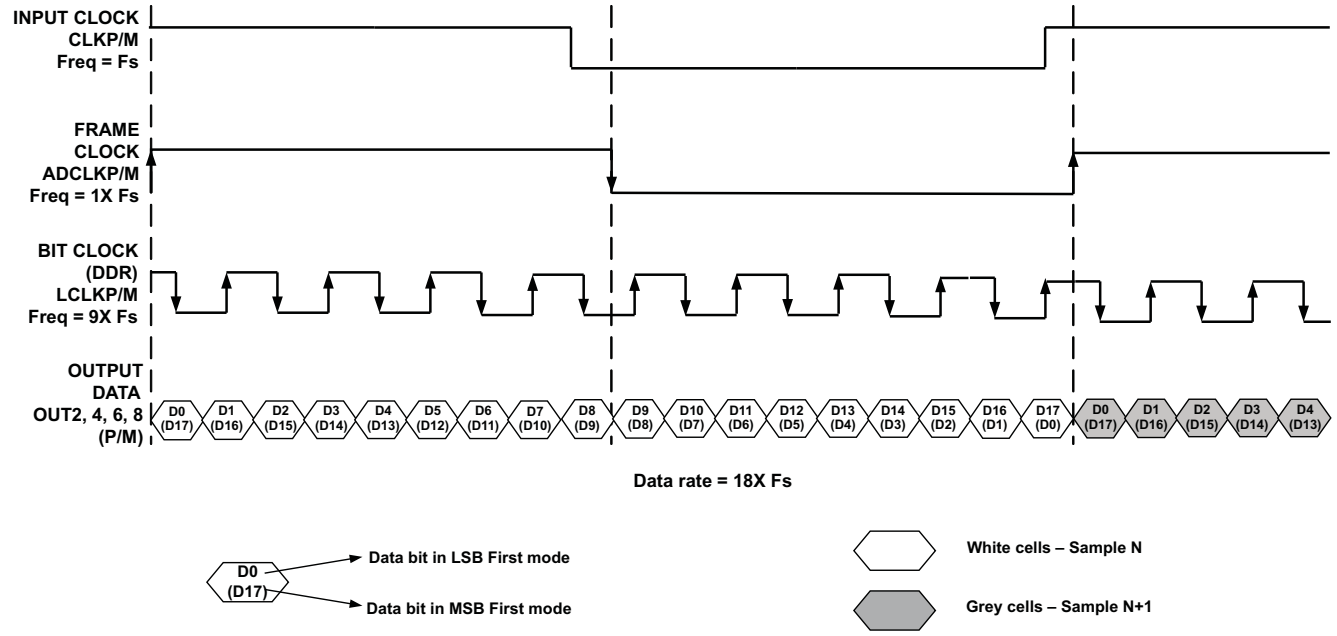


Figure 56. LVDS Output Interface, 1-Wire, 18× Serialization

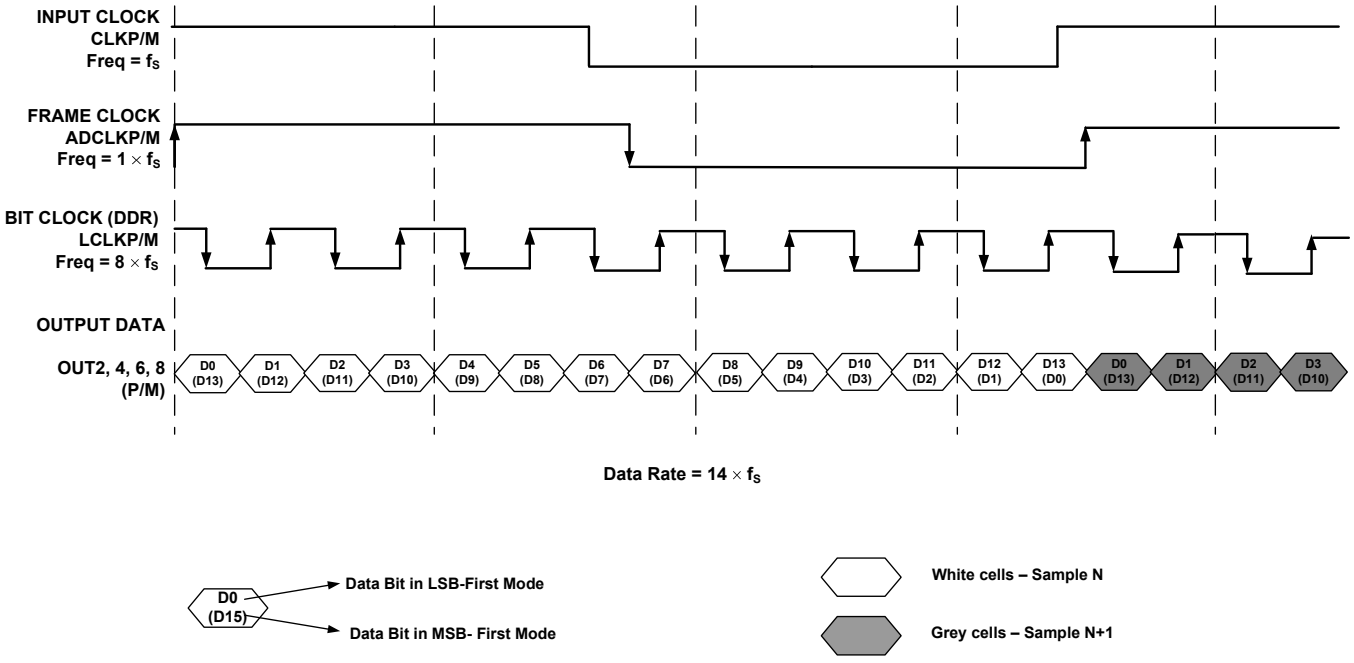


Figure 57. LVDS Output Interface, 1-Wire, 14× Serialization

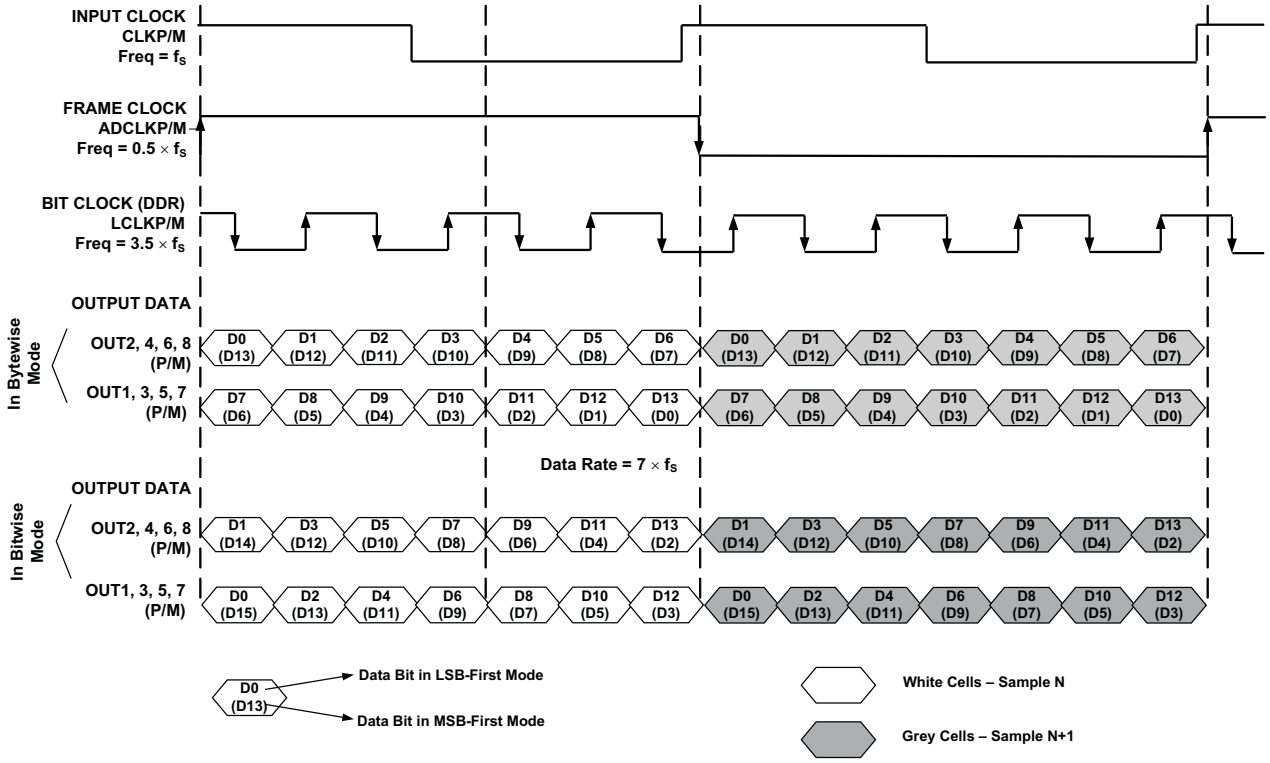


Figure 58. LVDS Output Interface, 2-Wire, 7× Serialization

8.3.9 Programmable LCLK Phase

The ADS5263 allows programmability of the edge of the output bit clock (LCLK) using register bits <PHASE_DDR> as follows:

The default value of PHASE_DDR after reset is 10, and the default phase corresponds to Figure 59.

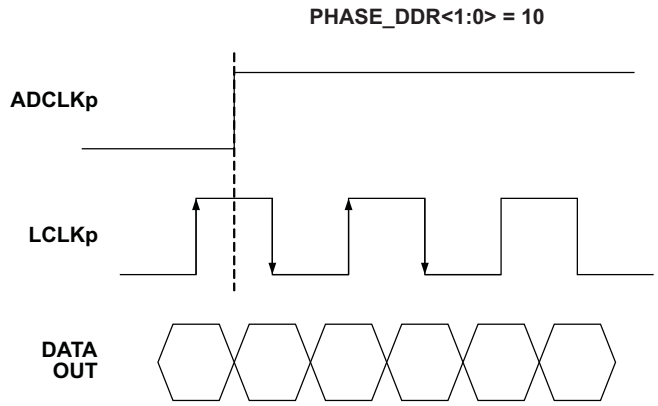


Figure 59. Default LCLK Phase

The phase can also be changed to one of the following states by changing the value of the <PHASE_DDR1:0> bits (and setting register bit EN_REG_42 = 1).

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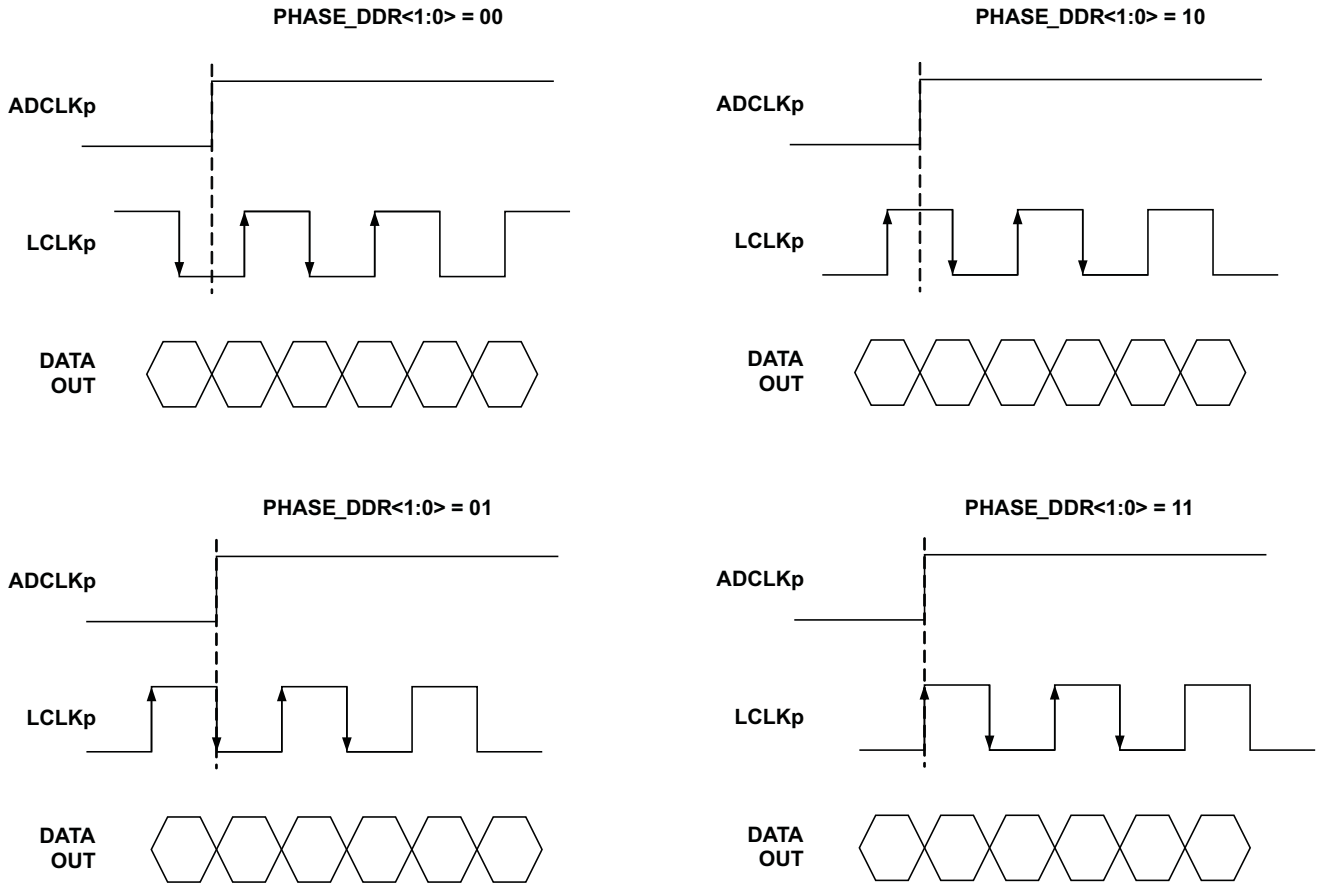


Figure 60. Programmable LCLK Phases

8.4 Device Functional Modes

8.4.1 Device Configuration

ADS5263 has several modes that can be configured using a serial programming interface, as described below. In addition, the device has dedicated parallel pins for controlling common functions such as power down and internal or external reference selection.

Table 8. PDN CONTROL PIN

VOLTAGE APPLIED ON PDN	STATE OF REGISTER BIT <CONFIG PDN pin>	DESCRIPTION
0 V	X (don't care)	Normal operation
Logic HIGH	0	Device enters global power-down mode
	1	Device enters standby mode

Table 9. $\overline{\text{INT/EXT}}$ CONTROL PIN

VOLTAGE APPLIED ON $\overline{\text{INT/EXT}}$	DESCRIPTION
0 V	External reference mode. Apply voltage on VCM pin to set the references for ADC operation.
Logic HIGH	Internal reference

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8.4.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back on SDOUT pin. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, after power up and device reset, the SDOUT pin is in the high-impedance state. When the readout mode is enabled using the register bit <READOUT>, SDOUT outputs the contents of the selected register serially, described as follows.

- Set register bit <READOUT> = 1 to put the device in serial readout mode. This disables any further writes into the internal registers, EXCEPT the register at address 1. Note that the <READOUT> bit itself is also located in register 1.
  The device can exit readout mode by writing <READOUT> to 0.
  Only the contents of register at address 1 cannot be read in the register readout mode.
- Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content is to be read.
- The device serially outputs the contents (D15–D0) of the selected register on the SDOUT pin.
- The external controller can latch the contents at the rising edge of SCLK.
- To exit the serial readout mode, reset register bit <READOUT> = 0, which enables writes into all registers of the device. At this point, the SDOUT pin enters the high-impedance state.

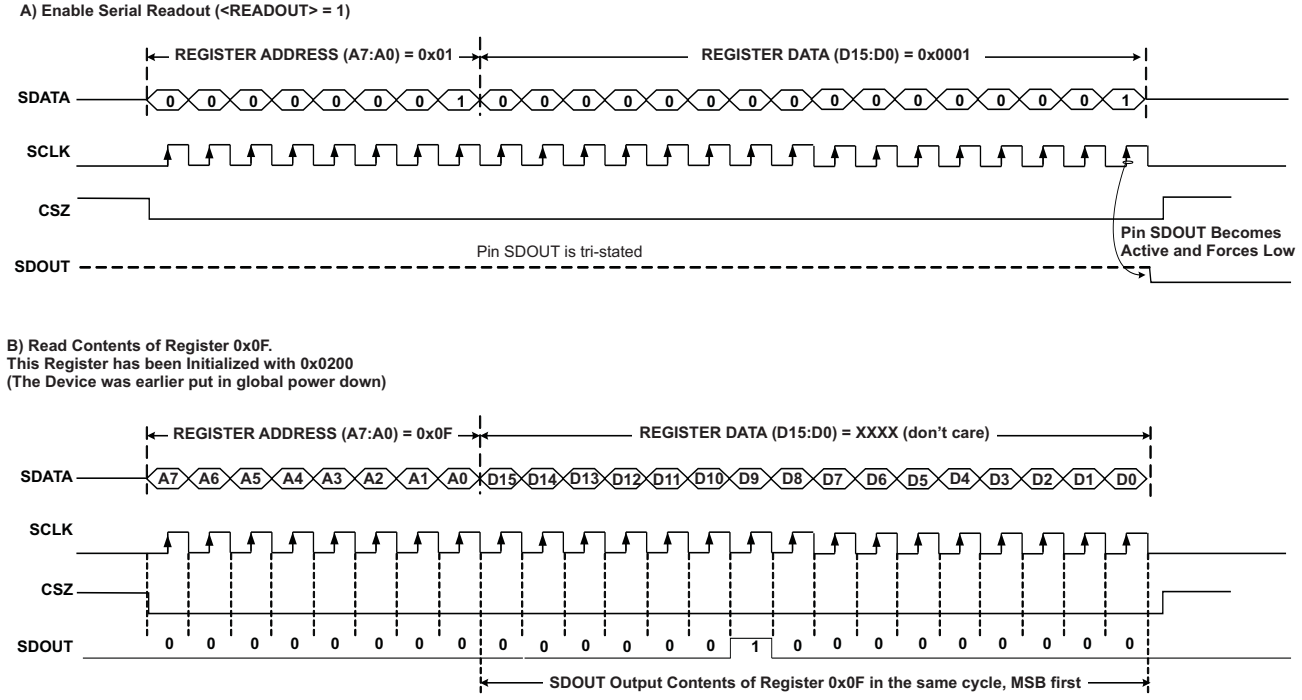


Figure 61. Serial Readout Timing

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8.5 Programming

8.5.1 Serial Interface

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins $\overline{CS}$ (serial interface enable), SCLK (serial interface clock) and SDATA (serial interface data).

When $\overline{CS}$ is low,

- Serial shift of bits into the device is enabled.
- Serial data (on SDATA pin) is latched at every rising edge of SCLK.
- The serial data is loaded into the register at every 24th SCLK rising edge.

In case the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse.

The first 8 bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (a few hertz) and also with non-50% SCLK duty cycle.

8.5.2 Register Initialization

After power up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Through a hardware reset by applying a low-going pulse on the $\overline{RESET}$ pin (of width greater than 10 ns) as shown in Figure 62.

   OR

2. By applying software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the **<RESET>** bit to ***low***. In this case, the RESET pin is kept high (inactive).

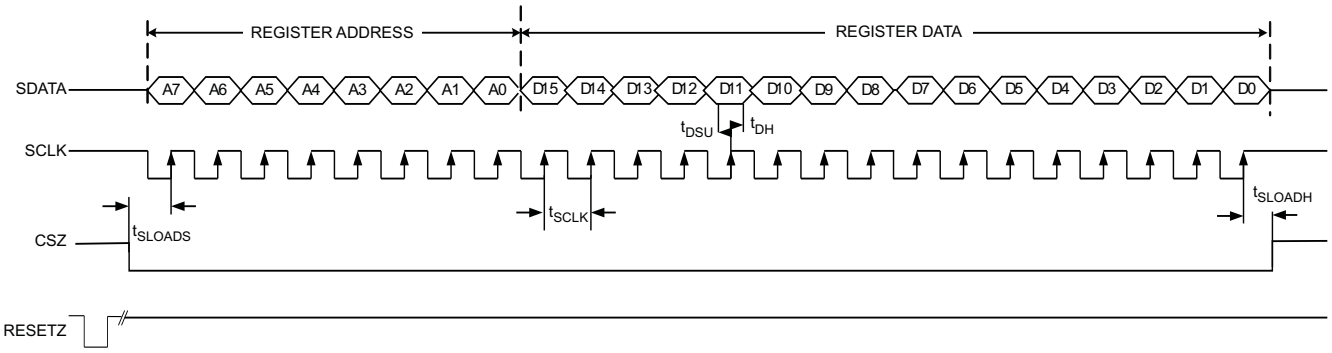


Figure 62. Serial Interface Timing

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8.6 Register Maps

Table 10. Summary of Functions Supported by Serial Interface(1)

Register Address	Register Data(2)															
A7-A0 in HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<RESET>
1	0	0	0	0	0	0	0	0	0	0	0	<EN _HIGH _ADDRS>	0	0	0	<READOUT>
2	0	0	<EN SYNC>	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	<EN _CLAMP>	0	0	0	0	0	0	0	0	0	0
F	0	0	0	0	0	<CONFIG PD PIN>	<GLOBAL PDN>	<STANDBY >	<PDN CH 4B>	<PDN CH 3B>	<PDN CH 2B>	<PDN CH 1B>	<PDN CH 4A>	<PDN CH 3A>	<PDN CH 2A>	<PDN CH 1A>
11	0	0	0	0	0	<LVDS CURR DATA>			0	<LVDS CURR ADCLK>			0	<LVDS CURR LCLK>		
12	0	<ENABLE LVDS TERM>	0	0	0	<LVDS TERM DATA>			0	<LVDS TERM ADCLK>			0	<LVDS TERM LCLK>		
14	0	0	0	0	0	0	0	0	0	0	0	0	<EN LFNS CH 4>	<EN LFNS CH 3>	<EN LFNS CH 2>	<EN LFNS CH 1>
25	0	0	0	0	0	0	0	0	0	<RAMP TEST PATTERN>	<DUAL CUSTOM PATTERN >	<SINGLE CUSTOM PATTERN>	CUSTOM PATTERN B DATA[15...14]		CUSTOM PATTERN A DATA[15...14]	
26	CUSTOM PATTERN A DATA[13..0]														0	0
27	CUSTOM PATTERN B DATA[13..0]														0	0
28	<EN WORD-WISE CONTROL>												<WORD-WISE CH4	<WORD-WISE CH3>	<WORD-WISE CH2>	<WORD-WISE CH1>
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<EN DIG FILTER>	<EN AVG>
2A	<GAIN CH4>				<GAIN CH3>				<GAIN CH2>				<GAIN CH1>			
2C	0	0	0	0	0	0	0	0	<AVG OUT 4>		<AVG OUT 3>		<AVG OUT 2>		<AVG OUT 1>	
2E	0	0	0	0	0	0	<FILTER TYPE CH1>			<DEC by RATE CH1>			0	<ODD TAP CH1>	0	<USE FILTER CH1>
2F	0	0	0	0	0	0	<FILTER TYPE CH2>			<DEC by RATE CH2>			0	<ODD TAP CH2>	0	<USE FILTER CH2>
30	0	0	0	0	0	0	<FILTER TYPE CH3>			<DEC by RATE CH3>			0	<ODD TAP CH3>	0	<USE FILTER CH3>
31	0	0	0	0	0	0	<FILTER TYPE CH4>			<DEC by RATE CH4>			0	<ODD TAP CH4>	0	<USE FILTER CH4>
38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<OUTPUT RATE>	
42	<EN_REG_42>	0	0	0	0	0	0	0	0	<PHASE_DDR>		0	<EXT_REF_VCM>	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.
(2) All registers are cleared to zero after software or hardware reset is applied.

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Register Maps (continued)

Table 10. Summary of Functions Supported by Serial Interface(1) (continued)

Register Address	Register Data(2)															
A7-A0 in HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<SYNC PATTERN>	<DESKEW PATTERN>
46	<EN SERIALIZATION>	0	0	<18x SERIALIZATION>	<16× SERIALIZATION>	<14× SERIALIZATION>	0	0	0	0	<PAD two 0s>	0	<MSB FIRST>	<2S COMPL>	0	<2-WIRE 0.5X FRAME>
50	<EN MAP1>	0	0	0	<MAP_Ch1234_OUT2A>				<MAP_Ch1234_OUT1B>				<MAP_Ch1234_OUT1A>			
51	<EN MAP2>	0	0	0	<MAP_Ch1234_OUT3B>				<MAP_Ch1234_OUT3A>				<MAP_Ch1234_OUT2B>			
52	<EN MAP3>	0	0	0	0	0	0	0	<MAP_Ch1234_OUT4B>				<MAP_Ch1234_OUT4A>			
57	0	0	0	0	0	0	0	0	0	0	<DIS STATIC OFFSET CORR>	0	0	0	0	0
5A to 65	<EN CUSTOM FILT CH1>				<COEFFn SET CH1>(3)											
66 to 71	<EN CUSTOM FILT CH2>				<COEFFn SET CH2>(3)											
72 to 7D	<EN CUSTOM FILT CH3>				<COEFFn SET CH3>(3)											
7E to 89	<EN CUSTOM FILT CH4>				<COEFFn SET CH4>(3)											
CB	<EN DITH1>	0	0	0	0	0	0	<EN DITH2>	<EN DITH3>	0	0	0	0	0	0	0
B3	<EN ADC MODE>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<16B/14B ADC MODE>
F0	<EN_EXT_REF>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(3) Where n = 0 to 11

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8.6.1 Default State After Reset

- Device is in normal operation mode with 16-bit ADC enabled for all 4 channels.
- Output interface is 1-wire, 16× serialization with 8× bit clock and 1× frame clock frequency
- Serial readout is disabled
- PD pin is configured as global power-down pin
- LVDS output current is set to 3.5 mA; internal termination is disabled.
- Digital gain is set to 0 dB.
- Digital modes such as LFNS, digital filters are disabled.

8.6.2 Description of Serial Registers

Figure 63. Register Address 0

REGISTER ADDRESS	REGISTER DATA															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<RESET>

D0 <RESET>

1 Software reset applied – resets all internal registers to their default values and self-clears to 0

Figure 64. Register Address 1

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0	0	0	<EN_HIGH_ADDRS>	0	0	0	<READOUT>

D4 <EN_HIGH_ADDRS>

See section *External Reference Mode*

D0 <READOUT>

0 Serial readout of registers is disabled. Pin SDOUT is in the high-impedance state.

1 Serial readout enabled, SDOUT pin functions as serial data readout.

Figure 65. Register Address 2

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	0	0	<EN SYNC>	0	0	0	0	0	0	0	0	0	0	0	0	0

D13 <EN SYNC>

0 SYNC pin is disabled.

1 SYNC pin can be used to synchronize the decimation filters across channels and across multiple chips.

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Figure 66. Register Address 9

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
9	0	0	0	0	0	<EN_CLAMP>	0	0	0	0	0	0	0	0	0	0

D10 <EN_CLAMP>

0 Internal clamp is disabled.

1 Internal clamp is enabled. The clamp works only for the 14-bit ADC input pins. The clamping is synchronized with the pulse applied on the SYNC pin (see *Clamp Function for CCD Signals* in the application section).

Figure 67. Register Address F

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F	0	0	0	0	0	<CONFIG PD PIN>	<GLOBAL PDN>	<STAND BY>	<PDN CH 4B>	<PDN CH 3B>	<PDN CH 2B>	<PDN CH 1B>	<PDN CH 4A>	<PDN CH 3A>	<PDN CH 2A>	<PDN CH 1A>

D10 <CONFIG PDN PIN> Can be used to configure PDN pin as global power down or standby

0 PDN pin functions as global power down.

1 PDN pin functions as standby.

D9 <GLOBAL PDN>

0 Normal ADC operation

1 Device is put in global power down. All four channels are powered down, including LVDS output data and clock buffers.

D8 <STANDBY>

0 Normal ADC operation

1 Device is put in standby. All four ADCs are powered down. Internal PLL, LVDS bit clock, and frame clock are running.

D7–D0 <PDN CH X> Individual channel power down

0 Channel X is powered up.

1 Channel X is powered down.

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Figure 68. Register Address 11

REGISTER ADDRESS	REGISTER DATA															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	0	0	0	0	0	<LVDS CURR DATA>			0	<LVDS CURR ADCLK>			0	<LVDS CURR LCLK>		

D10–D8 <LVDS CURR DATA> LVDS current control for data buffers

000 3.5 mA
001 2.5 mA
010 1.5 mA
011 0.5 mA
100 7.5 mA
101 6.5 mA
110 5.5 mA
111 4.5 mA

D6–D4 <LVDS CURR LCLK> LVDS current control for frame-clock buffer

000 3.5 mA
001 2.5 mA
010 1.5 mA
011 0.5 mA
100 7.5 mA
101 6.5 mA
110 5.5 mA
111 4.5 mA

D2–D0 <LVDS CURR LCLK> LVDS current control for bit-clock buffer

000 3.5 mA
001 2.5 mA
010 1.5 mA
011 0.5 mA
100 7.5 mA
101 6.5 mA
110 5.5 mA
111 4.5 mA

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Figure 69. Register Address 12

REGISTER ADDRESS	REGISTER DATA															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12	0	<ENABLE LVDS TERM>	0	0	0	<LVDS TERM DATA>			0	<LVDS TERM ADCLK>			0	<LVDS TERM LCLK>		

D14 <ENABLE LVDS TERM>

0 Internal termination disabled

1 Internal termination enabled

D10–D8 <LVDS TERM DATA> Internal LVDS termination for data buffers

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

D6–D4 <LVDS TERM ADCLK> Internal LVDS termination for frame clock buffer

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

D2–D0 <LVDS TERM LCLK> Internal LVDS termination for bit clock buffer

000 No internal termination

001 150 Ω

010 100 Ω

011 60 Ω

100 80 Ω

101 55 Ω

110 45 Ω

111 35 Ω

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Figure 70. Register Address 14

REGISTER ADDRESS	REGISTER DATA															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
14	0	0	0	0	0	0	0	0	0	0	0	0	<EN LFNS CH4>	<EN LFNS CH3>	<EN LFNS CH2>	<EN LFNS CH1>

D3–D0 <EN LFNS CH X> low-frequency noise-suppression mode is enabled for channel X.

0 LFNS mode is disabled.

1 LFNS mode is enabled for channel X.

In 16-bit ADC mode, <EN LFNS CH X> enables LFNS for channel CH X.

In 14-bit ADC mode, <EN LFNS CH X> enables LFNS for channel CH X B.

Figure 71. Register Address 25

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25	0	0	0	0	0	0	0	0	0	<RAMP TEST PATTERN>	<DUAL CUSTOM PATTERN>	<SINGLE CUSTOM PATTERN>	CUSTOM PATTERN B DATA[15...14]		CUSTOM PATTERN A DATA[15...14]	

D6 <RAMP TEST PATTERN>

0 Ramp test pattern is disabled.

1 Ramp test pattern is enabled; output code increments by one LSB every clock cycle.

D5 <DUAL CUSTOM PATTERN>

0 Dual custom pattern is disabled.

1 Dual custom pattern is enabled.

Two custom patterns can be specified in registers PATTERN A and PATTERN B. The two patterns are output one after the other (instead of ADC data).

D5 <SINGLE CUSTOM PATTERN>

0 Single custom pattern is disabled.

1 Single custom pattern is enabled.

The custom pattern can be specified in register A and is output every clock cycle instead of ADC data.

D3–D2 <CUSTOM PATTERN B bits D15 and D14>

D1–D0 <CUSTOM PATTERN A bits D15 and D14>

Specify bits D15 and D14 of custom pattern in these register bits.

Figure 72. Register Address 26 and 27

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
26	CUSTOM PATTERN A DATA[13..0]														0	0
27	CUSTOM PATTERN B DATA[13..0]														0	0

Specify bits D13 to D0 of custom pattern in these registers.

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Figure 73. Register Address 28

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
28	<EN WORD-WISE CONTROL>												<WORD-WISE CH4>	<WORD-WISE CH3>	<WORD-WISE CH2>	<WORD-WISE CH1>

D15 <EN WORD-WISE CONTROL>

0 Control of word-wise mode is disabled.

1 Control of word-wise mode is enabled.

D3–D0 <WORD-WISE CH XL>

0 Output data is serially sent in byte-wise format.

1 Output data is serially sent in word-wise format ONLY when 2-wire mode is enabled (see register 0x46).

Figure 74. Register Address 2A

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2A	<GAIN CH4>				<GAIN CH3>				<GAIN CH2>				<GAIN CH1>			

<GAIN CH x> Individual channel gain control

In 16-bit ADC mode, <GAIN CH X> sets gain for channel CH X A.

In 14-bit ADC mode, <GAIN CH X> sets gain for channel CH X B.

0000 0 dB

0001 1 dB

0010 2 dB

0011 3 dB

0100 4 dB

0101 5 dB

0110 6 dB

0111 7 dB

1000 8 dB

1001 9 dB

1010 10 dB

1011 11 dB

1100 12 dB

1101 to 1111 Unused

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Figure 75. Register Address 2C

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2C	0	0	0	0	0	0	0	0	<AVG OUT 4>		<AVG OUT 3>		<AVG OUT 2>		<AVG OUT 1>	

<AVG OUT 1> **These bits determine which data stream is output on LVDS pins OUT1A/1B.**
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

00 LVDS OUT1A/1B buffers are powered down.

01 OUT1A/1B output digital data corresponding to the signal applied on analog input pin IN1.

10 OUT1A/1B output digital data corresponding to the average of signals applied on analog input pins IN1 and IN2.

11 OUT1A/1B output digital data corresponding to the average of signals applied on analog input pins IN1, IN2, IN3, and IN4.

<AVG OUT 2> **These bits determine which data stream is output on LVDS pins OUT2A/2B**
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

00 LVDS OUT2A/2B buffers are powered down.

01 OUT2A/2B output digital data corresponding to the signal applied on analog input pin IN2.

10 OUT2A/2B output digital data corresponding to the signal applied on analog input pin IN3.

11 OUT2A/2B output digital data corresponding to the average of signals applied on analog input pins IN3 and IN4.

<AVG OUT 3> **These bits determine which data stream is output on LVDS pins OUT3A/3B**
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

00 LVDS OUT3A/3B buffers are powered down.

01 OUT3A/3B output digital data corresponding to the signal applied on analog input pin IN3.

10 OUT3A/3B output digital data corresponding to the signal applied on analog input pin IN2.

11 OUT3A/3B output digital data corresponding to the average of signals applied on analog input pins IN1 and IN4.

<AVG OUT 4> **These bits determine which data stream is output on LVDS pins OUT4A/4B**
(after global enable bit for averaging is enabled <EN AVG GLO> = 1)

00 LVDS OUT4A/4B buffers are powered down.

01 OUT4A/4B output digital data corresponding to the signal applied on analog input pin IN4.

10 OUT4A/4B output digital data corresponding to the average of signals applied on analog input pins IN3 and IN4.

11 OUT4A/4B output digital data corresponding to the average of signals applied on analog input pins IN1, IN2, IN3, and IN4.

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Figure 76. Register Address 29

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<EN DIG FILTER>	<EN AVG GLO>

D1 <EN DIG FILTER>

0 Digital filter mode is disabled.

1 Digital filter mode is enabled on all channels. To turn filter on or off for individual channels, also set the **<USE FILTER CH X>** register bit.

D0 <EN AVG GLO>

0 Averaging mode is disabled.

1 Averaging mode is enabled on all channels.

Figure 77. Register Address 2E, 2F, 30, and 31

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2E	0	0	0	0	0	0	<FILTER TYPE CH1>			<DEC by RATE CH1>			0	0	0	<USE FILTER CH1>
2F	0	0	0	0	0	0	<FILTER TYPE CH2>			<DEC by RATE CH2>			0	0	0	<USE FILTER CH2>
30	0	0	0	0	0	0	<FILTER TYPE CH3>			<DEC by RATE CH3>			0	0	0	<USE FILTER CH3>
31	0	0	0	0	0	0	<FILTER TYPE CH4>			<DEC by RATE CH4>			0	0	0	<USE FILTER CH4>

D0 <USE FILTER CH X>

0 Filter is turned OFF on channel X

1 Filter is turned ON on channel X.

D2 <ODD TAP CH X> select filter with even or odd tap for channel X

0 Even tap filter is selected.

1 Odd tap filter is selected.

D6–D4 <DEC by RATE CH X> select decimation rates for channel X

000 Decimate-by-2 rate is selected.

001 Decimate-by-4 rate is selected.

100 Decimate-by-8 rate is selected.

Other combinations Do not use

D9–D7 <FILTER TYPE CH X> select type of filter for channel X

000 Low-pass filter with decimate-by-2 rate

001 High-pass filter with decimate-by-2 rate

010 Low-pass filter with decimate-by-4 rate

011 Band-pass filter #1 with decimate-by-4 rate

100 Band-pass filter #2 with decimate-by-4 rate

101 High-pass filter with decimate-by-4 rate

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Figure 78. Register Address 38

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<OUTPUT RATE>	

D1–D0 <OUTPUT RATE>

00 Output data rate = 1× sample rate

01 Output data rate = 0.5× sample rate

02 Output data rate = 0.25× sample rate

03 Output data rate = 0.125× sample rate

Figure 79. Register Address 42

REGISTER ADDRESS	REGISTER DATA															
A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
42	<EN_REG_42>	0	0	0	0	0	0	0	0	<PHASE_DDR>		0	<EXT_REF_VCM>	0	0	0

D15 <EN_REG_42>

0 Disables register bits D6, D5 and D3

1 Enables register bits D6, D5 and D3

D6-D5 <PHASE_DDR>

Note that the default value of <PHASE_DDR> bit = 10. However, in this condition, if the contents of the register 0x42 are readout, they will be read as 00.
If the value of <PHASE_DDR> bit is now modified by writing into this resgister, then subsequent writes will read back the written value.
Register bit <PHASE_DDR> can be used to control the phase of LCLK (with respect to the rising edge of the frame clock, ADCLK). See *Programmable LCLK Phase* for details.

D3 EXT_REF_VCM

0 Internal reference mode

1 External reference mode, Apply voltage on VCM input
See section *External Reference Mode*
To use this mode, the register bit <EN_EXT_REF> in register 0xF0 must also be set to 1.

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Figure 80. Register Address 45

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<SYNC PATTERN>	<DESKEW PATTERN>

D1 <SYNC PATTERN>

0 Sync pattern disabled.

1 Sync pattern enabled.

All channels output a repeating pattern of 8 1s and 8 0s instead of ADC data.

Output data [15…0] = 0xFF00

D0 <DESKEW PATTERN>

0 Deskew pattern disabled.

1 Deskew pattern enabled.

All channels output a repeating pattern of 1010101010101010 instead of ADC data.

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Figure 81. Register Address 46

A7-A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
46	<ENABLE SERIALIZATION>	0	0	<18b SERIALIZATION>	<16b SERIALIZATION>	<14b SERIALIZATION>	0	0	0	0	<PAD two 0s>	0	<MSB FIRST>	<2S COMPL>	0	<2-WIRE 0.5X FRAME>

D15 <ENABLE SERIALIZATION> Enable bit for serialization bits in register 46>

0 Disable control of serialization register bits in register 0x46.

1 Enable control of serialization register bits in register 0x46.

D12 <18b SERIALIZATION> Enable 18-bit serialization, to be used to send 18-bit data when using digital processing modes (see section *Performance with Digital Processing Blocks*)

0 Disable 18-bit serialization.

1 Enable 18-bit serialization. ADC data bits D[17..0] are serialized.

D11 <16b SERIALIZATION> Enable 16-bit serialization, to be used in 16-bit ADC mode

0 Disable 16-bit serialization.

1 Enable 16-bit serialization. ADC data bits D[15..0] are serialized.

D10 <14b SERIALIZATION> Enable 14-bit serialization, to be used in 14-bit ADC mode

0 Disable 14-bit serialization.

1 Enable 14-bit serialization. ADC data bits D[13..0] are serialized.

D5 <PAD two 0s>

0 Padding disabled.

1 Two zero bits are padded to the ADC data on the LSB side and the combined data is then serialized. When the bit <4b SERIALIZATION> is also enabled, two zero bits are padded to the 14-bit ADC data. The combined data (= ADC[13..0],0,0) is serially output.

D3 <MSB First>

0 ADC data is output serially, with LSB bit first.

1 ADC data is output serially, with MSB bit first.

D2 <2s COMPL>

0 Output data format is offset binary.

1 Output data format is 2s complement.

D0 <2-WIRE 0.5× frame clock>

0 Enables 1-wire LVDS interface with 1× frame clock.

1 Enables 2-wire LVDS interface with 0.5× frame clock.

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Figure 82. Register Address 50

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
50	<EN MAP1>	0	0	0	<MAP_Ch1234_OUT2A>				<MAP_Ch1234_OUT1B>				<MAP_Ch1234_OUT1A>			

D15 <EN MAP1>

0 Mapping function for outputs OUT1A, OUT1B, and OUT2A is disabled.

1 Mapping function for outputs OUT1A, OUT1B, and OUT2A is enabled.

D3–D0 <MAP_Ch1234_OUT1A>

0000 MSB byte corresponding to input IN1 is output on OUT1A.

0001 LSB byte corresponding to input IN1 is output on OUT1A.

0010 MSB byte corresponding to input IN2 is output on OUT1A.

0011 LSB byte corresponding to input IN2 is output on OUT1A.

0100 MSB byte corresponding to input IN3 is output on OUT1A.

0101 LSB byte corresponding to input IN3 is output on OUT1A.

0110 MSB byte corresponding to input IN4 is output on OUT1A.

0111 LSB byte corresponding to input IN4 is output on OUT1A.

1xxx OUT1A LVDS buffer is powered down.

D7–D4 <MAP_Ch1234_OUT1B>

0000 MSB byte corresponding to input IN1 is output on OUT1B.

0001 LSB byte corresponding to input IN1 is output on OUT1B.

0010 MSB byte corresponding to input IN2 is output on OUT1B.

0011 LSB byte corresponding to input IN2 is output on OUT1B.

0100 MSB byte corresponding to input IN3 is output on OUT1B.

0101 LSB byte corresponding to input IN3 is output on OUT1B.

0110 MSB byte corresponding to input IN4 is output on OUT1B.

0111 LSB byte corresponding to input IN4 is output on OUT1B.

1xxx OUT1B LVDS buffer is powered down.

D11–D8 <MAP_Ch1234_OUT2A>

0000 MSB byte corresponding to input IN1 is output on OUT2A.

0001 LSB byte corresponding to input IN1 is output on OUT2A.

0010 MSB byte corresponding to input IN2 is output on OUT2A.

0011 LSB byte corresponding to input IN2 is output on OUT2A.

0100 MSB byte corresponding to input IN3 is output on OUT2A.

0101 LSB byte corresponding to input IN3 is output on OUT2A.

0110 MSB byte corresponding to input IN4 is output on OUT2A.

0111 LSB byte corresponding to input IN4 is output on OUT2A.

1xxx OUT2A LVDS buffer is powered down.

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Figure 83. Register Address 51

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
51	<EN MAP2>	0	0	0	<MAP_Ch1234_OUT3B>				<MAP_Ch1234_OUT3A>				<MAP_Ch1234_OUT2B>			

D15 <EN MAP2>

0 Mapping function for outputs OUT3B, OUT3A, and OUT2B is disabled.

1 Mapping function for outputs OUT3B, OUT3A, and OUT2B is enabled.

D3–D0 <MAP_Ch1234_OUT2B>

0000 MSB byte corresponding to input IN1 is output on OUT2B.

0001 LSB byte corresponding to input IN1 is output on OUT2B.

0010 MSB byte corresponding to input IN2 is output on OUT2B.

0011 LSB byte corresponding to input IN2 is output on OUT2B.

0100 MSB byte corresponding to input IN3 is output on OUT2B.

0101 LSB byte corresponding to input IN3 is output on OUT2B.

0110 MSB byte corresponding to input IN4 is output on OUT2B.

0111 LSB byte corresponding to input IN4 is output on OUT2B.

1xxx OUT2B LVDS buffer is powered down.

D7–D4 <MAP_Ch1234_OUT3A>

0000 MSB byte corresponding to input IN1 is output on OUT3A.

0001 LSB byte corresponding to input IN1 is output on OUT3A.

0010 MSB byte corresponding to input IN2 is output on OUT3A.

0011 LSB byte corresponding to input IN2 is output on OUT3A.

0100 MSB byte corresponding to input IN3 is output on OUT3A.

0101 LSB byte corresponding to input IN3 is output on OUT3A.

0110 MSB byte corresponding to input IN4 is output on OUT3A.

0111 LSB byte corresponding to input IN4 is output on OUT3A.

1xxx OUT3A LVDS buffer is powered down.

D11–D8 <MAP_Ch1234_OUT3B>

0000 MSB byte corresponding to input IN1 is output on OUT3B.

0001 LSB byte corresponding to input IN1 is output on OUT3B.

0010 MSB byte corresponding to input IN2 is output on OUT3B.

0011 LSB byte corresponding to input IN2 is output on OUT3B.

0100 MSB byte corresponding to input IN3 is output on OUT3B.

0101 LSB byte corresponding to input IN3 is output on OUT3B.

0110 MSB byte corresponding to input IN4 is output on OUT3B.

0111 LSB byte corresponding to input IN4 is output on OUT3B.

1xxx OUT3B LVDS buffer is powered down.

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Figure 84. Register Address 52

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
52	<EN MAP3>	0	0	0	0	0	0	0	<MAP_Ch1234_OUT4B>				<MAP_Ch1234_OUT4B>			

D15 <EN MAP3>

0 Mapping function for outputs OUT4A and OUT4B is disabled.

1 Mapping function for outputs OUT4A and OUT4B is enabled.

D3–D0 <MAP_Ch1234_OUT4A>

0000 MSB byte corresponding to input IN1 is output on OUT4A.

0001 LSB byte corresponding to input IN1 is output on OUT4A.

0010 MSB byte corresponding to input IN2 is output on OUT4A.

0011 LSB byte corresponding to input IN2 is output on OUT4A.

0100 MSB byte corresponding to input IN3 is output on OUT4A.

0101 LSB byte corresponding to input IN3 is output on OUT4A.

0110 MSB byte corresponding to input IN4 is output on OUT4A.

0111 LSB byte corresponding to input IN4 is output on OUT4A.

1xxx OUT4A LVDS buffer is powered down.

D7–D4 <MAP_Ch1234_OUT4B>

0000 MSB byte corresponding to input IN1 is output on OUT4B.

0001 LSB byte corresponding to input IN1 is output on OUT4B.

0010 MSB byte corresponding to input IN2 is output on OUT4B.

0011 LSB byte corresponding to input IN2 is output on OUT4B.

0100 MSB byte corresponding to input IN3 is output on OUT4B.

0101 LSB byte corresponding to input IN3 is output on OUT4B.

0110 MSB byte corresponding to input IN4 is output on OUT4B.

0111 LSB byte corresponding to input IN4 is output on OUT4B.

1xxx OUT4B LVDS buffer is powered down.

Figure 85. Register Address 57

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
57	0	0	0	0	0	0	0	0	0	0	<DIS STATIC OFFSET CORR>	0	0	0	0	0

D5 <DIS STATIC OFFSET CORR> Disables algorithm to correct static offset in sub-ranging flash ADC inside pipeline, to be used in imaging applications where ADC is used to convert DC signal

0 Algorithm is active.

1 Algorithm is disabled.

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Figure 86. Register Address 5A to 65, 66 to 71, 72 to 7D, and 7E to 89

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
5A to 65	<EN CUSTOM FILT CH1>	0	0	0	<COEFFn SET CH1>											
66 to 71	<EN CUSTOM FILT CH2>				<COEFFn SET CH2>											
72 to 7D	<EN CUSTOM FILT CH3>				<COEFFn SET CH3>											
7E to 89	<EN CUSTOM FILT CH4>				<COEFFn SET CH4>											

D15 <EN CUSTOM FILT CH1> to <EN CUSTOM FILT CH4>

For description of these registers see Table 4.

D11–D0 <COEFFn SET CH1> to <COEFFn SET CH4>

For description of these registers see Table 4.

Figure 87. Register Address CB

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CB	<EN DITH1>	0	0	0	0	0	0	<EN DITH2>	<EN DITH3>	0	0	0	0	0	0	0

D15, D8, D7 <EN DITH1:3> Enable bits for dither algorithm

Set register bit EN_HIGH_ADDRS to 1 before programming these bits.

000 Dither algorithm is disabled.

111 Dither algorithm is enabled for all channels.
Using dither algorithm improves INL curve.
However, it may degrade the noise by as much as 3dB.

Figure 88. Register Address B3

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B3	<ENABLE ADC MODE>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	<16B/14B ADC MODE>

D15 <ENABLE ADC MODE>

0 Disable selection of 14-bit ADC mode.

1 Enables selection of 14 bit ADC mode.

D0 <16B/14B ADC MODE>

0 16-bit ADC operation is enabled.

1 14-bit ADC operation is enabled.

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Figure 89. Register Address F0

A7–A0 IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F0	<EN_EXT_REF>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D15 <EN_EXT_REF>

0 Internal reference mode.

1 Enable external reference mode using VCM pin, set the register bits in register 0x42.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ADS5263 is a high-performance 16-bit quad-channel ADC with sample rates up to 100 MSPS.

The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 16 clock cycles. The output is available as 16-bit data in serial LVDS format, coded in either offset binary or binary 2s-complement format.

The device also has a 14-bit low-power mode, where it operates as a quad-channel 14-bit ADC. The 16-bit front-end stage is powered down and the part consumes almost half the power, compared to the 16-bit mode. The ADS5263 can be dynamically switched between the two resolution modes. This allows systems to use the same part in a high-resolution, high-power mode or a low-resolution, low-power mode.

The INxA pins are used as the 16-bit ADC inputs, and the INxB pins function as the 14-bit ADC inputs.

9.1.1 Analog Input

The analog input consists of a switched-capacitor based differential sample and hold architecture.

This differential topology results in very good ac performance, even for high input frequencies at high sampling rates. The INxP and INxM pins must be externally biased around a common-mode voltage of 1.5 V, available on the VCM pin. For a full-scale differential input, each input pin INP, INM must swing symmetrically between VCM + 1 V and VCM – 1 V, resulting in a 4-Vpp differential input swing.

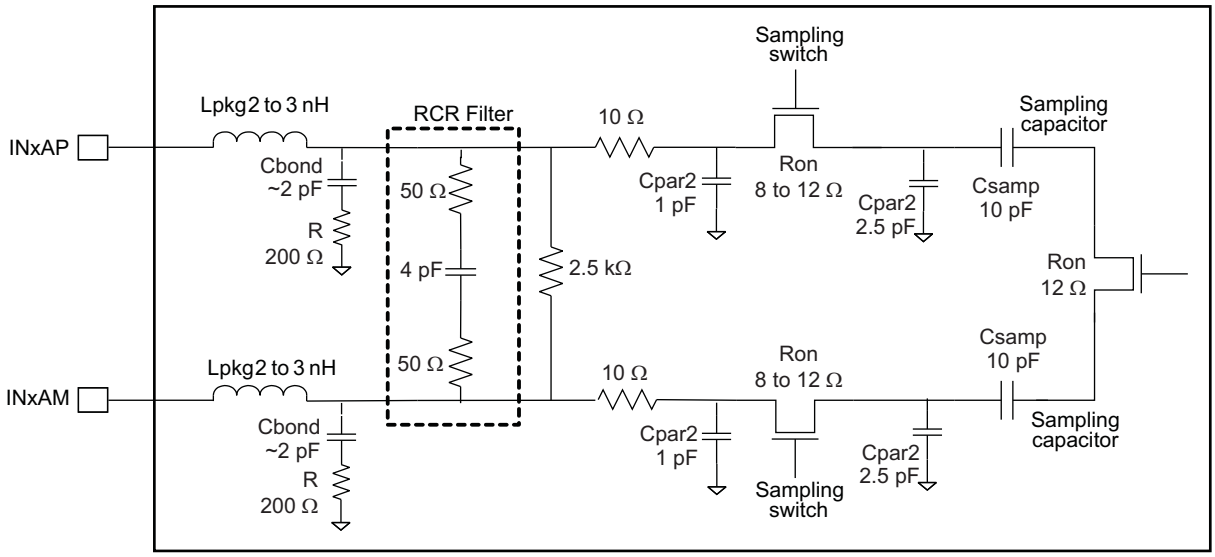


Figure 90. 16-Bit ADC – Analog Input Equivalent Circuit

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Application Information (continued)

9.1.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (<50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

Note that the device includes an internal R-C-R filter across the input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported, but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the drive circuit to support these glitches.

Figure 91 and Figure 92 show the impedance (Zin = Rin || Cin) looking across the differential ADC input pins. While designing the external drive circuit, the ADC input impedance must be considered.

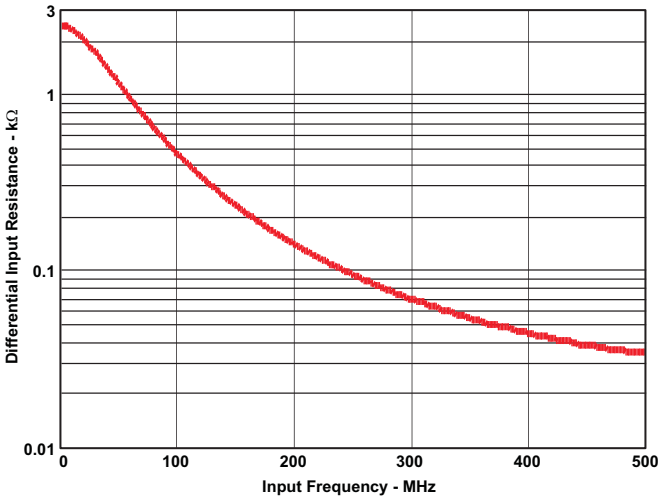


Figure 91. ADC Analog Input Resistance (Rin) Across Frequency

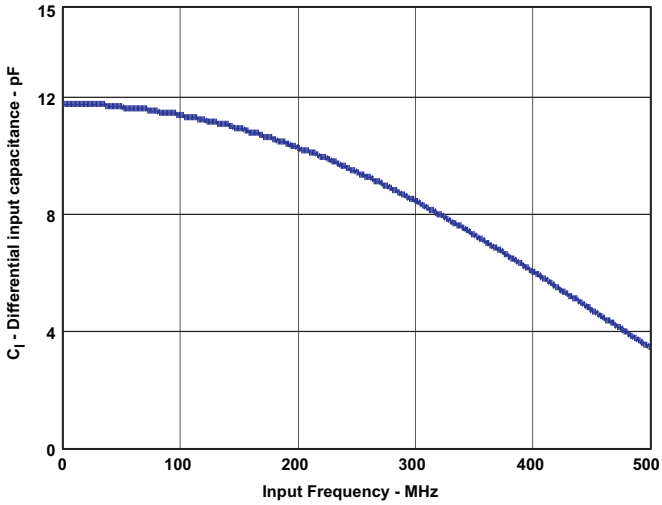


Figure 92. ADC Analog Input Capacitance (C_{IN}) Across Frequency

9.1.2 Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 700 MHz. When using an amplifier to drive the ADS5263, the total noise of the amplifier up to the small signal bandwidth must be considered.

The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5263 supports 4 V_{PP} amplitude for input signal frequency up to 70 MHz. For higher frequencies (>70 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 140 MHz, the device supports a maximum of 2 V_{PP} signal and at 280 MHz, it can handle a maximum of 1 V_{PP}.

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Application Information (continued)

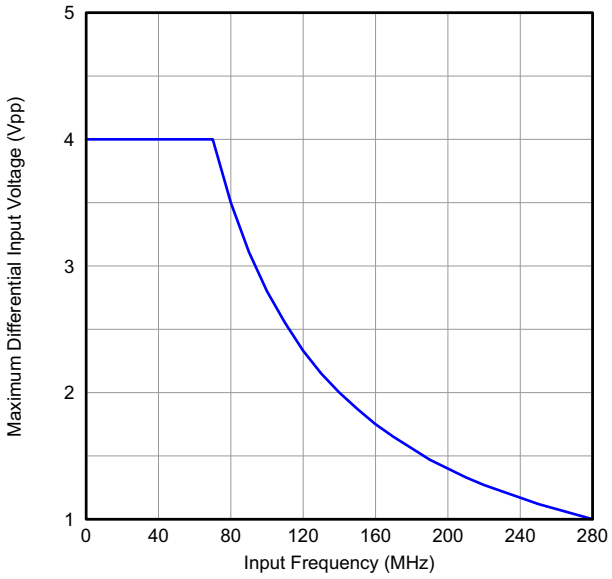


Figure 93. FullScale Input Amplitude Across Input Frequency

9.1.3 Clamp Function For CCD Signals

The 14-bit ADC analog inputs have an integrated clamp function that can be used to interface to a CCD sensor output.

9.1.3.1 Differential Input Drive

The clamp function can be used with a differential input signal only. As most CCD signals are single-ended, use either a fully differential amplifier or transformer to translate the single-ended CCD signal to a differential signal for applying to the ADS5263 analog inputs through ac-coupling capacitors, as Figure 94 shows.

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Application Information (continued)

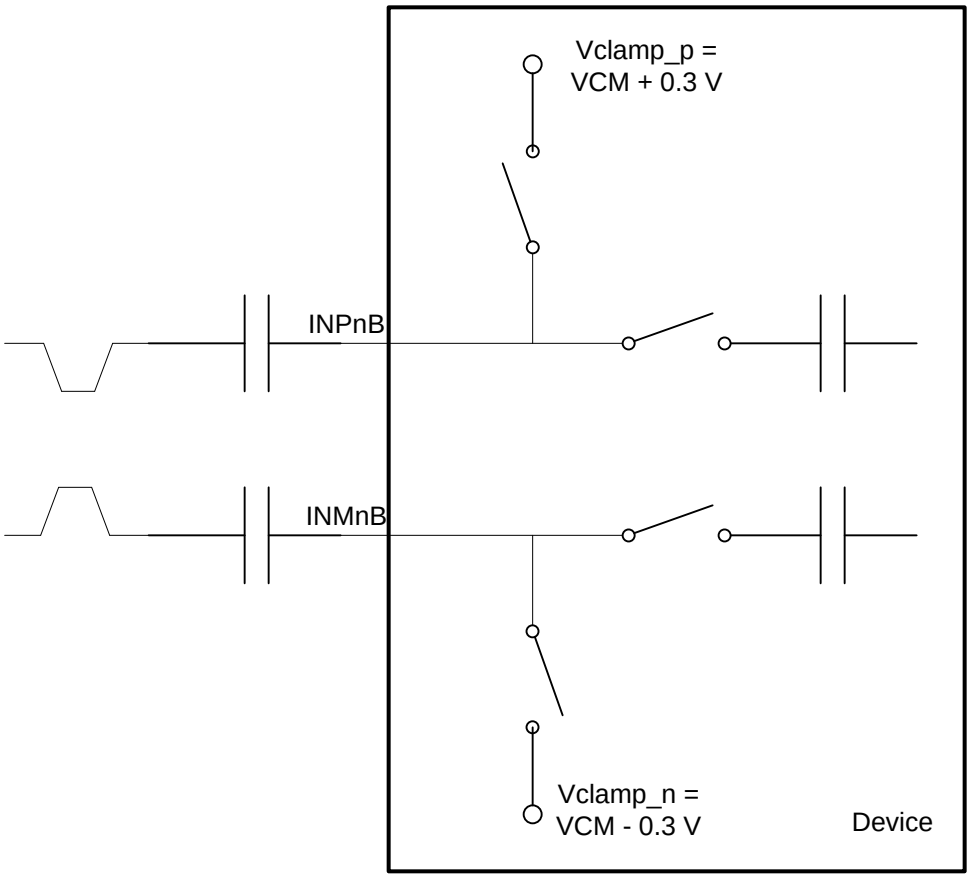


Figure 94. Differential Input Drive with Internal Clamp Mode

The analog inputs of the ADS5263 are internally clamped to voltages Vclamp_p (1.8 V, typical) and Vclamp_n (1.2 V, typical). With a differential input, the voltage on INP can swing from Vclamp_p down to 1 V, whereas INM swings from Vclamp_n up to 2 V. This ensures maintaining of the input common-mode at 1.5 V while supporting a differential input swing of 1.6 Vpp.

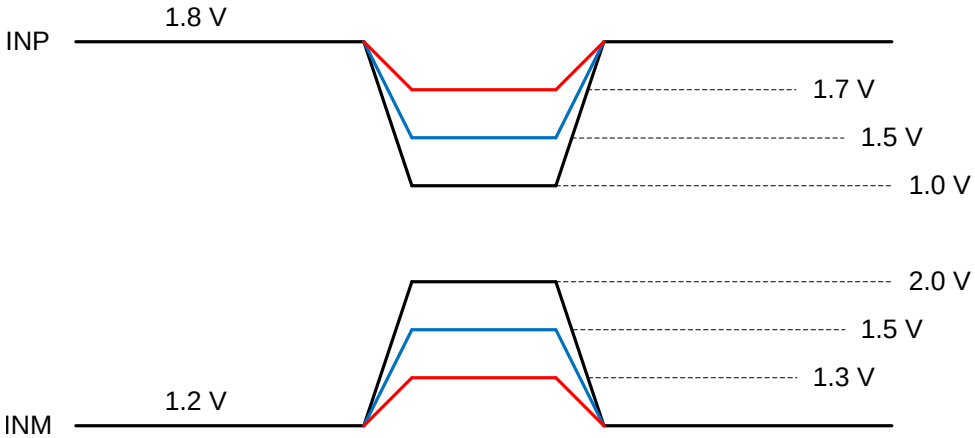


Figure 95. Analog Input Voltage Range With Clamp Enabled

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Application Information (continued)

9.1.3.2 Clamp Operation

The clamp function can be enabled by setting the register bit <EN_CLAMP> in register 0x09.

The effect of the clamp operation can be verified by measuring the voltage on the INP and INM pins. With no input signal applied, the voltages on INP and INM will be 1.8 V dc and 1.2 V dc, respectively.

9.1.3.3 Synchronization to External CCD Timing

A typical CCD sensor output has three timing phases – a reset phase followed by a reference phase and the actual picture phase.

An internally generated CLAMP clock signal controls the clamping action. The CLAMP clock can be timed to happen during the reset phase of the CCD signal by applying a synchronized high-going pulse on SYNC pin. Once synchronized, the internal CLAMP signal remains high for one ADC clock cycle and low for two clock cycles and repeats in this fashion. Figure 96 shows an oscilloscope snapshot of the external input signals applied to the ADS5263 and the alignment of the CCD signal to the SYNC input. shows the relation between the external signals, the internally generated CLAMP signal, and the data actually sampled by the ADC.

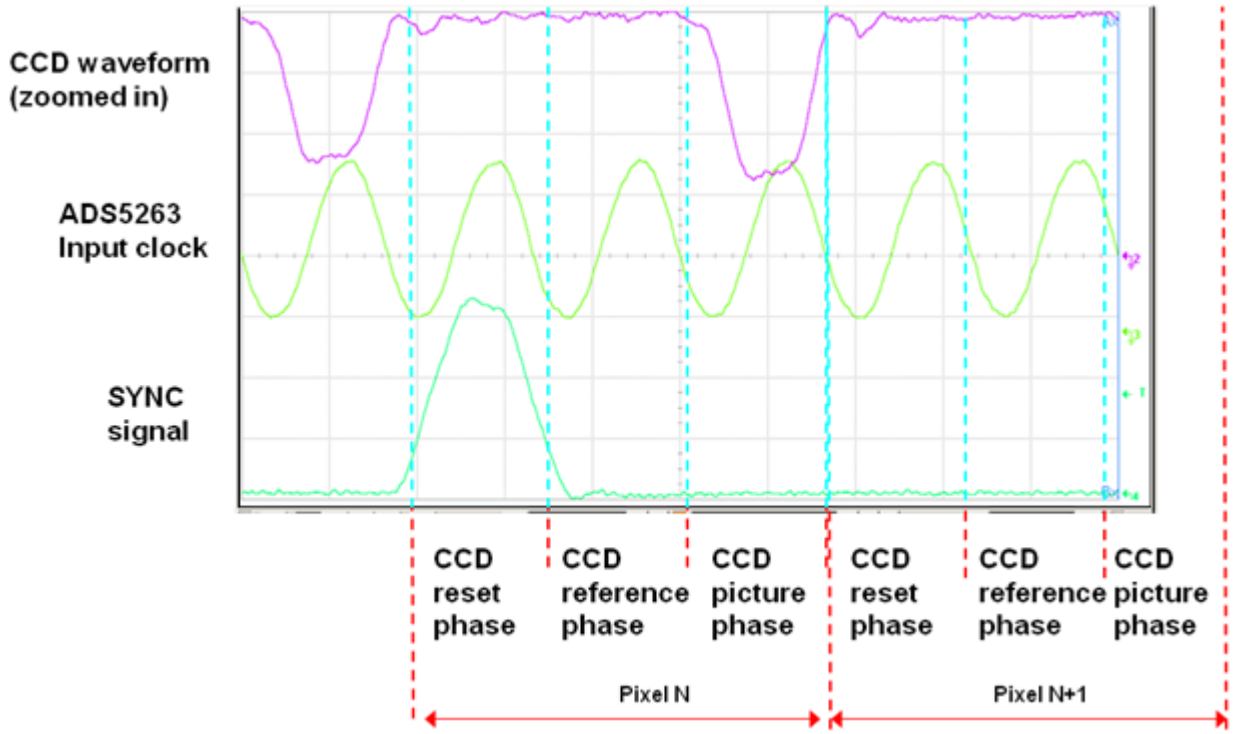
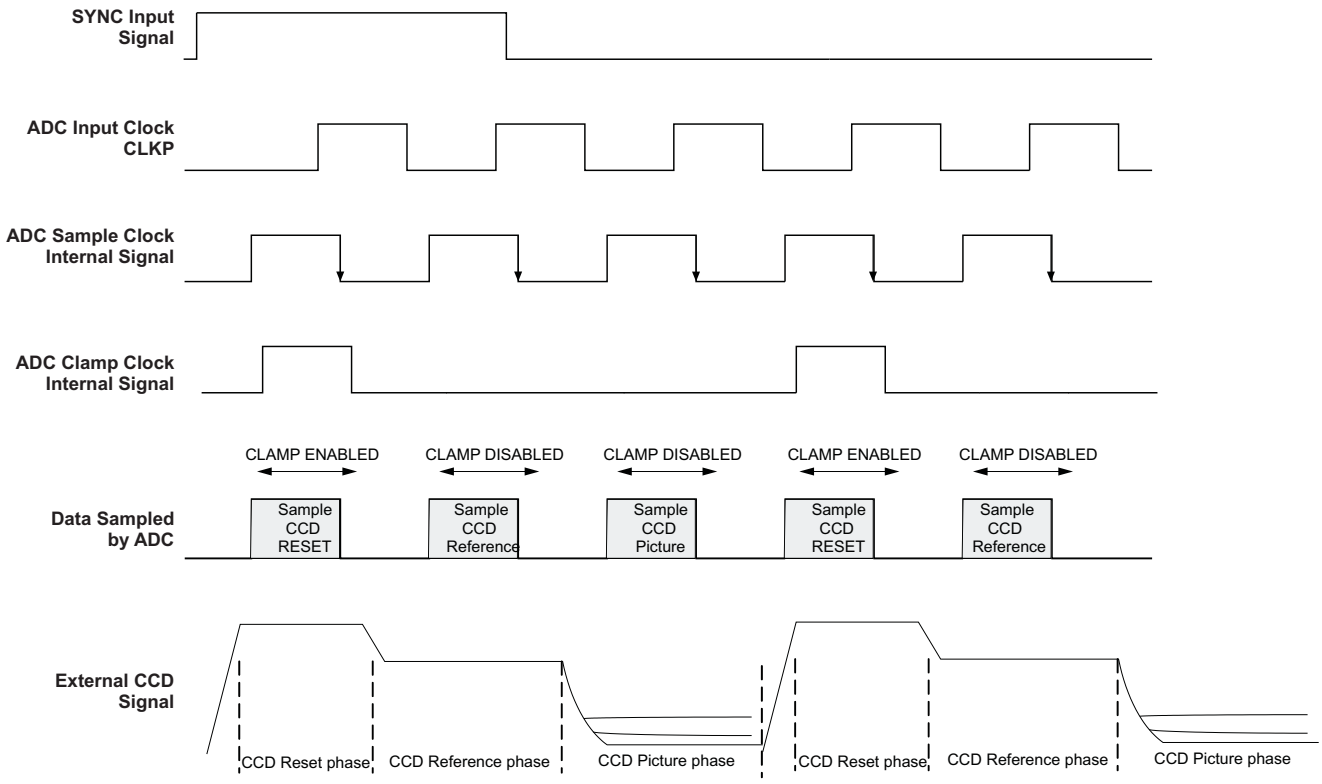


Figure 96. Synchronizing CCD Signal with ADS5263's Clamp Operation Using SYNC signal

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Application Information (continued)



Clamp Timing Diagram

9.1.4 Low-Frequency Noise Suppression

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the low frequency band of dc to 1 MHz. By setting this mode, the low-frequency noise spectrum band around dc is shifted to a similar band around (f_S/2 or Nyquist frequency). As a result, the noise spectrum from dc to about 1 MHz improves significantly as shown by the following spectrum plots.

This function can be selectively enabled in each channel using the register bits **<EN LFNS CH x>**. The following plots show the effect of this mode on the spectrum.

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Application Information (continued)

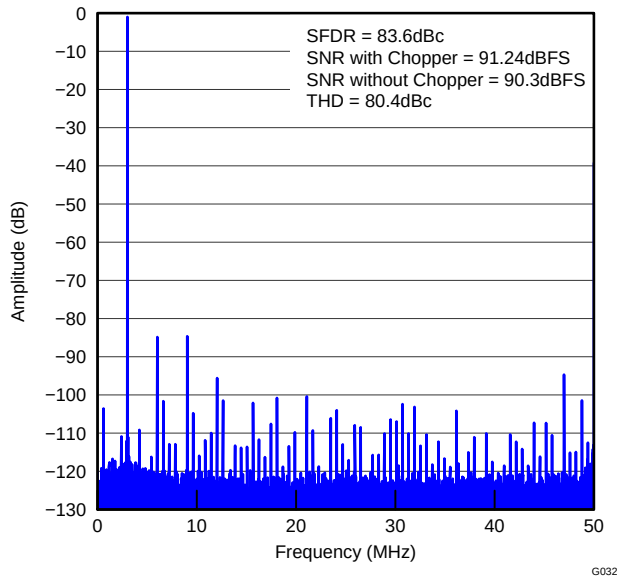


Figure 97. Full-Scale Input Amplitude

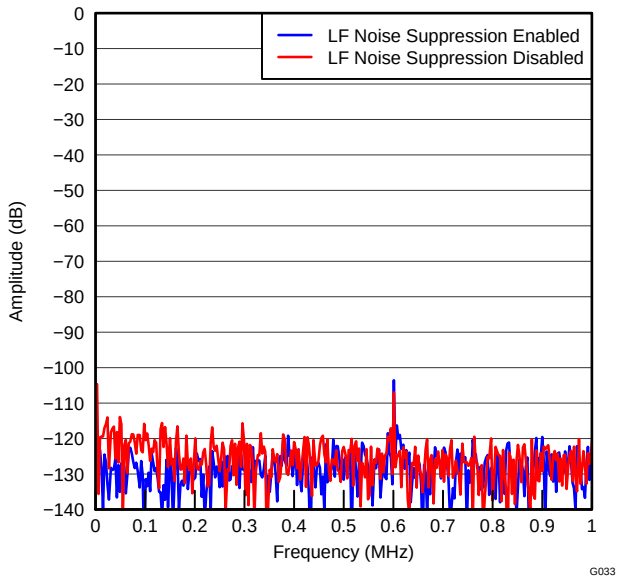


Figure 98. Spectrum (Zoomed) from DC to 1 MHz

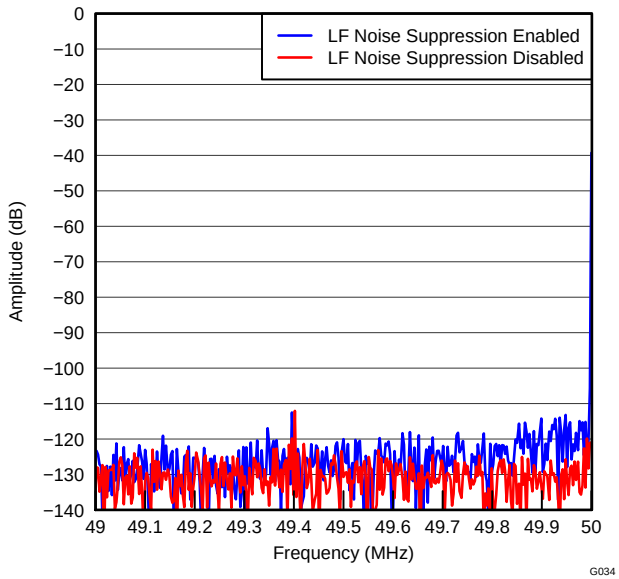


Figure 99. Spectrum (Zoomed) in 1-MHz Band from 49 MHz to 50 MHz (f_S=100 MSPS)

9.1.5 External Reference Mode

The ADS5263 supports an external reference mode of operation by applying an input voltage on VCM pin.

As shown in the figure, in this mode, the reference amplifier is still active. Instead of being driven by the internal band-gap voltage, the reference amplifier is driven by the voltage applied on the VCM pin. By driving the VCM pin with a low drift reference, it is possible to improve the reference temperature drift compared to the internal reference mode. The relation between the full-scale voltage of the ADC and the applied voltage on VCM is

Full-scale input voltage = (8/3) x V_{REFIN}

To enable this mode, set the register bits as shown in Table 11. This changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be 1.5 V ± 50 mV. The current drawn by VCM pin in this mode is around 0.5 mA.

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Application Information (continued)

Table 11. Register Settings for External Reference Mode

REGISTER ADDRESS	FIELD NAME	VALUE
0x01	EN_HIGH_ADDRS	1
0xF0	EN_EXT_REF	1
0x42	EN_REG_42	1
0x42	EXT_REF_VCM	1

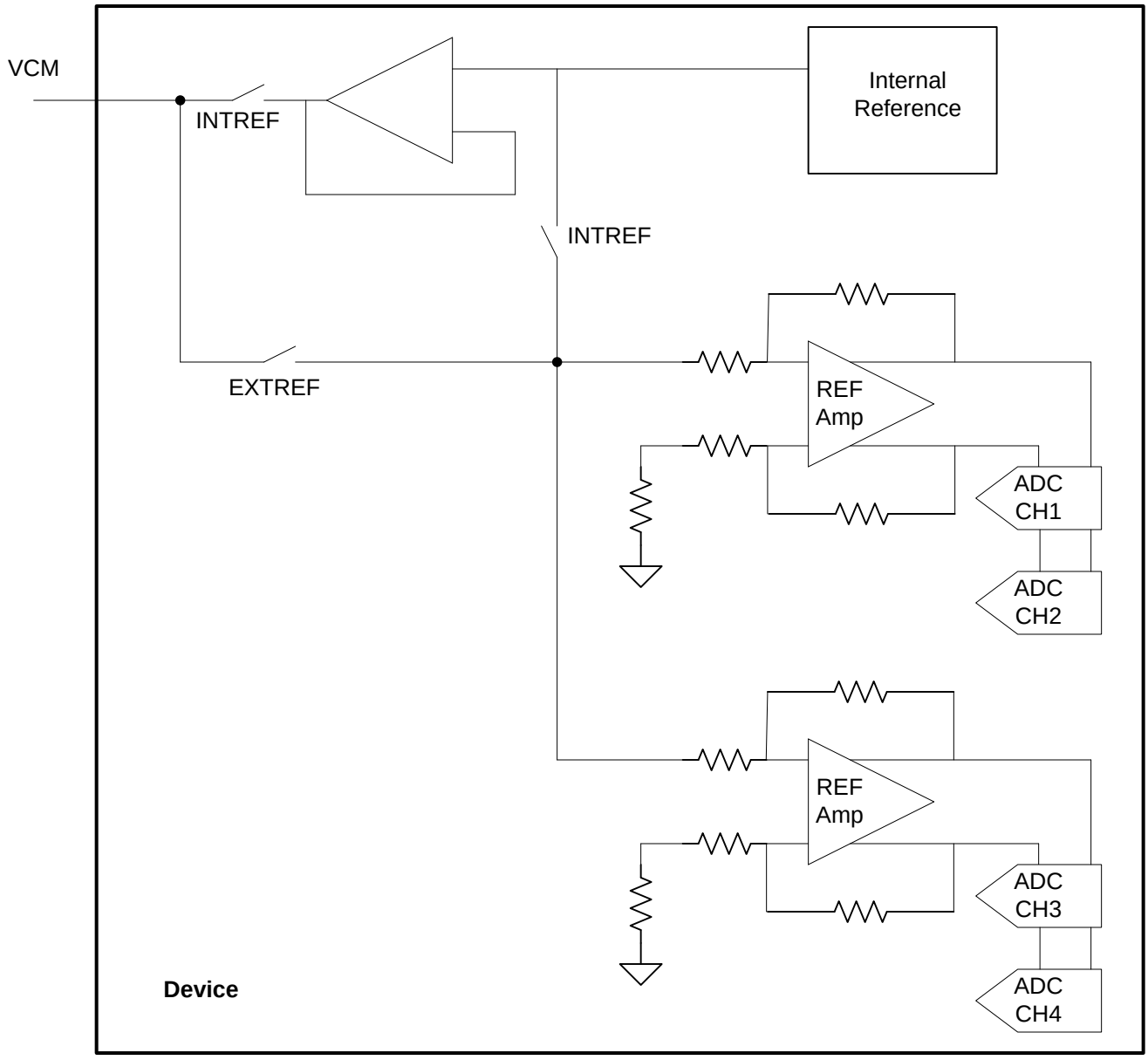


Figure 100. Reference Block Diagram

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9.2 Typical Applications

9.2.1 Driving Circuit Design: Low Input Frequencies (< 50 MHz)

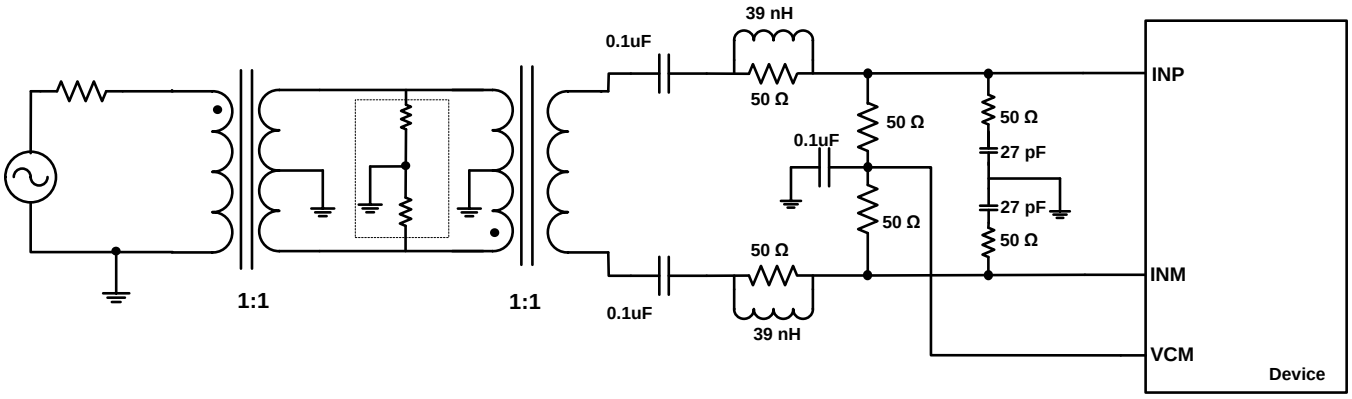


Figure 101. Driving Circuit for Low Input Frequencies

9.2.1.1 Design Requirements

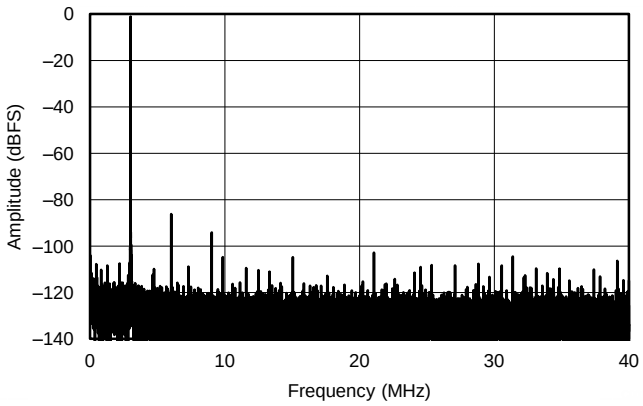
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitics. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

9.2.1.2 Detailed Design Procedure

A typical application using two back-to-back coupled transformers is illustrated in Figure 101. The circuit is optimized for low input frequencies. An external R-C-C-R filter using 50-Ω resistors and a 27-pF capacitor is used. With the series inductor (39 nH), this combination helps absorb the sampling glitches.

9.2.1.3 Application Curve

Typical performance at full-scale 10 MHz input frequency is shown in Figure 102.



f_S = 80 MSPS, SNR = 85 dBFS, f_{IN} = 3 MHz , SFDR = 83 dBc

Figure 102. Performance FFT at 10 MHz (Low Input Frequency)

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Typical Applications (continued)

9.2.2 Driving Circuit Design: Input Frequencies > 50 MHz

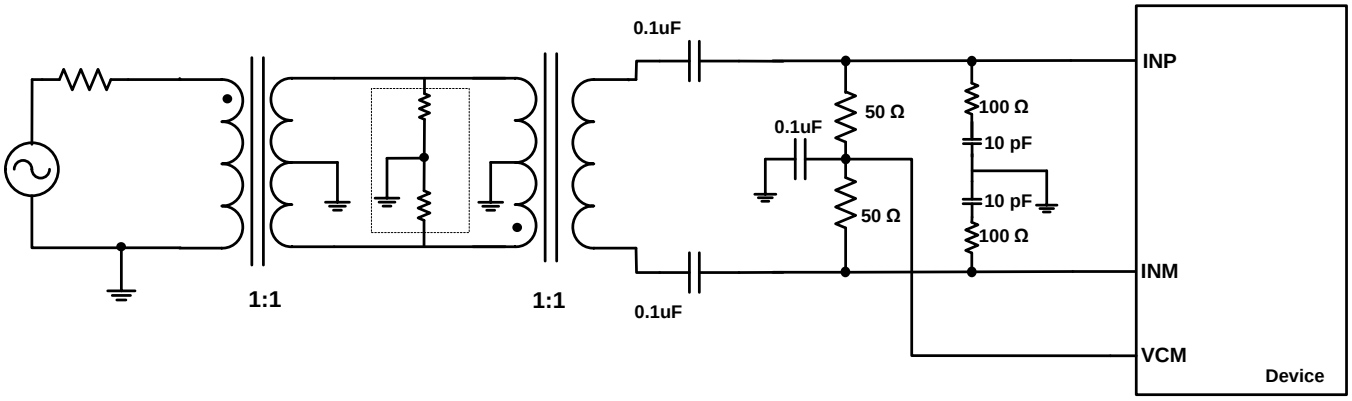


Figure 103. Driving Circuit for High Input Frequencies (f_{IN} > 50 MHz)

9.2.2.1 Design Requirements

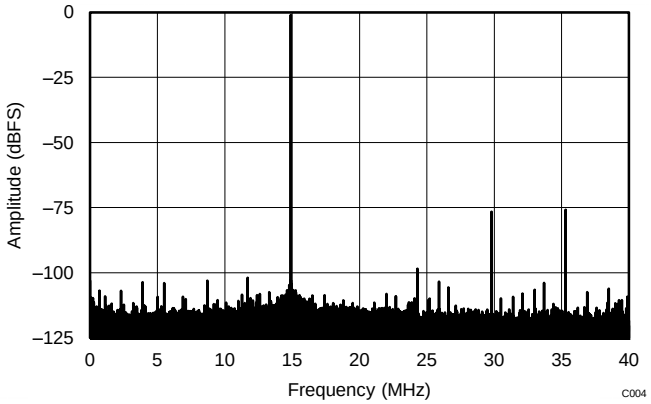
To achieve optimum performance at high input frequencies, an example driving circuit is shown in Figure 103.

9.2.2.2 Detailed Design Procedure

When input frequencies are greater than 50 MHz, series inductance from low frequency driving circuit should be removed so as not limit the signal bandwidth. The corner frequency of R-C-C-R low pass filter should also be changed to suit the input frequency.

9.2.2.3 Application Curve

Figure 104 shows the performance obtained by using the circuit shown in Figure 104.



f_S = 80 MSPS, SNR = 78.2 dBFS, f_{IN} = 65 MHz, SFDR = 75 dBc

Figure 104. Performance FFT at 65 MHz

10 Power Supply Recommendations

The device requires 3.3-V for Analog Supply (AVDD) and 1.8-V for Digital Supply (LVDD). There is no specific sequence required to bring-up the power-supplies. AVDD and LVDD can power up in any order.

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11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.

1. Use wide and short traces for the main current path and for the power ground tracks without using vias if possible. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2. At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1-µF de-coupling capacitor close to the device. A separate de-coupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.
3. Use of a ground plane is recommended.
4. Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.

Since ADS5263 provides charging current and system power with internal linear regulators, users need to consider thermal condition.

1. PowerPAD should be soldered to a thermal land on the PCB.
2. Vias on the thermal land of the PCB are necessary. This is a thermal path through the other side of the PCB.
3. A thermal pad of the same size is required on the other side of the PCB. All thermal pads should be connected by vias.
4. A metal layer should cover all of the PCB if possible.
5. Place vias to connect other sides to create thermal paths.

With these steps, the thermal resistance of ADS5263 can be lowered.

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11.2 Layout Example

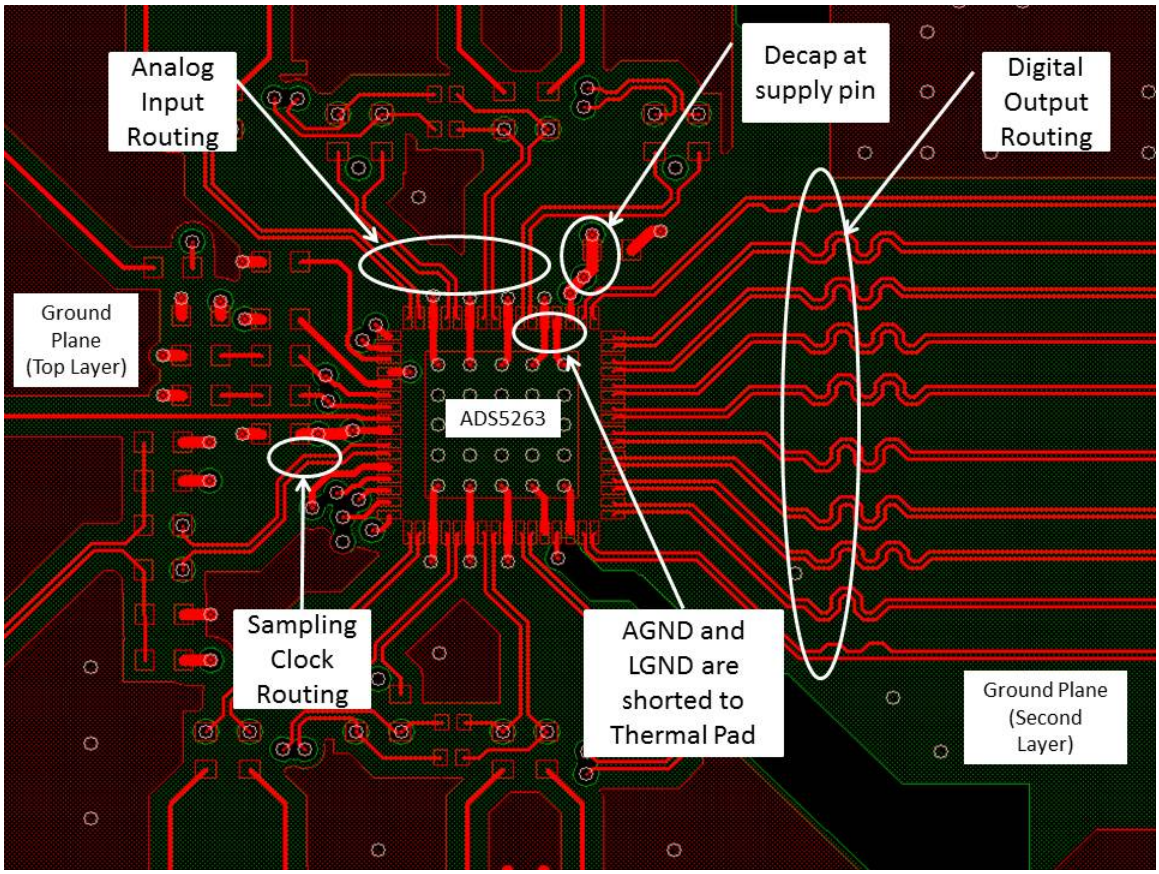


Figure 105. Layout of Board

12 器件和文档支持

12.1 器件支持

12.1.1 技术规范定义

模拟带宽 – 基频功率相对低频值下降 3dB 时的模拟输入频率。

孔径延迟 – 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。该延迟在各通道中会有所不同。最大差值被定义为孔径延迟差异（通道间）。

孔径不确定性（抖动） – 采样间的孔径延迟差异。

时钟脉冲宽度/占空比 – 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。占空比通常以百分比的形式表示。理想差分正弦波时钟的占空比为 50%。

最大转换速率 – 执行指定操作时所采用的最大采样率。除非另外注明，否则所有参数测试均以该采样率执行。

最小转换速率 – ADC 正常工作时的最小采样率。

微分非线性 (DNL) – 理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

积分非线性 (INL) – INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

增益误差 – 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。增益误差以理想输入满量程范围的百分比形式表示。增益误差包括两部分：基准不精确所导致的误差和通道所导致的误差。这两种误差分别定义为 E_{GREF} 和 E_{GCHAN}。

对于一阶近似，总增益误差 $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$。

例如，如果 $E_{TOTAL} = \pm 0.5\%$，则满量程输入范围为 $(1 – 0.5 / 100) \times FS_{ideal}$ 至 $(1 + 0.5 / 100) \times FS_{ideal}$。

偏移误差 – 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。该数量通常转换为毫伏。

温度漂移 – 温度漂移系数（相对于增益误差和偏移误差）指定参数从 T_{MIN} 到 T_{MAX} 每摄氏度的变化量。温度漂移的计算方法是用参数在 T_{MIN} 至 T_{MAX} 范围内的最大变化量除以 $T_{MAX} – T_{MIN}$ 的值。

信噪比 – SNR 是指基频功率 (P_S) 与噪底功率 (P_N) 的比值，不包括直流功率和前 9 个谐波的功率。

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

信噪比和失真 (SINAD) – SINAD 是指基频功率 (P_S) 与所有其他频谱成分（包括噪声 (P_N) 和失真 (P_D)，但不包括直流）功率的比值。

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

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器件支持 **(**接下页**)**

有效位数 **(ENOB) –** ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

总谐波失真 **(THD) –** THD 是指基频功率 (P_S) 与前 9 个谐波功率 (P_D) 的比值。

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (4)$$

THD 通常以 dBc 为单位（相对于载波的分贝数）。

无杂散动态范围 **(SFDR) –** 基频功率与最高的其他频谱成分（毛刺或谐波）功率的比值。SFDR 通常以 dBc 为单位（相对于载波的分贝数）。

双频互调失真 **–** IMD3 是指基频功率（f_1 和 f_2 频率处）与最差频谱成分（$2f_1 – f_2$ 或 $2f_2 – f_1$ 频率处）功率的比值。当基频的绝对功率用作基准时，IMD3 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，IMD3 以 dBFS（相对于满量程的分贝数）为单位。

直流电源抑制比 **(DC PSRR) –** DC PSSR 是偏移误差变化量与模拟电源电压变化量的比值。DC PSRR 通常以 mV/V 为单位进行表示。

交流电源抑制比 **(AC PSRR) –** AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。如果 ΔV_{SUP} 表示电源电压的变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (5)$$

电压过载恢复 **–** 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。然后记录下过载后前几个采样（相对于期望值）的偏差。

共模抑制比 **(CMRR) –** CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。如果 ΔV_{CM_IN} 表示输入引脚的共模电压变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (6)$$

串扰（仅限多通道 **ADC**）**–** 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。串扰分两种情况：一种是与紧邻通道（近端通道）之间的耦合，另一种是与跨封装通道（远端通道）之间的耦合。通常采用对邻近通道施加满量程信号的方式来测量串扰。串扰是指耦合信号功率（在目标通道的输出端测得）与邻近通道输入端所施加信号功率的比值。串扰通常以 dBc 为单位进行表示。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

13.1 封装

13.1.1 外露焊盘

封装底部的外露焊盘是主要散热路径。因此，必须将焊盘焊接到 PCB 的接地层，以便获得最佳散热性能。将焊盘连接到接地层时，请务必控制好所用过孔的数量。

详细信息，请参见应用手册《*QFN 布局布线准则*》（文献编号：SLOA122）和《QFN/SON PCB 连接》（文献编号：SLUA271），这两本应用手册均可从 TI 网站 (www.ti.com.cn) 下载。您也可以访问 TI 网站查看有关散热方面的网页：www.ti.com/thermal。

13.1.2 非磁性封装

磁共振成像 (MRI) 应用 中有一项重要要求，即 RF 线圈区域附近所安装组件的磁兼容性。组件封装中的任何铁磁性材料都会在 MRI 图像中引入伪影。因此，首选采用非磁性封装的组件。

ADS5263 采用一种特殊的非磁性封装，即使在高磁场环境下也不会产生任何伪影。欲订购非磁性部件，请认准“-NM”后缀。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5263IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263
ADS5263IRGCR-NM	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263NM
ADS5263IRGCR-NM.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263NM
ADS5263IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263
ADS5263IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263
ADS5263IRGCT-NM	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263NM
ADS5263IRGCT-NM.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263NM
ADS5263IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	ADS5263

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

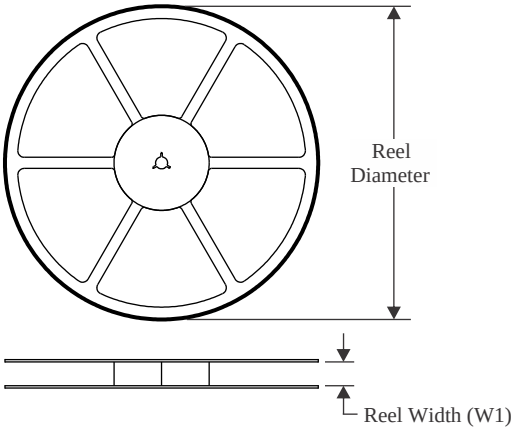
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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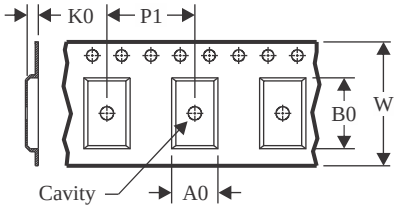
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

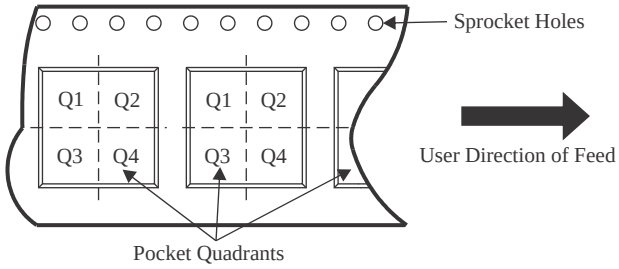


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

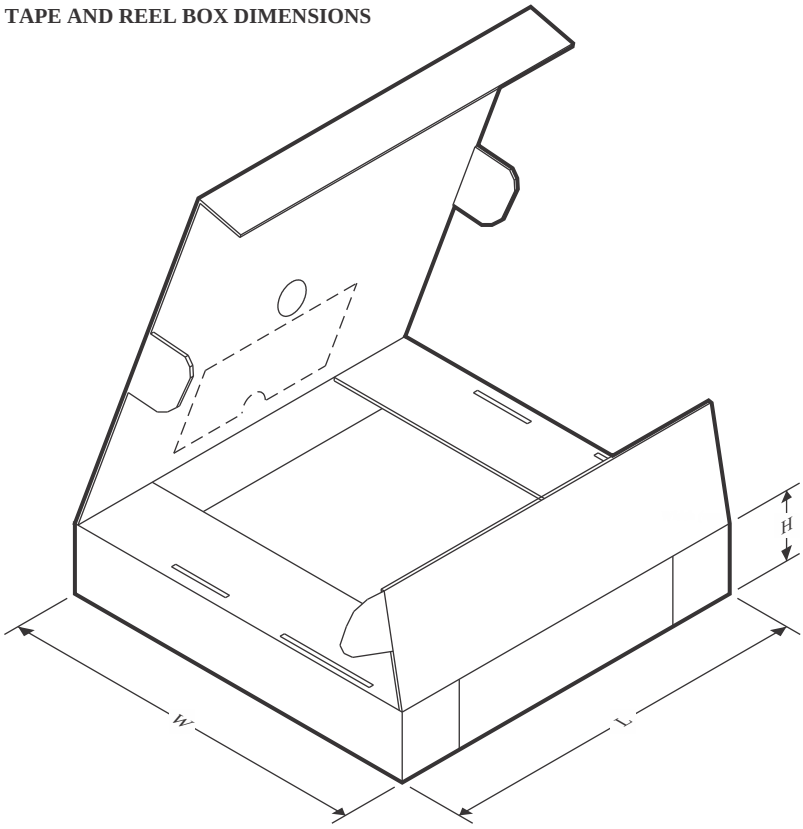
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5263IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS5263IRGCR-NM	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5263IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS5263IRGCR-NM	VQFN	RGC	64	2000	350.0	350.0	43.0

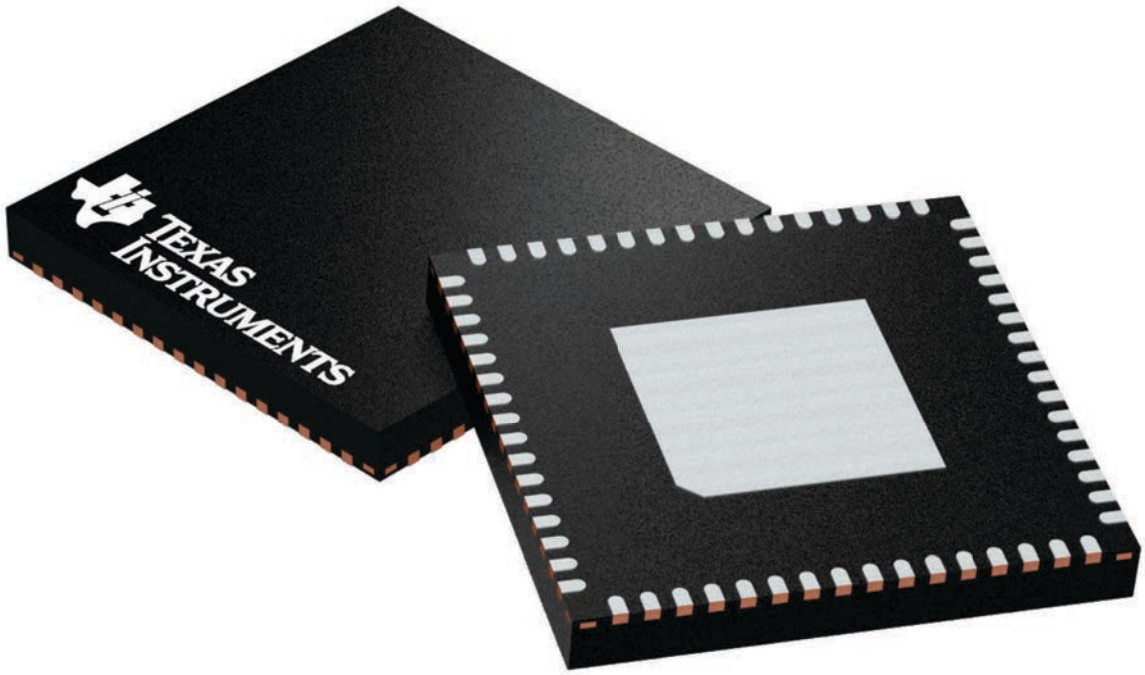
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

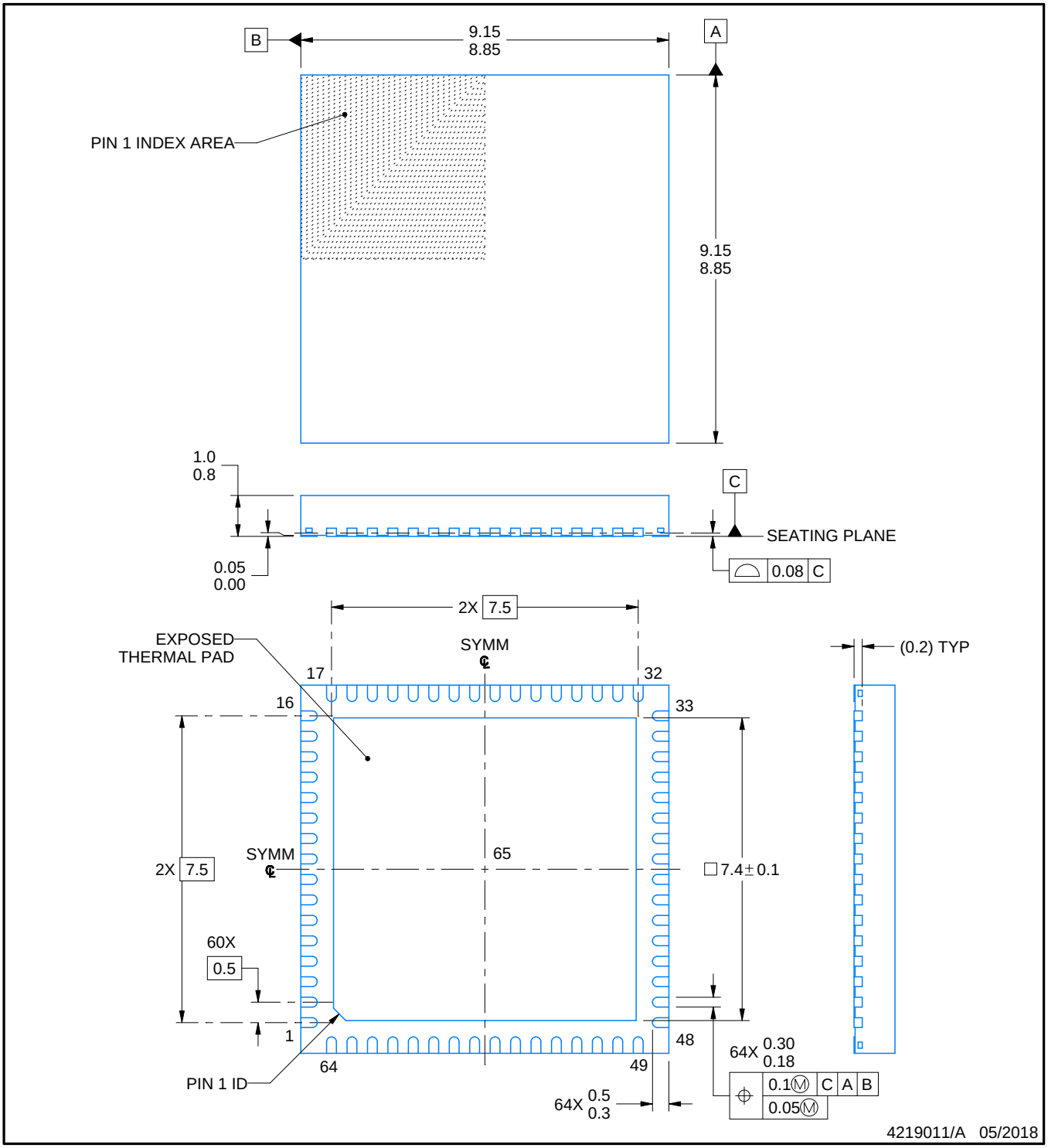
4224597/A

RGC0064H

PACKAGE OUTLINE

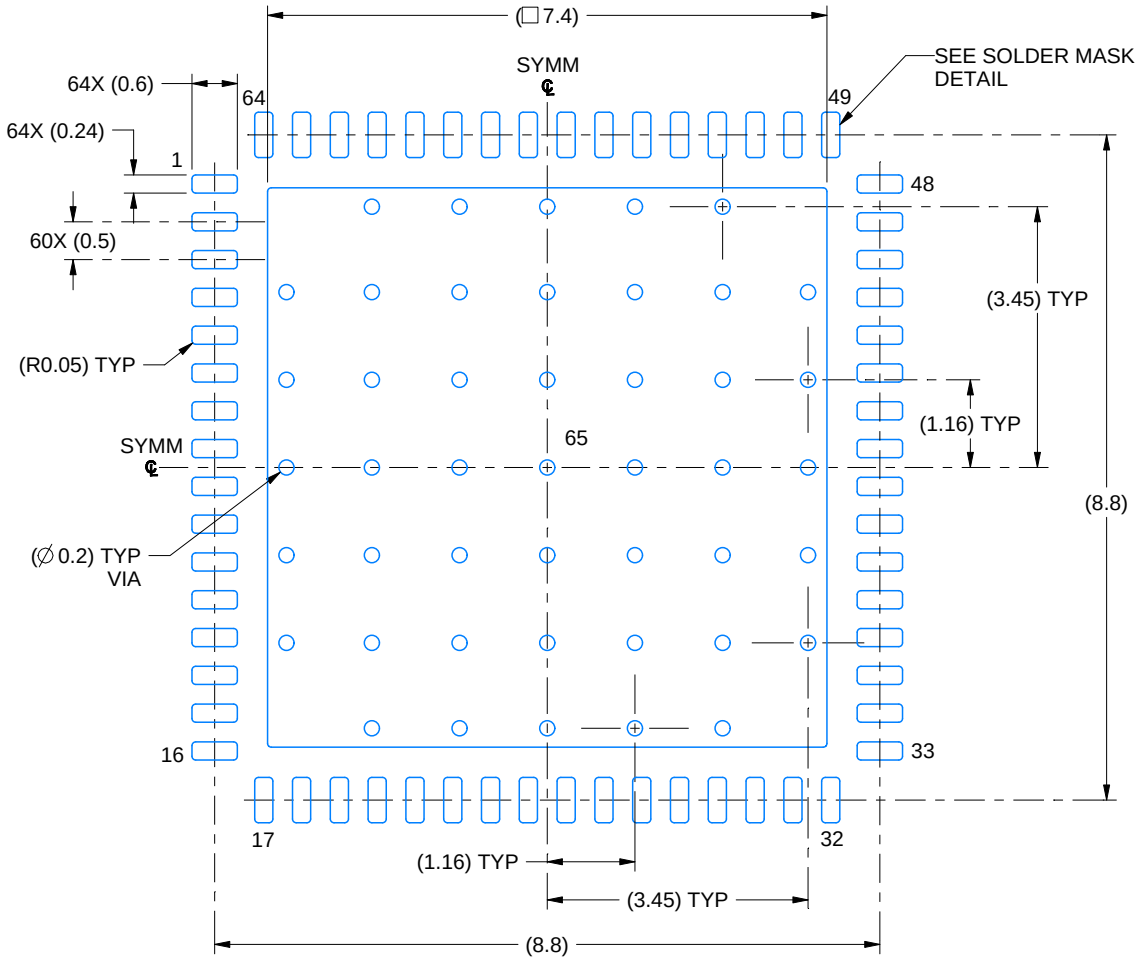
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

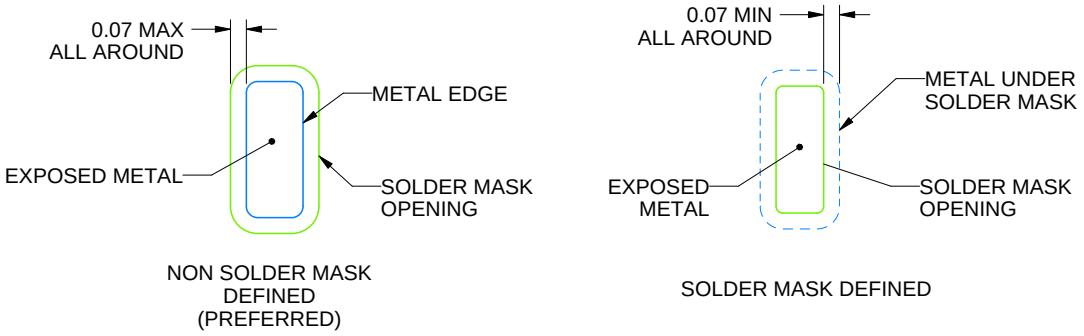


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

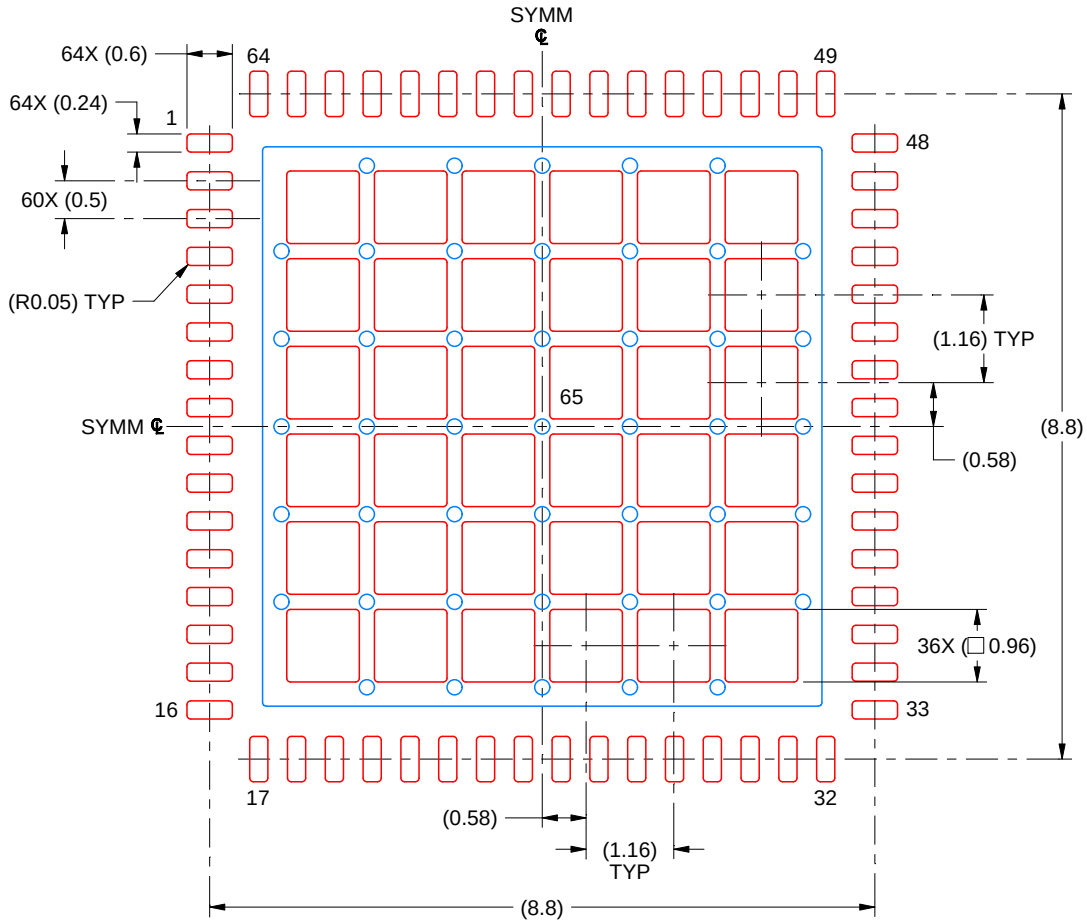


SOLDER MASK DETAILS

4219011/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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