ADS1282-SP 抗辐射加固保障高分辨率 ΔΣ ADC

1 特性

- QMLV（QML V 类）MIL-PRF-38535 认证和抗辐射加固保障 (RHA)，SMD 5962-14231
  - 5962L1423101VXC - 符合军用级温度范围要求（–55°C 至 125°C）
  - 5962L1423102VXC - 符合缩减温度范围要求（–55°C 至 115°C），提高动态性能
- 5962L14231：
  - 抗辐射加固保障 (RHA) 高达 50kRAD (Si) 总电离剂量 (TID)
  - 在 125°C 的环境温度下，单粒子锁定 (SEL) 对于 LET 的抗扰度为 50MeV-cm^2/mg
  - 在 85°C 的环境温度下，单粒子锁定 (SEL) 对于 LET 的抗扰度为 60MeV-cm^2/mg
- 高分辨率：124dB 信噪比 (SNR) (1000SPS)
- 高精度：总谐波失真 (THD)：–102dB
  积分非线性 (INL)：0.5ppm
- 低噪声可编程增益放大器 (PGA)
- 双通道输入多路复用器 (MUX)
- 固有稳定性的调制器，支持快速响应超范围检测
- 灵活的数字滤波器：
  - 正弦 + 有限脉冲响应 (FIR) + 无限脉冲响应 (IIR)（可选）
  - 线性或最小相位响应
  - 可编程的高通滤波器
  - 可选择 FIR 数据速率：250SPS 至 4kSPS
- 滤波器旁路选项
- 低功耗：25mW
- 偏移和增益校准引擎
- SYNC 输入
- 模拟电源：单极 (5V) 或双极 (±2.5V)
- 数字电源：1.75V 至 3.3V

2 应用

- 太空卫星温度和温度检测
- 太空卫星精密和科学 应用
- 高精度仪器
- 可提供工程评估 (/EM) 样片(1)

(1) 这些部件仅适用于工程评估。以非合规性流程对其进行了处理（即未进行老化处理等操作）并且仅在 25°C 额定温度下进行了测试。这些部件不适用于质检、生产、辐射测试或飞行。这些零部件无法在 –55°C 至 125°C 的完整 MIL 额定温度范围或运行寿命内保证其性能。

3 说明

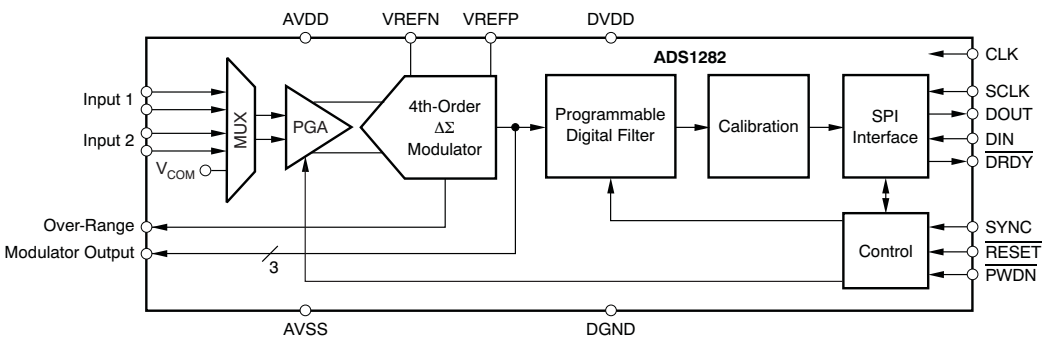
ADS1282-SP 是一款超高性能的抗辐射单芯片模数转换器 (ADC)，具有集成式低噪声可编程增益放大器 (PGA) 和双通道输入多路复用器 (MUX)。ADS1282-SP 具备超精密性能，适合要求较高的太空 应用；同时能够保持较高的抗辐射性能，适用于各类卫星、有效载荷及其他环境恶劣的 应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1282-SP	CFP (HKV) (28)	18.23mm x 12.70mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

Changes from Revision A (December 2016) to Revision B **Page**

- 将文档标题从：“ADS1282-SP 耐辐射...” 更改为“ADS1282-SP 抗辐射加固保障...” ... 1
- 在*特性* 中将“单粒子锁定 (SEL) 对于 LET 的抗扰度为 40...” 更改为“单粒子锁定 (SEL) 对于 LET 的抗扰度为 50...” ... 1
- 在*特性* 中添加“单粒子锁定 (SEL) 对于 LET 的抗扰度为 60...” ... 1
- 已添加 工程评估样片列表项和脚注至*应用* 列表 ... 1
- Changed the HKV Package appearance ... 4

Changes from Original (March 2016) to Revision A **Page**

- 已添加 5962L1423102VXC 缩减温度范围列表项至*特性* 部分 ... 1
- Added *ESD Ratings* table to *Specifications* section ... 5
- Added T_J values for 5962L1423102VXC to *Recommended Operating Conditions* table ... 5
- Added MIN, TYP and MAX values for 5962L1423102VXC to *Electrical Characteristics* table ... 6
- 已添加 *接收文档更新通知* 至*器件和文档支持* 部分 ... 57

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5 （说明 （续））

此转换器使用一个固有稳定性的四阶 Δ-Σ 调制器来获得出色的抗噪性能和线性度。该调制器可与片上数字滤波器搭配使用，也可通过旁路与后处理滤波器结合使用。

输入 MUX 可灵活提供附加的外部输入用于测量以及内部自检连接。PGA 具有 出色的低噪声性能 (5nV/$\sqrt{Hz}$) 和高输入阻抗，能够与较宽增益范围内的传感器轻松连接。

数字滤波器提供 250SPS 至 4000SPS 的可选数据速率。高通滤波器 (HPF) 具有 可调节的角频率。片上增益和偏移调节寄存器支持系统校准。

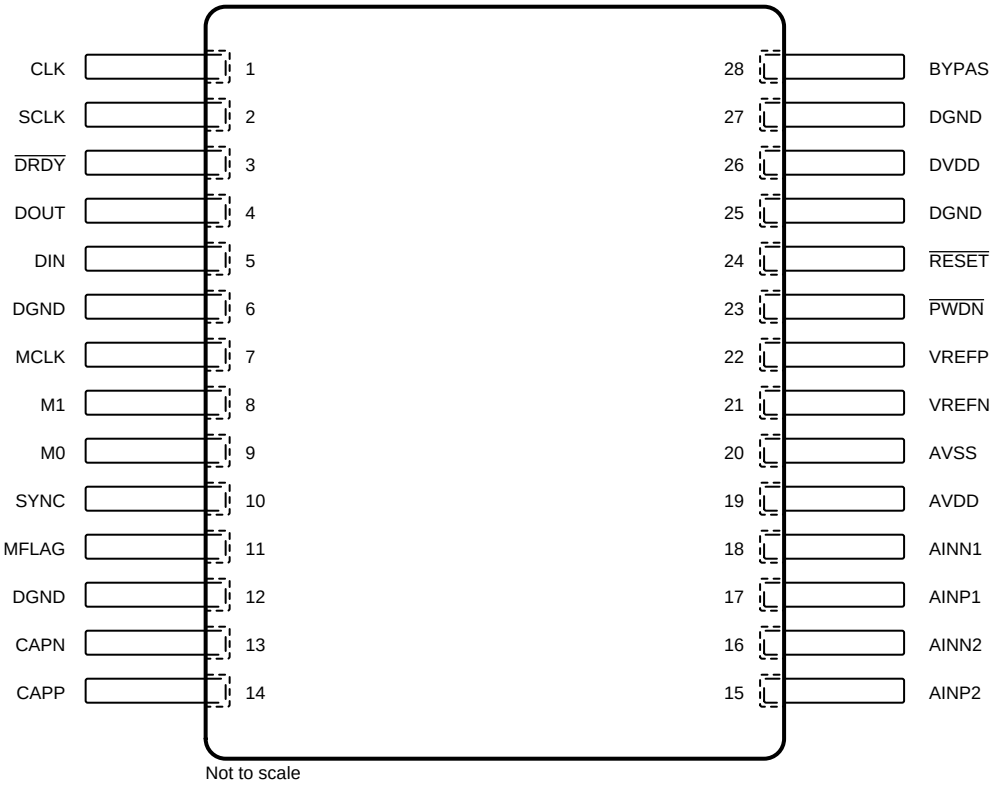
同步输入 (SYNC) 可用于对多个 ADS1282 的转换操作进行同步。SYNC 输入还接受外部时钟源输入，用于对转换操作进行持续校准。

放大器、调制器和滤波器三者的总功耗为 30mW。ADS1282-SP 在 –55°C 至 125°C 温度范围内完全额定运行。

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6 Pin Configuration and Functions

HKV Package
28-Pin CFP (HKV)
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CLK	Digital input	Master clock input
2	SCLK	Digital input	Serial clock input
3	$\overline{\text{DRDY}}$	Digital output	Data ready output: read data on falling edge
4	DOUT	Digital output	Serial data output
5	DIN	Digital input	Serial data input
6, 12, 27, 25	DGND	Digital ground	Digital ground, pin 12 is the key ground point
7	MCLK	Digital I/O	"Modulator clock output; if in modulator mode: MCLK: Modulator clock output Otherwise, the pin is an unused input (must be tied)."
8	M1	Digital I/O	"Modulator data output 1; if in modulator mode: M1: Modulator data output 1 Otherwise, the pin is an unused input (must be tied)."
9	M0	Digital I/O	"Modulator data output 0; if in modulator mode: M0: Modulator data output 0 Otherwise, the pin is an unused input (must be tied)."
10	SYNC	Digital input	Synchronize input
11	MFLAG	Digital output	Modulator Over-Range flag: 0 = Normal 1 = Modulator over-range
13	CAPN	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN
14	CAPP	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
15	AINP2	Analog input	Positive analog input 2
16	AINN2	Analog input	Negative analog input 2
17	AINP1	Analog input	Positive analog input 1
18	AINN1	Analog input	Negative analog input 1
19	AVDD	Analog supply	Positive analog power supply
20	AVSS	Analog supply	Negative analog power supply
21	VREFN	Analog input	Negative reference input
22	VREFP	Analog input	Positive reference input
23	$\overline{\text{PWDN}}$	Digital input	Power-down input, active low
24	$\overline{\text{RESET}}$	Digital input	Reset input, active low
26	DVDD	Digital supply	Digital power supply: 1.8 V to 3.3 V
28	BYPAS	Analog	Sub-regulator output: Connect 1-μF capacitor to DGND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	5.5	V
AVSS to DGND	–2.8	0.3	V
DVDD to DGND	–0.3	3.9	V
Input current		100, momentary	mA
Input current		10, continuous	mA
Analog input voltage (AINP1, AINN1, AINP2, AINN2, VREFN, VREFP, CAPP, CAPN)	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage to DGND (CLK, SCLK, $\overline{\text{DRDY}}$, DOUT, DIN, MCLK, M1, M0, MFLAG, SYNC, $\overline{\text{PWDN}}$, $\overline{\text{RESET}}$)	–0.3	DVDD + 0.3	V
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J Operating temperature	5962L1423101VXC	–55		125	°C
	5962L1423102VXC	–55		115	

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7.4 Thermal Information

THERMAL METRIC(1)		ADS1282-SP HKV [CFP (TBAR)] 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, over operating temperature range, unless otherwise noted. Typical values are T_J = 25°C. A total ionizing dose of 50 kRad (Si) exposure at a low dose rate of < 10 mRads (Si)/s, post tested at 25°C.

PARAMETER		TEST CONDITIONS	5962L1423101VXC			5962L1423102VXC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS									
	Full-scale input voltage	V_{IN} = (AINP – AINN)		(VREFP – VREFN) / (PGA)			(VREFP – VREFN) / (PGA)		Vpp-diff
AINP or AINN	Absolute input range		AVSS + 0.7		AVDD – 1.25	AVSS + 0.7		AVDD – 1.25	V
	PGA input voltage noise density			5			5		nV/√Hz
	Differential input impedance(2)			1			1		GΩ
	Common-mode input impedance			100			100		MΩ
	Input bias current			1			1		nA
	Crosstalk	f = 31.25 Hz		–128			–128		dB
	MUX on-resistance			30			30		Ω
PGA OUTPUT (CAPP, CAPN)									
	Absolute output range		AVSS + 0.4		AVDD – 0.4	AVSS + 0.4		AVDD – 0.4	V
	PGA differential output impedance			600			600		Ω
	Output impedance tolerance			±10%			±10%		
	External bypass capacitance			10	100		10	100	nF
	Modulator differential input impedance			55			55		kΩ
AC PERFORMANCE									
SNR	Signal-to-noise ratio(3)		112	124		112	124		dB

(1) f_{CLK} = system clock.
(2) Input impedance is improved by disabling input chopping (CHOP bit = 0).
(3) V_{IN} = 20 mV_{DC} / PGA, see Table 1.

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Electrical Characteristics (continued)

AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, over operating temperature range, unless otherwise noted. Typical values are T_J = 25°C. A total ionizing dose of 50 kRad (Si) exposure at a low dose rate of < 10 mRads (Si)/s, post tested at 25°C.

PARAMETER		TEST CONDITIONS		5962L1423101VXC			5962L1423102VXC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
THD	Total harmonic distortion(4)	PGA = 1...16			–122	–99		–122	–101	dB
		PGA = 32			–117	–90		–117	–92	
		PGA = 64			–115			–115		
SFDR	Spurious-free dynamic range				123			123		dB
DC PERFORMANCE										
	Resolution	No missing codes		31			31			bits
f_{DATA}	Data rate	FIR filter mode		250		4000	250		4000	SPS
		SINC filter mode		8000		128000	8000		128000	
	Integral nonlinearity (INL)(5)	Differential input			0.00005	0.0090		0.00005	0.0090	% FSR(6)
			Offset error			0.0170			0.0170	
	Offset error after calibration(7)	Shorted input			50	200		50	200	µV
			Offset drift			750			750	
	Gain error(8)				1			1		µV
	Gain error after calibration(7)				0.02			0.02		µV/°C
	Gain drift			–1.5%	–1.0%	–0.5%	–1.5%	–1.0%	–0.5%	
	Gain matching(9)				0.0002%			0.0002 %		
	Common-mode rejection	PGA = 1			2			2		ppm/°C
		PGA = 16			9			9		
					0.3%	0.8%		0.3%	0.8%	
		f_{CM} = 60 Hz(10)		82	110		82	110		dB
AVDD, AVSS	Power-supply rejection	f_{PS} = 60 Hz(10)		80	90		80	90		dB
			Post 50 kRads (Si), T_J = 25°C(11)	64	90		64	90		dB
DVDD				90	115		90	115		dB
VOLTAGE REFERENCE INPUTS										
	Reference input voltage	(V_{REF} = VREFP – VREFN)		0.5	5	(AVDD – AVSS) + 0.2	0.5	5	(AVDD – AVSS) + 0.2	V
VREFN	Negative reference input			AVSS – 0.1		VREFP – 0.5	AVSS – 0.1		VREFP – 0.5	V
VREFP	Positive reference input			VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
	Reference input impedance				85			85		kΩ
DIGITAL FILTER RESPONSE										
	Passband ripple					±0.003			±0.003	dB

(4) V_{IN} = 31.25 Hz, –0.5 dBFS.
(5) Best-fit method.
(6) FSR: Full-scale range = ±V_{REF} / (2 × PGA).
(7) Calibration accuracy is on the level of noise reduced by 4 (calibration averages 16 readings).
(8) The PGA output impedance and the modulator input impedance results in –1% systematic gain error.
(9) Gain match relative to PGA = 1.
(10) f_{CM} is the input common-mode frequency. f_{PS} is the power-supply frequency.
(11) The maximum limit applies to SMD 5962L14231 post 50 kRads (Si) test at 25°C.

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Electrical Characteristics (continued)

AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, over operating temperature range, unless otherwise noted. Typical values are T_J = 25°C. A total ionizing dose of 50 kRad (Si) exposure at a low dose rate of < 10 mRads (Si)/s, post tested at 25°C.

PARAMETER		TEST CONDITIONS		5962L1423101VXC			5962L1423102VXC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Passband (–0.01 dB)				0.375 × f_{DATA}			0.375 × f_{DATA}		Hz
	Bandwidth (–3 dB)				0.413 × f_{DATA}			0.413 × f_{DATA}		Hz
	High-pass filter corner			0.1		10	0.1		10	Hz
	Stop band attenuation(12)			135			135			dB
	Stop band				0.500 × f_{DATA}			0.500 × f_{DATA}		Hz
	Group delay	Minimum phase filter(13)			5 / f_{DATA}			5 / f_{DATA}		s
		Settling time (latency)			31 / f_{DATA}			31 / f_{DATA}		s
		Minimum phase filter			62 / f_{DATA}			62 / f_{DATA}		s
		Linear phase filter			62 / f_{DATA}			62 / f_{DATA}		s
DIGITAL INPUT/OUTPUT										
V_{IH}				0.8 × DVDD		DVDD	0.8 × DVDD		DVDD	V
V_{IL}				DGND		0.2 × DVDD	DGND		0.2 × DVDD	V
V_{OH}		I_{OH} = 1 mA		0.8 × DVDD			0.8 × DVDD			V
V_{OL}		I_{OL} = 1 mA				0.2 × DVDD			0.2 × DVDD	V
	Input leakage	0 < $V_{DIGITAL\ IN}$ < DVDD				±10			±10	µA
f_{CLK}	Clock input			1		4.096	1		4.096	MHz
f_{SCLK}	Serial clock rate					f_{CLK} / 2			f_{CLK} / 2	MHz
POWER SUPPLY										
AVSS				–2.6		0	–2.6		0	V
AVDD				AVSS + 4.75		AVSS + 5.25	AVSS + 4.75		AVSS + 5.25	V
DVDD				1.75		3.6	1.75		3.6	V
	AVDD, AVSS current	High-resolution mode			4.5	7.2		4.5	6.5	|mA|
			Post 50 kRads (Si), T_J = 25°C(11)			11			11	|mA|
		Power-down mode			–200	200		-200	200	|µA|
			Post 50 kRads (Si), T_J = 25°C(11)			5			5	|mA|
		Standby mode			–200	200		-200	200	|µA|
			Post 50 kRads (Si), T_J = 25°C(11)			5			5	|mA|

(12) Input frequencies in the range of Nf_{CLK} / 512 ± f_{DATA} / 2 (N = 1, 2, 3...) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120 dB, typ.
(13) At DC. See Figure 42.

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Electrical Characteristics (continued)

AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, over operating temperature range, unless otherwise noted. Typical values are T_J = 25°C. A total ionizing dose of 50 kRad (Si) exposure at a low dose rate of < 10 mRads (Si)/s, post tested at 25°C.

PARAMETER	TEST CONDITIONS		5962L1423101VXC			5962L1423102VXC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DVDD current	High-resolution mode			0.6	1.5		0.6	1.2	mA
	Power-down mode(14)			32	120		32	120	µA
	Standby mode			73	175		73	175	µA
Power dissipation	High-resolution mode			25	41		25	41	mW
		Post 50 kRads (Si), T_J = 25°C(11)			60			60	mW
	Power-down mode			0.45	0.95		0.45	0.95	mW
		Post 50 kRads (Si), T_J = 25°C(11)			25.4			25.4	mW
	Standby mode			0.58	1.1		0.58	1.1	mW
		Post 50 kRads (Si), T_J = 25°C(11)			25.4			25.4	mW

(14) CLK input stopped.

7.6 Timing Requirements

At T_A = –55°C to 125°C and DVDD = 1.65 to 3.6 V, unless otherwise noted.

		MIN	MAX	UNIT
t_{SCLK}	SCLK period	2	16	1 / f_{CLK}
$t_{SPWH, L}$	SCLK pulse width, high and low(1)	0.8	10	1 / f_{CLK}
t_{DIST}	DIN valid to SCLK rising edge: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	50		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: propagation delay(2)		100	ns
t_{DOHD}	SCLK falling edge to DOUT invalid: hold time	0		ns
t_{SCDL}	Final SCLK rising edge of command to first SCLK rising edge for register read/write data	24		1 / f_{CLK}

(1) Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the serial interface.
(2) Load on DOUT = 20 pF || 100 kΩ.

7.7 Pulse-Sync Timing Requirements

See Figure 46 and Figure 47 for timing diagrams.

		MIN	MAX	UNIT
t_{SYNC}	SYNC period(1)	1	Infinite	n / f_{DATA}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10		ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10		ns
$t_{SPWH, L}$	SYNC pulse width, high or low	2		1 / f_{CLK}
t_{DR}	Time for data ready (SINC filter)	See *器件支持*, 表 21		
	Time for data ready (FIR filter)	62.98046875 / f_{DATA} + 466 / f_{CLK}		

(1) Continuous-Sync mode; a free-running SYNC clock input without causing re-synchronization.

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7.8 Reset Timing Requirements

See Figure 48 for timing diagram.

		MIN	MAX	UNIT
t_{CRHD}	CLK to RESET hold time	10		ns
t_{RCSU}	RESET to CLK setup time	10		ns
t_{RST}	RESET low	2		1 / f_{CLK}
t_{DR}	Time for data ready	62.98046875 / f_{DATA} + 468 / f_{CLK}		s

7.9 Read Data Timing Requirements

		MIN	MAX	UNIT
t_{DDPD}	$\overline{DRDY}$ to valid MSB on DOUT propagation delay (see Figure 54)(1)		100	ns
t_{DR}	Time for new data after data read command (see Figure 55)	0	1	f_{DATA}

(1) Load on DOUT = 20 pF || 100 kΩ.

7.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay(1)	Minimum phase filter		5 / f_{DATA}		s
	Linear phase filter		31 / f_{DATA}		s
Settling time (latency)	Minimum phase filter		62 / f_{DATA}		s
	Linear phase filter		62 / f_{DATA}		s

(1) At DC. See Figure 42.

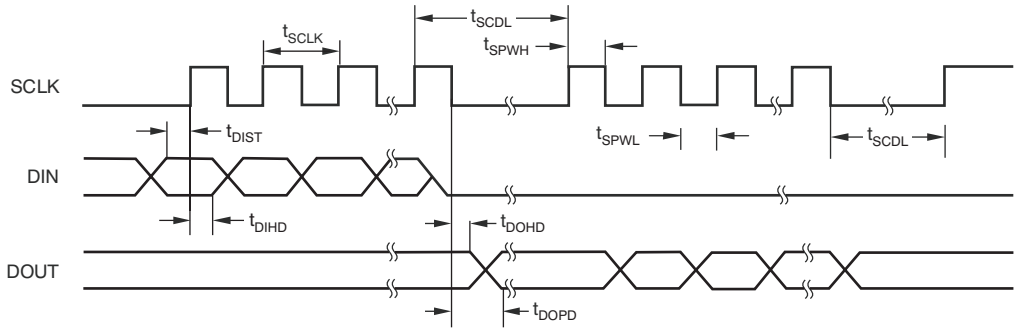


Figure 1. Timing Diagram

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7.11 Typical Characteristics

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

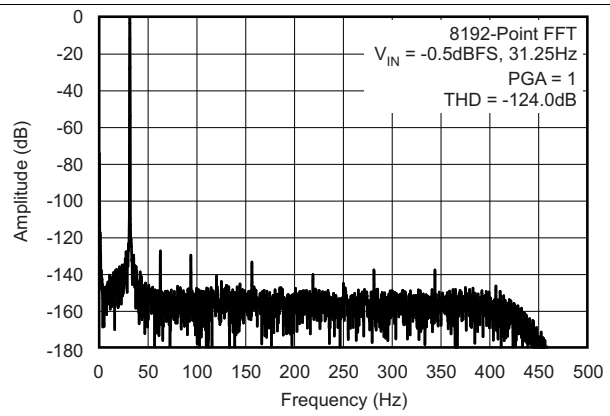


Figure 2. Output Spectrum

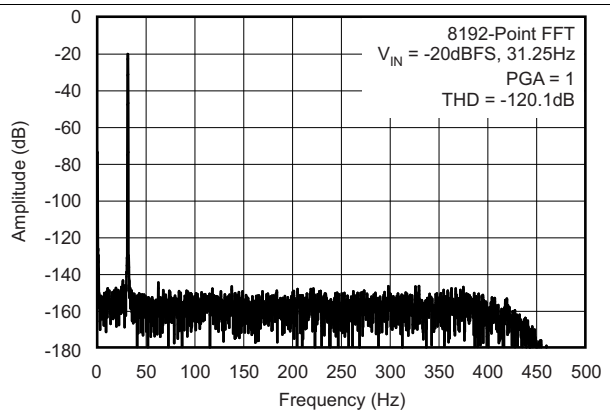


Figure 3. Output Spectrum

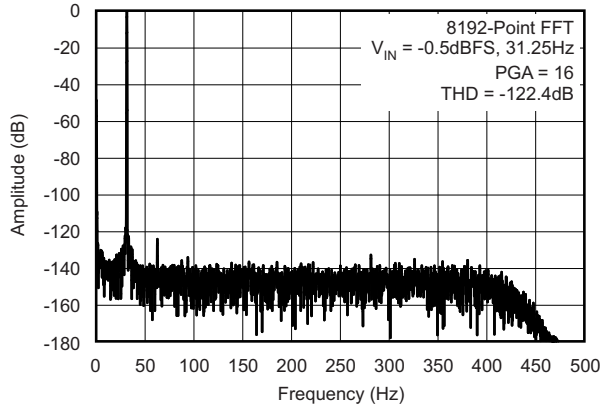


Figure 4. Output Spectrum

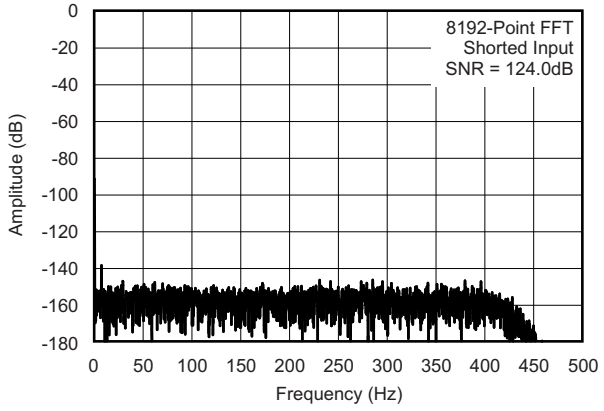


Figure 5. Output Spectrum

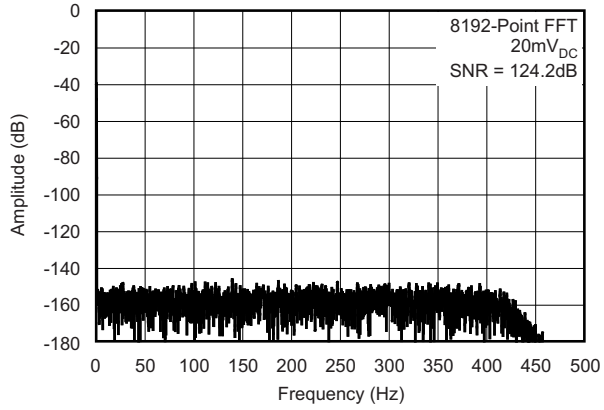


Figure 6. Output Spectrum

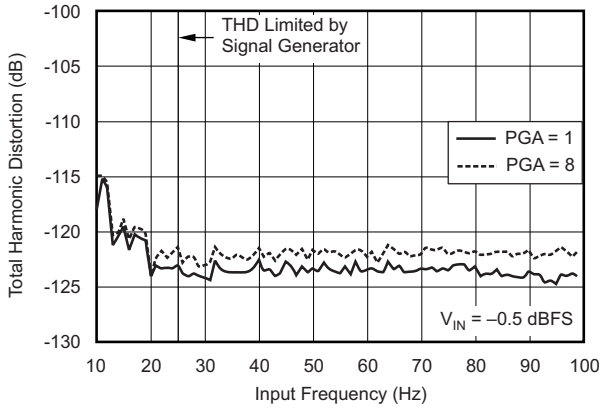


Figure 7. THD vs Input Frequency

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Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

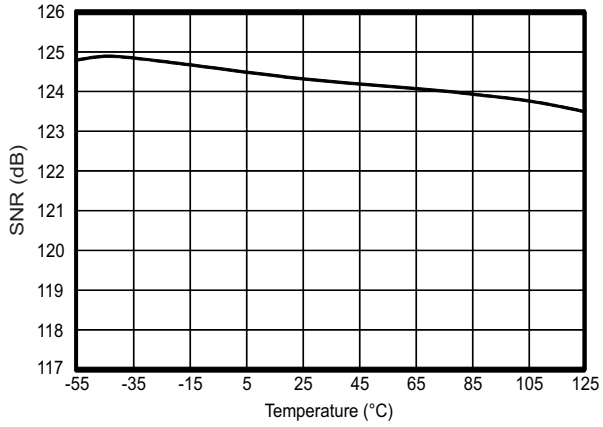


Figure 8. SNR (1000 SPS) vs Temperature

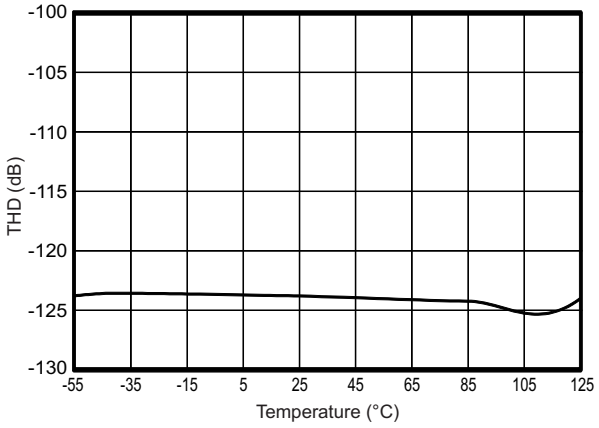


Figure 9. THD (G = 8) vs Temperature

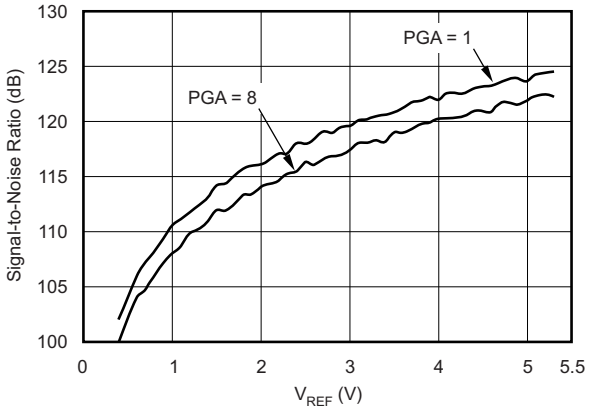


Figure 10. SNR vs Reference Voltage

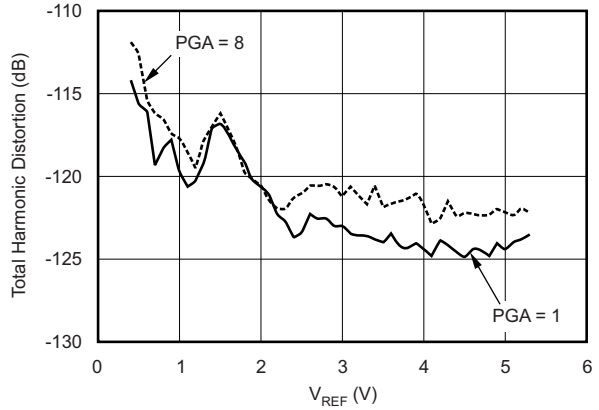


Figure 11. THD vs Reference Voltage

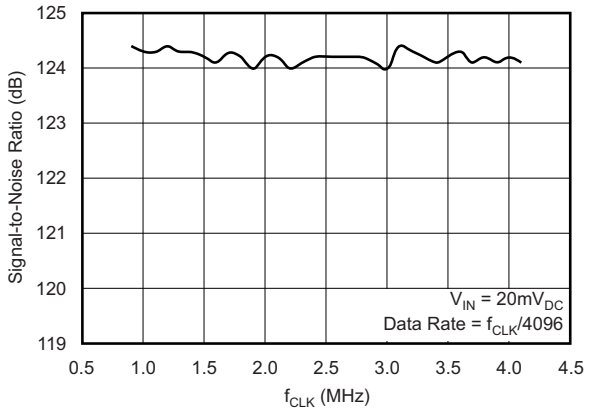


Figure 12. SNR vs Clock Frequency

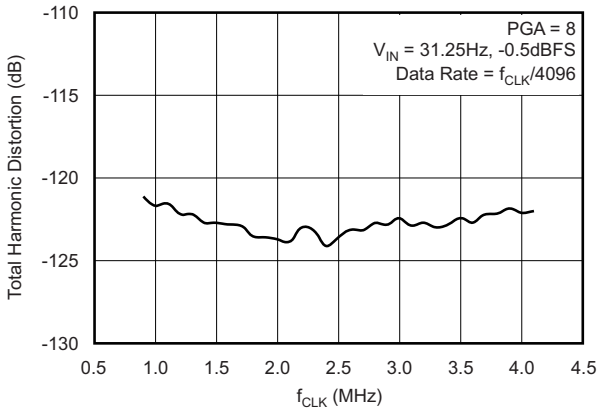


Figure 13. THD vs Clock Frequency

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Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

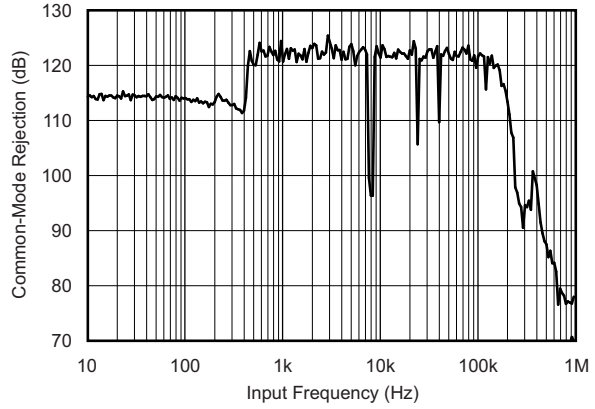


Figure 14. CMR vs Input Frequency

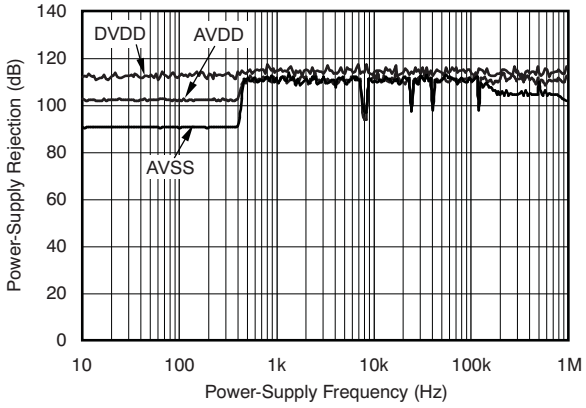


Figure 15. Power-Supply Rejection vs Frequency

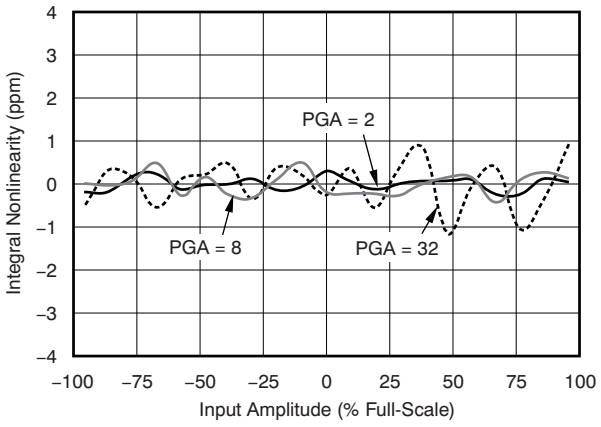


Figure 16. INL vs Input Amplitude

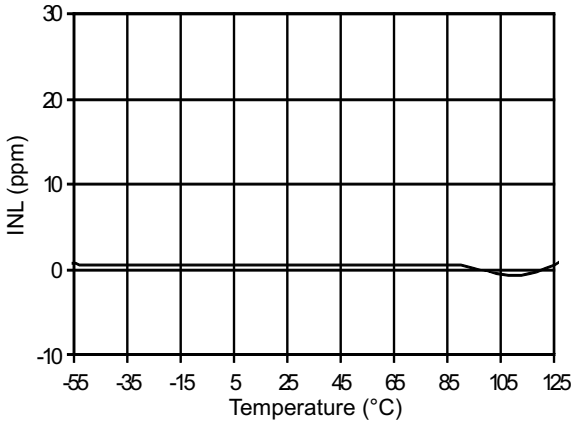


Figure 17. INL vs Temperature

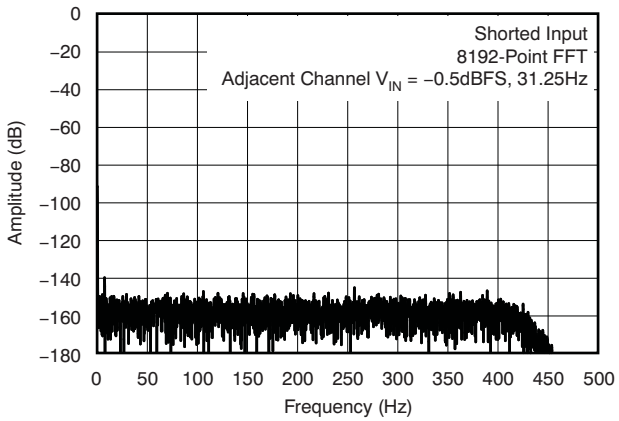


Figure 18. Crosstalk Output Spectrum

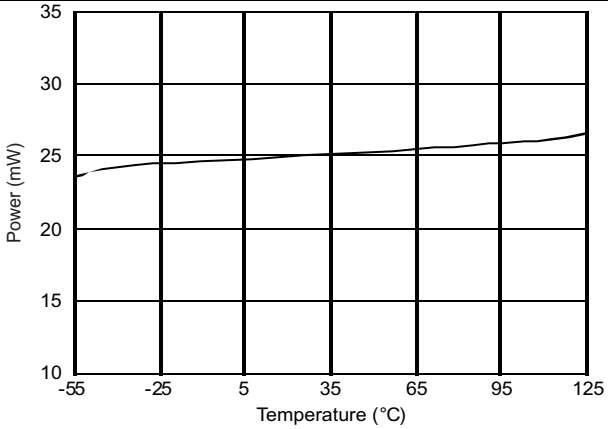


Figure 19. Power vs Temperature

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Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

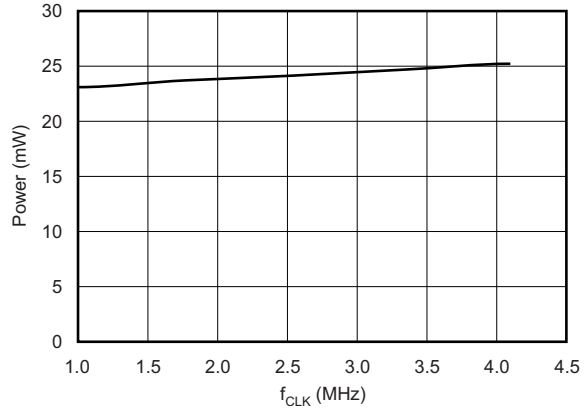


Figure 20. Power vs Clock Frequency

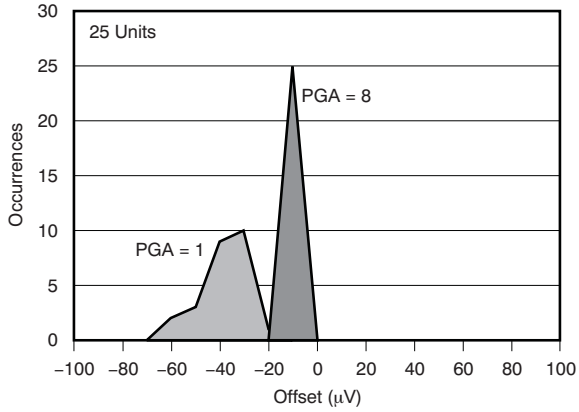


Figure 21. Offset Histogram

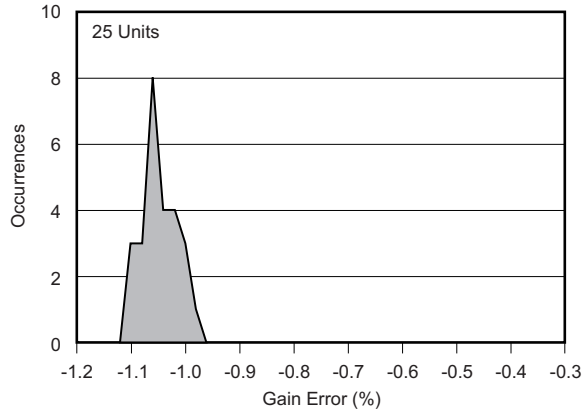


Figure 22. Gain Error Histogram

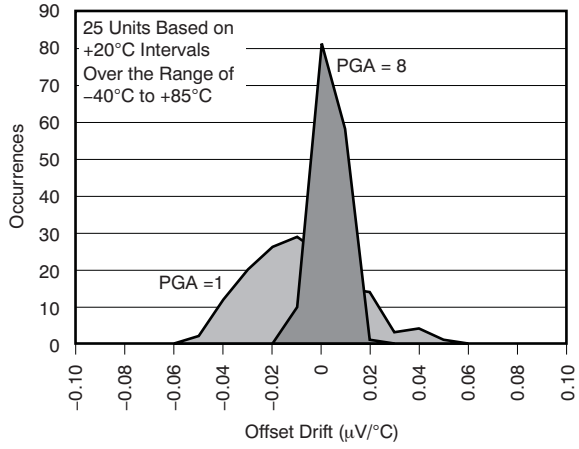


Figure 23. Offset Drift Histogram

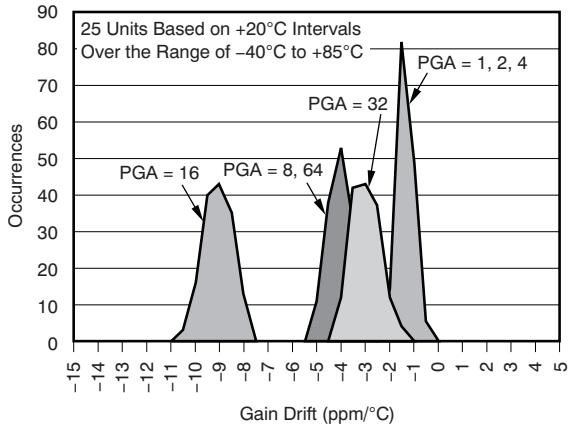


Figure 24. Gain Drift Histogram

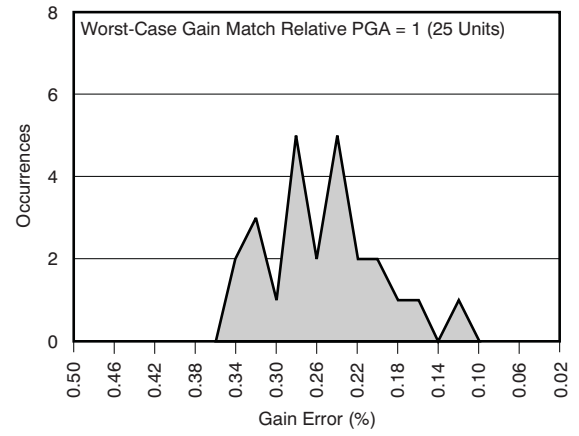


Figure 25. Gain Match Histogram

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8 Detailed Description

8.1 Overview

The ADS1282-SP is a high-performance analog-to-digital converter (ADC) intended for space satellite temperature sensing, precision scientific and high accuracy applications. The converter provides 24- or 32-bit output data in data rates from 250 SPS to 4000 SPS. The *Functional Block Diagram* shows the block diagram of the ADS1282-SP.

The two-channel input MUX allows five configurations: Input 1; Input 2; Input 1 and Input 2 shorted together; shorted with 400-Ω test; and common-mode test. The input MUX is followed by a continuous time PGA, featuring very low noise of 5 nV/$\sqrt{\text{Hz}}$. The PGA is controlled by register settings, allowing gains of 1 to 64, in powers of 2.

The inherently-stable, fourth-order, delta-sigma modulator measures the differential input signal V_{IN} = (AINP – AINN) × PGA against the differential reference V_{REF} = (VREFP – VREFN). A digital output (MFLAG) indicates that the modulator is in overload as a result of an overdrive condition. The modulator output is available directly on the MCLK, M0, and M1 output pins when in modulator mode. The modulator connects to an on-chip digital filter that provides the output code readings.

The digital filter consists of a variable decimation rate, fifth-order sinc filter followed by a variable phase, decimate-by-32, finite-impulse response (FIR) low-pass filter with programmable phase, and then by an adjustable high-pass filter for DC removal of the output reading. The output of the digital filter can be taken from the sinc, the FIR low-pass, or the infinite impulse response (IIR) high-pass sections as long as the maximum clock rate of the SPI (fclk/2) is respected.

Gain and offset registers scale the digital filter output to produce the final code value. The scaling feature can be used for calibration and sensor gain matching. The output data word is provided as either a 24-bit word or a full 32-bit word, allowing complete utilization of the inherently high resolution.

The SYNC input resets the operation of both the digital filter and the modulator, allowing synchronization conversions of multiple ADS1282-SP devices to an external event. The SYNC input supports a continuously-toggled input mode that accepts an external data frame clock locked to the conversion rate.

The $\overline{\text{RESET}}$ input resets the register settings and also restarts the conversion process. The $\overline{\text{PWDN}}$ input sets the device into a micro-power state. The register settings are not retained in $\overline{\text{PWDN}}$ mode. Use the STANDBY command in its place if it is desired to retain register settings (the quiescent current in the Standby mode is slightly higher).

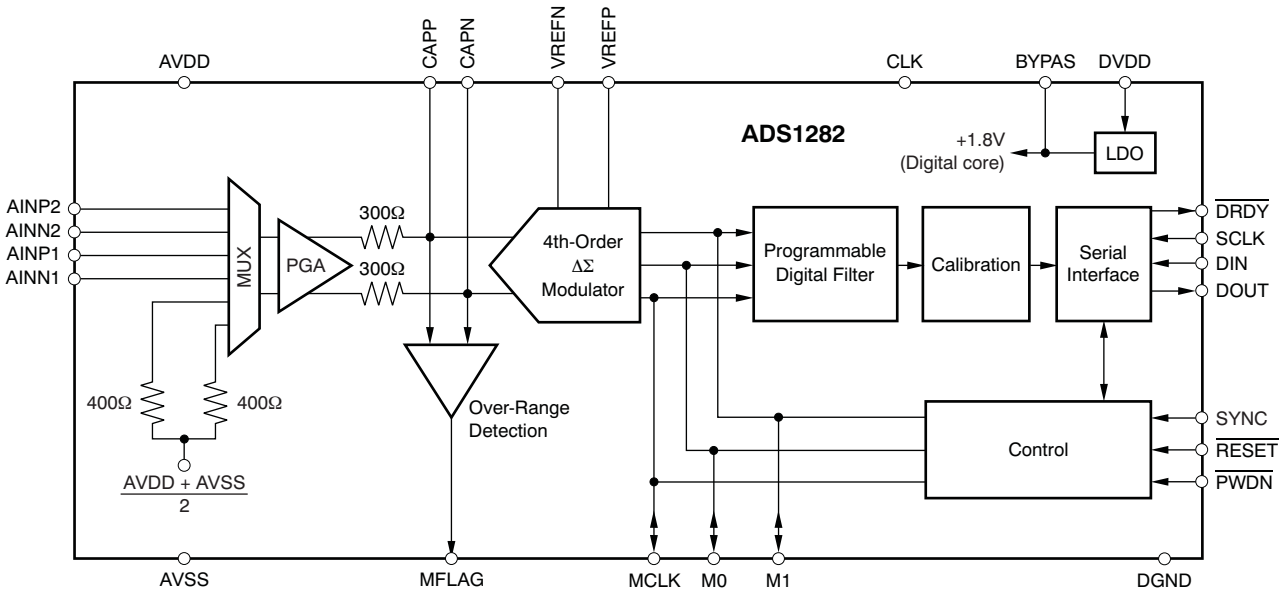
Noise-immune Schmitt-trigger and clock-qualified inputs ($\overline{\text{RESET}}$ and SYNC) provide increased reliability in high-noise environments. The serial interface is used to read conversion data, in addition to reading from and writing to the configuration registers.

The device features unipolar and bipolar analog power supplies (AVDD and AVSS, respectively) for input range flexibility and a digital supply accepting 1.8 V to 3.3 V. The analog supplies may be set to 5 V to accept unipolar signals (with input offset) or set lower in the range of ±2.5 V to accept true bipolar input signals (ground referenced).

An internal sub-regulator is used to supply the digital core from DVDD. The BYPAS pin (pin 28) is the sub-regulator output and requires a 1-μF capacitor for noise reduction. BYPAS should not be used to drive external circuitry.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Noise Performance

The ADS1282-SP device offers outstanding noise performance (SNR). SNR depends on the data rate, the PGA setting, and the mode. As the bandwidth is reduced by decreasing the data rate, the SNR improves correspondingly. Similarly, as the PGA gain is increased, the SNR decreases. Table 1 summarizes the noise performance versus data rate, PGA setting, and mode.

8.3.2 Input-Referred Noise

The input-referred noise is related to SNR by Equation 1:

$$SNR = 20\log \frac{FSR_{RMS}}{N_{RMS}} \quad (1)$$

where:

- FSR_{RMS} = Full-scale range RMS = (VREFP – VREFN)/(2 × √2 × PGA)
- N_{RMS} = Noise RMS (input-referred)

8.3.3 Idle Tones

The ADS1282-SP modulator incorporates an internal dither signal that randomizes the idle tone energy. Low-level idle tones may still be present, typically –137-dB less than full-scale. The low-level idle tones can be shifted out of the passband with an external offset = 20 mV/PGA. See the *Application Information* section for the recommended offset circuit.

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Feature Description (continued)

8.3.4 Operating Mode

The default mode is high-resolution.

Table 1. Signal-to-Noise Ratio (dB)(1)

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
250	130	130	129	128	125	119	114
500	127	127	126	125	122	116	111
1000	124	124	123	122	119	113	108
2000	121	121	120	119	116	111	106
4000	118	118	117	116	113	108	103

(1) V_{IN} = 20 mV_{DC} / PGA.

8.3.5 Analog Inputs and Multiplexer

Figure 26 shows a diagram of the input multiplexer.

ESD diodes protect the multiplexer inputs. If either input is taken less than AVSS – 0.3 V or greater than AVDD + 0.3 V, the ESD protection diodes may turn on. If these conditions are possible, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings*).

Also, overdriving one unused input may affect the conversions of the other input. If overdriven inputs are possible, TI recommends clamping the signal with external Schottky diodes.

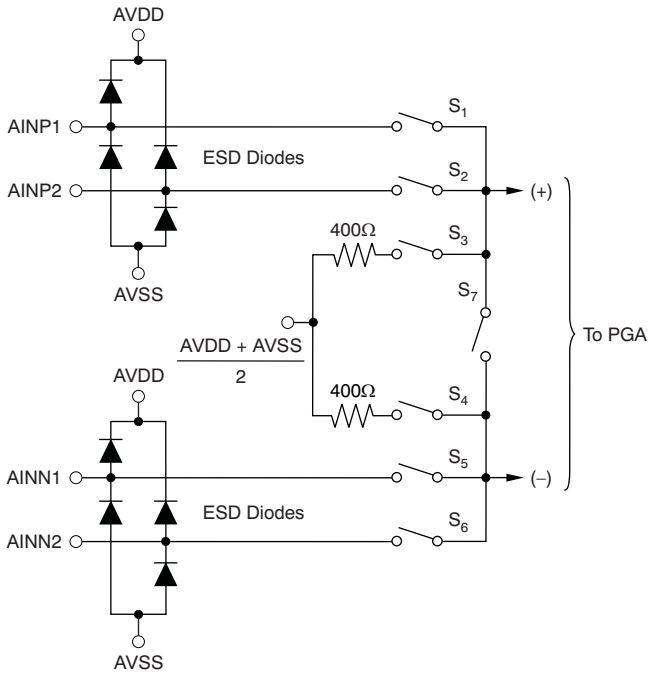


Figure 26. Analog Inputs and Multiplexer

The specified input operating range of the PGA is shown in Equation 2:

AVSS + 0.7 V < (AINN or AINP) < AVDD – 1.25 V (2)

Absolute input levels (input signal level and common-mode level) should be maintained within these limits for best operation.

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The multiplexer connects one of the two external differential inputs to the preamplifier inputs, in addition to internal connections for various self-test modes. Table 2 summarizes the multiplexer configurations for Figure 26.

Table 2. Multiplexer Modes

MUX[2:0]	SWITCHES	DESCRIPTION
000	S_1, S_5	AINP1 and AINN1 connected to preamplifier
001	S_2, S_6	AINP2 and AINN2 connected to preamplifier
010	S_3, S_4	Preamplifier inputs shorted together through 400Ω internal resistors
011	S_1, S_5, S_2, S_6	AINP1, AINN1 and AINP2, AINN2 connected together and to the preamplifier
100	S_6, S_7	External short, preamplifier inputs shorted to AINN2 (common-mode test)

The typical on-resistance (R_{ON}) of the multiplexer switch is 30 Ω. When the multiplexer is used to drive an external load on one input by a signal generator on the other input, on-resistance and on-resistance amplitude dependency can lead to measurement errors. Figure 27 shows THD versus load resistance and amplitude. THD improves with high-impedance loads and with lower amplitude drive signals. The data are measured with the circuit from Figure 28 with MUX[2:0] = 011.

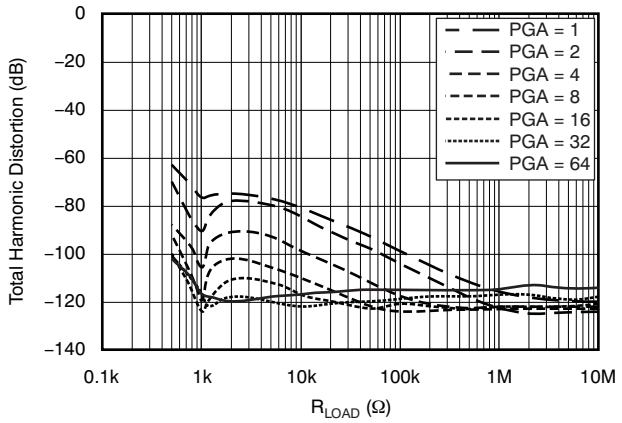


Figure 27. THD vs External Load and Signal Magnitude (PGA) (See Figure 28)

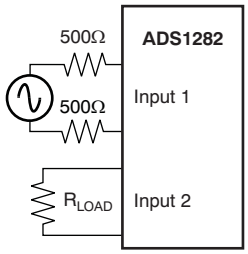


Figure 28. Driving an External Load Through the MUX

8.3.6 PGA (Programmable Gain Amplifier)

The PGA of the ADS1282-SP is a low-noise, continuous-time, differential-in/differential-out CMOS amplifier. The gain is programmable from 1 to 64, set by register bits, PGA[2:0]. The PGA differentially drives the modulator through 300-Ω internal resistors. A COG capacitor (10 nF typical) must be connected to CAPP and CAPN to filter modulator sampling glitches. The external capacitor also serves as an anti-alias filter. The corner frequency is given in Equation 3:

$$f_P = \frac{1}{6.3 \times 600 \times C} \quad (3)$$

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Referring to Figure 29, amplifiers A_1 and A_2 are chopped to remove the offset, offset drift, and the 1/f noise. Chopping moves the effects to f_{CLK}/128 (8 kHz), which is safely out of the passband. Chopping can be disabled by setting the CHOP register bit = 0. With chopping disabled, the impedance of the PGA increases substantially (>> 1 GΩ). As shown in Figure 30, chopping maintains flat noise density; if chopping is disabled, however, it results in a rising 1/f noise profile.

The PGA has programmable gains from 1 to 64. Table 3 shows the register bit setting for the PGA and resulting full-scale differential range.

The specified output operating range of the PGA is shown in Equation 4:

$$AVSS + 0.4\ V < (CAPN \text{ or } CAPP) < AVDD - 0.4\ V \quad (4)$$

PGA output levels (signal plus common-mode) should be maintained within these limits for best operation.

Table 3. PGA Gain Settings

PGA[2:0]	GAIN	DIFFERENTIAL INPUT RANGE (V)(1)
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.312
100	16	±0.156
101	32	±0.078
110	64	±0.039

(1) V_{REF} = VREFP – VREFN = 5 V

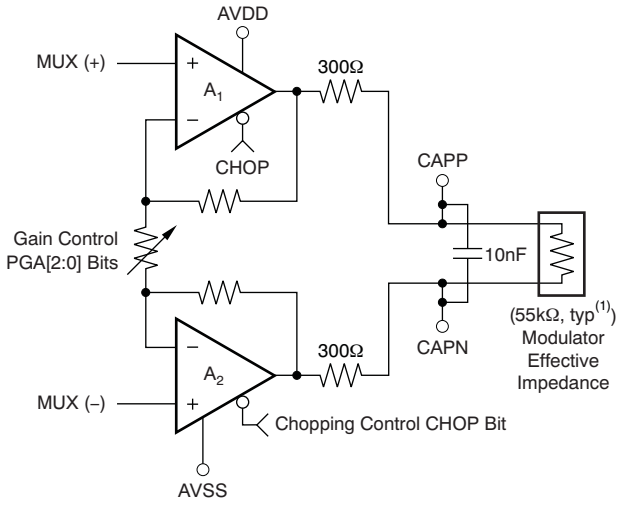


Figure 29. PGA Block Diagram

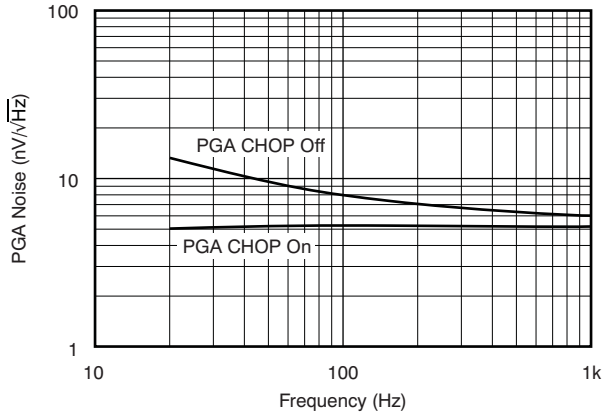


Figure 30. PGA Noise

8.3.7 ADC

The ADC block of the ADS1282-SP is composed of two sections: a high-accuracy modulator and a programmable digital filter.

8.3.8 Modulator

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as Figure 31 shows. It shifts the quantization noise to a higher frequency (out of the passband) where digital filtering can easily remove it. The modulator can be filtered either by the on-chip digital filter or by use of post-processing filters.

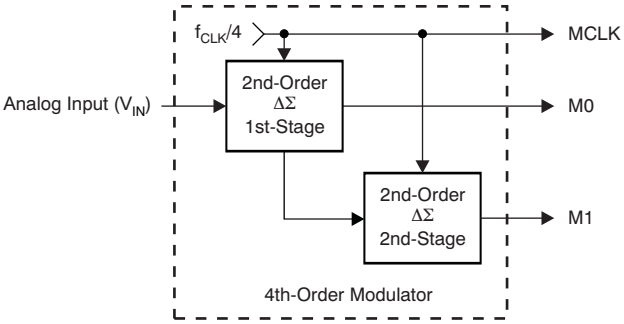


Figure 31. Fourth-Order Modulator

The modulator first stage converts the analog input voltage into a pulse-code modulated (PCM) stream. When the level of differential analog input (AINP – AINN) is near one-half the level of the reference voltage 1/2 × (VREFP – VREFN), the '1' density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM '0' and '1' densities are nearly equal. At the two extremes of the analog input levels (+FS and –FS), the '1' density of the PCM streams is approximately 90% and 10%, respectively.

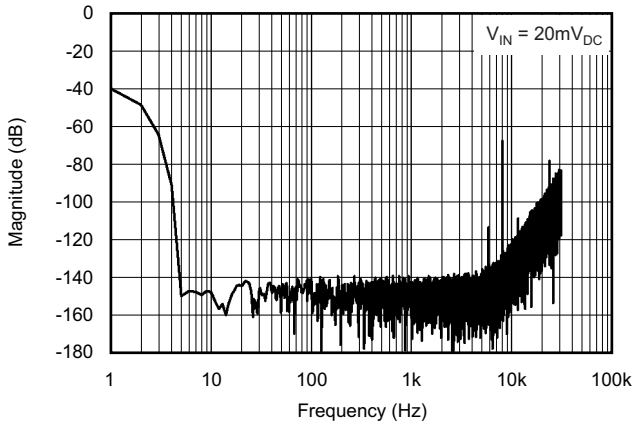
The modulator second stage produces a '1' density data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are then combined before the digital filter stage, as shown in Equation 5.

$$Y[n] = 3M0[n – 2] – 6M0[n –3] + 4M0[n – 4] + 9(M1[n] – 2M1[n – 1] + M1[n – 2]) \quad (5)$$

M0[n] represents the most recent first-stage output while M0[n – 1] is the previous first-stage output. When the modulator output is enabled, the digital filter shuts down to save power.

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The modulator is optimized for input signals within a 4-kHz passband. As Figure 32 shows, the noise shaping of the modulator results in a sharp increase in noise greater than 6 kHz. The modulator has a chopped input structure that further reduces noise within the passband. The noise moves out of the passband and appears at the chopping frequency (f_{CLK} / 512 = 8 kHz). The component at 5.8 kHz is the tone frequency, shifted out of band by an external 20 mV/PGA offset. The frequency of the tone is proportional to the applied DC input and is given by PGA × V_{IN}/0.003 (in kHz).



1-Hz resolution

Figure 32. Modulator Output Spectrum

8.3.9 Modulator Over-Range

The ADS1282-SP modulator is inherently stable, and therefore, has predictable recovery behavior resulting from an input overdrive condition. The modulator does not exhibit self-resetting behavior, which often results in an unstable output data stream.

The ADS1282-SP modulator outputs a 1s density data stream at 90% duty cycle with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but less than 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input returns to the normal range from a long duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (31 readings for linear phase FIR). 31 additional readings (62 total) are required for completely settled data.

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle, all 1s or all 0s, the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small duration overdrive may not always clip the output code. When the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires an additional 62 conversions for fully settled data (linear phase FIR).

In the extreme case of over-range, either input is overdriven, exceeding the voltage of either analog supply voltage plus an internal ESD diode drop. The internal diodes begin to conduct and the signal on the input is clipped. When the input overdrive is removed, the diodes recover quickly. Keep in mind that the input current must be limited to 100-mA peak or 10-mA continuous if an overvoltage condition is possible.

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8.3.10 Modulator Input Impedance

The modulator samples the buffered input voltage with an internal capacitor to perform conversions. The charging of the input sampling capacitor draws a transient current from the PGA output. The average value of the current can be used to calculate an effective input impedance of:

$$R_{EFF} = 1 / (f_{MOD} \times C_S) \quad (6)$$

where

- f_{MOD} = Modulator sample frequency, Mode = CLK / 4
- C_S = Input sampling capacitor (17 pF, typ)

The resulting modulator input impedance for CLK = 4.096 MHz is 55 kΩ. The modulator input impedance and the PGA output resistors result in a systematic gain error of –1%. C_S can vary ±20% over production lots, affecting the gain error.

8.3.11 Modulator Over-Range Detection (MFLAG)

The ADS1282-SP has a fast-responding over-range detection that indicates when the differential input exceeds ±100% full scale. The threshold tolerance is ±2.5%.The MFLAG output asserts high when in an over-range condition. As Figure 33 and Figure 34 illustrate, the absolute differential input is compared to 100% of range. The output of the comparator is sampled at the rate of f_{MOD} / 2, yielding the MFLAG output. The minimum MFLAG pulse width is f_{MOD} / 2.

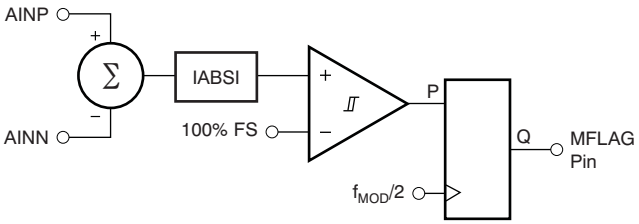


Figure 33. Modulator Over-Range Block Diagram

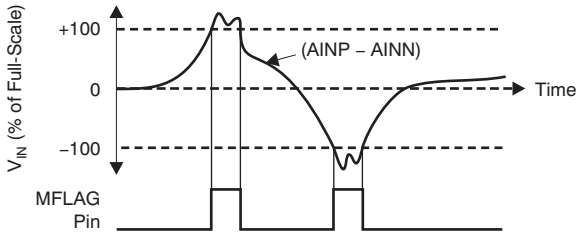


Figure 34. Modulator Over-Range Flag Operation

8.3.12 Voltage Reference Inputs (VREFP, VREFN)

The voltage reference for the ADS1282-SP is the differential voltage between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry of the reference inputs shown in Figure 35. The average load presented by the switched capacitor reference input can be modeled with an effective differential impedance of $R_{EFF} = t_{SAMPLE} / C_{IN}$ ($t_{SAMPLE} = 1/f_{MOD}$). The effective impedance of the reference inputs loads the external reference.

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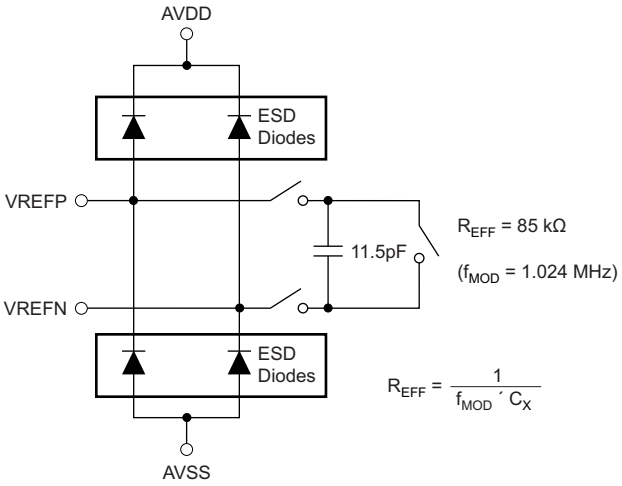


Figure 35. Simplified Reference Input Circuit

The ADS1282-SP reference inputs are protected by ESD diodes. In order to prevent these diodes from turning on, the voltage on either input must stay within the range shown in Equation 7:

$$AVSS - 300\ mV < (VREFP \text{ or } VREFN) < AVDD + 300\ mV \quad (7)$$

The minimum valid input for VREFN is AVSS – 0.1 V and maximum valid input for VREFP is AVDD + 0.1 V.

A high-quality 5 V reference voltage is necessary for achieving the best performance from the ADS1282-SP. Noise and drift on the reference degrade overall system performance, and it is critical that special care be given to the circuitry generating the reference voltages in order to achieve full performance. See *Application Information* for reference recommendations.

8.3.13 Digital Filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter is comprised of three cascaded filter stages: a variable-decimation, fifth-order sinc filter; a fixed-decimation FIR, low-pass filter (LPF) with selectable phase; and a programmable, first-order, high-pass filter (HPF), as shown in Figure 36.

The output can be taken from one of the three filter blocks, as Figure 36 shows. To implement the digital filter completely off-chip, select the filter bypass setting (modulator output). For partial filtering by the ADS1282-SP, select the sinc filter output. For complete on-chip filtering, activate both the sinc and FIR stages. The HPF can then be included to remove DC and low frequencies from the data. Table 4 shows the filter options.

Table 4. Digital Filter Selection

FILTR[1:0] BITS	DIGITAL FILTERS SELECTED
00	Bypass; modulator output mode
01	Sinc
10	Sinc + FIR
11	Sinc + FIR + HPF (low-pass and high-pass)

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8.3.13.1 Sinc Filter Stage (Sinx/X)

The sinc filter is a variable decimation rate, fifth-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} (f_{CLK}/4). The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter; it is set by the DR[2:0] register bits, as shown in Table 5.

Equation 8 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5 \tag{8}$$

Table 5. Sinc Filter Data Rates (Clk = 4.096 MHz)

DR[2:0] REGISTER	DECIMATION RATIO (N)	SINC DATA RATE (SPS)
000	128	8000
001	64	16000
010	32	32000
011	16	64000
100	8	128000

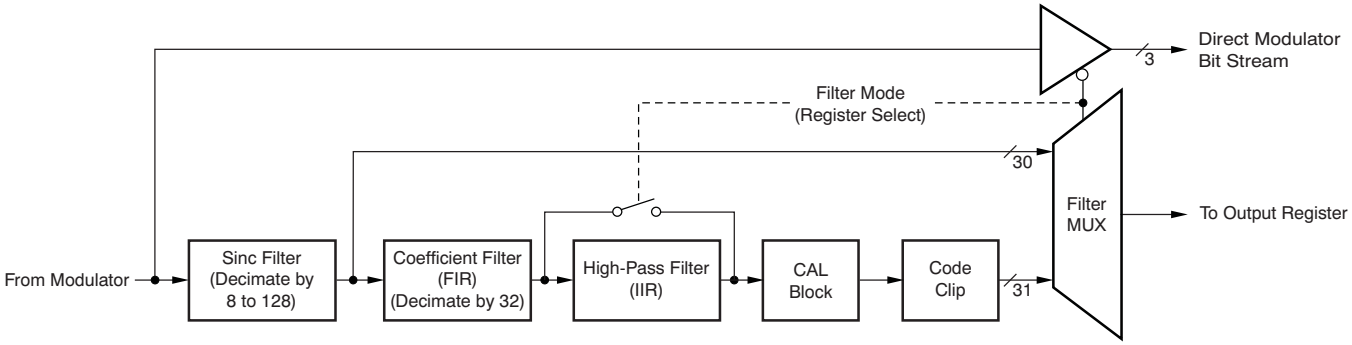


Figure 36. Digital Filter and Output Code Processing

Equation 9 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \tag{9}$$

where

- N = Decimation ratio (see Table 5)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. Figure 37 shows the frequency response of the sinc filter and Figure 38 shows the roll-off of the sinc filter.

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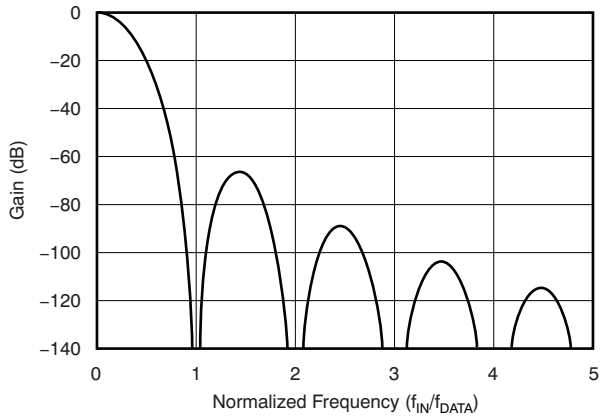


Figure 37. Sinc Filter Frequency Response

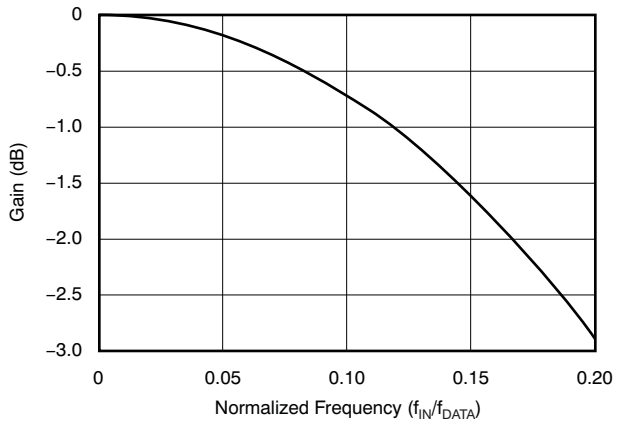


Figure 38. Sinc Filter Roll-Off

8.3.13.2 FIR Stage

The second stage of the ADS1282-SP digital filter is an FIR low-pass filter. Data are supplied to this stage from the sinc filter. The FIR stage is segmented into four sub-stages, as shown in Figure 39. The first two sub-stages are half-band filters with decimation ratios of 2. The third sub-stage decimates by 4 and the fourth sub-stage decimates by 2. The overall decimation of the FIR stage is 32. Two coefficient sets are used for the third and fourth sections, depending on the phase selection. 表 20 (in *器件支持*) lists the FIR stage coefficients. Table 6 lists the data rates and overall decimation ratio of the FIR stage.

Table 6. Fir Filter Data Rates

DR[2:0] REGISTER	DECIMATION RATIO (N)	FIR DATA RATE (SPS)
000	4096	250
001	2048	500
010	1024	1000
011	512	2000
100	256	4000

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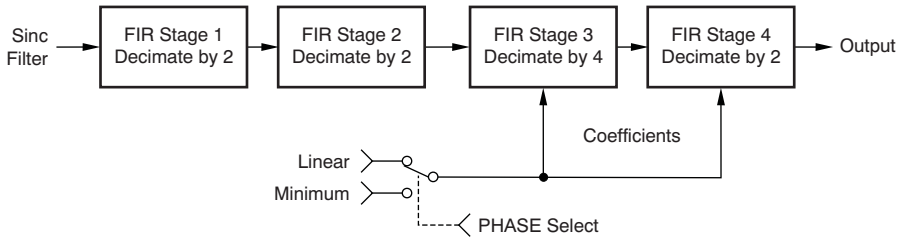


Figure 39. Fir Filter Sub-Stages

As shown in Figure 40, the FIR frequency response provides a flat passband to 0.375 of the data rate (±0.003-dB passband ripple). Figure 41 shows the transition from passband to stop band.

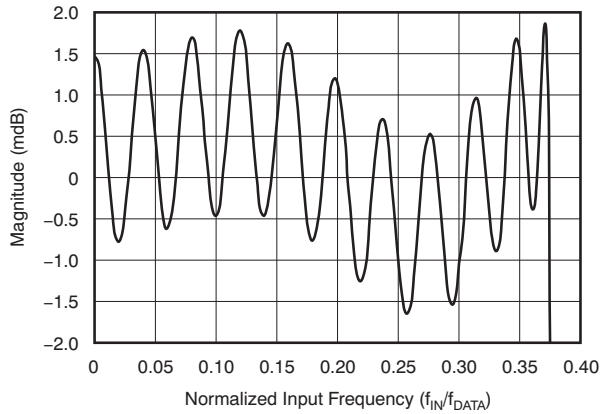


Figure 40. FIR Passband Magnitude Response (F_{DATA} = 500 Hz)

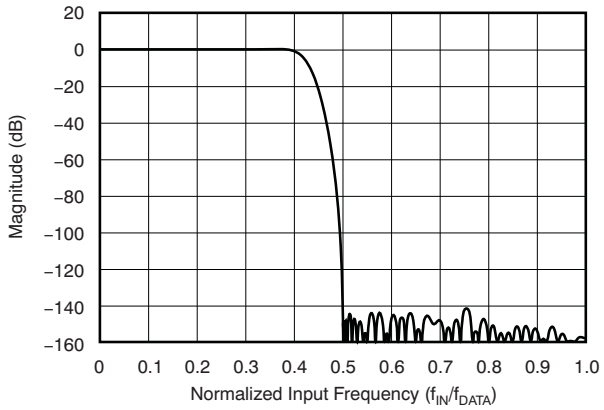


Figure 41. FIR Transition Band Magnitude Response

Although not shown in Figure 41, the passband response repeats at multiples of the modulator frequency ($Nf_{MOD} - f_0$ and $Nf_{MOD} + f_0$, where N = 1, 2, and so forth, and f_0 = passband). These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the passband and cause errors. A low-pass signal filter reduces the effect of aliasing. Often, the RC low-pass filter provided by the PGA output resistors and the external capacitor connected to CAPP and CAPN provides sufficient signal attenuation.

8.3.13.3 Group Delay and Step Response

The FIR block is implemented as a multi-stage FIR structure with selectable linear or minimum phase response. The passband, transition band, and stop band responses of the filters are nearly identical but differ in the respective phase responses.

8.3.13.3.1 Linear Phase Response

Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Linear phase filters have the property that the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of the signal nature. This filter behavior results in essentially zero phase error when analyzing multi-tone signals. However, the group delay and settling time of the linear phase filter are somewhat larger than the minimum phase filter, as shown in Figure 42.

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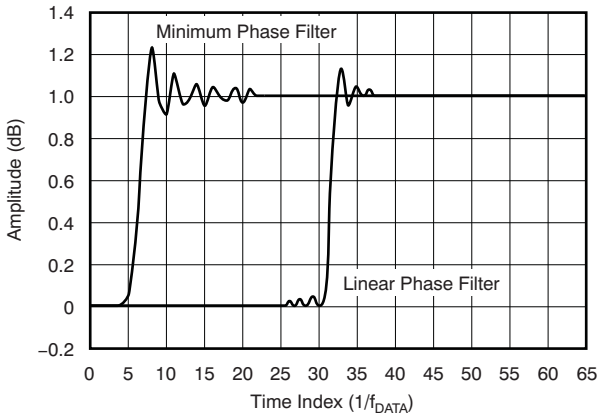


Figure 42. FIR Step Response

8.3.13.3.2 Minimum Phase Response

The minimum phase filter provides a short delay from the arrival of an input signal to the output, but the relationship (phase) is not constant versus frequency, as shown in Figure 43. The filter phase is selected by the PHS bit, as Table 7 shows.

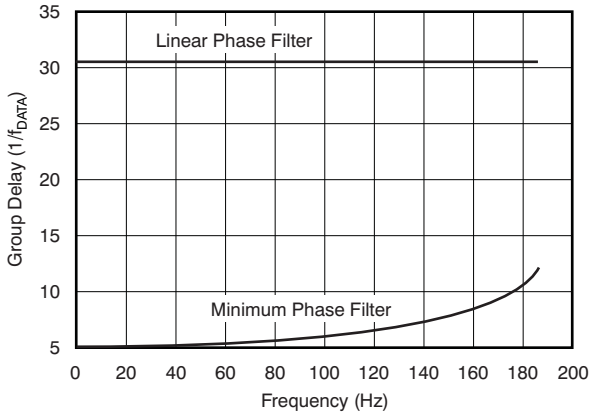


Figure 43. FIR Group Delay (F_{DATA} = 500 Hz)

Table 7. Fir Phase Selection

PHS BIT	FILTER PHASE
0	Linear
1	Minimum

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8.3.13.4 HPF Stage

The last stage of the ADS1282-SP filter block is a first-order HPF implemented as an IIR structure. This filter stage blocks DC signals and rolls off low-frequency components below the cut-off frequency. The transfer function for the filter is shown in 公式 17 of the *器件支持*.

The high-pass corner frequency is programmed by registers HPF[1:0], in hexadecimal. Equation 10 is used to set the high-pass corner frequency. Table 8 lists example values for the high-pass filter.

$$HPF[1:0] = 65{,}536 \left[1 - \sqrt{1 - 2\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}} \right] \quad (10)$$

where

- HPF = High-pass filter register value (converted to hexadecimal)
- $\omega_N = 2\pi f_{HP}/f_{DATA}$ (normalized frequency, radians)
- f_{HP} = High-pass corner frequency (Hz)
- f_{DATA} = Data rate (Hz)

Table 8. High-Pass Filter Value Examples

f_{HP} (Hz)	DATA RATE (SPS)	HPF[1:0]
0.5	250	0337h
1	500	0337h
1	1000	019Ah

The HPF causes a small gain error, in which case the magnitude of the error depends on the ratio of f_{HP}/f_{DATA}. For many common values of (f_{HP}/f_{DATA}), the gain error is negligible. Figure 44 shows the gain error of the HPF. The gain error factor is illustrated in 公式 16 (see *器件支持*).

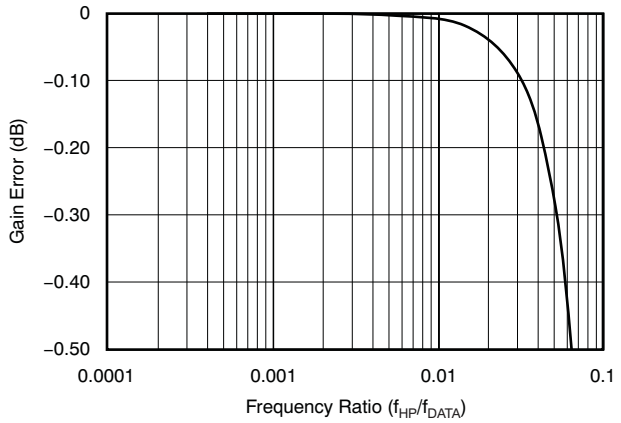


Figure 44. HPF Gain Error

Figure 45 shows the first-order amplitude and phase response of the HPF. In the case of applying step inputs or synchronizing, the settling time of the filter should be taken into account.

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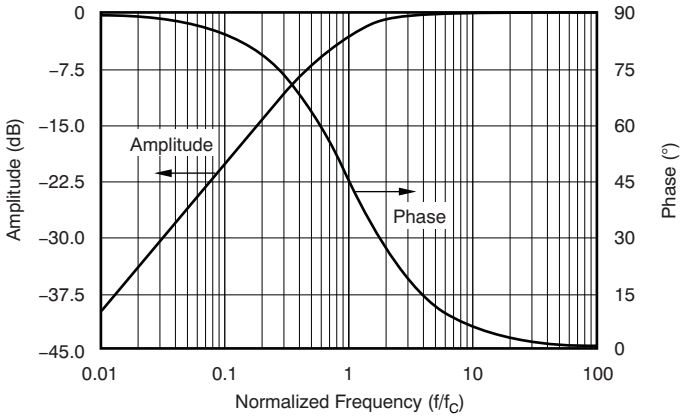


Figure 45. HPF Amplitude and Phase Response

8.3.14 Master Clock Input (CLK)

The ADS1282-SP requires a clock input for operation. The clock is applied to the CLK pin. The data conversion rate scales directly with the CLK frequency. Power consumption versus CLK frequency is relatively constant (see the *Typical Characteristics*).

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keep the clock trace as short as possible and use a 50-Ω series resistor close to the source.

8.3.15 Synchronization (SYNC Pin and Sync Command)

The ADS1282-SP can be synchronized to an external event, as well as synchronized to other ADS1282-SP devices if the sync event is applied simultaneously.

The ADS1282-SP has two sources for synchronization: the SYNC input pin and the SYNC command. The ADS1282-SP also has two synchronizing modes: Pulse-sync and Continuous-sync. In Pulse-sync mode, the ADS1282-SP synchronizes to a single sync event. In Continuous-sync mode, either a single SYNC event is used to synchronize conversions or a continuous clock is applied to the pin with a period equal to integer multiples of the data rate. When the periods of the sync input and the $\overline{\text{DRDY}}$ output do not match, the ADS1282-SP re-synchronizes and conversions are restarted.

8.3.16 Pulse-Sync Mode

In pulse-sync mode, the ADS1282-SP stops and restarts the conversion process when a sync event occurs (by pin or command). When the sync event occurs, the device resets the internal memory; $\overline{\text{DRDY}}$ goes high (pulse SYNC mode) otherwise in Continuous SYNC mode, $\overline{\text{DRDY}}$ continues to toggle, and after the digital filter has settled, new conversion data are available, as shown in Figure 46 and *Pulse-Sync Timing Requirements*.

Resynchronization occurs on the next rising CLK edge after the rising edge of the SYNC pin or after the eighth rising SCLK edge for opcode SYNC commands. To be effective, the SYNC opcode should be broadcast to all devices simultaneously.

8.3.17 Continuous-Sync Mode

In Continuous-sync mode, either a single sync pulse or a continuous clock may be applied. When a single sync pulse is applied (rising edge), the device behaves similar to the Pulse-sync mode. However, in this mode, $\overline{\text{DRDY}}$ continues to toggle unaffected but the DOUT output is held low until data are ready, 63 $\overline{\text{DRDY}}$ periods later. When the conversion data are non-zero, new conversion data are ready (as shown in Figure 46).

When a continuous clock is applied to the SYNC pin, the period must be an integral multiple of the output data rate or the device re-synchronizes. Synchronization results in the restarting of the digital filter and an interruption of 63 readings (refer to *Pulse-Sync Timing Requirements*).

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When the sync input is first applied, the device re-synchronizes (under the condition $t_{SYNC} \neq N / f_{DATA}$). $\overline{DRDY}$ continues to output but DOUT is held low until the new data are ready. Then, if SYNC is applied again and the period matches an integral multiple of the output data rate, the device freely runs without re-synchronization. The phase of the applied clock and output data rate ($\overline{DRDY}$) are not matched because of the initial delay of $\overline{DRDY}$ after SYNC is first applied. Figure 47 shows the timing for Continuous-Sync mode.

A SYNC clock input should be applied after the Continuous-Sync mode is set. The first rising edge of SYNC then causes a synchronization.

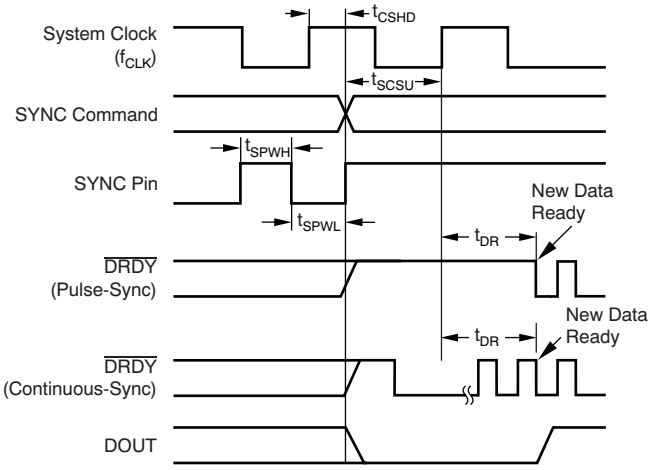


Figure 46. Pulse-Sync Timing, Continuous-Sync Timing With Single Sync

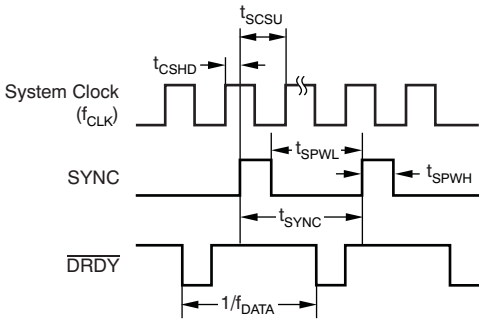


Figure 47. Continuous-Sync Timing With Sync Clock

8.3.18 Reset ($\overline{RESET}$ Pin and Reset Command)

The ADS1282-SP may be reset in two ways: toggle the $\overline{RESET}$ pin low or send a Reset command. When using the $\overline{RESET}$ pin, take it low and hold for at least $2 / f_{CLK}$ to force a reset. The ADS1282-SP is held in reset until the pin is released. By command, RESET takes effect on the next rising edge of f_{CLK} after the eighth rising edge of SCLK of the command. To ensure the Reset command can function, the SPI interface may require resetting itself; see *Serial Interface*.

In reset, registers are set to default and the conversions are synchronized on the next rising edge of CLK. New conversion data are available, as shown in Figure 48 and *Reset Timing Requirements*.

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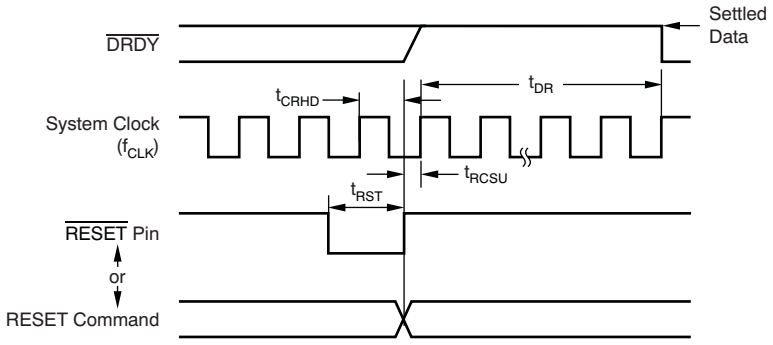


Figure 48. Reset Timing

8.3.19 Power-Down ($\overline{\text{PWDN}}$ Pin and Standby Command)

There are two ways to power-down the ADS1282-SP: take the $\overline{\text{PWDN}}$ pin low or send a Standby command. When the $\overline{\text{PWDN}}$ pin is pulled low, the internal circuitry is disabled to minimize power and the contents of the register settings are reset.

In power-down, the device outputs remain active and the device inputs must not float. When the Standby command is sent, the SPI port and the configuration registers are kept active. Figure 49 and Pulse-Sync Timing Requirements show the timing.

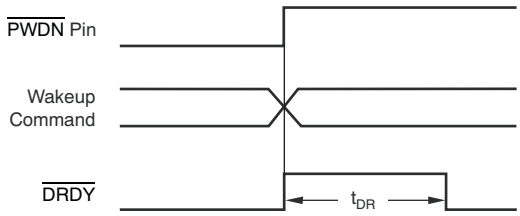


Figure 49. $\overline{\text{PWDN}}$ Pin and Wake-Up Command Timing (Pulse-Sync Timing Requirements Shows t_{DR})

8.3.20 Power-On Sequence

The ADS1282-SP has three power supplies: AVDD, AVSS, and DVDD. Figure 50 shows the power-on sequence of the ADS1282-SP. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate an internal reset whose outputs are summed to generate a global internal reset. After the supplies have crossed the minimum thresholds, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, new conversion data are available, as shown in Figure 50 and *Pulse-Sync Timing Requirements*.

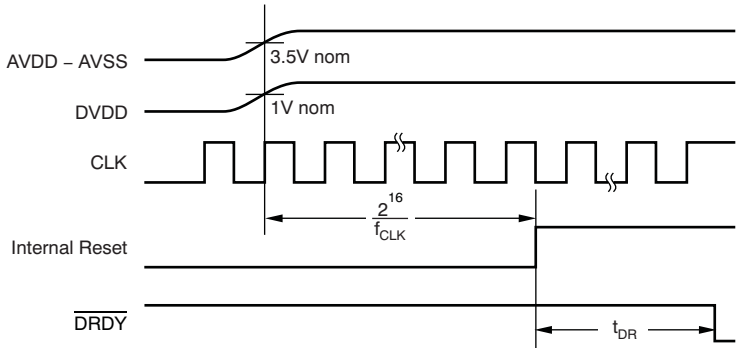


Figure 50. Power-On Sequence

8.3.21 Serial Interface

A serial interface is used to read the conversion data and access the configuration registers. The interface consists of three basic signals: SCLK, DIN, and DOUT. An additional output, $\overline{\text{DRDY}}$, transitions low in Read Data Continuous mode when data are ready for retrieval. Figure 51 shows the connection when multiple converters are used.

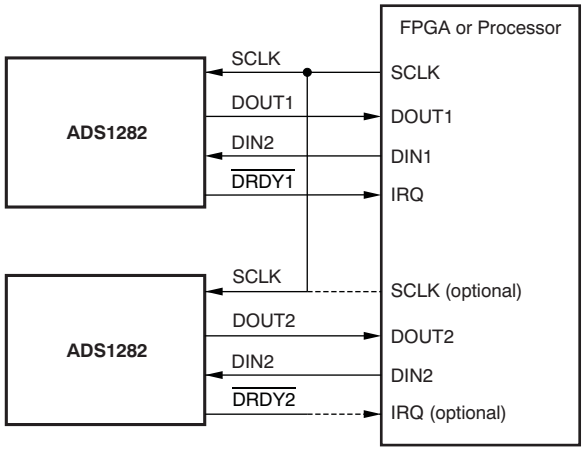


Figure 51. Interface for Multiple Devices

8.3.21.1 Serial Clock (SCLK)

The serial clock (SCLK) is an input that is used to clock data into (DIN) and out of (DOUT) the ADS1282-SP. This input is a Schmitt-trigger input that has a high degree of noise immunity. However, TI recommends keeping SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. If SCLK is held low for 64 $\overline{\text{DRDY}}$ cycles, data transfer or commands in progress terminate and the SPI interface resets. The next SCLK pulse starts a new communication cycle. This time-out feature can be used to recover the interface when a transmission is interrupted or SCLK inadvertently glitches. SCLK should remain low when not active.

8.3.21.2 Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADS1282-SP. Keep DIN low when reading conversion data in the Read Data Continuous mode (except when issuing a STOP Read Data Continuous command). Data on DIN are shifted into the converter on the rising edge of SCLK. In Pin mode, DIN is not used.

8.3.21.3 Data Output (DOUT)

The data output pin (DOUT) is used to output data from the ADS1282-SP. Data are shifted out on DOUT on the falling edge of SCLK.

8.3.21.4 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output; when it transitions low, this transition indicates new conversion data are ready, as shown in Figure 52. When reading data by the continuous mode, the data must be read within four CLK periods before $\overline{\text{DRDY}}$ goes low again or the data are overwritten with new conversion data. When reading data by the command mode, the read operation can overlap the occurrence of the next $\overline{\text{DRDY}}$ without data corruption.

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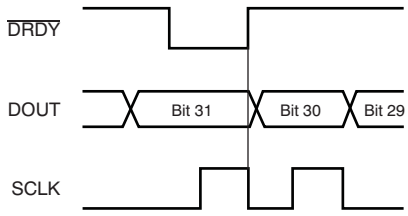


Figure 52. $\overline{\text{DRDY}}$ With Data Retrieval

$\overline{\text{DRDY}}$ resets high on the first falling edge of SCLK. Figure 52 and Figure 53 show the function of $\overline{\text{DRDY}}$ with and without data readback, respectively.

If data are not retrieved (no SCLK provided), $\overline{\text{DRDY}}$ pulses high for four f_{CLK} periods during the update time, as shown in Figure 53.

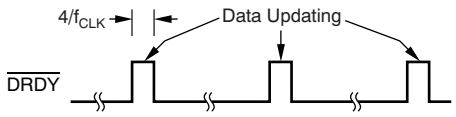


Figure 53. $\overline{\text{DRDY}}$ With No Data Retrieval

8.3.22 Data Format

The ADS1282-SP provides 32 bits of conversion data in binary twos complement format, as shown in Table 9. The LSB of the data is a redundant sign bit: '0' for positive numbers and '1' for negative numbers. However, when the output is clipped to +FS, the LSB = 1; when the output is clipped to –FS, the LSB = 0. If desired, the data readback may be stopped at 24 bits. In sinc filter mode, the output data are scaled by 1/2.

Table 9. Ideal Output Code Versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	32-BIT IDEAL OUTPUT CODE(1)	
	FIR FILTER	SINC FILTER(2)
$> \frac{V_{REF}}{2 \times PGA}$	7FFFFFFFh	(3)
$\frac{V_{REF}}{2 \times PGA}$	7FFFFFFEh	3FFFFFFFh
$\frac{V_{REF}}{2PGA \times (2^{30} - 1)}$	00000002h	00000001h
0	00000000h	00000000h
$\frac{-V_{REF}}{2PGA \times (2^{30} - 1)}$	FFFFFFFFh	FFFFFFFFh
$\frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000000h	(3)

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(1) Excludes effects of noise, linearity, offset, and gain errors.
(2) Due to the reduction in oversampling ratio (OSR) related to the sinc filter high data rates, full 32-bit available resolution is reduced.
(3) In sinc filter mode, the output does not clip at half-scale code when the full-scale range is exceeded.

8.3.23 Reading Data

The ADS1282-SP has two ways to read conversion data: Read Data Continuous and Read Data By Command.

8.3.23.1 Read Data Continuous

In the Read Data Continuous mode, the conversion data are shifted out directly from the device without the need for sending a read command. This mode is the default mode at power-on. This mode is also enabled by the RDATAC command. When $\overline{\text{DRDY}}$ goes low, indicating that new data are available, the MSB of data appears on DOUT, as shown in Figure 54. The data are normally read on the rising edge of SCLK, at the occurrence of the first falling edge of SCLK, $\overline{\text{DRDY}}$ returns high. After 32 bits of data have been shifted out, further SCLK transitions cause DOUT to go low. If desired, the read operation may be stopped at 24 bits. The data shift operation must be completed within four CLK periods before $\overline{\text{DRDY}}$ falls again or the data may be corrupted.

When a Stop Read Data Continuous command is issued, the $\overline{\text{DRDY}}$ output is blocked but the ADS1282-SP continues conversions. In stop continuous mode, the data can only be read by command.

8.3.23.2 Read Data by Command

The Read Data Continuous mode is stopped by the SDATAC command. In this mode, conversion data are read by command. In the Read Data By Command mode, a read data command must be sent to the device for each data conversion (as shown in Figure 55). When the read data command is received (on the eighth SCLK rising edge), data are available to read only when $\overline{\text{DRDY}}$ goes low (t_{DR}). When $\overline{\text{DRDY}}$ goes low, conversion data appear on DOUT. The data may be read on the rising edge of SCLK.

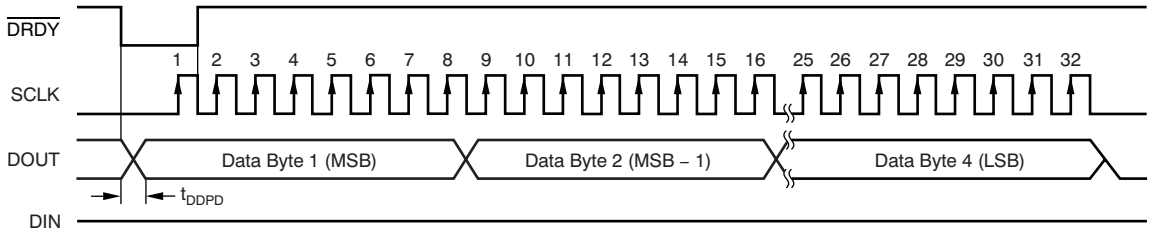


Figure 54. Read Data Continuous

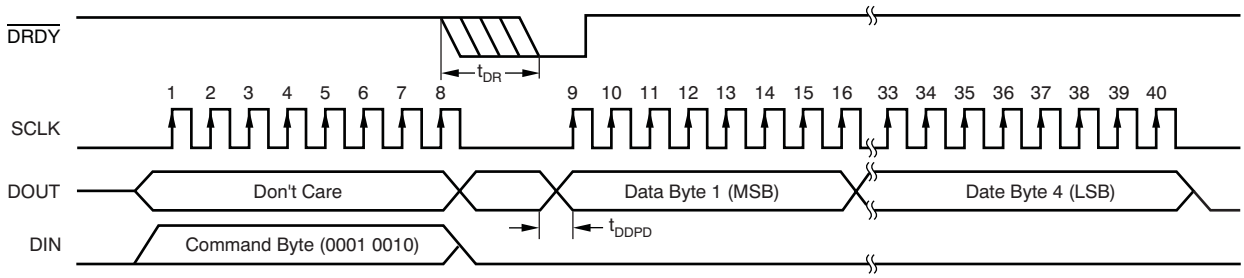


Figure 55. Read Data By Command, Rdata (T_{DDPD} Timing Is Given In *Read Data Timing Requirements*)

8.3.24 One-Shot Operation

The ADS1282-SP can perform very power-efficient, one-shot conversions using the STANDBY command while under software control. Figure 73 shows this sequence. First, issue the STANDBY command to set the Standby mode.

When ready to make a measurement, issue the WAKEUP command. Monitor $\overline{\text{DRDY}}$; when it goes low, the fully settled conversion data are ready and may be read directly in Read Data Continuous mode. Afterwards, issue another STANDBY command. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

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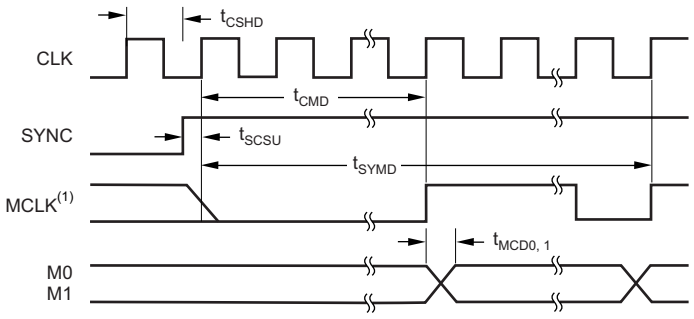
8.4 Device Functional Modes

8.4.1 Modulator Output Mode

The modulator digital stream output is accessible directly, bypassing and disabling the internal digital filter. The modulator output mode is activated by setting the CONFIG0 register bits FILTR[1:0] = 00. Pins M0 and M1 then become the modulator data outputs and the MCLK becomes the modulator clock output. When not in the modulator mode, these pins are inputs and must be tied.

The modulator output is composed of three signals: one output for the modulator clock (MCLK) and two outputs for the modulator data (M0 and M1). The modulator clock output rate is f_{MOD} (f_{CLK} / 4). The SYNC input resets the MCLK phase, as shown in Figure 56. The SYNC input is latched on the rising edge of CLK. The MCLK resets and the next rising edge of MCLK occurs five CLK periods later.

The modulator output data are two bits wide, which must be merged together before being filtered. Use the time domain equation of Equation 5 to merge the data outputs.



(1) MCLK = f_{CLK} / 4.

Figure 56. Modulator Mode Timing

Table 10. Modulator Output Timing for Figure 56

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MCD0}, 1	MCLK rising edge to M0, M1 valid propagation delay				100	ns
t_{CMD}	CLK rising edge (after SYNC rising edge) to MCLK rising edge CMD			5		1/f_{CLK}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge		10			ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge		10			ns
t_{SYMD}	SYNC to stable bit stream				16	1/f_{MOD}

8.5 Programming

8.5.1 Commands

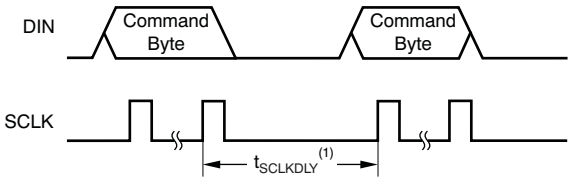
The commands listed in Table 11 control the operation of the ADS1282-SP. Most commands are stand-alone (that is, 1 byte in length); the register reads and writes require a second command byte in addition to the actual data bytes.

A delay of 24 f_{CLK} cycles between commands and between bytes within a command is required, starting from the last SCLK rising edge of one command to the first SCLK rising edge of the following command. This delay is shown in Figure 57.

In Read Data Continuous mode, the ADS1282-SP places conversion data on the DOUT pin as SCLK is applied. As a consequence of the potential conflict of conversion data on DOUT and data placed on DOUT resulting from a register or Read Data By Command operation, it is necessary to send a STOP Read Data Continuous command before Register or Data Read By Command. The STOP Read Data Continuous command disables the direct output of conversion data on the DOUT pin.

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Programming (continued)



(1) $t_{SCLKDLY} = 24/f_{CLK}$ (min).

Figure 57. Consecutive Commands

Table 11. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1st COMMAND BYTE(1)(2)	2nd COMMAND BYTE(3)
WAKEUP	Control	Wake-up from Standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter Standby mode	0000 001X (0 h or 03h)	
SYNC	Control	Synchronize the A/D conversion	0000 010X (04h or 5h)	
$\overline{\text{RESET}}$	Control	Reset registers to default values	0000 011X (06h or 07h)	
RDATAC	Control	Read data continuous	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* register(s) at address *rrrrr*(4)	00r rrrr (20h + 000r rrrr)	000n nnnn (00h + n nnnn)
WREG	Register	Write *nnnnn* register(s) at address *rrrrr*	010r rrrr (40h + 000r rrrr)	000n nnnn (00h + n nnnn)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = Don't care.
(2) rrrrr = starting address for register read and write commands.
(3) nnnnn = number of registers to be read/written – 1. For example, to read/write three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel Read Data Continuous mode before sending a command.

8.5.1.1 WAKEUP: Wake-Up from Standby Mode

This command is used to exit the standby mode. Upon sending the command, the time for the first data to be ready is illustrated in Figure 49 and Table 9. Sending this command during normal operation has no effect; for example, reading data by the Read Data Continuous method with DIN held low.

8.5.1.2 STANDBY: Standby Mode

This command places the ADS1282-SP into Standby mode. In Standby, the device enters a reduced power state where a low quiescent current remains to keep the register settings and SPI interface active. For complete device shutdown, take the $\overline{\text{PWDN}}$ pin low (register settings are not saved). To exit Standby mode, issue the WAKEUP command. The operation of Standby mode is shown in Figure 58.

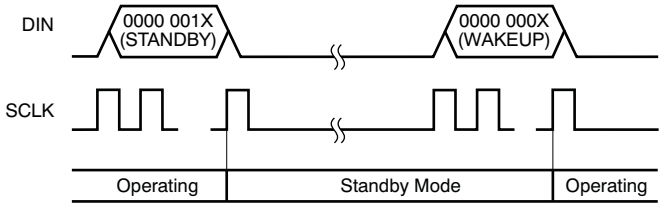


Figure 58. Standby Command Sequence

8.5.1.3 SYNC: Synchronize the A/D Conversion

This command synchronizes the A/D conversion. Upon receipt of the command, the reading in progress is cancelled and the conversion process is re-started. In order to synchronize multiple ADS1282-SPs, the command must be sent simultaneously to all devices. The SYNC pin must be high for this command.

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8.5.1.4 RESET: Reset the Device

The RESET command resets the registers to default values, enables the Read Data Continuous mode, and restarts the conversion process; the RESET command is functionally the same as the $\overline{\text{RESET}}$ pin. See Figure 48 for the RESET command timing.

8.5.1.5 RDATAC: Read Data Continuous

This command enables the Read Data Continuous mode (default mode). In this mode, conversion data can be read from the device directly without the need to supply a data read command. Each time $\overline{\text{DRDY}}$ falls low, new data are available to read. See *Read Data Continuous* for more details.

8.5.1.6 SDATAC: Stop Read Data Continuous

This command stops the Read Data Continuous mode. Exiting the Read Data Continuous mode is required before sending Register and Data read commands. This command suppresses the $\overline{\text{DRDY}}$ output, but the ADS1282-SP continues conversions.

8.5.1.7 RDATA: Read Data By Command

This command reads the conversion data. See *Read Data by Command* for more details.

8.5.1.8 RREG: Read Register Data

This command is used to read single or multiple register data. The command consists of a two-byte op-code argument followed by the output of register data. The first byte of the op-code includes the starting address, and the second byte specifies the number of registers to read – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to read.

Starting with the 16th falling edge of SCLK, the register data appear on DOUT.

The RREG command is illustrated in Figure 59. The a delay of 24 f_{CLK} cycles is required between each byte transaction.

8.5.1.9 WREG: Write to Register

This command writes single or multiple register data. The command consists of a two-byte op-code argument followed by the input of register data. The first byte of the op-code contains the starting address and the second byte specifies the number of registers to write – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to write.

Data byte(s): one or more register data bytes, depending on the number of registers specified.

Figure 60 illustrates the WREG command.

A delay of 24 f_{CLK} cycles is required between each byte transaction.

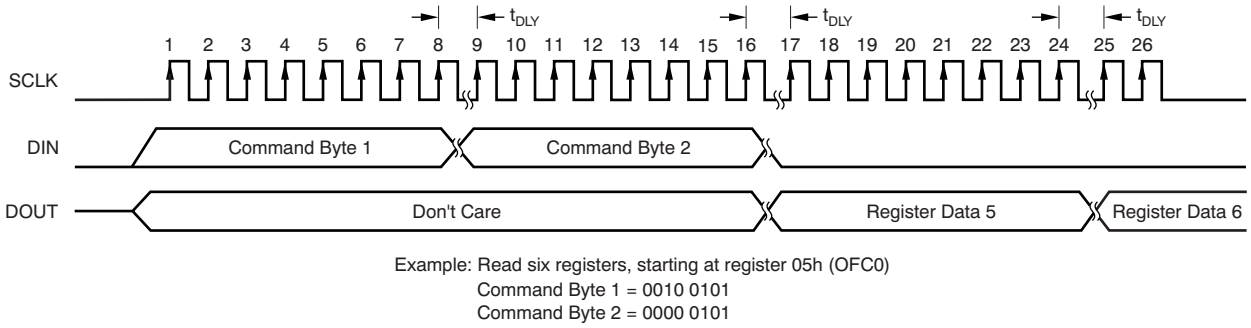
8.5.1.10 OFSCAL: Offset Calibration

This command performs an offset calibration. The inputs to the converter (or the inputs to the external pre-amplifier) should be zeroed and allowed to stabilize before sending this command. The offset calibration register updates after this operation. See *Calibration Commands* for more details.

8.5.1.11 GANCAL: Gain Calibration

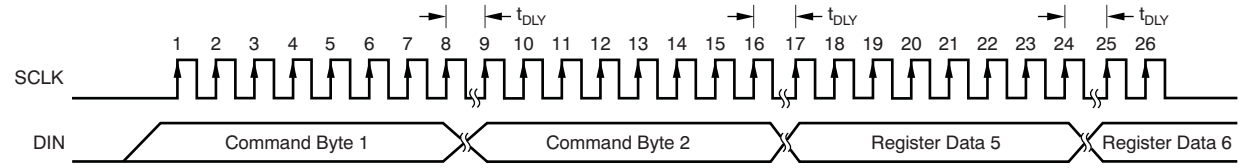
This command performs a gain calibration. The inputs to the converter should have a stable DC input, preferably close to (but not exceeding) positive full-scale. The gain calibration register updates after this operation. See *Calibration Commands* for more details.

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Example: Read six registers, starting at register 05h (OFC0)
Command Byte 1 = 0010 0101
Command Byte 2 = 0000 0101

Figure 59. Read Register Data (Equation 11 Shows t_{DLY})



Example: Write six registers, starting at register 05h (OFC0)
Command Byte 1 = 0100 0101
Command Byte 2 = 0000 0101

Figure 60. Write Register Data (Equation 11 Shows t_{DLY})

$$t_{DLY} = 24 / f_{CLK} \quad (11)$$

8.5.2 Calibration Commands

Calibration commands may be sent to the ADS1282-SP to calibrate the conversion data. The values of the offset and gain calibration registers are internally written to perform calibration. The appropriate input signals must be applied to the ADS1282-SP inputs before sending the commands. Use slower data rates to achieve more consistent calibration results; this effect is a byproduct of the lower noise that these data rates provide. Also, if calibrating at power-on, be sure the reference voltage is fully settled.

Figure 61 shows the calibration command sequence. After the analog input voltage (and reference) have stabilized, send the Stop Data Continuous command followed by the SYNC and Read Data Continuous commands. 64 data periods later, $\overline{\text{DRDY}}$ goes low. After $\overline{\text{DRDY}}$ goes low, send the Stop Data Continuous, then the Calibrate command followed by the Read Data Continuous command. After 16 data periods, calibration is complete and conversion data may be read at this time. The SYNC input must remain high during the calibration sequence.

The calibration commands apply to specific PGA settings. If the PGA is changed, recalibration is necessary. Calibration is bypassed in the sinc filter mode.

8.5.2.1 OFSCAL Command

The OFSCAL command performs an offset calibration. Before sending the offset calibration command, a *zero* input signal must be applied to the ADS1282-SP and the inputs allowed to stabilize. When the command is sent, the ADS1282-SP averages 16 readings and then writes this value to the OFC register. The contents of the OFC register may be subsequently read or written. During offset calibration, the full-scale correction is bypassed.

8.5.2.2 GANCAL Command

The GANCAL command performs a gain calibration. Before sending the GANCAL command, a DC input signal must be applied that is in the range of, but not exceeding, positive or negative full-scale. After the signal has stabilized, the command can be sent. The ADS1282-SP averages 16 readings, then computes the value that compensates for the gain error. The gain correction value is then written to the FSC register. The contents of the GANCAL register may be subsequently read or written. While the gain calibration command corrects for gain errors greater than 1 (gain correction <1), to avoid input overload, the analog inputs cannot exceed full-scale range. The gain calibration should be performed after the offset calibration.

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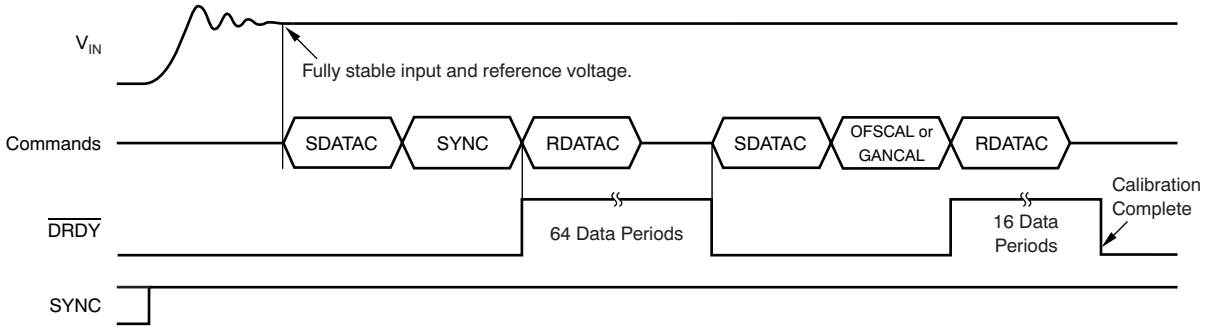


Figure 61. Offset/Gain Calibration Timing

8.5.3 User Calibration

System calibration of the ADS1282-SP can be performed without using the calibration commands. This procedure requires the calibration values to be externally calculated and then written to the calibration registers. The steps for this procedure are:

1. Set the OFSCAL[2:0] register = 0h and GANCAL[2:0] = 400000h. These values set the offset and gain registers to 0 and 1, respectively.
2. Apply a *zero* differential input to the input of the system. Wait for the system to settle and then average *n* output readings. Higher numbers of averaged readings result in more consistent calibration. Write the averaged value to the OFC register.
3. Apply a differential positive or negative DC signal, or an AC signal, less than the *full-scale* input to the system. Wait for the system to settle and then average the *n* output readings.

The value written to the FSC registers is calculated by Equation 12.

DC signal calibration is shown in Equation 12. The expected output code is based on 31-bit output data.

$$FSC[2:0] = 400000h \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \tag{12}$$

For AC signal calibration, use an RMS value of collected data (as shown in Equation 13).

$$FSC[2:0] = 400000h \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \tag{13}$$

8.5.4 Configuration Guide

After RESET or power-on, the registers can be configured using the following procedure:

1. **Reset the serial interface.** Before using the serial interface, it may be necessary to recover the serial interface (undefined I/O power-up sequencing may cause false SCLK detection). To reset the SPI interface, toggle the $\overline{\text{RESET}}$ pin or, when in Read Data Continuous mode, hold SCLK low for 64 $\overline{\text{DRDY}}$ periods.
2. **Configure the registers.** The registers are configured by either writing to them individually or as a group. Software may be configured in either mode. The SDATAC command must be sent before register read/write operations to cancel the Read Data Continuous mode.
3. **Verify register data.** The register may be read back for verification of device communications.
4. **Set the data mode.** After register configuration, the device may be configured for Read Data Continuous mode, either by the Read Data Continuous command or configured in Read Data By Register mode using SDATAC command.
5. **Synchronize readings.** Whenever SYNC is high, the ADS1282-SP freely runs the data conversions. To stop and re-sync the conversions, take SYNC low and then high.
6. **Read data.** If the Read Data Continuous mode is active, the data are read directly after $\overline{\text{DRDY}}$ falls by applying SCLK pulses. If the Read Data Continuous mode is inactive, the data can only be read by Read Data By Command. The Read Data opcode command must be sent in this mode to read each conversion result ($\overline{\text{DRDY}}$ only asserts after each read data command is sent).

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8.6 Register Maps

8.6.1 ADS1282-SP Register Map Information

Collectively, the registers contain all the information needed to configure the part, such as data rate, filter selection, calibration, and so forth. The registers are accessed by the RREG and WREG commands. The registers can be accessed individually or as a block of registers by sending or receiving consecutive bytes. After a register write operation the ADC resets, resulting in an interruption of 63 readings.

Table 12. ADS1282-SP Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	X0h	ID3	ID2	ID1	ID0	0	0	0	0
01h	CONFIG0	52h	SYNC	MODE	DR2	DR1	DR0	PHS	FILTR1	FILTR0
02h	CONFIG1	08h	0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

8.6.2 ID Register

Figure 62. ID: ID Register (Address 00h)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	Reserved			
				0	0	0	0

Reset value = X0h

Table 13. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	ID[3:0]			Factory-programmed identification bits (read-only)
3:0	Reserved			Always write '0'

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8.6.3 Configuration Registers

8.6.3.1 Configuration Register 0

Figure 63. CONFIG0: Configuration Register 0 (Address 01h)

7	6	5	4	3	2	1	0
SYNC	MODE	DR2	DR1	DR0	PHASE	FILTR1	FILTR0

Reset value = 52h

Table 14. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC			Synchronization mode 0: Pulse SYNC mode (default) 1: Continuous SYNC mode
6	MODE			1: High-resolution mode (default)
5:3	DR[2:0]			Data Rate Select(1) 000: 250SPS 001: 500SPS 010: 1000SPS (default) 011: 2000SPS 100: 4000SPS
2	PHASE			FIR Phase Response 0: Linear phase (default) 1: Minimum phase
1:0	FILTR[1:0]			Digital Filter Select Digital filter configuration 00: On-chip filter bypassed, modulator output mode 01: Sinc filter block only 10: Sinc + LPF filter blocks (default) 11: Sinc + LPF + HPF filter blocks

(1) Sample rate based on 4.096-Mhz clock.

8.6.3.2 Configuration Register 1

Figure 64. CONFIG1: Configuration Register 1 (Address 02h)

7	6	5	4	3	2	1	0
RSVD	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
0							

Reset value = 08h

Table 15. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Always write '0'
6:4	MUX[2:0]			MUX Select 000: AINP1 and AINN1 (default) 001: AINP2 and AINN2 010: Internal short via 400Ω 011:AINP1 and AINN1 connected to AINP2 and AINN2 100: External short to AINN2
3	CHOP			PGA Chopping Enable 0: PGA chopping disabled 1: PGA chopping enabled (default)
2:0	PGA[2:0]			PGA Gain Select 000: G = 1 (default) 001: G = 2 010: G = 4 011: G = 8 100: G = 16 101: G = 32 110: G = 64

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8.6.4 HPF1 and HPF0

These two bytes (high-byte and low-byte, respectively) set the corner frequency of the high-pass filter.

8.6.4.1 High-Pass Filter Corner Frequency, Low Byte

Figure 65. HPF0: High-Pass Filter Corner Frequency, Low Byte (Address 03h)

7	6	5	4	3	2	1	0
HP07	HP06	HP05	HP04	HP03	HP02	HP01	HP00

Reset value = 32h

8.6.4.2 High-Pass Filter Corner Frequency, High Byte

Figure 66. HPF1: High-Pass Filter Corner Frequency, High Byte (Address 04h)

7	6	5	4	3	2	1	0
HP15	HP14	HP13	HP12	HP11	HP10	HP09	HP08

Reset value = 03h

8.6.5 OFC2, OFC1, OFC0

These three bytes set the offset calibration value.

8.6.5.1 Offset Calibration, Low Byte

Figure 67. OFC0: Offset Calibration, Low Byte (Address 05h)

7	6	5	4	3	2	1	0
OC07	OC06	OC05	OC04	OC03	OC02	OC01	OC00

Reset value = 00h

8.6.5.2 Offset Calibration, Mid Byte

Figure 68. OFC1: Offset Calibration, Mid Byte (Address 06h)

7	6	5	4	3	2	1	0
OC15	OC14	OC13	OC12	OC11	OC10	OC09	OC08

Reset value = 00h

8.6.5.3 Offset Calibration, High Byte

Figure 69. OFC2: Offset Calibration, High Byte (Address 07h)

7	6	5	4	3	2	1	0
OC23	OC22	OC21	OC20	OC19	OC18	OC17	OC16

Reset value = 00h

8.6.6 FSC2, FSC1, FSC0

These three bytes set the full-scale calibration value.

8.6.6.1 Full-Scale Calibration, Low Byte

Figure 70. FSC0: Full-Scale Calibration, Low Byte (Address 08h)

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

Reset value = 00h

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8.6.6.2 Full-Scale Calibration, Mid Byte

Figure 71. FSC1: Full-Scale Calibration, Mid Byte (Address 09h)

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

Reset value = 00h

8.6.6.3 Full-Scale Calibration, High Byte

Figure 72. FSC2: Full-Scale Calibration, High Byte (Address 0Ah)

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

Reset value = 40h

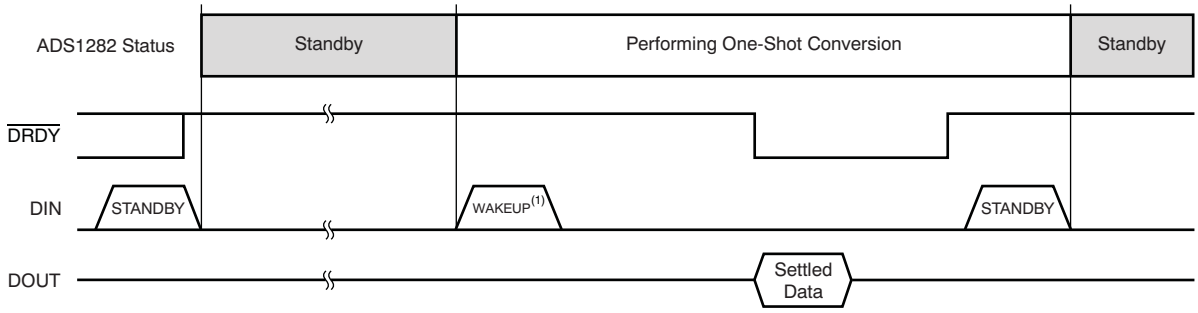
8.6.7 Offset and Full-Scale Calibration Registers

The conversion data can be scaled for offset and gain before yielding the final output code. As shown in Figure 74, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 14 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (14)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

The offset and full-scale calibrations apply to specific PGA settings. When the PGA changes, the contents of these registers may have to be recalculated. Calibration is bypassed in the sinc filter mode.



(1) See Figure 49 and Pulse-Sync Timing Requirements for time to new data.

Figure 73. One-Shot Conversions Using the Standby Command

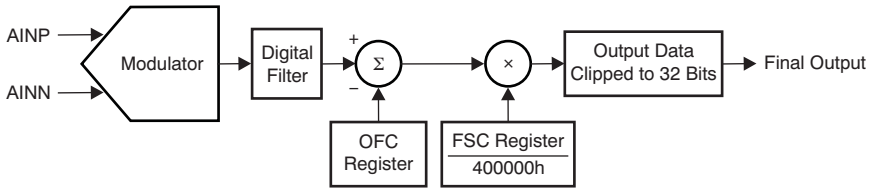


Figure 74. Calibration Block Diagram

8.6.7.1 OFC[2:0] Registers

The offset calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 18. The offset register is left-justified to align with the 32-bits of conversion data. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value). While the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 16), to avoid input overload, the analog inputs cannot exceed the full-scale range.

Table 16. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	80000000h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
800000h	7FFFFF00h

(1) Full 32-bit final output code with zero code input.

8.6.7.2 FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 19. The full-scale calibration value is 24-bit, straight offset binary, normalized to 1 at code 400000h. Table 17 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). While the gain calibration register value corrects gain errors greater than 1 (gain correction <1), the full-scale range of the analog inputs cannot be exceeded to avoid input overload.

Table 17. Full-Scale Calibration Register Values

FSC REGISTER	GAIN CORRECTION
800000h	2
400000h	1
200000h	0.5
000000h	0

Table 18. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	7	6	5	4	3	2	1	0 (LSB)
OFC1	MID	15	14	13	12	11	10	9	8
OFC2	MSB	23 (MSB)	22	21	20	19	18	17	16

Table 19. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	7	6	5	4	3	2	1	0 (LSB)
FSC1	MID	15	14	13	12	11	10	9	8
FSC2	MSB	23 (MSB)	22	21	20	19	18	17	16

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS1282-SP is a high-resolution ΔΣ ADC with space grade qualification making it an ideal candidate for space applications in temperature sensing, accelerometers, and precision instrumentation.

9.2 Typical Application

9.2.1 Thermocouple Temperature Sensing Application

Thermocouples are among the most commonly used sensors to measure temperature. Thermocouples work on the principle that two dissimilar metals placed in contact will generate an output voltage as a function of temperature as shown in Figure 75. This output voltage is proportional to the difference between the hot junction temperature and the cold junction temperature by a scaling factor (α) known as the Seeback coefficient. To ensure the measured output voltage accurately represents that generated by the hot junction the two junctions from where Vout is measured should remain at the same (cold junction) reference temperature. Therefore, in order to determine the temperature of the hot junction the thermocouple output voltage must be measured, the cold junction temperature known, and the voltage versus temperature characteristics (Seeback coefficient) for the type of thermocouple used be known.

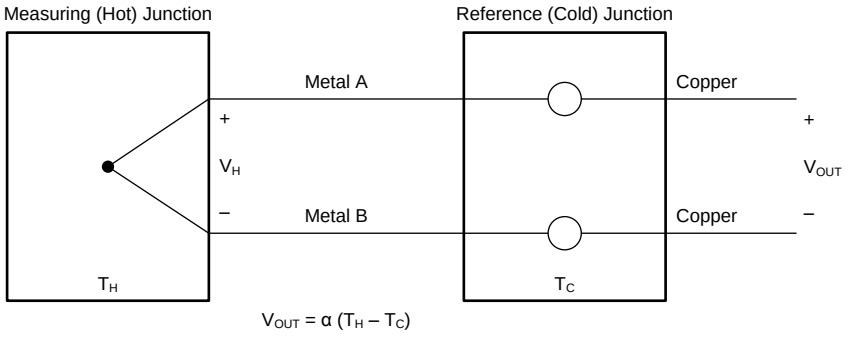


Figure 75. Basic Thermocouple Configuration

The output voltage of the common type thermocouples is very repeatable and well documented by the American National Institute of Standards (ANSI). Figure 76 shows the thermocouple output voltage versus temperature for the most common types of thermocouples. As the graph illustrates, the output voltage is relatively small, less than 90 mV across all types of thermocouples.

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Typical Application (continued)

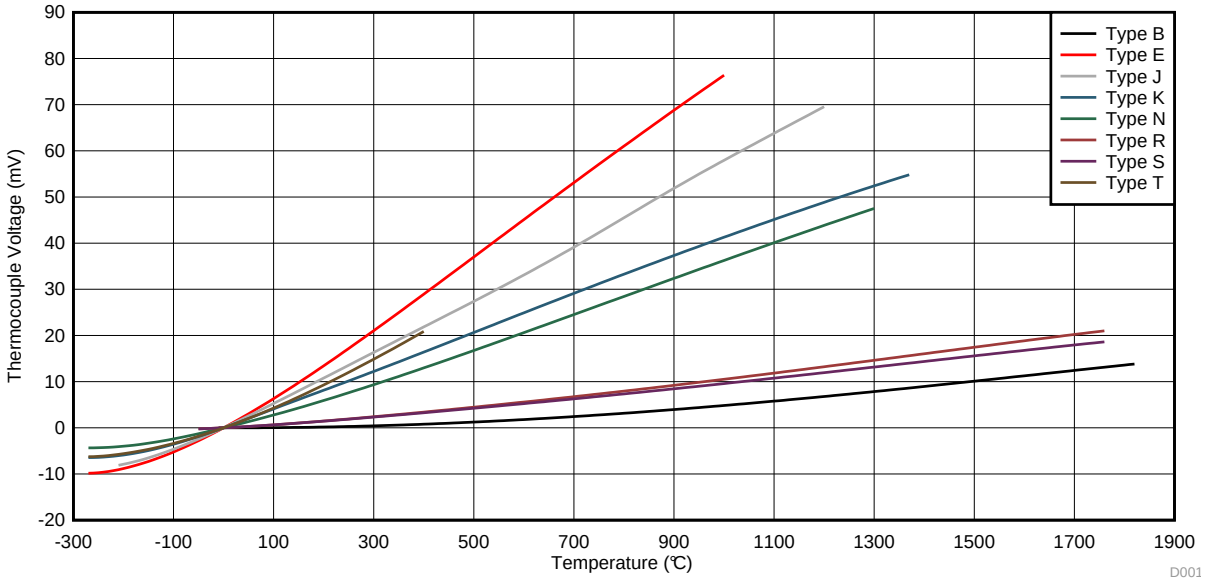


Figure 76. Thermocouple Voltage vs Temperature vs TC Type

9.2.1.1 Design Requirements

Since the output voltages of common thermocouple types are well documented, the accuracy of a thermocouple measurement reduces to accurately measuring the output voltage of the thermocouple at the cold junction and accurately determining the temperature at that cold junction. Once the cold junction temperature is determined, the output voltage can be compensated to reflect the actual hot junction temperature. This compensation can be implemented in hardware on the analog front-end or in software and/or firmware on the digital back-end, each of which presents its own challenges. Analog compensation is challenging in that any components used in compensation circuits are also potential sources of error while back-end digital compensation puts additional processing requirements and algorithms on the FPGA or microprocessor. The premise of this application writing is that cold junction compensation will be implemented in the digital domain so that minimal circuitry is used in the analog domain. With this, the front-end design goal becomes effectively digitizing the thermocouple output voltage as well as the cold junction temperature voltage.

The ADS1282-SP is ideal for achieving these goals as the device offers two analog inputs that are mux'd to one delta-sigma modulator. Figure 77 illustrates how one input receives the thermocouple output voltage while the second receives the cold junction compensation voltage. The Temp Sensor shown in the figure can take on many forms such as a temp sensor IC, an RTD, or a thermistor.

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Typical Application (continued)

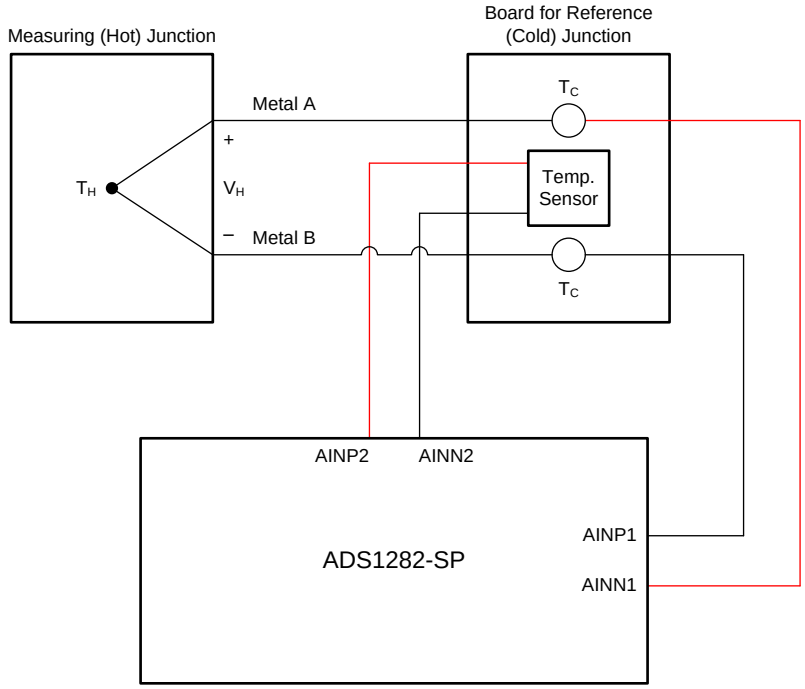


Figure 77. ADS1282-SP as Thermocouple DAQ

The ADS1282-SP offers a very high dynamic range. To realize this dynamic range, however, the small thermocouple voltage requires amplification to make use of the full scale range (FSR) of the ADC. The integrated programmable gain amplifier (PGA) provides this amplification in factors of 1x to 64x (in powers of 2) making the ADS1282-SP versatile for use with different types of thermocouples.

In addition to amplification, the analog input should be filtered. Filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from becoming a part of the measurement. As with any sampled system, aliasing can occur if proper anti-alias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as modulator frequency f(MOD), as shown in Figure 78. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

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Typical Application (continued)

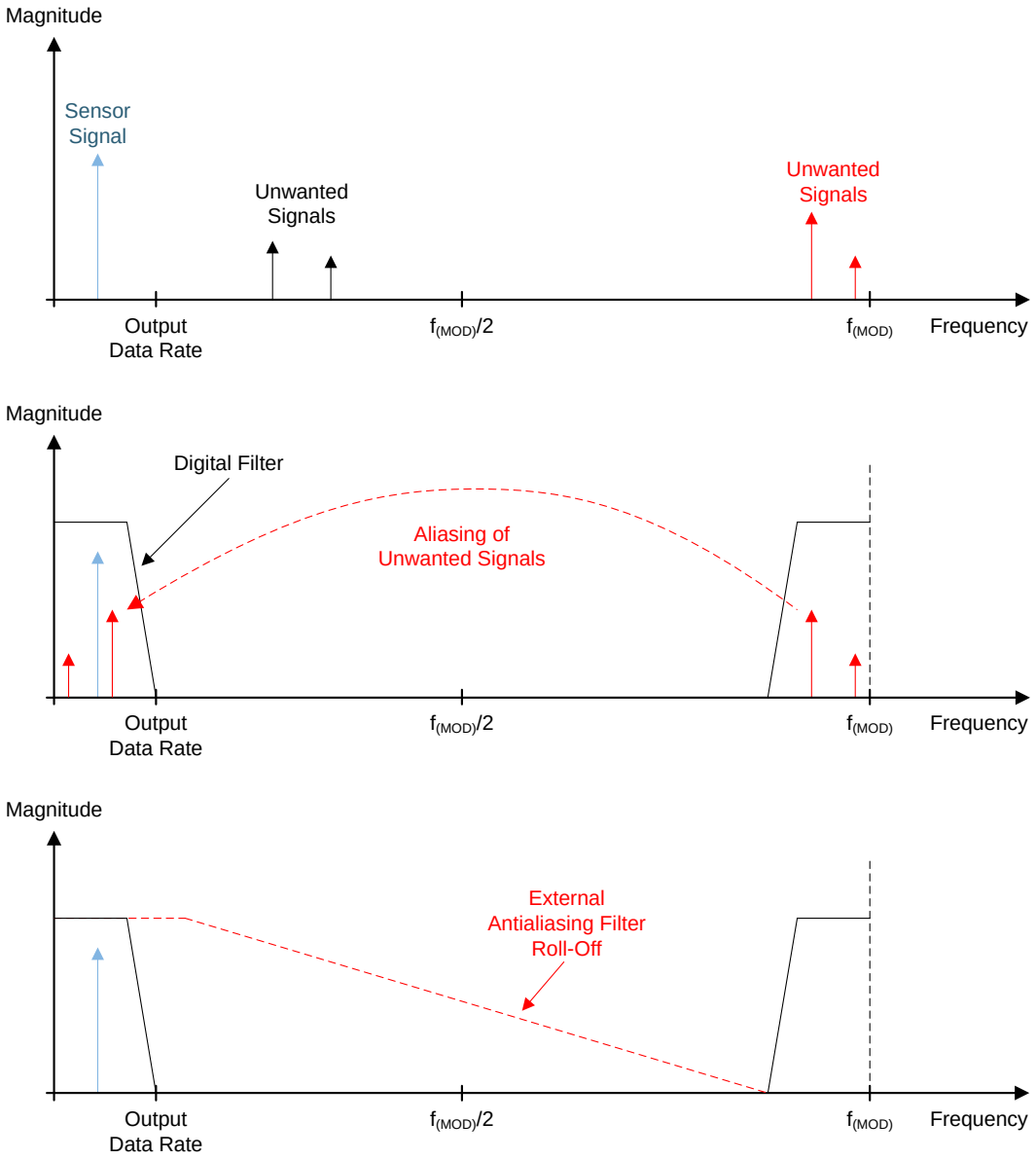


Figure 78. Effect of Aliasing

Many sensor signals, such as the thermocouple, are inherently band-limited; the output has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and RF transceivers. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result. A first-order, resistor-capacitor (RC) filter is, in most cases, sufficient to either eliminate such noise, or to reduce the effects to a level within the noise floor of the sensor.

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Typical Application (continued)

9.2.1.2 Detailed Design Procedure

Figure 79 below shows a typical thermocouple application utilizing both analog inputs to the ADS1282-SP; one for hot junction and one for cold junction. The biasing resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input is pulled to AVDD and the negative input is pulled to GND. The ADC consequently reads a full-scale value that is outside the normal measurement range of the thermocouple voltage to indicate this failure condition. When choosing the values of the biasing resistors, take care so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

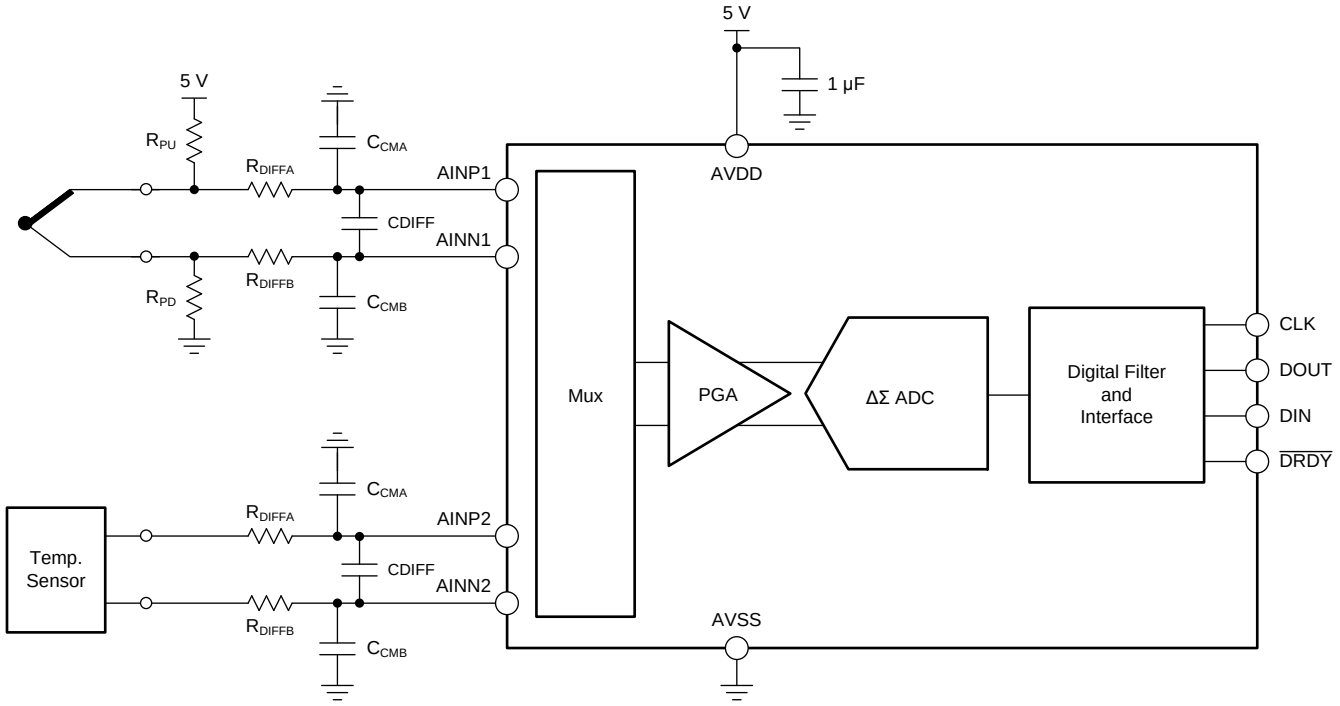


Figure 79. ADS1282-SP with Hot and Cold Junction Sensing

Although the device digital filter attenuates high-frequency components of noise, provide a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by RDIFFA, RDIFFB, and the differential capacitor CDIFF offers a cutoff frequency that is calculated using Equation 15. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. Limit the filter resistor values to below 1 kΩ for best performance.

$$fC = 1 / [2\pi \times (RDIFFA + RDIFFB) \times CDIFF] \quad (15)$$

Two common-mode filter capacitors (CCMA and CCMB) are also added to offer attenuation of high-frequency, common-mode noise components. Differential capacitor CDIFF must be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. For a type K thermocouple, the maximum thermocouple voltage (VTC) occurs at a thermocouple temperature (TTC) of 1370°C. At this temperature, VTC = 54.819 mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature (TCJ) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple

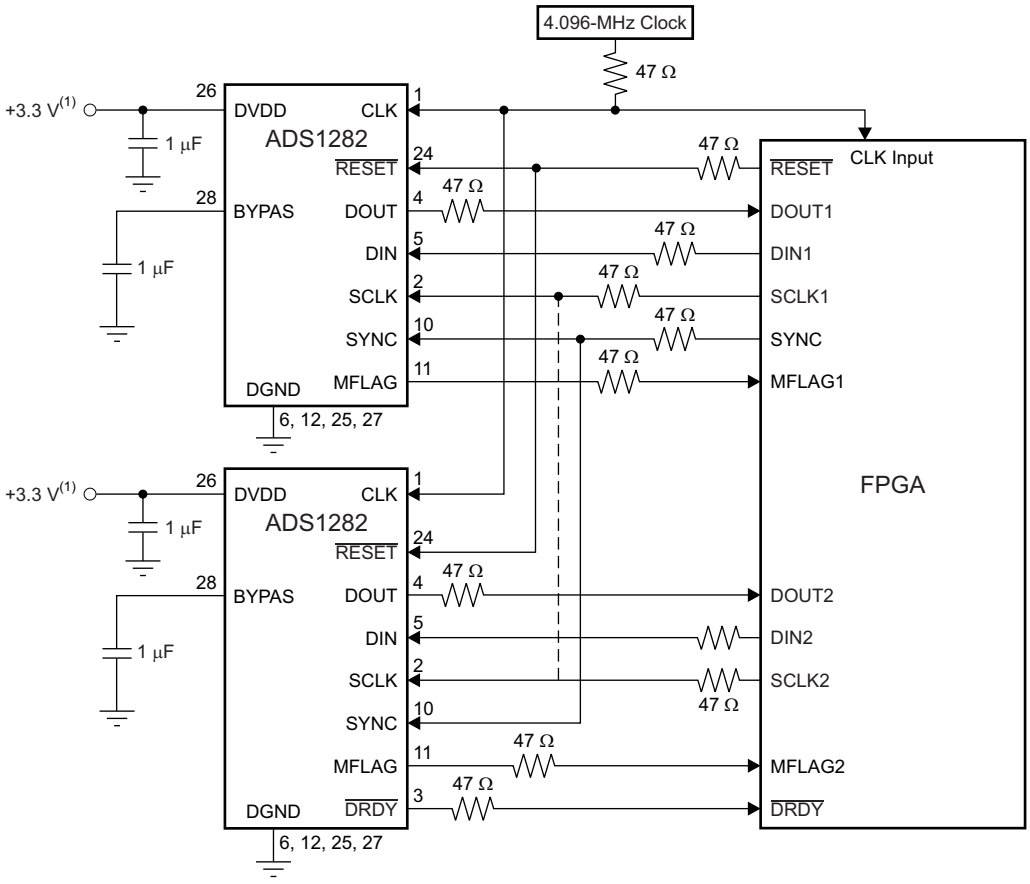
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Typical Application (continued)

produces a voltage larger than 54.819 mV. The isothermal block area is often constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –55°C. A K-type thermocouple at TTC = 1370°C produces an output voltage of VTC = 54.819 mV – (–2.067 mV) = 56.886 mV when referenced to a cold-junction temperature of TCJ = –55°C. When invoking the 64x amplification in the PGA the device offers a full-scale range of 70.3 mVpp-diff (with a reference of 4.5 V) allowing for nearly full utilization of the FSR with no additional external amplification required.

9.2.2 Digital Connection to a Field Programmable Gate Array (FPGA) Device Typical Application

Figure 80 shows the digital connection to a field programmable gate array (FPGA) device. In this example, two ADS1282-SP devices are shown connected. The $\overline{\text{DRDY}}$ output from each ADS1282-SP device can be used; however, when the devices are synchronized, the $\overline{\text{DRDY}}$ output from only one device is sufficient. A shared SCLK line between the devices is optional.



NOTE: Dashed line is optional.

(1) For DVDD < 2.25 V, see the *Power Supply Recommendations*.

Figure 80. Microcontroller Interface With Dual ADS1282-SPs

9.2.2.1 Design Requirements

It is critical to match the DVDD input and output thresholds of the ADS1282 to the IO voltage of the FPGA. The FPGA outputs with correct VOH and VOL levels must be compatible with VIH/VIL levels of ADS1282 utilizing respective DVDD voltage. Conversely the FPGA input thresholds must also be compatible with VOH/VOL levels of DVDD range of ADS1282. The wide DVDD range of the ADS1282 allows easy interfacing to 1.8-V, 2.5-V, and 3.3-V logic levels. If DVDD is less than 2.25, then the BYPAS pin must be directly connected to DVDD to BYPAS internal LDO.

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Typical Application (continued)

9.2.2.2 Detailed Design Procedure

The modulator over-range flag (MFLAG) from each device ties to the FPGA. For synchronization, one SYNC control line connects all ADS1282-SP devices. The RESET line also connects to all ADS1282-SP devices.

For best performance, the FPGA and the ADS1282-SPs should operate from the same clock. Avoid ringing on the digital inputs. 47-Ω resistors in series with the digital traces can help to reduce ringing by controlling impedances. Place the resistors at the source (driver) end of the trace. Unused digital inputs should not float; use pullups or pulldowns to DVDD or GND. This includes the modulator data pins, M0, M1, and MCLK.

Placement and layout of multiple ADS1282s should be done to allow digital and analog signals to be separated and not cross to minimize coupling of noise from digital signals to analog signals and prevent ground loops. FPGA firmware can monitor DRDY to initiate SPI transactions to obtain samples from both ADS1282s. Additional monitoring of MFLAG can be done to take appropriate action if signal is overrange.

10 Power Supply Recommendations

Bypass all supply pins with 1-µF ceramic capacitors. In order to minimize the lead and trace inductance, place the capacitors as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition to power supplies, the device has a reference supply at pins VREFP and VREFN that should also be bypassed. Bypass these pins with at least a 1-µF capacitor as higher value capacitors yield superior low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors and place as close as possible to the device pins.

The DVDD power supply operates over the range of 1.75 to 3.6 V. If DVDD is operated at less than 2.25 V, connect the DVDD pin to the BYPAS pin. If DVDD is greater than or equal to 2.25 V, do not connect DVDD to the BYPAS pin. Figure 81 shows this connection.

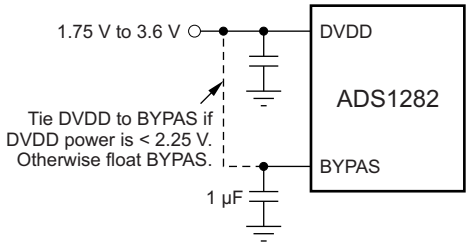


Figure 81. DVDD Power

11 Layout

11.1 Layout Guidelines

In any mixed-signal system design, the power-supply and grounding design plays a significant role. The device distinguishes between two different grounds: AVSS (analog ground) and DGND (digital ground). In low frequency applications such as temperature sensing with thermocouples, laying out the printed circuit board (PCB) to use a single ground plane is adequate but care must be taken so that ground loops are avoided. Ground loops act as loop antennas picking up interference currents which transform into voltage fluctuations. These fluctuations are effectively noise which can degrade system performance in high resolution applications. When placing components and routing over the ground plane, pay close attention to the path that ground currents will take. Avoid having return currents for digital functions pass close to analog sensitive devices or traces.

Additionally, the proximity of digital devices to an analog signal chain has the potential to induce unwanted noise into the system. One primary source of noise is the switching noise from any digital circuitry such as the data output serializer or the microprocessor receiving the data. For the device, care must be taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductances of the supply and ground pins results in better noise suppression. For this reason, multiple pins are used to connect to the digital ground. Low inductance properties must be maintained throughout the design of the PCB layout by use of proper planes and layer thickness.

To avoid noise coupling through supply pins, TI recommends to keep sensitive input pins (such as AINN1, AINP1, AINN2, AINP2 pins) away from the DVDD and DGND planes. For example, do not route the traces or vias connected to these pins across these planes; that is, avoid the digital power planes under the analog input pins. An exception may be acceptable to share DGND and AVSS when utilizing a unipolar supply for AVDD. As in the example below, DGND is shared with AVSS. Care should be taken to minimize inductance and route digital signals away from analog section.

The analog inputs represent the most sensitive node of the ADC as the total system accuracy depends on the how well the integrity of this signal is maintained. The analog differential inputs to the ADC should be routed tightly coupled and symmetrical for common mode rejection. These inputs should be as short in length as possible to minimize exposure to potential sources of noise.

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11.2 Layout Example

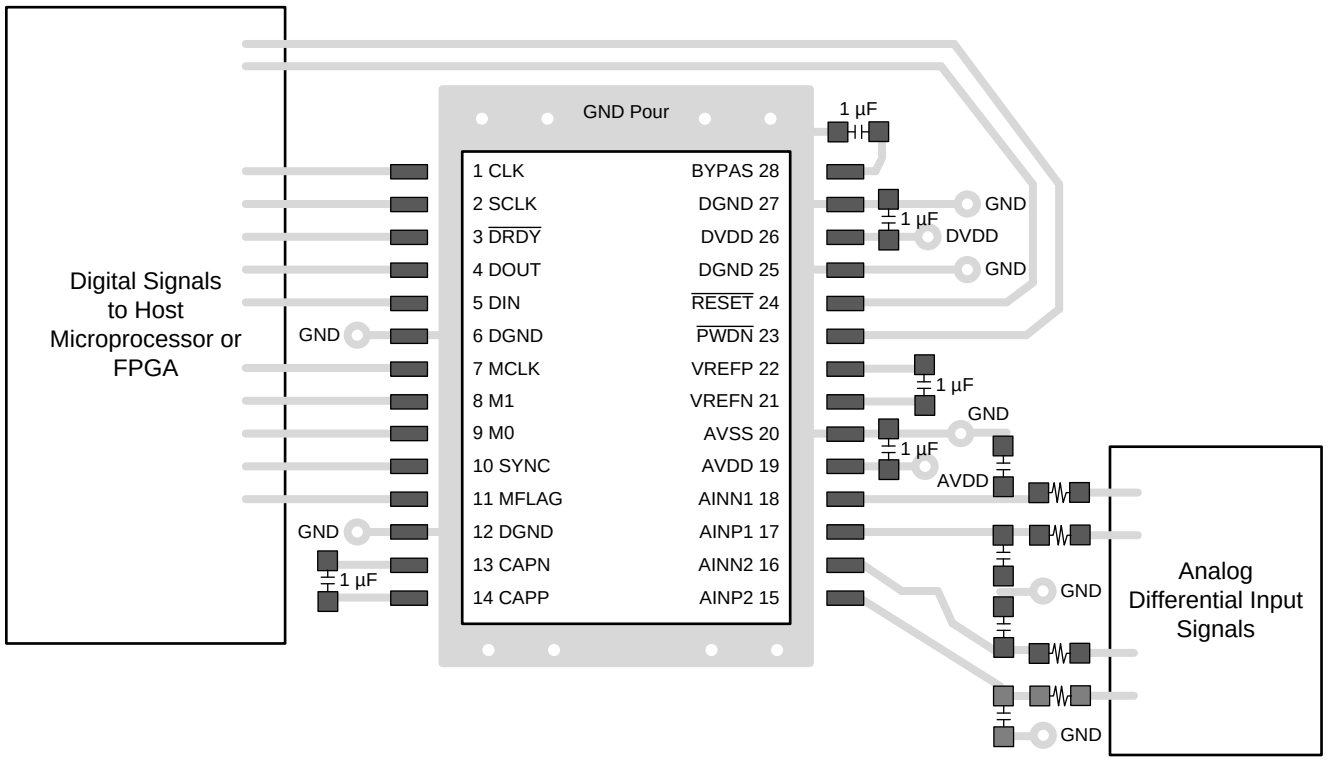


Figure 82. Unipolar Layout Example

12 器件和文档支持

12.1 器件支持

表 **20. FIR** 级系数

系数	第 **1** 部分	第 **2** 部分	第 **3** 部分		第 **4** 部分	
	换算系数 **= 1 / 8388608**		换算系数 **= 134217728**		换算系数 **= 134217728**	
			线性相位	最小相位	线性相位	最小相位
b_0	–10944	–774	–73	819	–132	11767
b_1	0	0	–874	8211	–432	133882
b_2	103807	8994	–4648	44880	–75	769961
b_3	0	0	–16147	174712	2481	2940447
b_4	–507903	–51663	–41280	536821	6692	8262605
b_5	0	0	–80934	1372637	7419	17902757
b_6	2512192	199523	–120064	3012996	–266	30428735
b_7	4194304	0	–118690	5788605	–10663	40215494
b_8	2512192	–629120	–18203	9852286	–8280	39260213
b_9	0	0	224751	14957445	10620	23325925
b_{10}	–507903	2570188	580196	20301435	22008	–1757787
b_{11}	0	4194304	893263	24569234	348	–21028126
b_{12}	103807	2570188	891396	26260385	–34123	–21293602
b_{13}	0	0	293598	24247577	–25549	–3886901
b_{14}	–10944	–629120	–987253	18356231	33460	14396783
b_{15}		0	–2635779	9668991	61387	16314388
b_{16}		199523	–3860322	327749	–7546	1518875
b_{17}		0	–3572512	–7171917	–94192	–12979500
b_{18}		–51663	–822573	–10926627	–50629	–11506007
b_{19}		0	4669054	–10379094	101135	2769794
b_{20}		8994	12153698	–6505618	134826	12195551
b_{21}		0	19911100	–1333678	–56626	6103823
b_{22}		–774	25779390	2972773	–220104	–6709466
b_{23}			27966862	5006366	–56082	–9882714
b_{24}			只显示一半；从 b_{22} 开始对称。	4566808	263758	–353347
b_{25}				2505652	231231	8629331
b_{26}				126331	–215231	5597927
b_{27}				–1496514	–430178	–4389168
b_{28}				–1933830	34715	–7594158
b_{29}				–1410695	580424	–428064
b_{30}				–502731	283878	6566217
b_{31}				245330	–588382	4024593
b_{32}				565174	–693209	–3679749
b_{33}				492084	366118	–5572954
b_{34}				231656	1084786	332589
b_{35}				–9196	132893	5136333
b_{36}				–125456	–1300087	2351253
b_{37}				–122207	–878642	–3357202
b_{38}				–61813	1162189	–3767666
b_{39}				–4445	1741565	1087392
b_{40}				22484	–522533	3847821
b_{41}				22245	–2490395	919792

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器件支持 (接下页)

表 20. FIR 级系数 (接下页)

系数	第 1 部分	第 2 部分	第 3 部分		第 4 部分	
	换算系数 = 1 / 8388608		换算系数 = 134217728		换算系数 = 134217728	
			线性相位	最小相位	线性相位	最小相位
b_{42}				10775	–688945	–2918303
b_{43}				940	2811738	–2193542
b_{44}				–2953	2425494	1493873
b_{45}				–2599	–2338095	2595051
b_{46}				–1052	–4511116	–79991
b_{47}				-43	641555	–2260106
b_{48}				214	6661730	–963855
b_{49}				132	2950811	1482337
b_{50}				33	–8538057	1480417
b_{51}					–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					只显示一半；从 b_{53} 开始对称。	644405
b_{56}						–675082
b_{57}						–806095
b_{58}						211391
b_{59}						740896
b_{60}						141976
b_{61}						–527673
b_{62}						–327618
b_{63}						278227
b_{64}						363809
b_{65}						–70646
b_{66}						–304819
b_{67}						–63159
b_{68}						205798
b_{69}						124363
b_{70}						–107173
b_{71}						–131357
b_{72}						31104
b_{73}						107182
b_{74}						15644
b_{75}						–71728
b_{76}						–36319
b_{77}						38331
b_{78}						38783
b_{79}						–13557
b_{80}						–31453
b_{81}						–1230
b_{82}						20983
b_{83}						7729
b_{84}						–11463
b_{85}						–8791

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器件支持 (接下页)

表 20. FIR 级系数 (接下页)

系数	第 1 部分	第 2 部分	第 3 部分		第 4 部分	
	换算系数 = 1 / 8388608		换算系数 = 134217728		换算系数 = 134217728	
			线性相位	最小相位	线性相位	最小相位
b_{86}						4659
b_{87}						7126
b_{88}						–732
b_{89}						–4687
b_{90}						–976
b_{91}						2551
b_{92}						1339
b_{93}						–1103
b_{94}						–1085
b_{95}						314
b_{96}						681
b_{97}						16
b_{98}						–349
b_{99}						–96
b_{100}						144
b_{101}						78
b_{102}						-46
b_{103}						–42
b_{104}						9
b_{105}						16
b_{106}						0
b_{107}						-4

$$\text{HPF Gain} = \frac{1 + \sqrt{1 - 2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}}{2 - \left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)} \tag{16}$$

有关该公式的使用示例，请参见*HPF Stage*。

12.1.1 HPF 传递函数

$$\text{HPF}(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \tag{17}$$

其中，*b* 的计算公式如公式 18 所示：

$$b = \frac{\left(1 + (1 - a)^2\right)^2}{2} \tag{18}$$

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表 **21.** 数据就绪时间 t_{DR}（正弦滤波器）

f_{DATA}	f_{CLK} (1)
128k	440
64k	616
32k	968
16k	1672
8k	2824

(1) 对于同时有同步命令和唤醒命令的情况，f_{CLK} = 从第八个 SCLK 上升沿后紧接着的下一个 CLK 上升沿到 DRDY 下降沿的 CLK 周期数。对于仅有唤醒命令的情况，减去两个 f_{CLK} 周期。

表 21 被*Pulse-Sync Timing Requirements*引用。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962L1423101VXC	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	5962L1423101VXC ADS1282-SP
5962L1423101VXC.A	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	5962L1423101VXC ADS1282-SP
5962L1423102VXC	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 115	5962L1423102VXC ADS1282-SP
5962L1423102VXC.A	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 115	5962L1423102VXC ADS1282-SP
ADS1282HKV/EM	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	25 to 25	ADS1282HKV/EM EVAL ONLY
ADS1282HKV/EM.A	Active	Production	CFP (HKV) | 28	25 | TUBE	Yes	AU	N/A for Pkg Type	25 to 25	ADS1282HKV/EM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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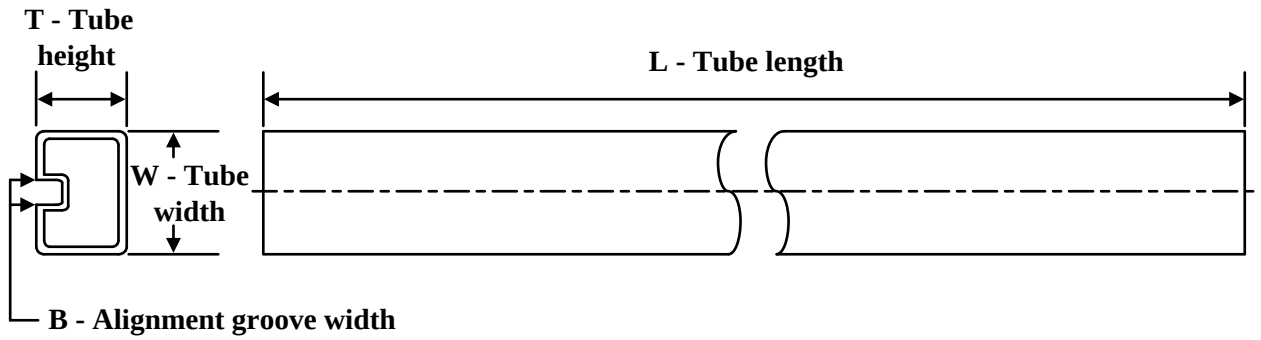
OTHER QUALIFIED VERSIONS OF ADS1282-SP :

- Catalog : ADS1282

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

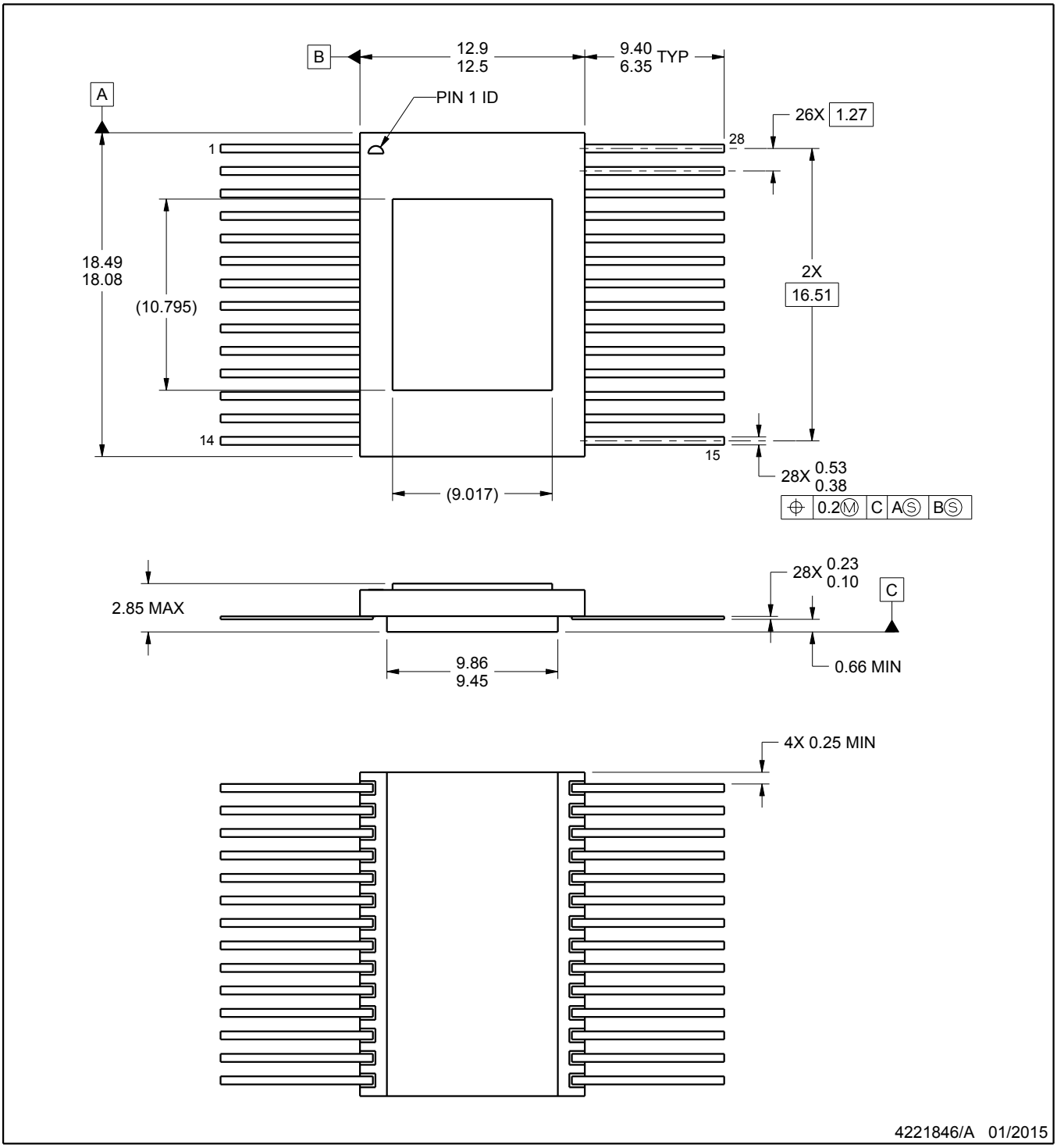
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962L1423101VXC	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA
5962L1423101VXC.A	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA
5962L1423102VXC	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA
5962L1423102VXC.A	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA
ADS1282HKV/EM	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA
ADS1282HKV/EM.A	HKV	CFP (TBAR)	28	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKV0028A

CFP - 2.85 mm max height

CERAMIC DUAL FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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