ADC16DV160 Dual Channel, 16-Bit, 160 MSPS Analog-to-Digital Converter with DDR LVDS Outputs

Check for Samples: ADC16DV160

FEATURES

- **Low Power Consumption**
- **On-Chip Precision Reference and Sample-and-Hold Circuit**
- **On-Chip Automatic Calibration During Power-Up**
- **Dual Data Rate LVDS Output Port**
- **Dual Supplies: 1.8V and 3.0V Operation**
- **Selectable Input Range: 2.4 and 2.0 V_{PP}**
- **Sampling Edge Flipping with Clock Divider by 2 Option**
- **Internal Clock Divide by 1 or 2**
- **On-Chip Low Jitter Duty-Cycle Stabilizer**
- **Power-Down and Sleep Modes**
- **Output Fixed Pattern Generation**
- **Output Clock Position Adjustment**
- **3-Wire SPI**
- **Offset Binary or 2's Complement Data Format**
- **68-Pin VQFN Package (10x10x0.8, 0.5mm Pin-Pitch)**

KEY SPECIFICATIONS

- **Resolution: 16 Bits**
- **Conversion Rate: 160 MSPS**
- **SNR (@FIN = 30 MHz): 78 dBFS (typ)**
- **SNR (@FIN = 197 MHz): 76 dBFS (typ)**
- **SFDR (@FIN = 30 MHz): 95 dBFS (typ)**
- **SFDR (@FIN = 197 MHz): 89 dBFS (typ)**
- **Full Power Bandwidth: 1.4 GHz (typ)**
- **Power Consumption:**
  - **Core per channel: 612 mW (typ)**
  - **LVDS Driver: 117 mW (typ)**
  - **Total: 1.3W (typ)**
- **Operating Temperature Range (-40°C ~ 85°C)**

APPLICATIONS

- **Multi-carrier, Multi-standard Base Station Receivers**
  - **MC-GSM/EDGE, CDMA2000, UMTS, LTE and WiMAX**
- **High IF Sampling Receivers**
- **Diversity Channel Receivers**
- **Test and Measurement Equipment**
- **Communications Instrumentation**
- **Portable Instrumentation**

DESCRIPTION

The ADC16DV160 is a monolithic dual channel high performance CMOS analog-to-digital converter capable of converting analog input signals into 16-bit digital words at rates up to 160 Mega Samples Per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and external component count while providing excellent dynamic performance. Automatic power-up calibration enables excellent dynamic performance and reduces part-to-part variation, and the ADC16DV160 can be re-calibrated at any time through the 3-wire Serial Peripheral Interface (SPI). An integrated low noise and stable voltage reference and differential reference buffer amplifier eases board level design. The on-chip duty cycle stabilizer with low additive jitter allows a wide range of input clock duty cycles without compromising dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.4 GHz. The interface between the ADC16DV160 and a receiver block can be easily verified and optimized via fixed pattern generation and output clock position features. The digital data is provided via dual data rate LVDS outputs – making possible the 68-pin, 10 mm x 10 mm VQFN package. The ADC16DV160 operates on dual power supplies of +1.8V and +3.0V with a power-down feature to reduce power consumption to very low levels while allowing fast recovery to full operation.

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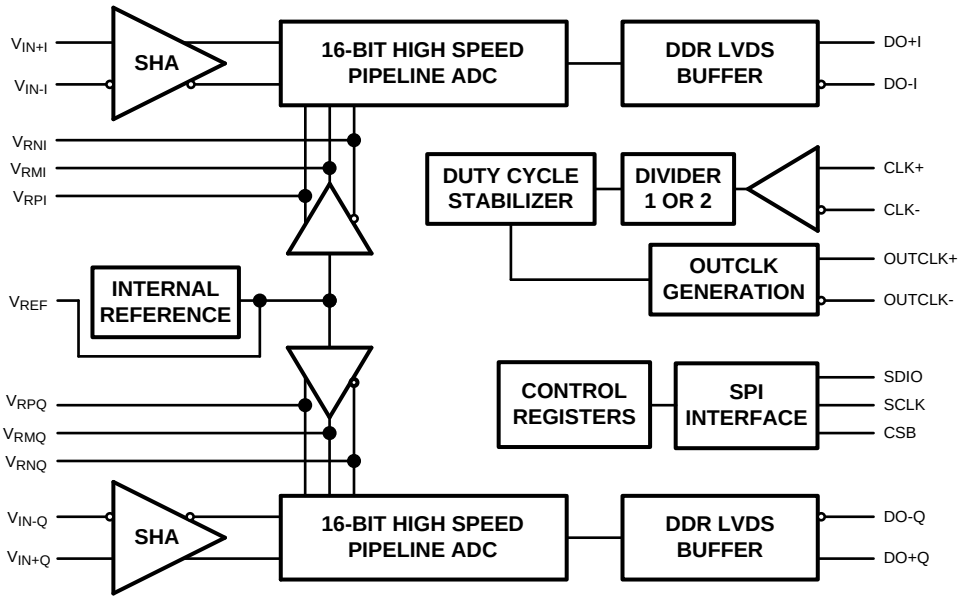


Figure 1. Functional Block Diagram

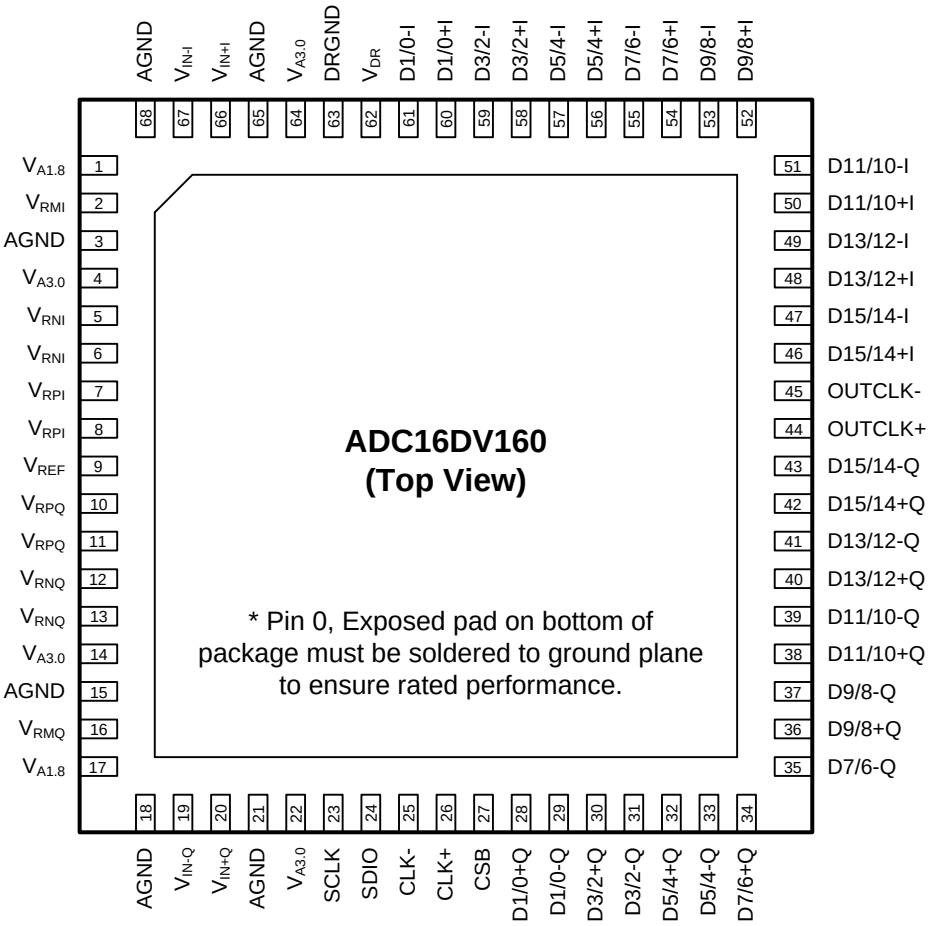


Figure 2. Pin-Out of ADC16DV160
See Package Number NKE0068A

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PIN DESCRIPTIONS

Pin(s)	Name	Type	Function and Connection
ANALOG I/O			
66 20	V_{IN+I} V_{IN+Q}	Input	Differential analog input pins. The differential full-scale input signal level is 2.4 V_{PP} by default, but can be set to 2.4/2.0 V_{PP} via SPI. Each input pin signal is centered on a common mode voltage, V_{CM}.
67 19	V_{IN-I} V_{IN-Q}	Input	
7, 8 10, 11	V_{RPI} V_{RPQ}	Output	Upper reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to **AGND** (low ESL 0.1 µF) should be placed very close to the pin to minimize stray inductance. V_{RP} needs to be connected to V_{RN} through a low ESL 0.1 µF and a low ESR 10 µF capacitors in parallel.
5, 6 12, 13	V_{RNI} V_{RNQ}	Output	Lower reference voltage. This pin should not be used to source or sink current. The decoupling capacitor to **AGND** (low ESL 0.1 µF) should be placed very close to the pin to minimize stray inductance. V_{RN} needs to be connected to V_{RP} through a low ESL 0.1 µF and a low ESR 10 µF capacitors in parallel.
2 16	V_{RMI} V_{RMQ}	Output	Common mode voltage These pins should be bypassed to **AGND** with a low ESL (equivalent series inductance) 0.1 µF capacitor placed as close to the pin as possible to minimize stray inductance, and a 10 µF capacitor should be placed in parallel. It is recommended to use V_{RM} to provide the common mode voltage for the differential analog inputs.
9	V_{REF}	Output/Input	Internal reference voltage output / External reference voltage input. By default, this pin is the output for the internal 1.2V voltage reference. This pin should not be used to sink or source current and should be decoupled to **AGND** with a 0.1 µF, low ESL capacitor. The decoupling capacitors should be placed as close to the pins as possible to minimize inductance and optimize ADC performance. The decoupling capacitor should not be larger than 0.1 µF, otherwise dynamic performance after power-up calibration can decrease due to the extended V_{REF} settling time. This pin can also be used as the input for a low noise external reference voltage. The output impedance for the internal reference at this pin is 10kΩ and this can be overdriven provided the impedance of the external source is < 10kΩ. Careful decoupling is just as essential when an external reference is used. The 0.1 µF low ESL decoupling capacitor should be placed as close to this pin as possible. The default Input differential voltage swing is equal to 2 * V_{REF}, although this can be changed through the SPI.
26	CLK+	Input	Differential clock input pins. DC biasing is provided internally. For single-ended clock mode, drive CLK+ through AC coupling while decoupling CLK- pin to **AGND**.
25	CLK−	Input	
DIGITAL I/O			
23	SCLK	Input	Serial Clock. Serial data is shifted into and out of the device synchronous with this clock signal.
24	SDIO	Input/Output	Serial Data In/Out. Serial data is shifted into the device on this pin while the CSB signal is asserted and data input mode is selected. Serial data is shifted out of the device on this pin while CSB is asserted and data output mode is selected.
27	CSB	Input	Serial Chip Select. When this signal is asserted SCLK is used to clock input or output serial data on the SDIO pin. When this signal is de-asserted, the SDIO pin is a high impedence and the input data is ignored.
28 - 43 61 - 46	D1/0+/-Q to D15/14+/-Q D1/0+/-I to D15/14+/-I	Output	LVDS Data Output. The 16-bit digital output of the data converter is provided on these ports in a dual data rate manner. A 100Ω termination resistor must be placed between each pair of differential signals at the far end of the transmission line. The odd bit data is output first and should be captured first when de-interleaving the data.
44, 45	OUTCLK+/-	Output	Output Clock. This pin is used to clock the output data. It has the same frequency as the sampling clock. One word of data is output in each cycle of this signal. A 100Ω termination resistor must be placed between the differential clock signals at the far end of the transmission line. The falling edge of this signal should be used to capture the odd bit data (D15, D13, D11…D1). The rising edge of this signal should be used to capture the even bit data (D14, D12, D10…D0).

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PIN DESCRIPTIONS (continued)

Pin(s)	Name	Type	Function and Connection
POWER SUPPLIES			
4, 14, 22, 64	$V_{A3.0}$	Analog Power	3.0V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to **AGND** with 0.1 µF capacitors located close to the power pins.
1, 17	$V_{A1.8}$	Analog Power	1.8V Analog Power Supply. These pins should be connected to a quiet source and should be decoupled to **AGND** with 0.1 µF capacitors located close to the power pins.
0, 3, 15, 18, 21, 65, 68	AGND	Analog Ground	Analog Ground Return. Pin 0 is the exposed pad on the bottom of the package. The exposed pad must be connected to the ground plane to ensure rated performance.
62	V_{DR}	Analog Power	Output Driver Power Supply. This pin should be connected to a quiet voltage source and be decoupled to DRGND with a 0.1 µF capacitor close to the power pins.
63	DRGND	Ground	Output Driver Ground Return.



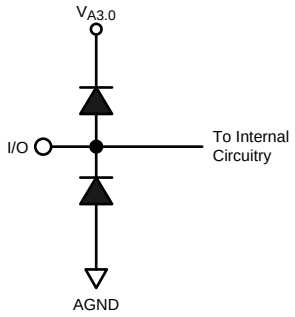
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)(3)(4)(5)

Supply Voltage ($V_{A3.0}$)		−0.3V to 4.2V
Supply Voltage ($V_{A1.8}$, V_{DR})		−0.3V to 2.35V
Voltage at any Pin **except** OUTCLK, CLK, V_{IN}, CSB, SCLK, SDIO, D15/14-D1/0		−0.3V to ($V_{A3.0}$ +0.3V) (Not to exceed 4.2V)
Voltage at CLK, V_{IN} Pins		-0.3V to ($V_{A1.8}$ +0.3V) (Not to exceed 2.35V)
Voltage at D15/14-D1/0, OUTCLK, CSB, SCLK, SDIO Pins		0.3V to (V_{DR} + 0.3V) (Not to exceed 2.35V)
Input Current at any Pin		5 mA
Storage Temperature Range		-65°C to +150°C
Maximum Junction Temp (T_J)		+150°C
Thermal Resistance (θ_{JA})		19.1°C/W
Thermal Resistance (θ_{JC})		1.0°C/W
ESD Rating	Machine Model Human Body Model (6) Charged Device Model	200V 2000V 1250V
Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. See (7)		
For soldering specifications: see product folder at www.ti.com and SNOSA549C		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5mA to 10.
(5) The inputs are protected as shown below. Input voltage magnitudes above $V_{A3.0}$ or below GND will not damage this device, provided current is limited per Note 4. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



(6) Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω.
(7) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings

Specified Temperature Range:	-40°C to +85°C
3.0V Analog Supply Voltage Range: ($V_{A3.0}$)	+2.7V to +3.6V
1.8V Supply Voltage Range: $V_{A1.8}$, V_{DR}	+1.7V to +1.9V
Clock Duty Cycle	30/70 %

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Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS Rterm = 100Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply for T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical(1)	Limits	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**16**	Bits
INL	Integral Non Linearity		±2.5		LSB
DNL	Differential Non Linearity		+0.7,-0.2		LSB
PGE	Positive Gain Error		−1.0		%FS
NGE	Negative Gain Error		-1.0		%FS
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)		0.1		%FS
	Under Range Output Code	0.5dB below negative full scale	0	**0**	
	Over Range Output Code	0.5dB above positive full scale	65535	**65535**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{CM}	Common Mode Input Voltage	V_{RM} is the common mode reference voltage	V_{RM}±0.05		V
V_{RM}	Reference Ladder Midpoint Output Voltage		1.15		V
V_{REF}	Internal Reference Voltage		1.20		V
	Differential Analog Input Range	Internal Reference, default input range is selected	2.4		V_{PP}

(1) Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS R_{TERM} = 100Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply for T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Limits	Units
SNR	Signal-to-Noise Ratio	Fin = 30 MHz at −1dBFS	78		dBFS
		Fin = 197 MHz at −1dBFS	76	**74.3**	dBFS
		Fin = 197 MHz at −7dBFS	77.3		dBFS
SFDR	Single-tone Spurious Free Dynamic Range(1)	Fin = 30 MHz at −1dBFS	95		dBFS
		Fin = 197 MHz at −1dBFS	89	**81**	dBFS
		Fin = 197 MHz at −7dBFS	99		dBFS
THD	Total Harmonic Distortion	Fin = 197 MHz at −1dBFS	−85	**-80**	dBFS
		Fin = 197 MHz at −7dBFS	−96		dBFS
H2	Second-order Harmonic(1)	Fin = 197 MHz at −1dBFS	−90		dBFS
		Fin = 197 MHz at −7dBFS	−99		dBFS
H3	Third-order Harmonic(1)	Fin = 197 MHz at −1dBFS	−93		dBFS
		Fin = 197 MHz at −7dBFS	−105		dBFS
SPUR	Worst Harmonic or Spurious Tone excluding H2 and H3	Fin = 197 MHz at −1dBFS	98	**90**	dBFS
		Fin = 197 MHz at −7dBFS	102		dBFS
	Full Power Bandwidth	-3dB Point	1.4		GHz
	Crosstalk	0 MHz tested channel, f_{IN}=32.5 MHz at -1dBFS other channel	110		dBFS
		0 MHz tested channel, f_{IN}=192 MHz at -1dBFS other channel	103		dBFS

(1) This parameter is specified in units of dBFS – dB relative to the ADC's input full-scale voltage.

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Logic and Power Supply Electrical Characteristics(1)

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS R_{TERM} = 100Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply for T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
$I_{A3.0}$	Analog 3.0V Supply Current	Full Operation(2)	345	374	mA
$I_{A1.8}$	Analog 1.8V Supply Current	Full Operation(2)	105	116	mA
I_{DR}	Output Driver Supply Current	Full Operation(2)	65	76	mA
	Core Power Consumption	$V_{A3.0}$ + $V_{A1.8}$ power per channel	612		mW
	Driver Power Consumption	V_{DR} power; Fin = 5MHz Rterm = 100Ω	117		mW
	Total Power Consumption	Full Operation(2)	1.34	1.47	W
	Power Consumption in Power Down State	Power down state, no external clock	4.4		mW
		Sleep state, no external clock	60		mW
DIGITAL INPUT CHARACTERISTICS (SCLK, SDIO, CSB)					
V_{IH}	Logical “1” Input Voltage	V_{DR} = 1.9V		**1.2**	V (min)
V_{IL}	Logical “0” Input Voltage	V_{DR} = 1.7V		**0.4**	V (max)
I_{IN1}	Logical “1” Input Current		10		µA
I_{IN0}	Logical “0” Input Current		−10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (SDIO)					
V_{OH}	Logical “1” Output Voltage	I_{OUT} = 0.5 mA, V_{DR} = 1.8V		**1.2**	V (min)
V_{OL}	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 1.8V		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	−10		mA
$-I_{SC}$	Output Short Circuit Source Current	V_{OUT} = V_{DR}	10		

(1) The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.
(2) This parameter is guaranteed only at 25°C. For power dissipation over temperature range, refer to Power vs. Temperature plot in Typical Performance Characteristics, Dynamic Performance.

LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS R_{TERM} = 100Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}. All other limits apply for T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS DC SPECIFICATIONS (Apply to pins D0 to D15, OUTCLK)						
V_{OD}	Output Differential Voltage	100Ω Differential Load	175	260	325	mV
V_{OS}	Output Offset Voltage	100Ω Differential Load	1.1	1.2	1.3	V

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Timing Specifications

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS R_{TERM} = 100 Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Parameter	Conditions	Typ	Limits	Units
Input Clock Frequency (F_{CLK})			**160**	MHz
Input Clock Frequency (F_{CLK})		20		MHz (min)
Input Clock Amplitude	Measured at each pin (CLK+, CLK-). Differential clock is 2.8 Vpp (typ)	1.4	0.85 1.7	V_{PP} (min) V_{PP} (max)
Data Output Setup Time (T_{SU})(1)	Measured @ V_{OD}/2; F_{CLK} = 160 MHz.	1.57	**1**	ns (min)
Data Output Hold Time (T_H)(1)	Measured @ V_{OD}/2; F_{CLK} = 160 MHz.	1.55	**1**	ns (min)
LVDS Rise/Fall Time (t_R, t_F)	CL= 5pF to GND, RL= 100Ω	270		ps
Pipeline Latency		11.5		Clock Cycles
Aperture Jitter		80		fs rms
Power-Up Time	From assertion of Power to specified level of performance.	0.5+ 10^3*(2^{22}+2^{17})/F_{CLK}		ms
Power-Down Recovery Time	From de-assertion of power down mode to output data available.	0.1+ 10^3*(2^{19}+2^{17})/F_{CLK}		ms
Sleep Recovery Time	From de-assertion of sleep mode to output data available.	100		µS

(1) This parameter is a function of the CLK frequency - increasing directly as the frequency is lowered.

Unless otherwise specified, the following specifications apply: $V_{A3.0}$ = 3.0V, $V_{A1.8}$ = 1.8V, V_{DR} = 1.8V, Differential sinusoidal clock, f_{CLK} = 160 MSPS at 2.8 V_{PP}, A_{IN} = -1dBFS, LVDS R_{TERM} = 100Ω, C_L = 5 pF. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Max	Units
f_{SCLK}	Serial Clock Frequency	$f_{SCLK} = 1 / t_P$		20	MHz (max)
t_{PH}	SCLK Pulse Width - High	% of SCLK Period		40 60	% (min) % (max)
t_{PL}	SCLK Pulse Width - Low	% of SCLK Period		40 60	% (min) % (max)
t_{SSU}	SDIO Input Data Setup Time			5	ns (min)
t_{SH}	SDIO Input Data Hold Time			5	ns (min)
t_{ODZ}	SDIO Output Data Driven-to-Tri-State Time			5	ns (max)
t_{OZD}	SDIO Output Data Tri-State-to-Driven Time			5	ns (max)
t_{OD}	SDIO Output Data Delay Time			15	ns (max)
t_{CSS}	CSB Setup Time			5	ns (min)
t_{CSH}	CSB Hold Time			5	ns (min)
t_{IAG}	Inter-access Gap	Minimum time CSB must be deasserted between accesses		30	ns (min)

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Timing Diagrams

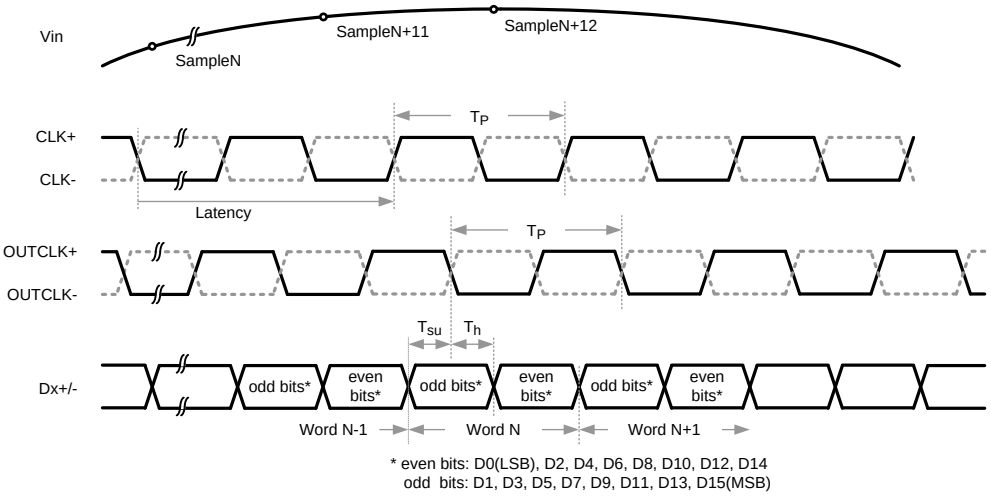


Figure 3. Digital Output Timing

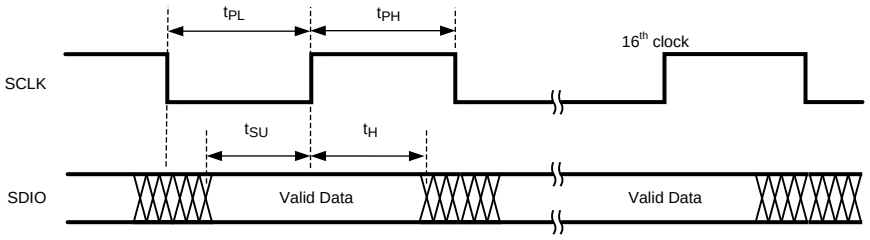


Figure 4. SPI Write Timing

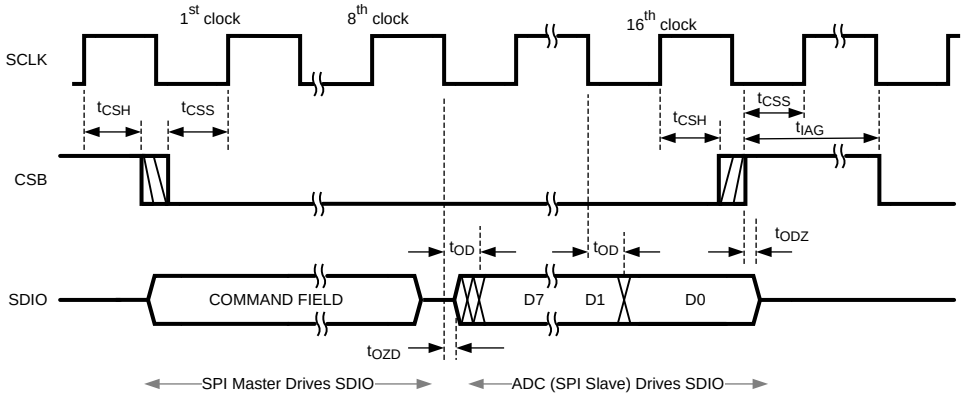


Figure 5. SPI Read Timing

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and the time when data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is the coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error − Negative Full Scale Error (1)

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error NGE = Offset Error - Negative Full Scale Error (2)

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC16DV160 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages ($V_{IN+} – V_{IN-}$) required to cause a transition from code 32767LSB and 32768LSB with offset binary data format.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the power of input signal to the total power of all other spectral components below one-half the sampling frequency, not including harmonics and DC.

SIGNAL TO NOISE AND DISTORTION (SINAD) Is the ratio, expressed in dB, of the power of the input signal to the total power of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

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SPUR (SPUR) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power, where a spurious signal is any signal present in the output spectrum that is not present at the input excluding the second and third harmonic distortion.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the power of input signal and the peak spurious signal power, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total power of the first eight harmonics to the input signal power. THD is calculated as:

$$THD = 20\log_{10}\sqrt{\frac{f_2^2 + f_3^2 + \ldots + f_9^2}{f_1^2}} \quad (3)$$

where f_1^2 is the power of the fundamental frequency and f_2^2 through f_9^2 are the powers of the first eight harmonics in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM or H2) is the difference expressed in dB, from the power of its 2nd harmonic level to the power of the input signal.

THIRD HARMONIC DISTORTION (3RD HARM or H3) is the difference expressed in dB, from the power of the 3rd harmonic level to the power of the input signal.

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Typical Performance Characteristics, DNL, INL

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, V_{DR} = 1.8V, f_{CLK} = 160 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 32.4MHz with –1dBFS.

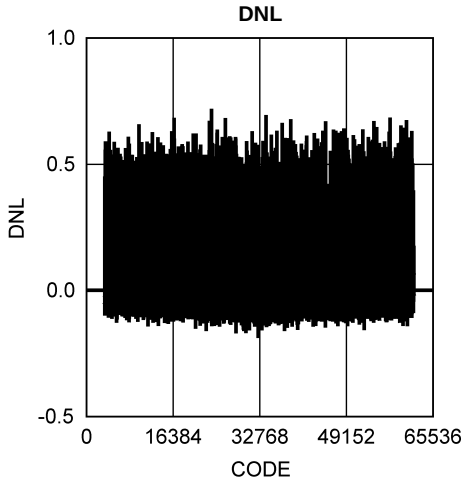


Figure 6.

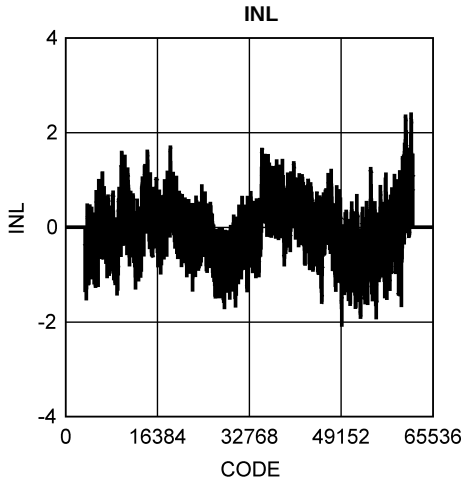


Figure 7.

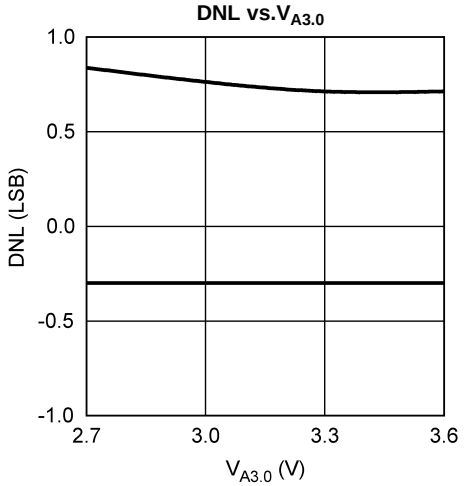


Figure 8.

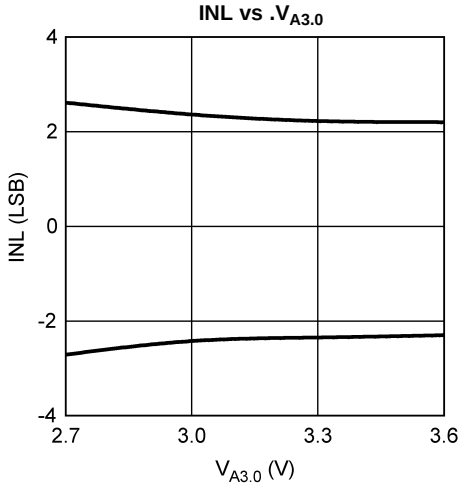


Figure 9.

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Typical Performance Characteristics, Dynamic Performance

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, V_{DR} = 1.8V, f_{CLK} = 160 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 197MHz with –1dBFS.

SNR, SINAD, SFDR vs. f_{IN}

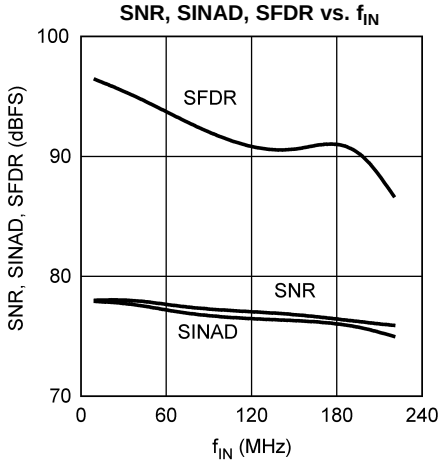


Figure 10.

DISTORTION vs. f_{IN}

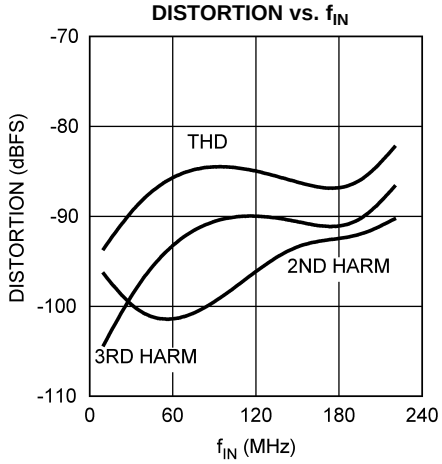


Figure 11.

SNR, SINAD, SFDR vs. $V_{A3.0}$

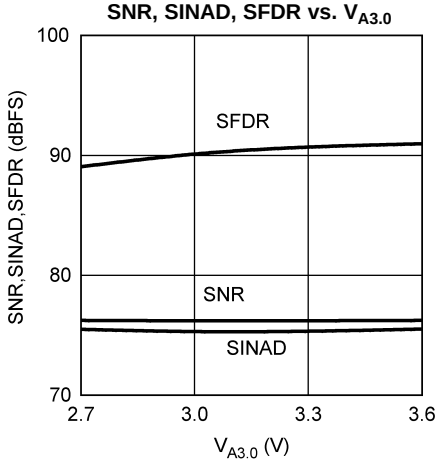


Figure 12.

DISTORTION vs. $V_{A3.0}$

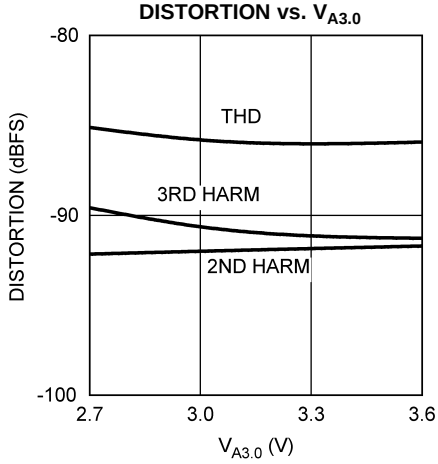


Figure 13.

SNR, SINAD, SFDR vs. $V_{A1.8}$

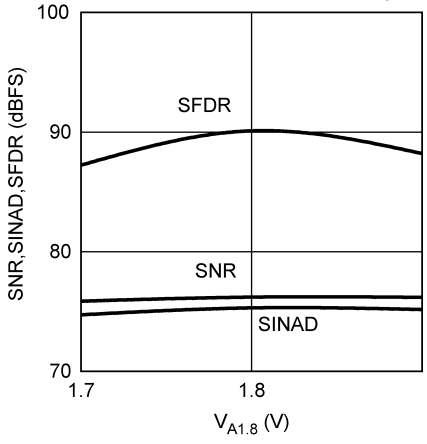


Figure 14.

DISTORTION vs. $V_{A1.8}$

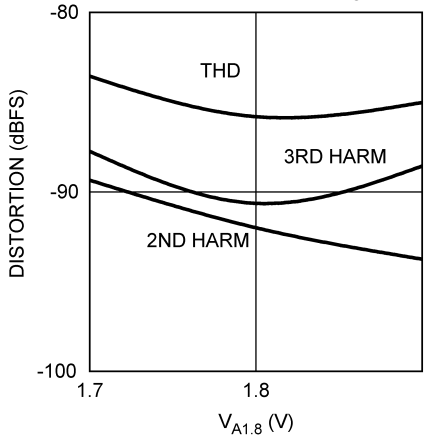


Figure 15.

Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, V_{DR} = 1.8V, f_{CLK} = 160 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 197MHz with –1dBFS.

SNR, SFDR vs. Input Amplitude (dBFS)

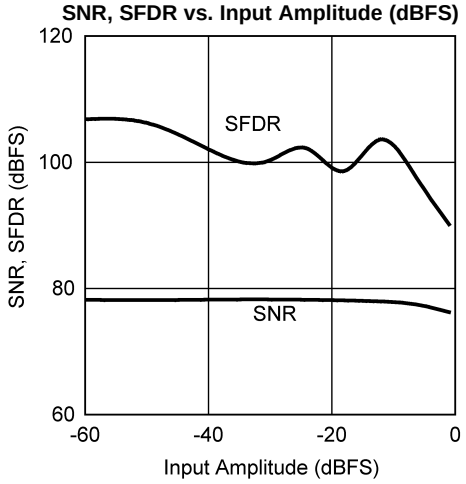


Figure 16.

SNR, SFDR vs. Input Amplitude (dBc)

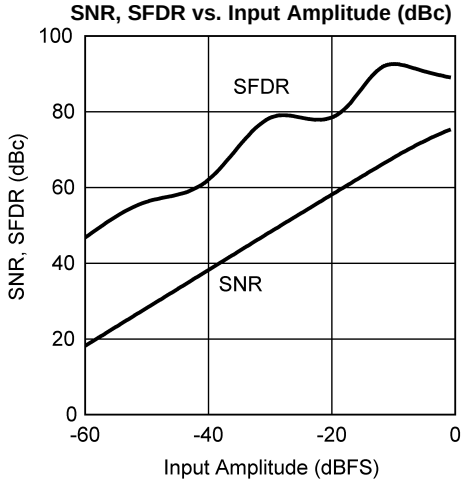


Figure 17.

Spectral Response @ 10.1 MHz

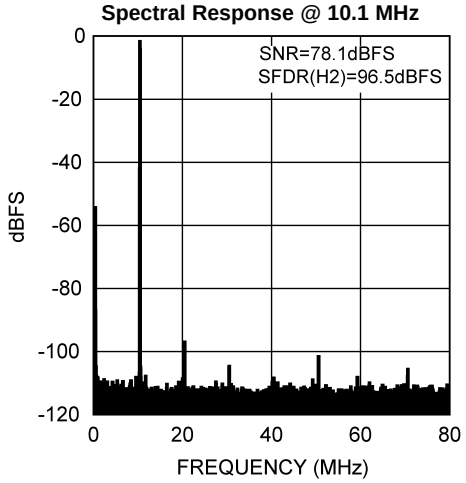


Figure 18.

Spectral Response @ 32.5 MHz

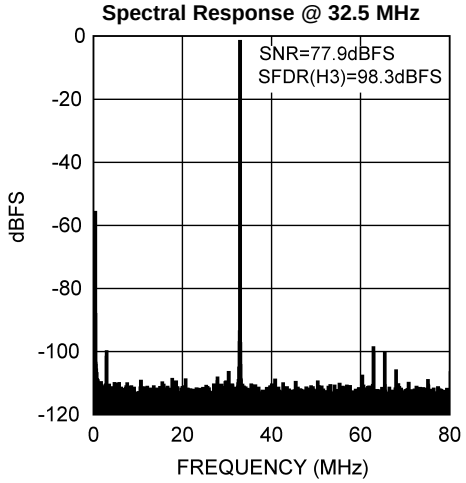


Figure 19.

Spectral Response at 70 MHz

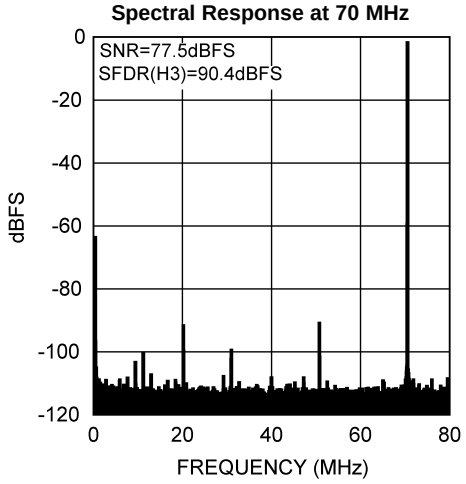


Figure 20.

Spectral Response @ 150 MHz

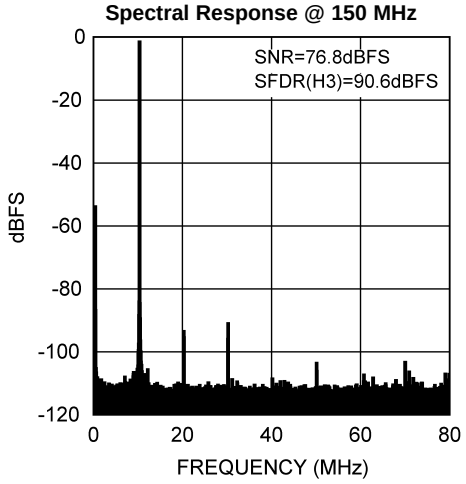


Figure 21.

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Typical Performance Characteristics, Dynamic Performance (continued)

Unless otherwise noted, these specifications apply: $V_{A3.0}$= +3.0V, $V_{A1.8}$, V_{DR} = 1.8V, f_{CLK} = 160 MSPS. Differential Clock Mode, Offset Binary Format. LVDS Rterm = 100 Ω. C_L = 5 pF. Typical values are at T_A = +25°C. Fin = 197MHz with –1dBFS.

Spectral Response @ 197 MHz

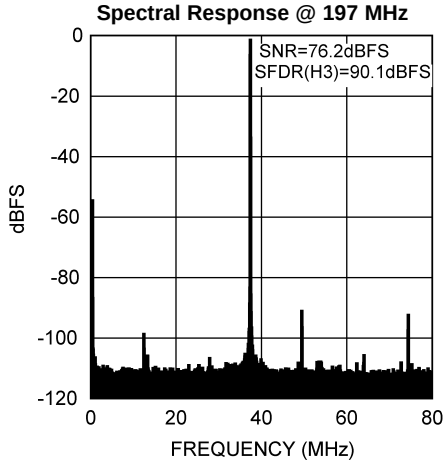


Figure 22.

Spectral Response @ 220 MHz

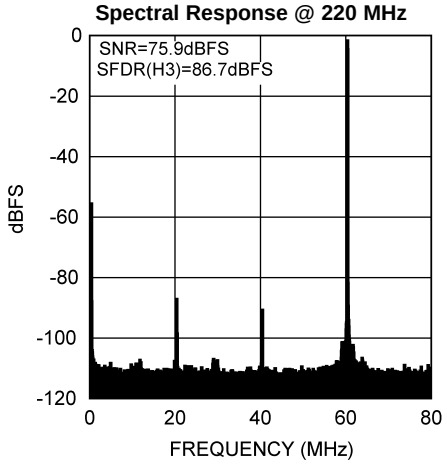


Figure 23.

Spectral Response @ 197 MHz, -7dBFS

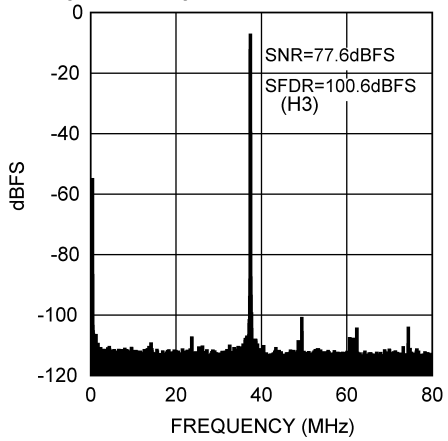


Figure 24.

Two Tone Spectral Response @ 197 MHz, 203 MHz

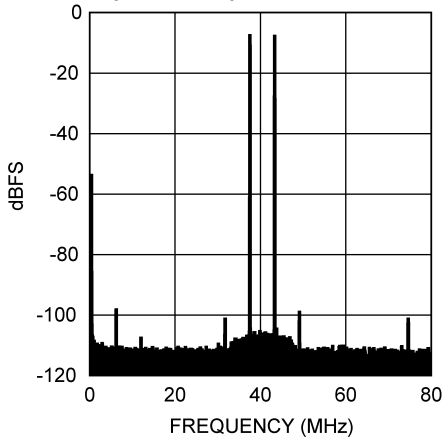


Figure 25.

Power vs. Temperature

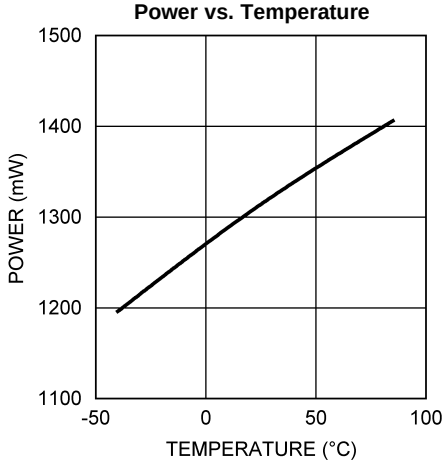


Figure 26.

FUNCTIONAL DESCRIPTION

Operating on dual +1.8V and +3.0V supplies, the ADC16DV160 digitizes a differential analog input signal to 16 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance. The user has the choice of using an internal 1.2V stable reference, or using an external 1.2V reference. The internal 1.2V reference has a high output impedance of > 9 kΩ and can be easily over-driven by an external reference. A 3-wire SPI-compatible serial interface facilitates programming and control of the ADC16DV160.

ADC Architecture

The ADC16DV160 architecture consists of a dual channel highly linear and wide bandwidth sample-and-hold circuit, followed by a switched capacitor pipeline ADC. Each stage of the pipeline ADC consists of low resolution flash sub-ADC and an inter-stage multiplying digital-to-analog converter (MDAC), which is a switched capacitor amplifier with a fixed stage signal gain and DC level shifting circuits. The amount of DC level shifting is dependent on sub-ADC digital output code. A 16-bit final digital output is the result of the digital error correction logic, which receives the digital output of each stage including redundant bits to correct offset error of each sub-ADC.

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APPLICATION INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC16DV160:

$2.7V \le V_{A3.0} \le 3.6V$

$1.7V \le V_{A1.8} \le 1.9V$

$1.7V \le V_{DR} \le 1.9V$

$20\ MSPS \le F_{CLK} \le 160\ MSPS$

$V_{REF} \le 1.2V$

$V_{CM} = 1.15V$ (from V_{RM})

ANALOG INPUTS

The analog input circuit of the ADC16DV160 is a differential switched capacitor sample-and-hold circuit (see Figure 27) that provides optimum dynamic performance wide input frequency range with minimum power consumption. The clock signal alternates sample mode (Q_S) and hold mode (Q_H). An integrated low jitter duty cycle stabilizer ensures constant optimal sample and hold time over a wide range of input clock duty cycle. The duty cycle stabilizer is always turned on during normal operation.

During sample mode, analog signals (V_{IN+}, V_{IN-}) are sampled across two sampling capacitors (C_S) while the amplifier in the sample-and-hold circuit is idle. The dynamic performance of the ADC16DV160 is likely determined during sampling mode. The sampled analog inputs (V_{IN+}, V_{IN-}) are held during hold mode by connecting input side of the sampling capacitors to output of the amplifier in the sample-and-hold circuit while driving pipeline ADC core.

The signal source, which drives the ADC16DV160, is recommended to have a source impedance less than 100Ω over a wide frequency range for optimal dynamic performance.

A shunt capacitor can be placed across the inputs to provide high frequency dynamic charging current during sample mode and also absorb any switching charge coming from the ADC16DV160. A shunt capacitor can be placed across each input to GND for similar purpose. Smaller physical size and low ESR and ESL shunt capacitors are recommended.

The value of shunt capacitance should be carefully chosen to optimize the dynamic performance at specific input frequency range. Larger value shunt capacitors can be used for lower input frequencies, but the value has to be reduced at high input frequencies.

Balancing impedance at positive and negative input pin over entire signal path must be ensured for optimal dynamic performance.

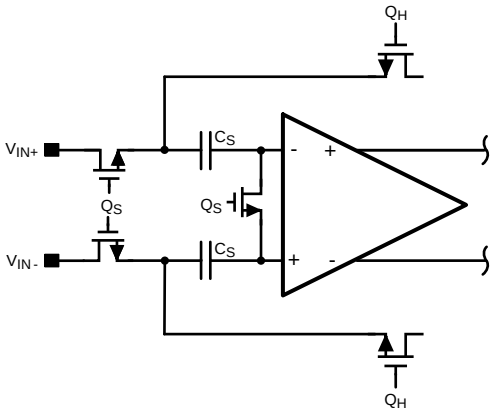


Figure 27. Simplified Switched-Capacitor Sample-and-hold Circuit

Input Common Mode

The analog inputs of the ADC16DV160 are not internally dc biased and the range of input common mode is very narrow. Hence it is highly recommended to use the common mode voltage (V_{RM}, typically 1.15V) as input common mode for optimal dynamic performance regardless of DC and AC coupling applications. Input common mode signal must be decoupled with low ESL 0.1 µF input bias resistors to minimize noise performance degradation due to any coupling or switching noise between the ADC16DV160 and input driving circuit.

Driving Analog Inputs

For low frequency applications, either a flux or balun transformer can convert single-ended input signals into differential and drive the ADC16DV160 without additive noise. An example is shown in Figure 28. The V_{RM} pin is used to bias the input common mode by connecting the center tap of the transformer's secondary ports. A flux transformer is used for this example, but AC coupling capacitors enable the use of a balun type transformer.

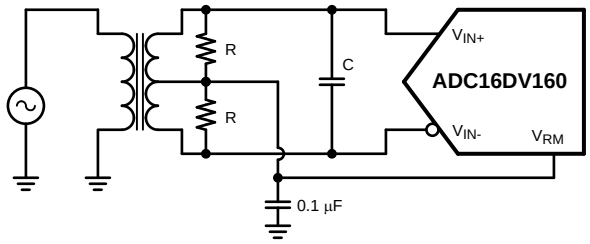


Figure 28. Transformer Drive Circuit for Low Input Frequency

Transformers act as band pass filters. The lower frequency limit is set by saturation at frequencies below a few MHz and parasitic resistance and capacitance set the upper frequency limit. The transformer core will be saturated with excessive signal power and it causes distortion as the equivalent load termination becomes heavier at high input frequencies. This is a reason to reduce shunt capacitors for high IF sampling applications to balance the amount of distortion caused by the transformer and charge kick-back noise from the device.

As input frequency goes higher with the input network in Figure 28, amplitude and phase unbalance increase between positive and negative inputs (V_{IN+} and V_{IN-}) due to the inherent impedance mismatch between the two primary ports of the transformer since one is connected to the signal source and the other is connected to GND. Distortion increases as a result.

The cascaded transmission line (balun) transformers in Figure 29 can be used for high frequency applications like high IF sampling base station receive channels. The transmission line transformer has less stray capacitance between primary and secondary ports and so the impedance mismatch at the secondary ports is effectively less even with the given inherent impedance mismatch on the primary ports. Cascading two transmission line transformers further reduces the effective stray capacitance from the secondary ports of the secondary transformer to primary ports of first transformer, where the impedance is mismatched. A transmission line transformer, for instance MABACT0040 from M/A-COM, with a center tap on the secondary port can further reduce amplitude and phase mismatch.

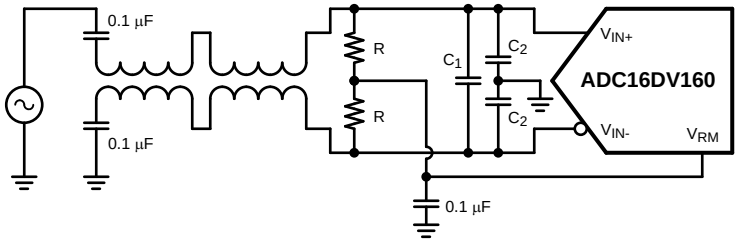


Figure 29. Transformer Drive Circuit for High Input Frequency

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Equivalent Input Circuit and Its S11

The input circuit of the ADC16DV160 during sample mode is a differential switched capacitor as shown in Figure 30. The bottom plate sampling switch is bootstrapped in order to reduce its turn on impedance and its variation across input signal amplitude. Bottom plate sampling switches, and top plate sampling switch are all turned off during hold mode. The sampled analog input signal is processed through the following pipeline ADC core. The equivalent impedance changes drastically between sample and hold mode and a significant amount of charge injection occurs during the transition between the two operating modes.

Distortion and SNR heavily rely on the signal integrity, impedance matching during sample mode and charge injection due to the sampling switches.

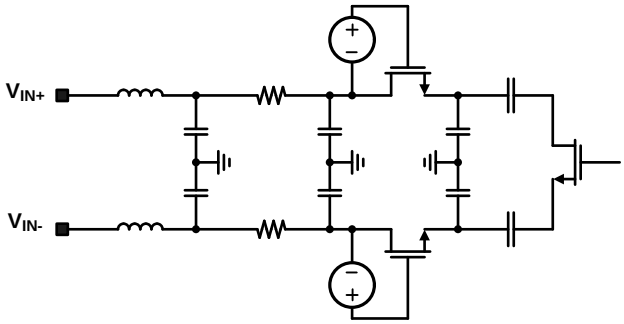


Figure 30. Input Equivalent Circuit

The S11 of the input circuit of the ADC16DV160 is shown in Figure 31. Up to 500 MHz, it is predominantly capacitive loading with small stray resistance and inductance as shown in Figure 31. An appropriate resistive termination at a given input frequency band has to be added to improve signal integrity. Any shunt capacitor on the analog input pin deteriorates signal integrity but it provides high frequency charge to absorb the charge injected by the sampling switches. An optimal shunt capacitor is dependent on input signal frequency as well as the impedance characteristic of the analog input signal path including components like transformers, termination resistors, and AC coupling capacitors.

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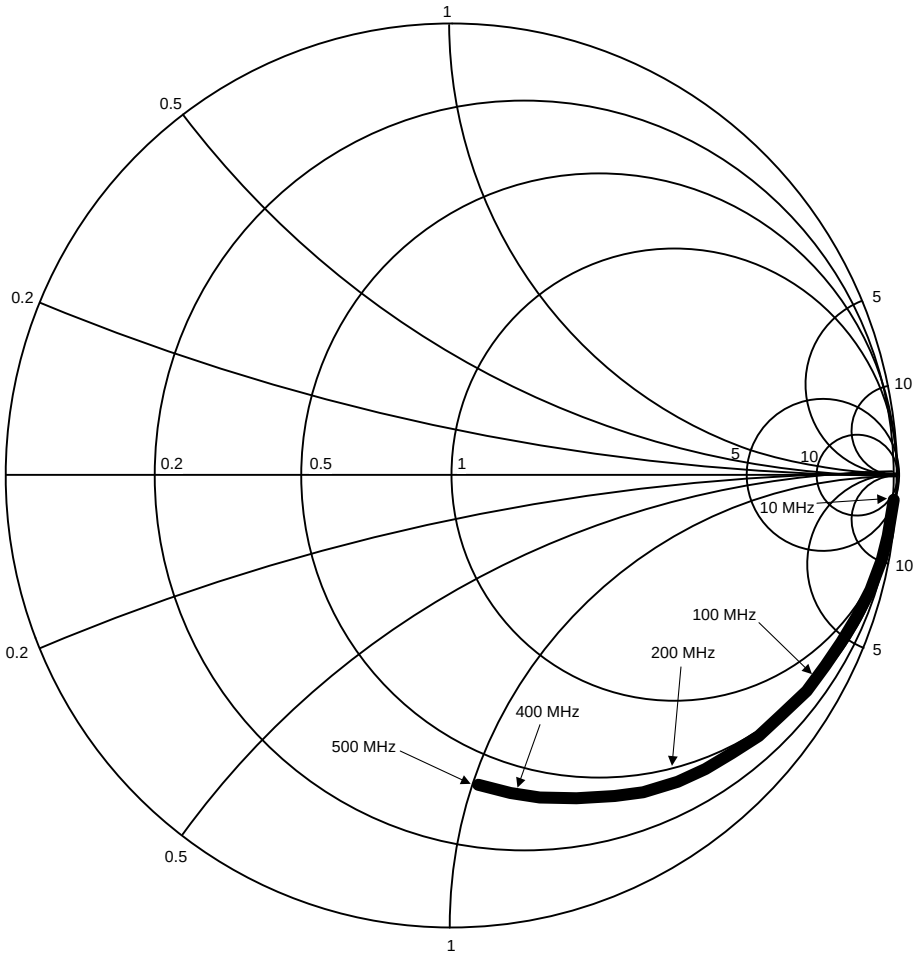


Figure 31. ADC16DV160 Input S11

CLOCK INPUT CONSIDERATIONS

Clock Input Modes

The ADC16DV160 provides a low additive jitter differential clock receiver for optimal dynamic performance over a wide input frequency range. The input common mode of the clock receiver is internally biased at $V_{A1.8}/2$ through a 10 kΩ resistor as shown in Figure 32. Normally the external clock input should be AC-coupled. It is possible to DC-couple the clock input, but the common mode (average voltage of CLK+ and CLK-) must not be higher than $V_{A1.8}/2$ to prevent substantial tail current reduction leading to lowered jitter performance. CLK+ and CLK- should never be lower than AGND. A high speed back-to-back diode connected between CLK+ and CLK- can limit the maximum swing, but this could cause signal integrity concerns when the diode turns on and reduces the load impedance instantaneously.

The preferred differential transformer coupled clocking approach is shown in Figure 33. A 0.1 µF decoupling capacitor on the center tap of the secondary of a flux type transformer stabilizes clock input common mode. Differential clocking increases the maximum amplitude of the clock input at the pins 6dB vs. the singled-ended circuit shown in Figure 34. The clock amplitude is recommended to be as large as possible while CLK+ and CLK- both never exceed the supply rails of $V_{A1.8}$ and **AGND**. With the equivalent input noise of the differential clock receiver shown in Figure 32, a larger clock amplitude at CLK+ and CLK- pins increases its slope around the zero-crossing point so that higher signal-to-noise results.

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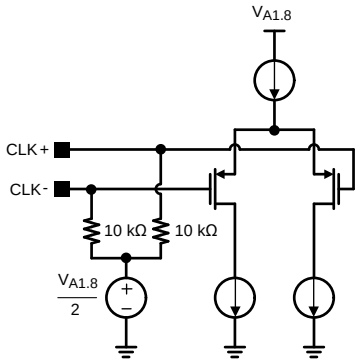


Figure 32. Equivalent Clock Receiver

The differential receiver of the ADC16DV160 has an extremely low-noise floor but its bandwidth is also extremely wide. The wide band clock noise folds back into the first Nyquist zone at the ADC output. Increased slope of the input clock lowers the equivalent noise contributed by the differential receiver.

A band-pass filter (BPF) with narrow pass band and low insertion loss can be added to the clock input signal path when the wide band noise of the clock source is noticeably large compared to the input equivalent noise of the differential clock receiver.

Load termination can be a combination of R and C instead of a pure R. This RC termination can improve the noise performance of the clock signal path by filtering out high frequency noise through a low pass filter. The size of R and C is dependent on the clock rate and slope of the clock input.

An LVPECL and/or LVDS driver can also drive the ADC16DV160. However the full dynamic performance of the ADC16DV160 might not be achieved due to the high noise floor of the driving circuit itself especially in high IF sampling applications.

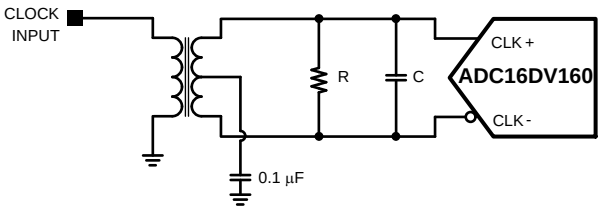


Figure 33. Differential Clocking, Transformer Coupled

A singled-ended clock can drive the CLK+ pin through a 0.1 µF AC coupling capacitor while CLK- is decoupled to AGND through a 0.1 µF capacitor as shown in Figure 34.

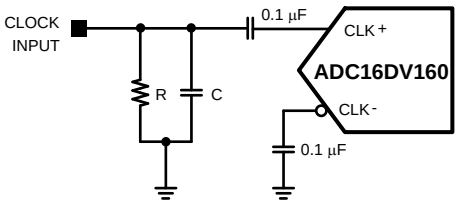


Figure 34. Singled-Ended 1.8V Clocking, Capacitive AC Coupled

Duty Cycle Stabilizer

The highest operating speed with optimal performance can only be achieved with a 50% clock duty cycle because the switched-capacitor circuit of the ADC16DV160 is designed to have equal amount of settling time between each stage. The maximum operating frequency could be reduced accordingly when the clock duty cycle departs from 50%.

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The ADC16DV160 contains a duty cycle stabilizer that adjusts the non-sampling (rising) clock edge to make the duty cycle of the internal clock 50% for a 30-to-70% input clock duty cycle. The duty cycle stabilizer is always on because the noise and distortion performance are not affected at all. It is not recommended to use the ADC16DV160 at clock frequencies less than 20 MSPS where the feedback loop in the duty cycle stabilizer becomes unstable.

Clock Jitter vs. Dynamic Performance

High speed and high resolution ADCs require a low-noise clock input to ensure full dynamic performance over wide input frequency range. SNR (SNR_{Fin}) at a given input frequency (Fin) can be calculated by:

$$SNR_{Fin} = 10\log_{10}\left[\frac{A^2/2}{V_N^2 + (2\pi Fin \times Tj)^2/2}\right]$$

with a given total noise power (V_N^2) of an ADC, total rms jitter (Tj), and input amplitude (A) in dBFS.

The clock signal path must be treated as an analog signal whenever aperture jitter affects the dynamic performance of the ADC16DV160. Power supplies for the clock drivers have to be separated from the ADC output driver supplies to prevent modulating the clock signal with the ADC digital output signals. Higher noise floor and/or increased distortion/spur may result from any coupling of noise from the ADC digital output signals to the analog input and clock signals.

In IF sampling applications, the signal-to-noise ratio is particularly affected by clock jitter as shown in Figure 35. Tj is the integrated noise power of the clock signal divided by the slope of clock signal around the tripping point. The upper limit of the noise integration is independent of applications and set by the bandwidth of the clock signal path. However, the lower limit of the noise integration highly relies on the application. In base station receive channel applications, the lower limit is determined by the channel bandwidth and space from an adjacent channel.

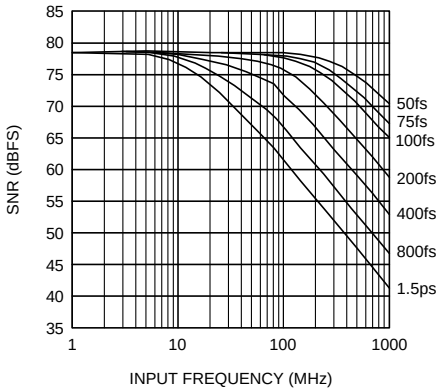


Figure 35. SNR with given Jitter vs. Input Frequency

CALIBRATION

The automatic calibration engine contained within the ADC16DV160 improves dynamic performance and reduces its part-to-part variation. Digital output signals including output clock (OUTCLK+/-) are all logic low while calibrating. The ADC16DV160 is automatically calibrated when the device is powered up. Optimal dynamic performance might not be obtained if the power-up time is longer than the internal delay time (~32 mS @ 160 MSPS clock rate). In this case, the ADC16DV160 can be re-calibrated by asserting and then de-asserting power down mode. Re-calibration is recommended whenever the operating clock rate changes.

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VOLTAGE REFERENCE

A stable and low-noise voltage reference and its buffer amplifier are built into the ADC16DV160. The input full scale is two times V_{REF}, which is the same as VBG (the on-chip bandgap output with a 10 kΩ output impedance) as well as V_{RP} - V_{RN} as shown in Figure 36. The input range can be adjusted by changing V_{REF} either internally or externally. An external reference with low output impedance can easily over-drive the V_{REF} pin. The default V_{REF} is 1.2V. The input common mode voltage (V_{RM}) is a fixed voltage level of 1.15V. Maximum SNR can be achieved at the maximum input range where V_{REF} = 1.2V. Although the ADC16DV160's dynamic and static performance is optimized at a V_{REF} of 1.2V, reducing V_{REF} can improve SFDR performance by sacrificing some of the ADC16DV160's SNR performance.

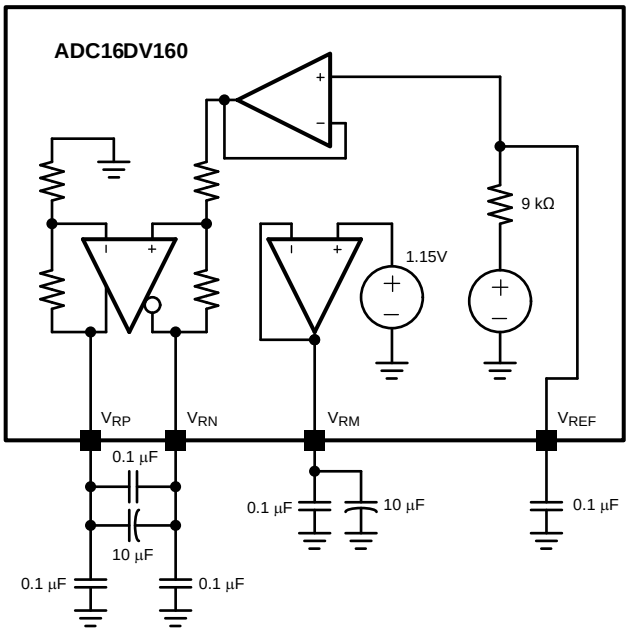


Figure 36. Internal References and their Decoupling

Reference Decoupling

It is highly recommended to place the external decoupling capacitors connected to V_{RP}, V_{RN}, V_{RM} and V_{REF} pins as close to the pins as possible. The external decoupling capacitors should have minimal ESL and ESR. During normal operation, inappropriate external decoupling with large ESL and/or ESR capacitors increase the settling time of the ADC core and result in lower SFDR and SNR performance. The V_{RM} pin may be loaded up to 1mA for setting input common mode. The remaining pins should not be loaded. Smaller capacitor values might result in degraded noise performance. The decoupling capacitor on the V_{REF} pin must not exceed 0.1 µF. Additional decoupling on this pin will cause improper calibration during power-up. All the reference pins except V_{REF} have a very low output impedance. Driving these pins via a low-output impedance external circuit for a long time period may damage the device.

When the V_{RM} pin is used to set the input common mode level via transformer, a smaller series resistor should be placed on the signal path to isolate any switching noise between the ADC core and input signal. The series resistor introduces a voltage error between V_{RM} and V_{CM} due to charge injection while the sampling switches are toggling. The series resistance should not be larger than 50Ω.

All grounds associated with each reference and analog input pin should be connected to a solid and quiet ground on the PC board. Coupling noise from digital outputs and their supplies to the reference pins and their ground can cause degraded SNR and SFDR performance.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC16DV160 between these areas, is required to achieve the specified performance.

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Even though LVDS outputs reduce ground bounce, the positive and negative signal path have to be well matched, and their traces should be kept as short as possible. It is recommend to place an LVDS repeater between the ADC16DV160 and digital data receiver block to prevent coupling noise from the receiving block when the length of the traces are long or the noise level of the receiving block is high.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. Because of the skin effect, the total surface area is more important than its thickness.

Generally, analog and digital lines should not cross. However whenever it is inevitable, make sure that these lines are crossing each other at 90° to minimize cross talk. Digital output and output clock signals must be separated from analog input, references and clock signals unconditionally to ensure the maximum performance from the ADC16DV160. Any coupling may result in degraded SNR and SFDR performance especially for high IF applications.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should not be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling. It is recommended to place the transformers of the input signal path on the top side, and the transformer for the clock signal path on the bottom side. Every critical analog signal path like analog inputs and clock inputs must be treated as a transmission line and should have a solid ground return path with a small loop area.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference pins and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC16DV160 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

The ground return current path can be well managed when the supply current path is precisely controlled and the ground layer is continuous and placed next to the supply layer. This is because of the proximity effect. A ground return current path with a large loop area will cause electro-magnetic coupling and results in poor noise performance. Note that even if there is a large plane for a current path, the high-frequency return current path is not spread evenly over the large plane, but only takes the path with lowest impedance. Instead of a large plane, using a thick trace for supplies makes it easy to control the return current path. It is recommended to place the supply next to the GND layer with a thin dielectric for a smaller ground return loop. Proper location and size of decoupling capacitors provides a short and clean return current path.

SUPPLIES AND THEIR SEQUENCE

There are three supplies for the ADC16DV160: one 3.0V supply $V_{A3.0}$ and two 1.8V supplies $V_{A1.8}$ and V_{DR}. It is recommended to separate V_{DR} from $V_{A1.8}$ supplies, any coupling from V_{DR} to the rest of the supplies and analog signals could cause lower SFDR and noise performance. When $V_{A1.8}$ and V_{DR} are both from the same supply source, coupling noise can be mitigated by adding a ferrite-bead on the V_{DR} supply path.

Different decoupling capacitors can be used to provide current over wide frequency range. The decoupling capacitors should be located close to the point of entry and close to the supply pins with minimal trace length. A single ground plane is recommended because separating ground under the ADC16DV160 could cause an unexpected long return current path.

The $V_{A3.0}$ supply must turn on before $V_{A1.8}$ and/or V_{DR} reaches a diode turn-on voltage level. If this supply sequence is reversed, an excessive amount of current will flow through the $V_{A3.0}$ supply. The ramp rate of the $V_{A3.0}$ supply must be kept less than 60 V/mS (i.e., 60 µS for 3.0V supply) in order to prevent excessive surge current through ESD protection devices.

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SERIAL CONTROL INTERFACE

The ADC16DV160 has a serial control interface that allows access to the control registers. The serial interface is a generic 3-wire synchronous interface that is compatible with SPI-type interfaces that are used on many microcontrollers and DSP controllers. Each serial interface access cycle is exactly 16 bits long. A register-read or register-write can be accomplished in one cycle. Register space supported by this interface is 64. Figure 37 and Figure 38 show the access protocol used by this interface. Each signal's function is described below. The SPI must be in a static condition during the normal operation of the ADC16DV160, otherwise the performance of the ADC16DV160 may degrade due to the coupling noise generated by the SPI control signals. When a SPI bus is used for multiple devices on the board, it is recommended to reduce the potential for noise coupling by placing logic buffers between the SPI bus and the ADC16DV160.

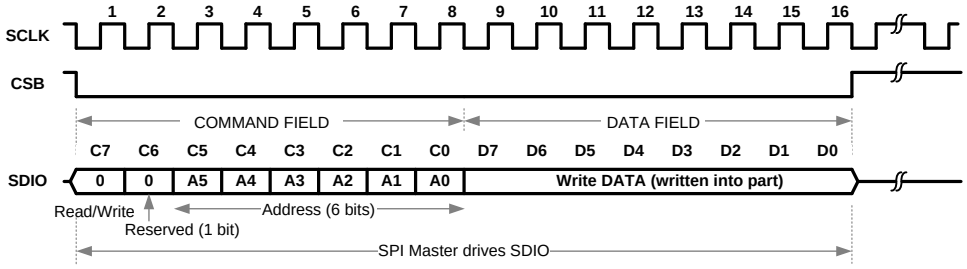


Figure 37. Serial Interface Protocol (Write Operation)

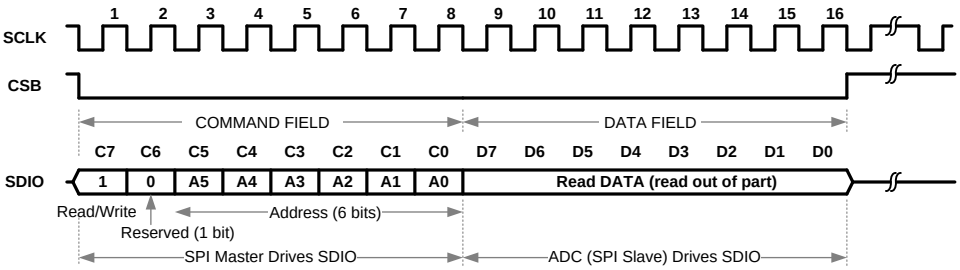


Figure 38. Serial Interface Protocol (Read Operation)

Signal Descriptions

SCLK: Used to register the input date (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. User may disable clock and hold it in the low-state, as long as clock pulse width min. spec is not violated when clock is enabled or disabled.

CSB: Chip Select Bar. Each assertion starts a new register access – i.e., the SDATA field protocol is required. CSB should be de-asserted after the 16th clock. If the CSB is de-asserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register.

SDIO: Serial Data. Must observe setup/hold requirements with respect to the SCLK. Each cycle is 16-bit long.

- R/W: A value of '1' indicates a read operation, while a value of '0' indicates a write operation
- Reserved: Reserved for future use. Must be set to 0.
- ADDR: Up to 64 registers can be addressed.
- DATA: In a write operation the value in this field will be written to the register addressed in this cycle when CSB is de-asserted. In a read operation this field is ignored.

FIXED PATTERN MODE

The ADC16DV160 provides user defined fixed patterns at digital output pins to check timing and connectivity with the receiving device on the board. The fixed pattern map is shown in Figure 39; there are 6 hard-wired fixed patterns (PATTERN (000) to PATTERN (101)) and 2 user-defined patterns (PATTERN (110) and PATTERN (111)). PATTERN (110) and PATTERN (111) can be written via SPI and all '0's are the default values for both. See Register Map address 0CH through 0FH for the details.

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PATTERN			16-bit DATA															
1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 39. Fixed Pattern Map

For flexibility, the user can determine a fixed pattern with a depth of 8 patterns as shown in Figure 40. The user can fill these 8 sequences (SEQ0 – SEQ7) with an arbitrary pattern (PATTERN (000) – PATTERN (111)). See Register Map address 08h through 0Bh below for the details. The default register value for all SEQ0 through SEQ7 sequences is 010, which generates alternating 0xFF and 0x00 at the ADC output as shown in Figure 41. Note that since the ADC outputs odd bits on the falling edge of the OUTCLK and even bits on the rising edge, the resulting 16-bit output codes are 0xAAAA.

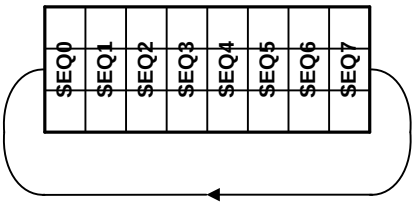


Figure 40. State Machine Generating Fixed Pattern Sequence

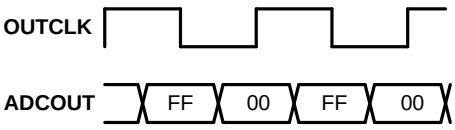


Figure 41. Fixed Pattern at ADC Output with Default SPI Register Values

SAMPLING EDGE

The internal clock divider features allows more flexible design from the perspective of the system clocking scheme. The ADC16DV160 supports divide by 1 or 2 clocking. This feature may cause a potential issue when synchronizing the sample edge of multiple ADCs when the internal clock is divided by 2 from the input clock (CLKIN). The ADC16DV160 samples the analog input signal at the falling edge of the input clock, which will be the falling edge of the internally divided by 2 clock when divide by 2 is configured as shown as dashed lines in Figure 42 below. If there is some timing skew of the SPI control signals and/or input clock between multiple ADCs with this clocking configuration, the sampling edge of some ADC, which is ADC SLAVE I for this example, could be out of phase compared to the ADC MASTER as shown in Figure 42. The sampling edge of the non-synchronized ADC can be synchronized if the internal clock can be inverted through some control bit. This sampling edge flipping function is provided by the ADC16DV160 via SPI. See the SPI Register Map below for the details.

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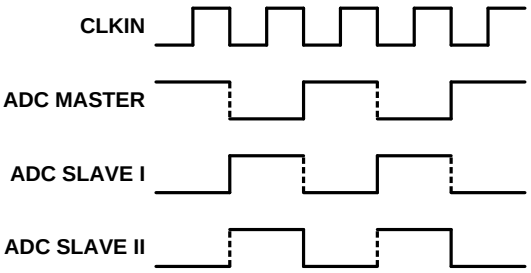


Figure 42. Sampling Edge of Multiple ADCs with Internal Division On

Register Map

NOTE

Accessing unspecified addresses may cause functional failure or damage. All reserved bits must be written with the listed default values.

Operation Mode			**Addr: 00h**				**R/W**
7	6	5	4	3	2	1	0
DF	Operation Mode		Reserved		Full Scale		Default
Bit 7	Data Format						
		1	Two's Complement				
		0	Offset Binary (Default)				
Bits (6:5)	Operation Mode						
	0	0	Normal Operation (Default)				
	0	1	Sleep Mode. Device is powered down, but it can wake up quickly.				
	1	0	Power down mode. Device is powered down at lowest power dissipation.				
	1	1	Fixed pattern mode. Device outputs fixed patterns to check connectivity with interfacing components.				
Bit 4	*Reserved. Must be set to 0.*						
Bit 3	*Reserved. Must be set to 0.*						
Bit 2	*Reserved. Must be set to 1.*						
Bit 1	Full scale. Full scale can be adjusted from 2.0 to 2.4V_{PP}.						
		0	2.0V_{PP}				
		1	2.4V_{PP} (default)				
Bit 0	Restore Default Register Values. Default values of SPI registers can be restored at the rising edge of this bit.						
		1	Restore default register values				
		0	As is (default)				

Synchronization Mode			**Addr: 01h**				**R/W**
7	6	5	4	3	2	1	0
Sample Phase	Clock Divider	Reserved	Output Clock Phase			Reserved	Reserved
Bit 7	Sampling Clock Phase. This is for synchronizing sampling edge for multiple devices while the ADC16DV160 is configured at clock divide by 2.						
	0	Keep sampling edge as is (default).					
	1	Invert internal clock to adjust sampling edge.					
Bit 6	Clock divider. Internal operating clock frequency can be programmed either to be divided by 1 or 2.						
	0	Divide by 1 (default).					

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Synchronization Mode			Addr: 01h				R/W
	1	Divide by 2					
Bit 5	*Reserved. Must be set to 0.*						
Bits (4:2)	Output Clock Phase Adjustment. User can adjust output clock phase from 31° to 143°. Each 1 LSB increment results in about 16° of output clock phase increase.						
	0	0	0	31°			
	0	0	1	47°			
	0	1	0	63°			
	0	1	1	79°			
	1	0	0	95° (default)			
	1	0	1	111°			
	1	1	0	127°			
	1	1	1	143°			
Bit 1	*Reserved. Must be set to 0.*						
Bit 0	*Reserved. Must be set to 0.*						

Fixed Pattern Mode: SEQ0 and SEQ1			Addr: 08h				R/W
7	6	5	4	3	2	1	0
SEQ1<2>	SEQ1<1>	SEQ1<0>	SEQ0<2>	SEQ0<1>	SEQ0<0>	*Reserved*	*Reserved*
Bits (7:5)	3 bit pattern code for SEQ1. 010 is the default.						
Bits (4:2)	3 bit pattern code for SEQ0. 010 is the default.						
Bit 1	*Reserved, Must be set to 0.*						
Bit 0	*Reserved, Must be set to 0.*						

Fixed Pattern Mode: SEQ2 and SEQ3			Addr: 09h				R/W
7	6	5	4	3	2	1	0
SEQ3<2>	SEQ3<1>	SEQ3<0>	SEQ2<2>	SEQ2<1>	SEQ2<0>	*Reserved*	*Reserved*
Bits (7:5)	3 bit pattern code for SEQ3. 010 is the default.						
Bits (4:2)	3 bit pattern code for SEQ2. 010 is the default.						
Bit 1	*Reserved, Must be set to 0.*						
Bit 0	*Reserved, Must be set to 0.*						

Fixed Pattern Mode: SEQ4 and SEQ5			Addr: 0Ah				R/W
7	6	5	4	3	2	1	0
SEQ5<2>	SEQ5<1>	SEQ5<0>	SEQ4<2>	SEQ4<1>	SEQ4<0>	*Reserved*	*Reserved*
Bits (7:5)	3 bit pattern code for SEQ5. 010 is the default.						
Bits (4:2)	3 bit pattern code for SEQ4. 010 is the default.						
Bit 1	*Reserved, Must be set to 0.*						
Bit 0	*Reserved, Must be set to 0.*						

Fixed Pattern Mode: SEQ6 and SEQ7			Addr: 0Bh				R/W
7	6	5	4	3	2	1	0
SEQ7<2>	SEQ7<1>	SEQ7<0>	SEQ6<2>	SEQ6<1>	SEQ6<0>	*Reserved*	*Reserved*
Bits (7:5)	3 bit pattern code for SEQ7. 010 is the default.						
Bits (4:2)	3 bit pattern code for SEQ6. 010 is the default.						
Bit 1	*Reserved, Must be set to 0.*						
Bit 0	*Reserved, Must be set to 0.*						

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Fixed Pattern Mode: LSB PATTERN <110>			**Addr: 0Ch**				**R/W**
7	6	5	4	3	2	1	0
D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
Bits (7:0)	8 LSBs of a fixed pattern for Sequence >110> All '0' for default.						

Fixed Pattern Mode: MSB PATTERN <110>			**Addr: 0Dh**				**R/W**
7	6	5	4	3	2	1	0
D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
Bits (7:0)	8 MSBs of a fixed pattern for Sequence >110> All '0' for default.						

Fixed Pattern Mode: LSB PATTERN <111>			**Addr: 0Eh**				**R/W**
7	6	5	4	3	2	1	0
D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
Bits (7:0)	8 LSBs of a fixed pattern for Sequence >111> All '0' for default.						

Fixed Pattern Mode: MSB PATTERN <1110>			**Addr: 0Fh**				**R/W**
7	6	5	4	3	2	1	0
D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
Bits (7:0)	8 MSBs of a fixed pattern for Sequence >111> All '0' for default.						

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REVISION HISTORY

Changes from Revision G (February 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	29

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC16DV160CILQ/NO.A	Active	Production	VQFN (NKE) | 68	168 | JEDEC TRAY (10+1)	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160
ADC16DV160CILQ/NOPB	Active	Production	VQFN (NKE) | 68	168 | JEDEC TRAY (10+1)	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160
ADC16DV160CILQE/NO.A	Active	Production	VQFN (NKE) | 68	250 | SMALL T&R	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160
ADC16DV160CILQE/NOPB	Active	Production	VQFN (NKE) | 68	250 | SMALL T&R	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160
ADC16DV160CILQX/NO.A	Active	Production	VQFN (NKE) | 68	2000 | LARGE T&R	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160
ADC16DV160CILQX/NOPB	Active	Production	VQFN (NKE) | 68	2000 | LARGE T&R	Yes	NIPDAUAG	Level-4-260C-72 HR	-40 to 85	ADC16DV160

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

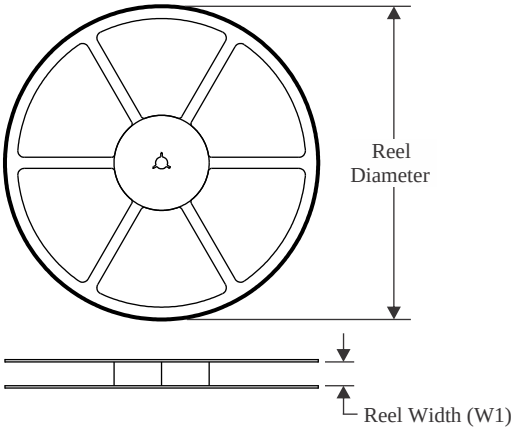
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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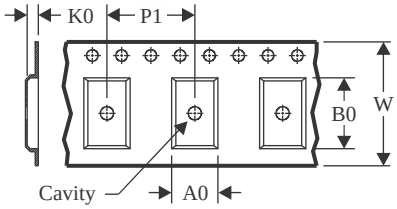
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

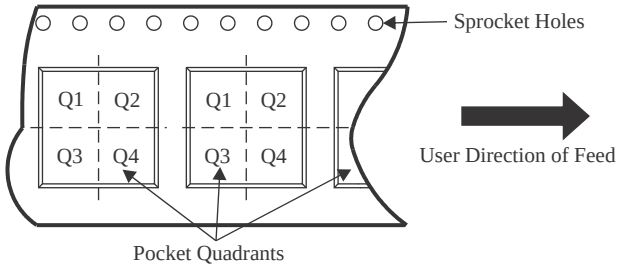


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

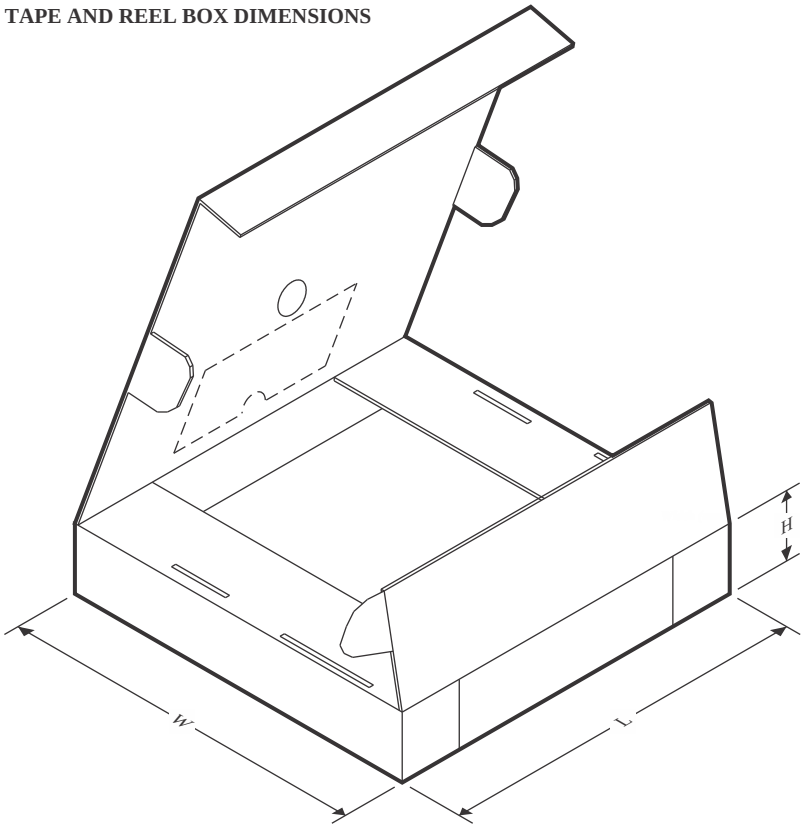
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC16DV160CILQE/ NOPB	VQFN	NKE	68	250	178.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1
ADC16DV160CILQX/ NOPB	VQFN	NKE	68	2000	330.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1

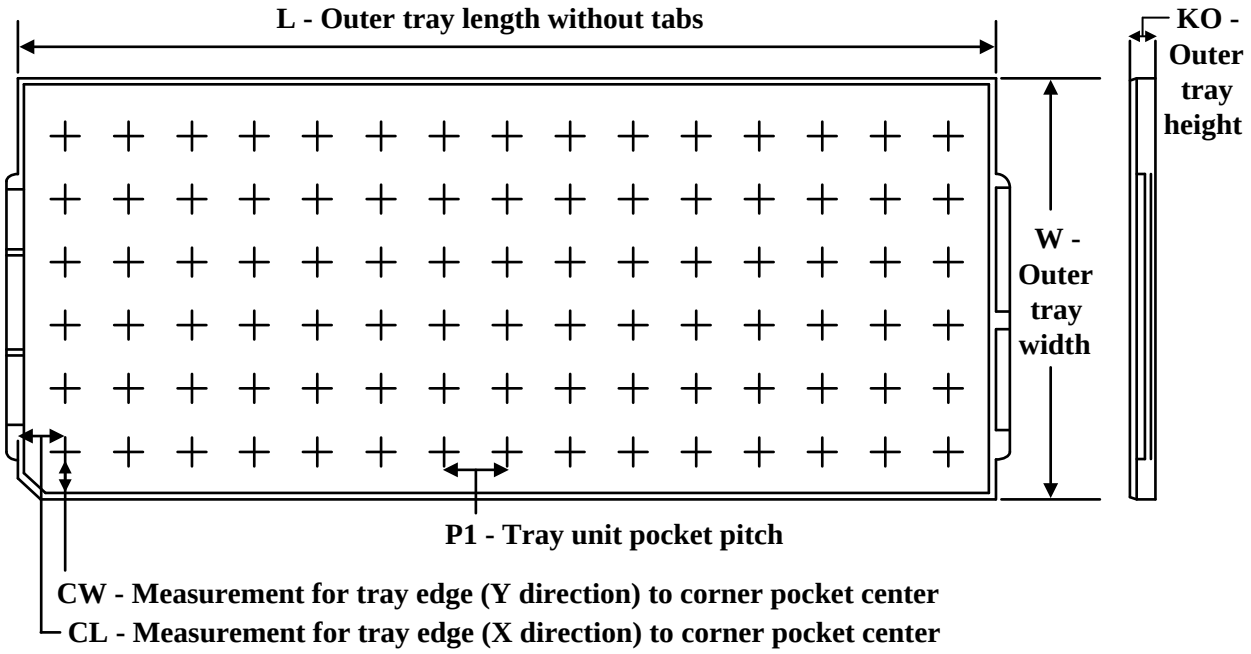
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC16DV160CILQE/ NOPB	VQFN	NKE	68	250	213.0	191.0	55.0
ADC16DV160CILQX/ NOPB	VQFN	NKE	68	2000	356.0	356.0	45.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

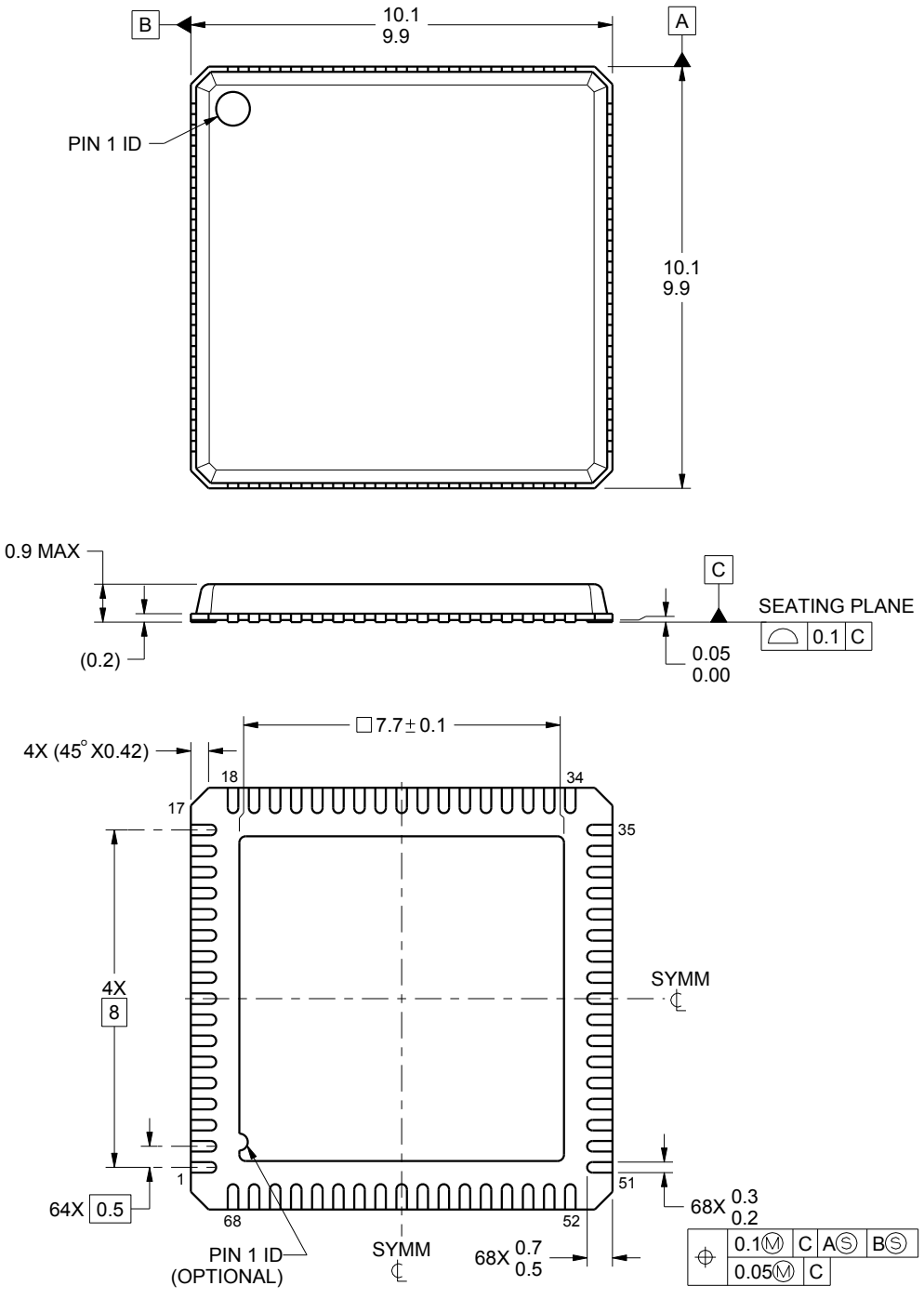
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC16DV160CILQ/NO.A	NKE	VQFNP	68	168	8 X 21	150	322.6	135.9	7620	14.65	11	11.95
ADC16DV160CILQ/NOPB	NKE	VQFNP	68	168	8 X 21	150	322.6	135.9	7620	14.65	11	11.95

PACKAGE OUTLINE

NKE0068A

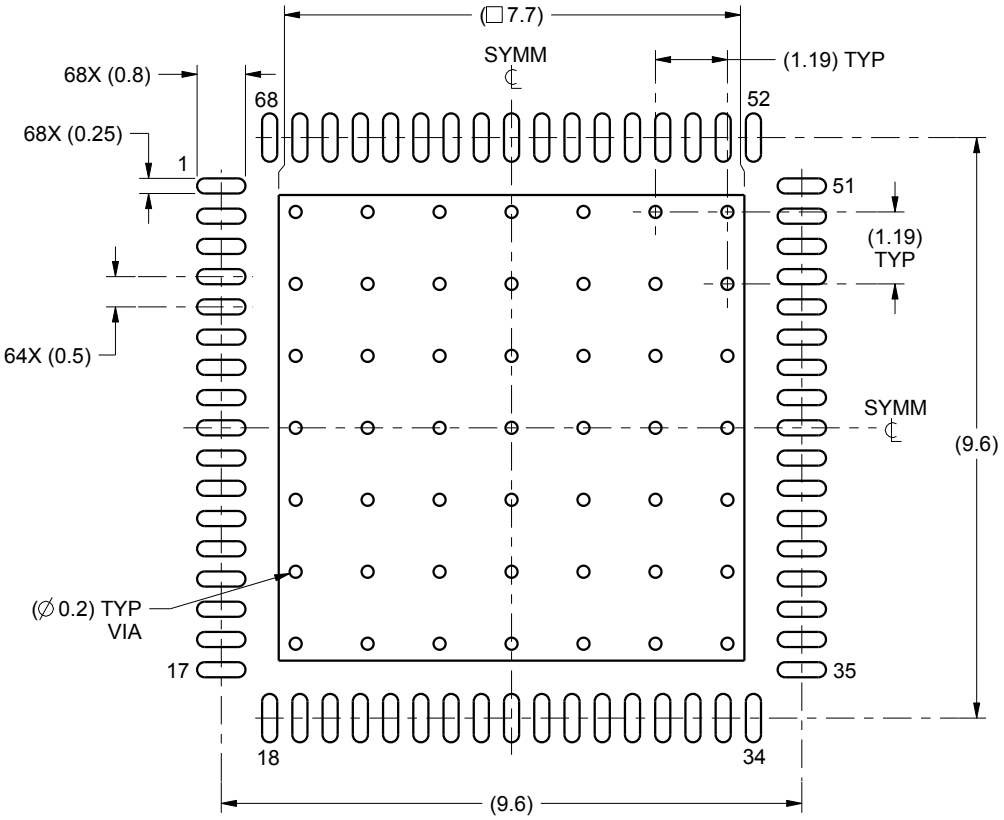
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

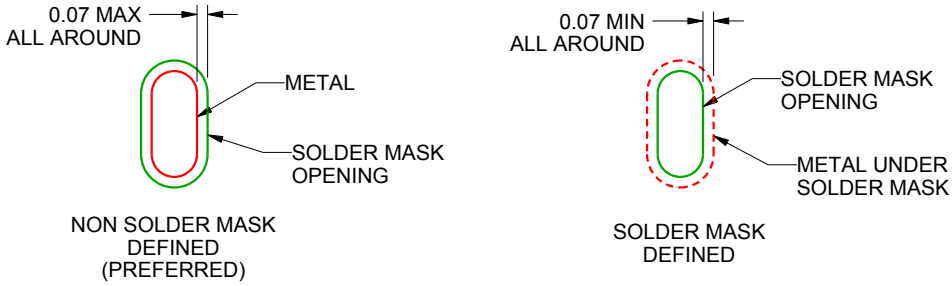


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

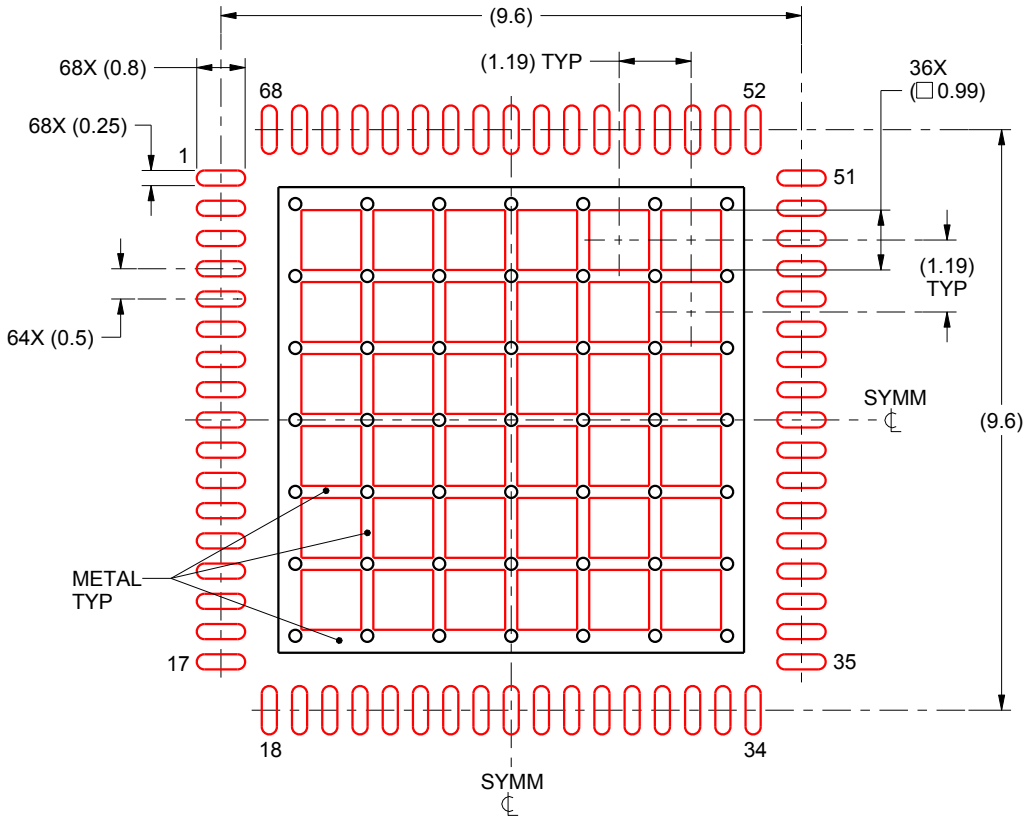


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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