Functional Safety Information

UCC27524-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for UCC27524-Q1 (SOIC and HVSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

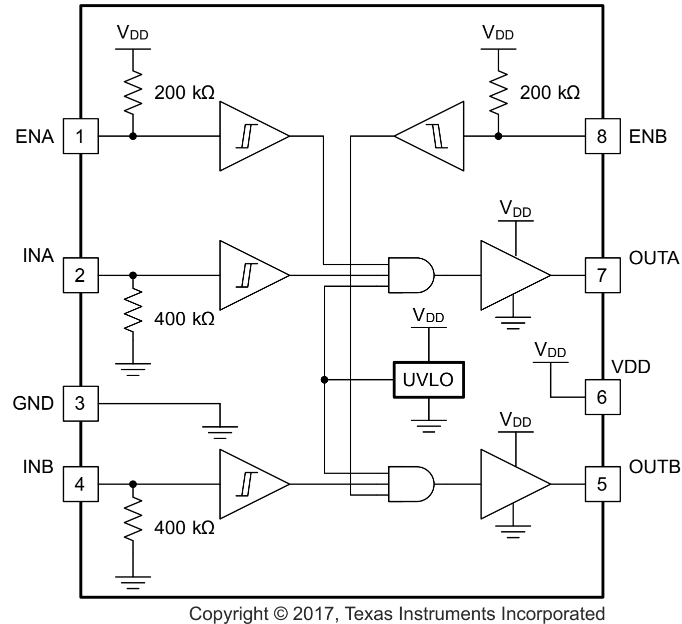

Figure 1-1. Functional Block Diagram

UCC27524-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC Package

This section provides Functional Safety Failure In Time (FIT) rates for SOIC package of UCC27524-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 HVSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for HVSSOP package of UCC27524-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

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Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27524-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTA stuck high	16.6%
OUTA stuck low	16.6%
OUTA unknown	16.6%
OUTB stuck high	16.6%
OUTB stuck low	16.6%
OUTB unknown	16.6%
UVLO not working	<1%
ENA or ENB not working	<1%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC27524-Q1 (SOIC and HVSSOP package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-6 and Table 4-2)
- Pin open-circuited (see Table 4-7 and Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-8 and Table 4-4)
- Pin short-circuited to supply (see Table 4-9 and Table 4-5)

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Adjacent pin short across the package is not considered. Pin #4 to Pin #5. Pin #1 to Pin #8
- Short to positive supply cases. The positive supply is VDD.

4.1 SOIC Package

Figure 4-1 shows the UCC27524-Q1 pin diagram for the SOIC package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27524-Q1 data sheet.

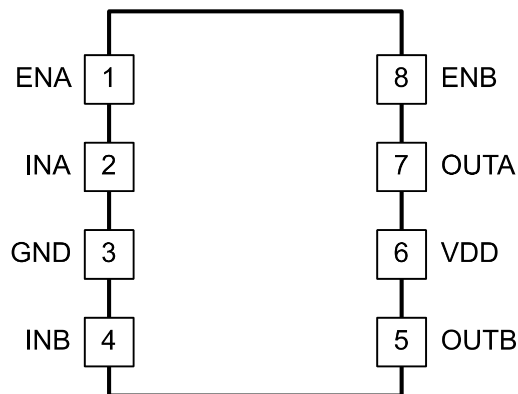

Figure 4-1. Pin Diagram (SOIC) Package Topview

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA stuck low.	B
INA	2	OUTA stuck low	B
GND	3	No effect.	D
INB	4	OUTB stuck low.	B
OUTB	5	OUTB stuck low. Devie may be damaged.	A
VDD	6	No power is applied to the device.	D
OUTA	7	OUTA stuck low. Devie may be damaged.	A
ENB	8	OUTB stuck low.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA is enabled. OUTA follows INA command.	B
INA	2	OUTA stuck low.	B
GND	3	No power is applied to the device. OUTA and OUTB pulled up to VDD.	D
INB	4	OUTB stuck low.	B
OUTB	5	No effect. OUTB is disconnected from the gate of power stage.	D
VDD	6	No power is applied to the device.	D
OUTA	7	No effect. OUTA is disconnected from the gate of power stage.	B
ENB	8	OUTB is enabled. OUTB follows INB command.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	INA	Lose ENA disabling control of OUTA.	B
INA	2	GND	OUTA stuck low.	B
GND	3	INB	OUTB stuck low	B
OUTB	5	VDD	OUTB stuck high. Device may be damaged.	A
VDD	6	OUTA	OUTA stuck high. Device may be damaged.	A
OUTA	7	ENB	OUTA unknown. Device may be damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA is enabled. OUTA follows INA command.	B
INA	2	OUTA is stuck high. Device may be damaged.	A
GND	3	No power is applied to the device.	D
INB	4	OUTB is stuck high.	B
OUTB	5	OUTB is stuck high. Device may be damaged.	A
VDD	6	No effect.	D
OUTA	7	OUTA is stuck high. Device may be damaged.	A
ENB	8	OUTB is enabled. OUTB follows INB command.	D

4.2 SOIC Package

Figure 4-2 shows the UCC27524-Q1 pin diagram for the HVSSOP package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27524-Q1 data sheet.

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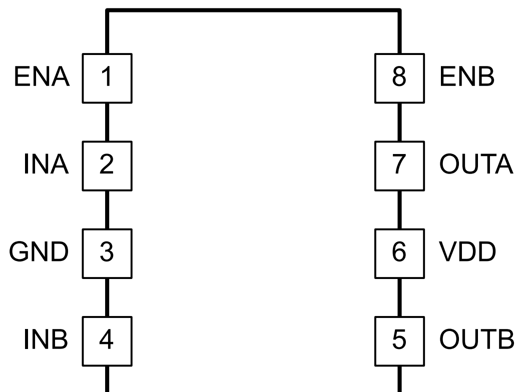

Figure 4-2. Pin Diagram (HVSSOP Package Topview)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA stuck low.	B
INA	2	OUTA stuck low	B
GND	3	No effect.	D
INB	4	OUTB stuck low.	B
OUTB	5	OUTB stuck low. Devie may be damaged.	A
VDD	6	No power is applied to the device.	D
OUTA	7	OUTA stuck low. Devie may be damaged.	A
ENB	8	OUTB stuck low.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA is enabled. OUTA follows INA command.	B
INA	2	OUTA stuck low.	B
GND	3	No power is applied to the device. OUTA and OUTB pulled up to VDD.	D
INB	4	OUTB stuck low.	B
OUTB	5	No effect. OUTB is disconnected from the gate of power stage.	D
VDD	6	No power is applied to the device.	D
OUTA	7	No effect. OUTA is disconnected from the gate of power stage.	B
ENB	8	OUTB is enabled. OUTB follows INB command.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	INA	Lose ENA disabling control of OUTA.	B
INA	2	GND	OUTA stuck low.	B
GND	3	INB	OUTB stuck low	B
OUTB	5	VDD	OUTB stuck high. Device may be damaged.	A
VDD	6	OUTA	OUTA stuck high. Device may be damaged.	A
OUTA	7	ENB	OUTA unknown. Device may be damaged.	A

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Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ENA	1	OUTA is enabled. OUTA follows INA command.	B
INA	2	OUTA is stuck high. Device may be damaged.	A
GND	3	No power is applied to the device.	D
INB	4	OUTB is stuck high.	B
OUTB	5	OUTB is stuck high. Device may be damaged.	A
VDD	6	No effect.	D
OUTA	7	OUTA is stuck high. Device may be damaged.	A
ENB	8	OUTB is enabled. OUTB follows INB command.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
6/2022		Initial Release

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