

# TPS62A2xx-Q1

## Functional Safety FIT Rate, FMD and Pin FMA

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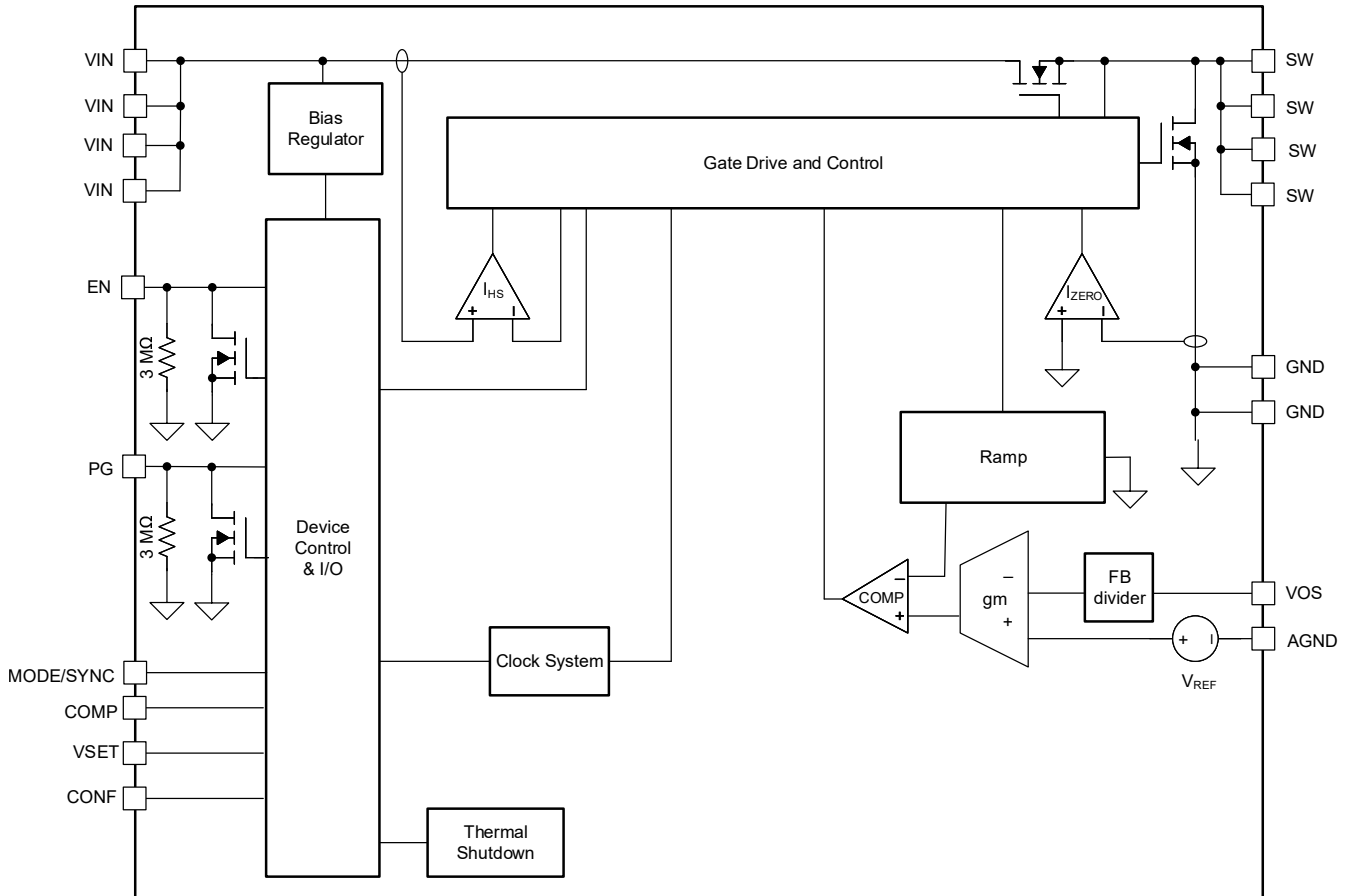
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## 1 Overview

This document contains information for the TPS62A2xx-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

The TPS62A2xx-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS62A2xx-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total component FIT rate	16
Die FIT rate	8
Package FIT rate	8

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1360mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS62A2xx-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
Software no output	20
Software output not in specification – voltage or timing	15
Software power high-side or low-side FET stuck on	35
EN or PG false trip or fails to trip	15
Switching frequency or output voltage range not in specification	15

The FMD in the *Die Failure Modes and Distribution* table excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to IEC 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS62A2xx-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

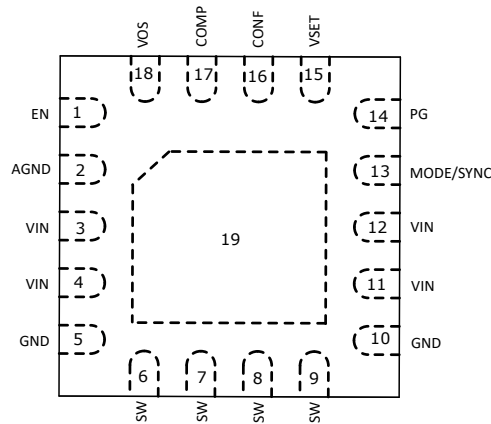
- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VIN (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the TPS62A2xx-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the [TPS62A2xx-Q1](#) datasheet.



**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The assumption is that the device is running in the typical application, please refer to the *Simplified Schematics* in the [TPS62A2xx-Q1](#) datasheet.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The device operates as normal. The device is disabled.	B
AGND	2	The device operates as normal, but the accuracy of the output voltage becomes increasingly worse.	C
VIN	3	The device does not power up and there is no output voltage.	B
VIN	4	The device does not power up and there is no output voltage.	B
GND	5	The device operates as normal.	D
SW	6	The device is potentially damaged.	A
SW	7	The device is potentially damaged.	A
SW	8	The device is potentially damaged.	A
SW	9	The device is potentially damaged.	A
GND	10	The device operates as normal.	D
VIN	11	The device does not power up and there is no output voltage.	B
VIN	12	The device does not power up and there is no output voltage.	B
MODE/SYNC	13	The device operates as normal and enters the FPWM mode of operation.	B
PG	14	The device operates as normal, but there is a loss of indication on the PG pin.	B
VSET	15	The device operates as normal. The VSET pin defines the start-up voltage.	B
CONF	16	The device operates as normal. The CONF pin defines the switching frequency and output voltage.	B
COMP	17	The device operates as normal. The COMP pin defines the compensation setting.	B
VOS	18	The device operates at the maximum duty cycle operation and the output voltage is unregulated.	B
GND	19	The device operates as normal.	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The pin is internally terminated with a 3MΩ resistor to GND. The device is disabled.	D
AGND	2	The device operates as normal, but the accuracy of the output voltage becomes increasingly worse.	C
VIN	3	The device operates as normal. The alternative VIN pins are still connected.	C
VIN	4	The device operates as normal. The alternative VIN pins are still connected.	C
GND	5	The device operates as normal. The alternative GND pins are still connected.	C
SW	6	The device operates as normal. The alternative SW pins are still connected.	C
SW	7	The device operates as normal. The alternative SW pins are still connected.	C
SW	8	The device operates as normal. The alternative SW pins are still connected.	C
SW	9	The device operates as normal. The alternative SW pins are still connected.	C
GND	10	The device operates as normal. The alternative GND pins are still connected.	C
VIN	11	The device operates as normal. The alternative VIN pins are still connected.	C
VIN	12	The device operates as normal. The alternative VIN pins are still connected.	C
MODE/SYNC	13	The device operates as normal. The operation mode is undefined.	B
PG	14	The device operates as normal, and there is a loss of indication on the PG pin.	B
VSET	15	The device operates as normal. The start-up voltage is undefined.	B
CONF	16	The device operates as normal. The switching frequency and output voltage are undefined.	B
COMP	17	The device operates as normal. The compensation setting is undefined.	B
VOS	18	The device goes out of regulation. The duty cycle is clamped at the maximum level.	B
GND	19	The device operates as normal. The alternative GND pins are still connected.	C

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN	1	2	The device operates as normal. The device is disabled.	B
AGND	2	3	The device does not power up and there is no output voltage.	B
VIN	3	4	The device operates as normal.	D
VIN	4	5	The device does not power up and there is no output voltage.	B
GND	5	6	The device is potentially damaged.	A
SW	6	7	The device operates as normal.	D
SW	7	8	The device operates as normal.	D
SW	8	9	The device operates as normal.	D
SW	9	10	The device is potentially damaged.	A
GND	10	11	The device does not power up and there is no output voltage.	B
VIN	11	12	The device operates as normal.	D
VIN	12	13	The device operates as normal and enters the PFM/PWM mode of operation.	B
MODE/SYNC	13	14	The device is potentially damaged.	A
PG	14	15	The device is potentially damaged.	A
VSET	15	16	The device does power up, but with the incorrect output voltage and switching frequency.	B
CONF	16	17	The device does power up, but with the incorrect output voltage and switching frequency.	B
COMP	17	18	The device is potentially damaged, or the device powers up with an incorrect compensation setting and the efficiency of the device degrades.	A
VOS	18	19	The device operates at the maximum duty cycle operation and the output voltage is unregulated.	B
GND	19	1	The device operates as normal. The device is disabled.	B

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	The device operates as normal.	D
AGND	2	The device does not power up and there is no output voltage.	B
VIN	3	The device operates as normal.	D
VIN	4	The device operates as normal.	D
GND	5	The device does not power up and there is no output voltage.	B
SW	6	The device is potentially damaged.	A
SW	7	The device is potentially damaged.	A
SW	8	The device is potentially damaged.	A
SW	9	The device is potentially damaged.	A
GND	10	The device does not power up and there is no output voltage.	B
VIN	11	The device operates as normal.	D
VIN	12	The device operates as normal.	D
MODE/SYNC	13	The device operates as normal and enters the PFM/PWM mode of operation.	B
PG	14	The device is potentially damaged.	A
VSET	15	The device operates as normal. The VSET pin defines the output voltage.	B
CONF	16	The device operates as normal. The CONF pin defines the switching frequency and output voltage.	B
COMP	17	The device operates as normal. The COMP pin defines the compensation setting.	B
VOS	18	The device is potentially damaged.	A

**Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)**

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	19	The device does not power up and there is no output voltage.	B

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

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