Functional Safety Information

INA241x-Q1 and INA296x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the INA241x-Q1 and INA296x-Q1 (SOT-23-8 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

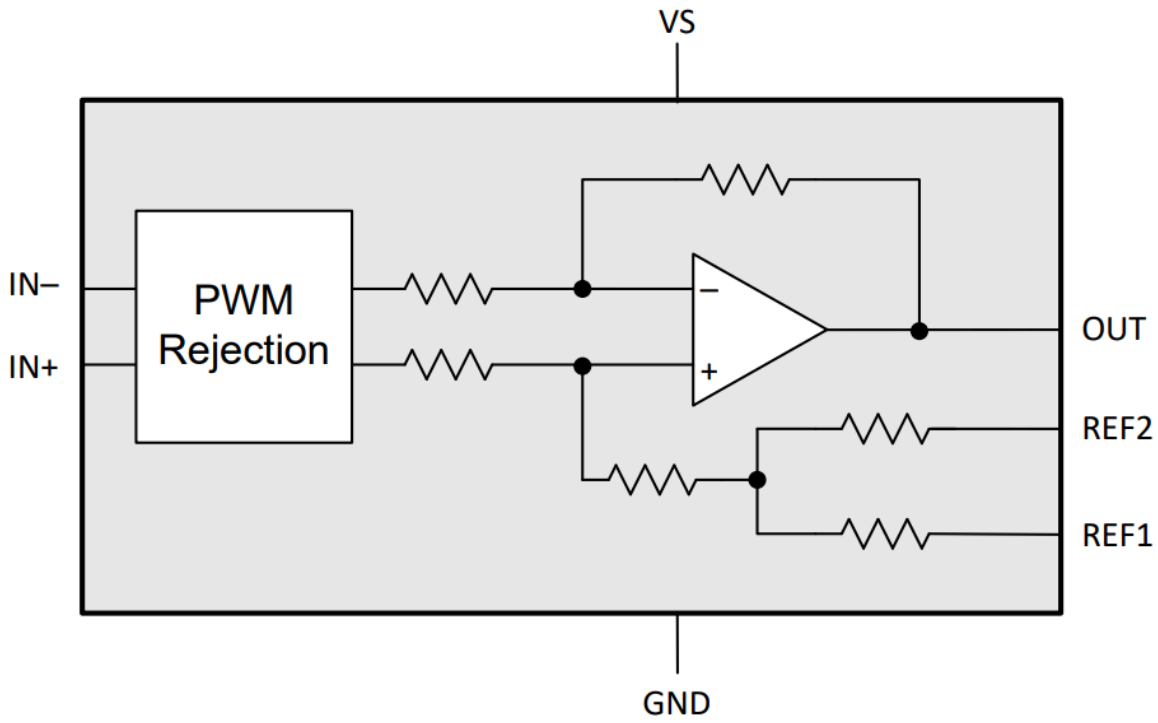

Figure 1-1. Functional Block Diagram

The INA241x-Q1 and INA296x-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23-8 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23-8 package of the INA241x-Q1 and INA296x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the INA241x-Q1 and INA296x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	10
Output to GND	30
Output to VS	30
Output functional, not in specification	10
Pin to pin short, any two pins	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the INA241x-Q1 and INA296x-Q1 (SOT-23-8 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Vs = 5 V
- Vcm = 48 V
- REF1 = REF2 = Vs / 2

4.1 SOT-23-8 Package

Figure 4-1 shows the INA241x-Q1 and INA296x-Q1 pin diagrams for the SOT-23-8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the INA241x-Q1 and INA296x-Q1 data sheets.

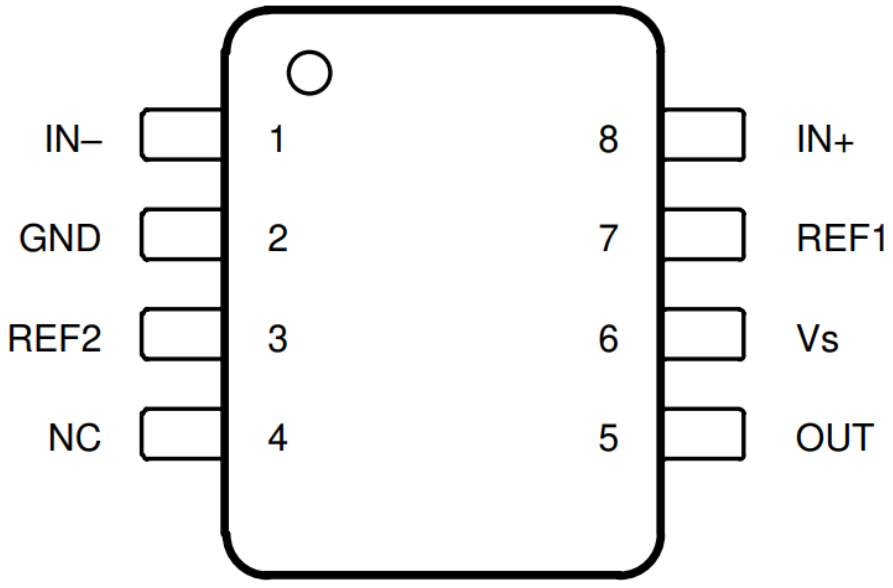

Figure 4-1. Pin Diagram (SOT-23-8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation	B for High side or D for low side
GND	2	Normal operation	D
REF2	3	If intended connection is anything other than GND, functionality will be affected	D if REF2=GND by design; B otherwise
NC	4	Normal operation	D
OUT	5	Output shorts to ground	B
Vs	6	Power supply shorted to ground	B
REF1	7	If intended connection is anything other than GND, functionality will be affected	D if REF1=GND by design; B otherwise
IN+	8	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	1	IN- will be at the same potential as IN+. Differential input voltage is effectively 0V	B
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND	B
REF2	3	Device loses reference voltage	B
NC	4	This pin has internal weak pull down. Even though possible, the likelihood of malfunction is low	D
OUT	5	Output can be left open, there is no effect on the IC	C
Vs	6	No power supply to device. Device may be biased through inputs. Output will be close to GND	B
REF1	7	Device loses reference voltage	B
IN+	8	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0V	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN-	1	GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation	B for High side or D for low side
GND	2	REF2	If intended connection is anything other than GND, functionality will be affected	D if REF2=GND by design; B otherwise
REF2	3	NC	Functionality will be affected if REF2 equals to anything but GND by design	C
NC	4	OUT	Changing output may affect functionality, but the likelihood is very low	C
OUT	5	Vs	Output shorts to supply	B
Vs	6	REF1	Functionality will be affected if REF1 equals to anything but Vs by design	D if REF1=Vs by design; B otherwise
REF1	7	IN+	If high voltage (>5.5V) is present, damage will occur	A
IN+	8	IN-	Input differential voltage=0V	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to Vs will occur. High current will flow from bus supply to Vs or vice versa. Device could be damaged	A for High side or B for low side
GND	2	Power supply shorted to GND	B
REF2	3	If intended connection is anything other than Vs, functionality will be affected	D if REF2=Vs by design; B otherwise
NC	4	Additional small amount of current is drawn by the pull down resistor	C
OUT	5	Output shorts to supply	B
Vs	6	Normal operation	D
REF1	7	If intended connection is anything other than Vs, functionality will be affected	D if REF1=Vs by design; B otherwise
IN+	8	In high-side configuration, a short from the bus supply to Vs will occur. High current will flow from bus supply to Vs or vice versa. Device could be damaged	A for High side or B for low side

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265