*Functional Safety Information*

# *LM74502-Q1, LM74502H-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

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# 1 Overview

This document contains information for LM74502-Q1, LM74502H-Q1 (SOT-23 8 pin DDF package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

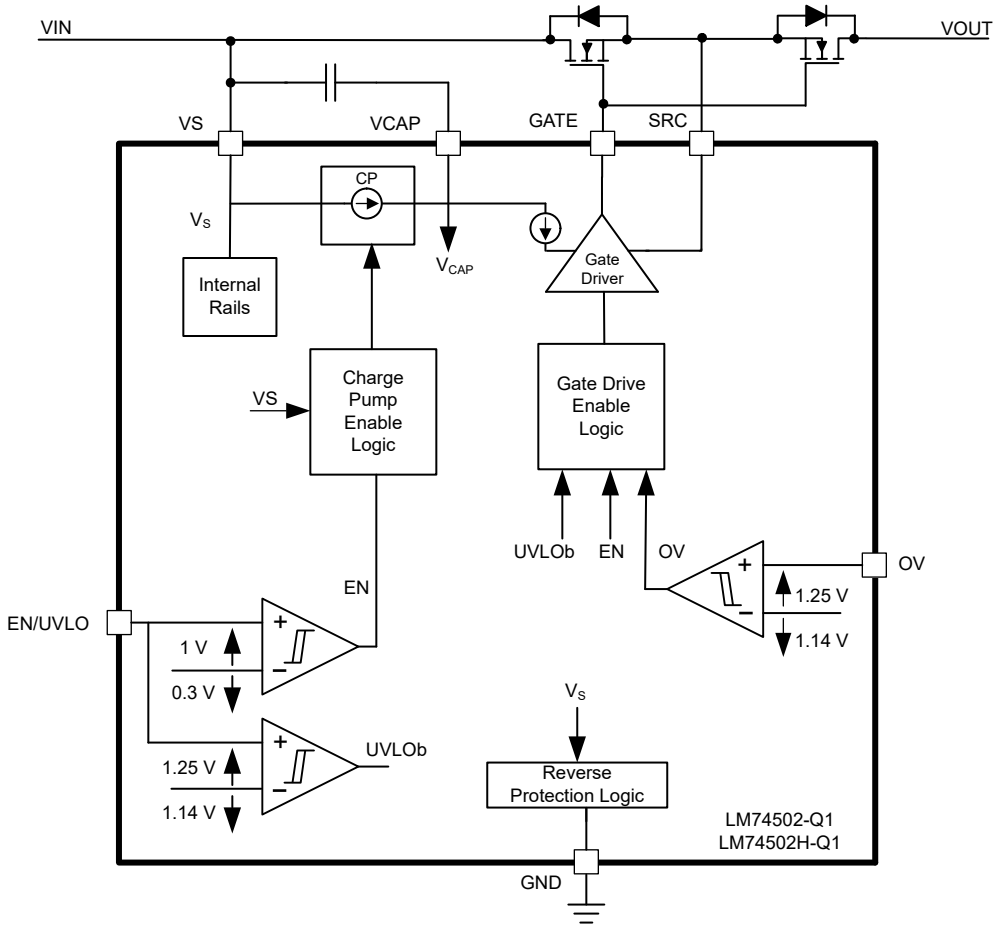


**Figure 1-1. Functional Block Diagram**

LM74502-Q1, LM74502H-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM74502-Q1, LM74502H-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 5 |
| Die FIT Rate | 3 |
| Package FIT Rate | 2 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 3.9mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 20 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM74502-Q1, LM74502H-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress. This failure mode distribution estimation is applicable for SOT-23 8 pin DDF package.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| GATE output stuck Low or HIZ | 45% |
| GATE output not in specification – voltage or timing | 50% |
| Short circuit any two pins | 5% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM74502-Q1, LM74502H-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Figure 4-1 shows the LM74502-Q1, LM74502H-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM74502-Q1, LM74502H-Q1 data sheet.

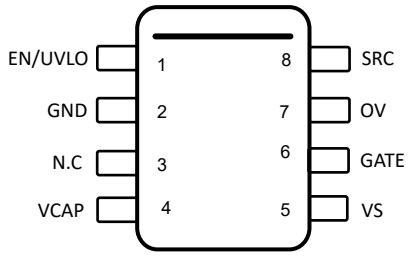


**Figure 4-1. Pin Diagram (DDF Package)**

The pin FMA is provided under the assumption that the device is operating under the specified ranges within the Recommended Operating Conditions section of the data sheet.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| EN/UVLO | 1 | Device will not power up and will be in shutdown mode. | B |
| GND | 2 | No effect on device behavior. | D |
| N.C | 3 | No effect on the device behavior. | D |
| VCAP | 4 | Device may heat up and damage due to increased quiescent current. | A |
| VS | 5 | Device will not power up. This is equivalent to input supply shorted to ground. | B |
| GATE | 6 | External MOSFET will not turn on. Device may heat up and damage due to increased quiescent current. | A |
| OV | 7 | Overvoltage functionality will not be available. | B |
| SRC | 8 | Device quiescent current may increase. Based on input voltage, external MOSFET may sustain damage due to GATE to SOURCE maximum voltage specification violation. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| EN/UVLO | 1 | Device will not power up and will be in shutdown mode due to internal pull down on EN/UVLO pin. | B |
| GND | 2 | Device will not power up. | B |
| N.C | 5 | No effect on the device behavior. | D |
| VCAP | 4 | Charge pump will not come up. External FET will be off. | B |
| VS | 5 | Device will not power up. This is equivalent to input supply not available. | B |
| GATE | 6 | External FET will not turn on. | B |
| OV | 7 | Overvoltage functionality will not be available. | B |
| SRC | 8 | Device will not be able to turn off external FETs completely. System will not have any protection from input reverse polarity after external FETs are turned on. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| EN/UVLO | 1 | GND | Device will not power up and will be in shutdown mode. | B |
| GND | 2 | N.C | No effect on the device performance. | D |
| N.C | 3 | VCAP | No effect on the device performance. | D |
| VCAP | 4 | - | VCAP is the corner pin. No effect on the device performance. | D |
| VS | 5 | GATE | External FET will not turn on. Device quiescent current may increase. | B |
| GATE | 6 | OV | Device GATE drive will be turned off due to OV comparator trigger. | B |
| OV | 7 | SRC | Device GATE drive will be turned off due to OV comparator trigger. Device GATE pin may oscillate between on and off state. | B |
| SRC | 8 | - | SRC is the corner pin. No effect on the device performance. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| EN/UVLO | 1 | Device will always be on. | B |
| GND | 2 | Device will not power up. It is equivalent to input supply short condition. | B |
| N.C | 3 | No effect on the device performance. | D |
| VCAP | 4 | Device charge pump will not come up. External FET will be off. | B |
| VS | 5 | No effect on the device performance. | D |
| GATE | 6 | External FET will be off. | B |
| OV | 7 | Device will be off due to OV comparator trigger. | B |
| SRC | 8 | Device will not be able to disconnect the load from supply due to input supply to SRC pin shorting. | B |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265