Functional Safety Information

TMP1827
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TMP1827 (WSON-8 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

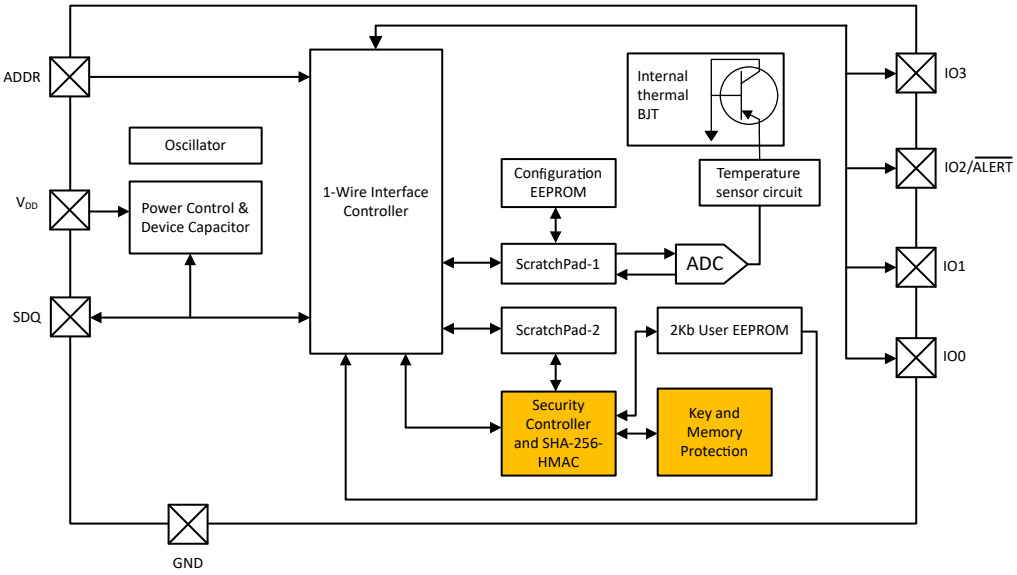

Figure 1-1. Functional Block Diagram

The TMP1827 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TMP1827 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 1.0 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMP1827 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Serial Communication Error	15%
ADC offset out of specification	10%
ADC gain out of specification	15%
ADC conversion output code bit error	20%
Scratchpad data bit error	20%
Internal capacitor fail to charge	20%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMP1827 (VSSOP-8 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2.)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on SDQ
- External resistor to GND connected to ADDR pin
- External pullup resistor to IO's connected to VDD
- Multi device environment. More than one device on single wire bus

4.1 WSON-8 Package

Figure 4-1 shows the TMP1827 pin diagram for the WSON-8 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMP1827 data sheet.

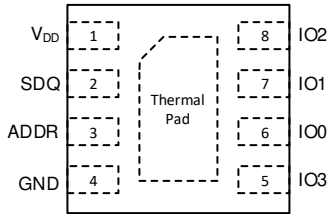

Figure 4-1. Pin Diagram (WSON-8 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	3	Limited address selection. Application has to revert to 64 bit addressing mode.	C
		If ADDR selection is not being used then no effect.	D
GND	4	No effect. Normal operation.	D
IO0	6	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO1	7	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO2	8	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO3	5	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
SDQ	2	No communication	B
VDD	1	Device is in bus powered mode	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	3	Limited address selection. Application has to revert to 64 bit addressing mode.	C
GND	4	When floating, possible latch-up	B
IO0	6	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO1	7	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO2	8	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO3	5	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
SDQ	2	No communication	B
VDD	1	Device is in bus powered mode	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	3	SDQ	The absolute maximum for ADDR pin is 1.65 V and if shorted to SDQ and SDQ being pulled to 5.5V could cause leakage currents to increase and damage the device during ADDR detection.	A
GND	4	ADDR	If ADDR is shorted to GND then limited address selection. Application has to revert to 64 bit addressing mode.	C
			GND is shorted to ADDR will have no affect during normal operation.	D
IO0	6	IO1	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
IO0	6	IO3	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
IO1	7	IO2	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
IO1	7	IO0	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
IO2	8	IO1	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
IO3	5	IO0	If I/O is used for controlling external component, functionality is lost.	B
			If I/O is not being used then no effect.	D
SDQ	2	VDD	Loss of functionality. Communication will be lost.	B
VDD	1	SDQ	Loss of functionality. Communication will be lost.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ADDR	3	Absolute maximum could be exceeded if ADDR pin is being used for address decoding.	A
		Other cases no device damage.	D
GND	4	Device unpowered. Device not functional. Make sure that the absolute maximum ratings for all device pins are met, otherwise device damage may be plausible.	B
IO0	6	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO1	7	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO2	8	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
IO3	5	If I/O is used for controlling external component, functionality is lost.	B
		If I/O is not being used then no effect.	D
SDQ	3	Loss of functionality. Communication will be lost.	B
VDD	1	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (May 2023) **Page**

- Removed the VSSOP-8 package 2
- Changed the *Functional Block Diagram* 2

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