Functional Safety Information

LM25149
Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for LM25149 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

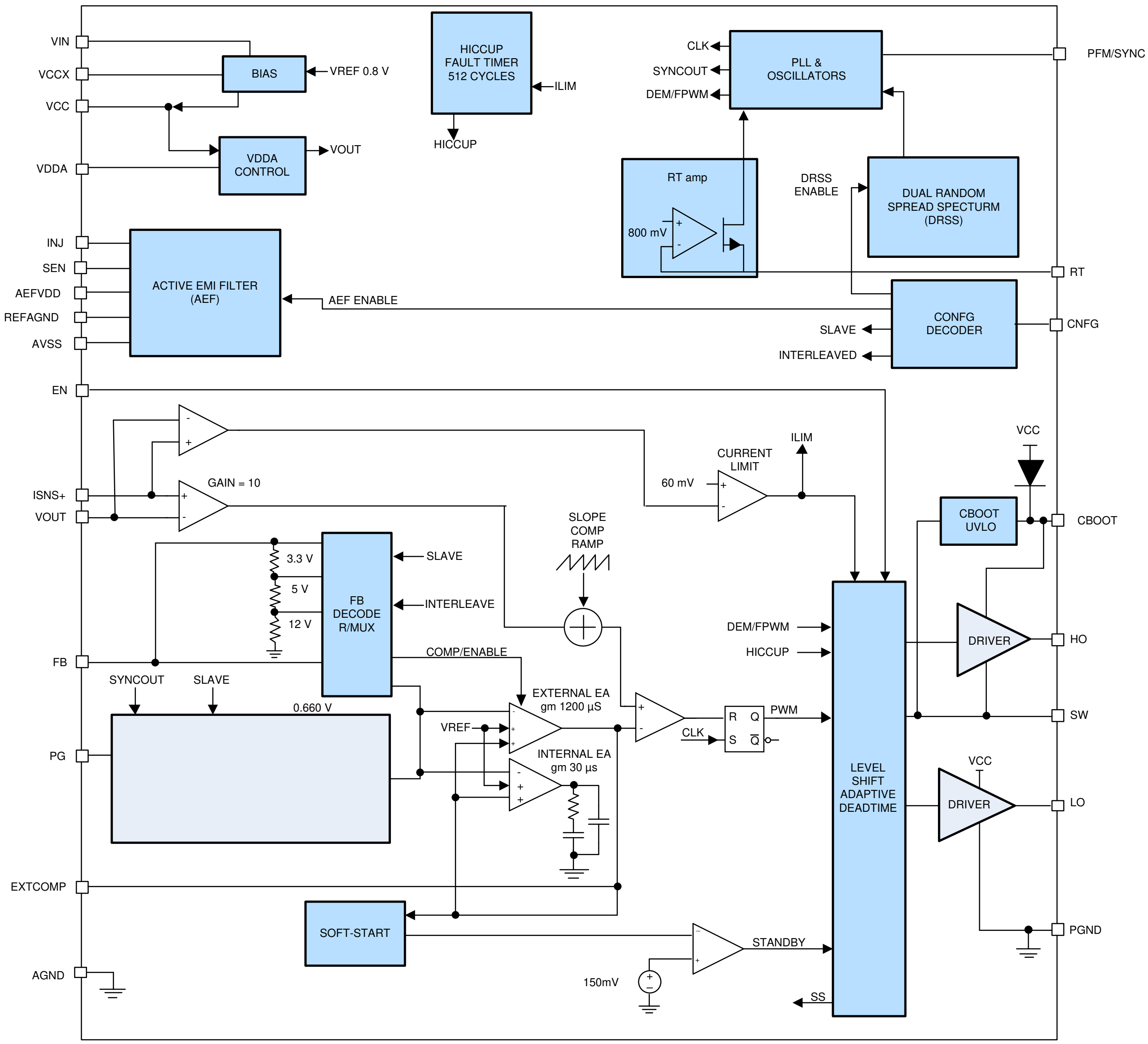

Figure 1-1. Functional Block Diagram

LM25149 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM25149 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	6
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog & mixed HV >50V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM25149 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification – voltage or timing	25%
Gate driver stuck on	5%
Power Good - False trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM25149. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM25149 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM25149 data sheet.

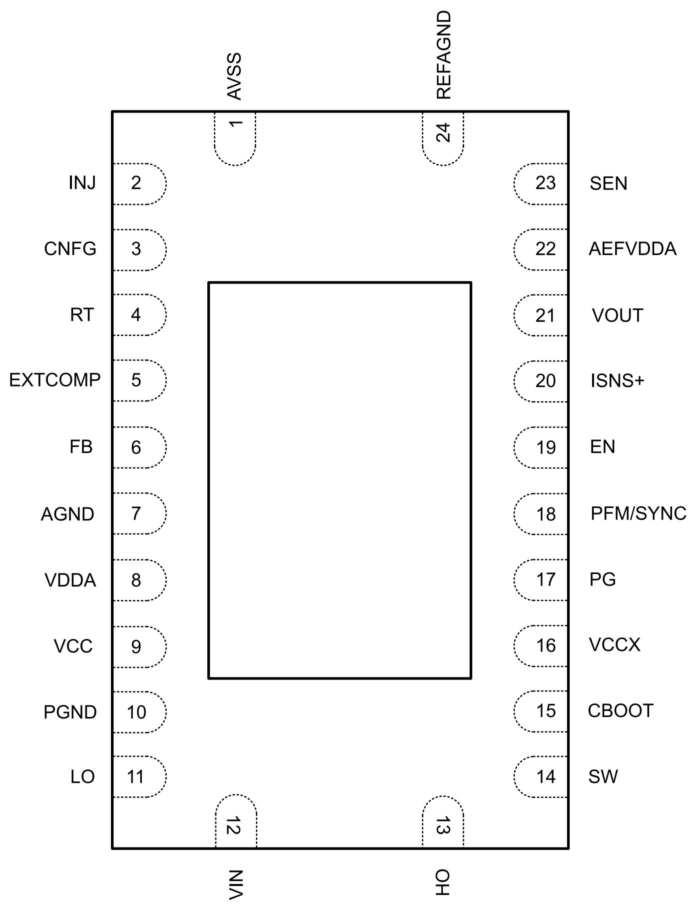

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application Circuit as per the LM25149 data sheet is used
  - PG is pulled up to VOUT

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVSS	1	AVSS is ground. V_{OUT} = expected V_{OUT}	D
INJ	2	Active EMI filtering will not work but the regulator will continue regulating. V_{OUT} = expected V_{OUT}	C
CNFG	3	Active EMI filtering will be disabled. V_{OUT} is unaffected.	C
RT	4	V_{OUT} will attempt to regulate at maximum f_{SW}, causing maximum power dissipation.	B
EXTCOMP	5	V_{OUT} = 0 V	B
FB	6	Internal FB mode, V_{OUT} = expected V_{OUT}	D
		External FB mode, V_{OUT} = V_{IN}	A
AGND	7	AGND is GND. V_{OUT} = expected V_{OUT}	D
VDDA	8	V_{OUT} = 0 V, no switching, loaded VCC output	B
VCC	9	V_{OUT} = 0 V, no switching, loaded VCC output	B
PGND	10	PGND is GND. V_{OUT} = expected V_{OUT}	D
LO	11	V_{OUT} = 0 V, VCC regulator loaded to the current limit	B
VIN	12	V_{OUT} = 0 V	B
HO	13	V_{OUT} = 0 V, VCC regulator loaded to the current limit	B
SW	14	V_{OUT} = 0 V. High-side FET is shorted from VIN to GND.	A
CBOOT	15	V_{OUT} = 0, VCC regulator loaded to the current limit	B
VCCX	16	V_{OUT} = expected V_{OUT}. The internal VCC regulator provides bias voltage.	C
PG	17	If in single phase, PG has no effect on operation. V_{OUT} = expected V_{OUT}	C
		If in interleaved primary mode, the secondary will detect no clock input and will shut down. Secondary phase is disabled and primary phase can current limit.	B
PFM/SYNC	18	V_{OUT} = expected V_{OUT}. No synchronization will be available and the LM25149 will be in FPWM mode.	C
EN	19	V_{OUT} = 0 V. The LM25149 enters shutdown.	C
ISNS+	20	V_{OUT} = 0 V; HO damaged	A
VOUT	21	V_{OUT} = 0 V. Current limit reached and hiccup mode occurs.	B
AEFVDDA	22	AEFVDDA = VCC. VCC is shorted and V_{OUT} = 0 V. VCC is loaded.	B
SEN	23	Active EMI filtering will not work but the regulator will continue regulating. V_{OUT} = expected V_{OUT}	B
REFAGND	24	REFAGND is ground. V_{OUT} = expected V_{OUT}	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVSS	1	Active EMI filtering will not work but the regulator will continue regulating. V_{OUT} = expected V_{OUT}	C
INJ	2	Active EMI filtering will not work but the regulator will continue regulating. V_{OUT} = expected V_{OUT}	C
CNFG	3	V_{OUT} will continue operating normally. CNFG is used during start-up and enables AEF.	C
RT	4	RT will regulate to 500 mV, but the internal oscillator will not function.	B
EXTCOMP	5	V_{OUT} will oscillate. If V_{OUT} oscillates to V_{IN}, damage can occur if V_{IN} > 60 V.	A
FB	6	Internal FB mode, V_{OUT} = expected V_{OUT}	D
		External FB mode, V_{OUT} = V_{IN}	A
AGND	7	V_{OUT} is indeterminate.	B
VDDA	8	Poor noise immunity	C
VCC	9	V_{OUT} = 0 V	B
PGND	10	V_{OUT} = 0 V	B
LO	11	V_{OUT} = expected V_{OUT} with reduced efficiency	C
VIN	12	V_{OUT} = 0 V	C
HO	13	If HO is opened while HO to SW has voltage, the high-side FET will never turn off. V_{OUT} = V_{IN}	A

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	14	V_{OUT} is indeterminate. The CBOOT floating rail has no reference to the actual SW node. V_{OUT} = V_{IN}	A
CBOOT	15	V_{OUT} = 0 V	B
VCCX	16	VCCX is held to ground by a weak pulldown. V_{OUT} = expected V_{OUT}	D
PG	17	If in single phase, PG has no effect on operation. V_{OUT} = expected V_{OUT}	C
		If in interleaved primary mode, the secondary will detect no clock input and will shut down. The secondary phase is disabled and primary phase can current limit.	B
PFM/SYNC	18	V_{OUT} = expected V_{OUT}	D
EN	19	V_{OUT} = expected V_{OUT}	D
ISNS+	20	The OPEN ISNS+ pin will block current limit and cause V_{OUT} oscillations.	A
VOUT	21	V_{OUT} = 0 V	B
AEFVDDA	22	Active EMI filtering will not function.	C
SEN	23	Active EMI filtering will not function.	C
REFAGND	24	Active EMI filtering will not function.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AVSS	1	INJ	Active EMI filtering will not function. VOUT = expected V_{OUT}	C
INJ	2	CNFG	Active EMI filtering will not function. VOUT = expected V_{OUT}	C
CNFG	3	RT	V_{OUT} = expected V_{OUT} with erratic switching	B
RT	4	EXTCOMP	COMP cannot regulate down due to clamping by the internal RT.	B
EXTCOMP	5	FB	External FB mode: COMP will regulate to .8 V and the output will be unregulated. V_{OUT} = any voltage	B
			Internal FB mode: COMP will rise up to VDD. V_{OUT} = V_{IN}	A
FB	6	AGND	External FB mode: V_{OUT} = V_{IN}	A
			Internal FB mode: V_{OUT} = expected V_{OUT}	D
AGND	7	VDDA	VDDA will be grounded. V_{OUT} = 0 V	B
VDDA	8	VCC	V_{OUT} = expected V_{OUT}	D
VCC	9	PGND	VCC will be grounded. V_{OUT} = 0 V	B
PGND	10	LO	V_{OUT} = 0 V. VCC is loaded by LO driver.	B
LO	11	VIN	V_{OUT} = 0 V. The driver will be damaged if V_{IN} > 6.5 V.	A
VIN	12	HO	V_{OUT} = V_{IN}	A
HO	13	SW	V_{OUT} = 0 V	B
SW	14	CBOOT	V_{OUT} = 0 V	B
CBOOT	15	VCCX	V_{OUT} < 5 V	A
VCCX	16	PG	PG pulldown can damage. V_{OUT} = expected V_{OUT}	A
PG	17	PFM/SYNC	V_{OUT} = expected V_{OUT}	C
PFM/SYNC	18	EN	V_{OUT} = expected V_{OUT}	A
EN	19	ISNS+	EN is high voltage rated. V_{OUT} = expected V_{OUT} if V_{OUT} > 1 V. If V_{OUT} < 1 V, the device is disabled.	B
ISNS+	20	VOUT	Current limit is disabled since the current limit resistor would be shorted. V_{OUT} cannot regulate since current mode feedback is shorted.	A
VOUT	21	AEFVDDA	Active EMI filtering will not function and damage will occur if V_{OUT} > 6.5 V. V_{OUT} = expected V_{OUT}	A
AEFVDDA	22	SEN	Active EMI filtering will not function. V_{OUT} = expected V_{OUT}	C
SEN	23	REFAGND	Active EMI filtering will not function. V_{OUT} = expected V_{OUT}	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
REFAGND	24	AVSS	No impact	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVSS	1	Active EMI filtering will not function, high V_{IN} current	A
INJ	2	Active EMI filtering will not function, high V_{IN} current	A
CNFG	3	$V_{OUT} = V_{IN}$	A
RT	4	V_{OUT} = 0 V; high V_{IN} current	A
EXTCOMP	5	This will bring VDDA up to V_{IN}. $V_{OUT} = V_{IN}$.	A
FB	6	This will bring VDDA up to V_{IN}. $V_{OUT} = V_{IN}$	A
AGND	7	$V_{OUT} = V_{IN}$; high VIN current	A
VDDA	8	If V_{IN} < 6.5 V, V_{OUT} = expected V_{OUT}	D
		If V_{IN} > 6.5 V, exceeds maximum ratings and VDDA is damaged.	A
VCC	9	If V_{IN} < 6.5 V, V_{OUT} = expected V_{OUT}	D
		If V_{IN} > 6.5 V, exceeds maximum ratings and VCC is damaged.	A
PGND	10	V_{OUT} = VIN; high V_{IN} current	A
LO	11	For V_{IN} < 6.5 V, V_{OUT} = 0; excess current from V_{IN}	B
		For V_{IN} > 6.5 V, exceeds maximum ratings and pin LO is damaged.	A
VIN	12	N/A	D
HO	13	For V_{IN} < 6.5 V, V_{OUT} = dropout lower than V_{IN}, no switching, excess current from V_{IN}	B
		For V_{IN} > 6.5 V, exceeds maximum ratings and HO is damaged, $V_{OUT} = V_{IN}$	A
SW	14	$V_{OUT} = V_{IN}$, excess current from V_{IN}. LO turns on and shorts against V_{IN}.	A
CBOOT	15	For V_{IN} < 6.5 V, V_{OUT} = expected V_{OUT}, erratic switching	B
		For V_{IN} > 6.5 V, exceeds maximum ratings and the CBOOT pin is damaged, HO damaged. $V_{OUT} = V_{IN}$	A
VCCX	16	If VCCX = V_{OUT}, for V_{IN} < 6.5 V, $V_{OUT} = V_{IN}$	B
		For V_{IN} > 6.5 V, exceeds maximum ratings and VCCX is damaged.	A
PG	17	For V_{IN} < 6.5 V, V_{OUT} = expected V_{OUT}, PG forced high	B
		For V_{IN} > 6.5 V, exceeds maximum ratings and PG is destroyed.	A
PFM/SYNC	18	If PFM = GND, V_{OUT} = 0 V, excess current from V_{IN}	B
		If PFM = VDDA and V_{IN} < 6.5 V, V_{OUT} = expected V_{OUT} and erratic switching.	B
		If V_{IN} > 6.5 V, exceeds maximum ratings and PFM is damaged. V_{OUT} = expected V_{OUT}	A
EN	19	The part will be always on. V_{OUT} = expected V_{OUT}	C
ISNS+	20	If V_{IN} < 60 V, $V_{OUT} = V_{IN}$	B
		If V_{IN} > 60 V, exceeds maximum ratings and CS is damaged.	A
VOUT	21	If V_{IN} < 60 V, $V_{OUT} = V_{IN}$	B
		If V_{IN} > 60 V, exceeds maximum ratings and CS is damaged.	A
AEFVDDA	22	Active EMI filtering will not function, high V_{IN} current	A
SEN	23	Active EMI filtering will not function, high V_{IN} current	A
REFAGND	24	Active EMI filtering will not function, high V_{IN} current	A