

# ADS131B04-Q1

## Functional Safety FIT Rate and Pin FMA



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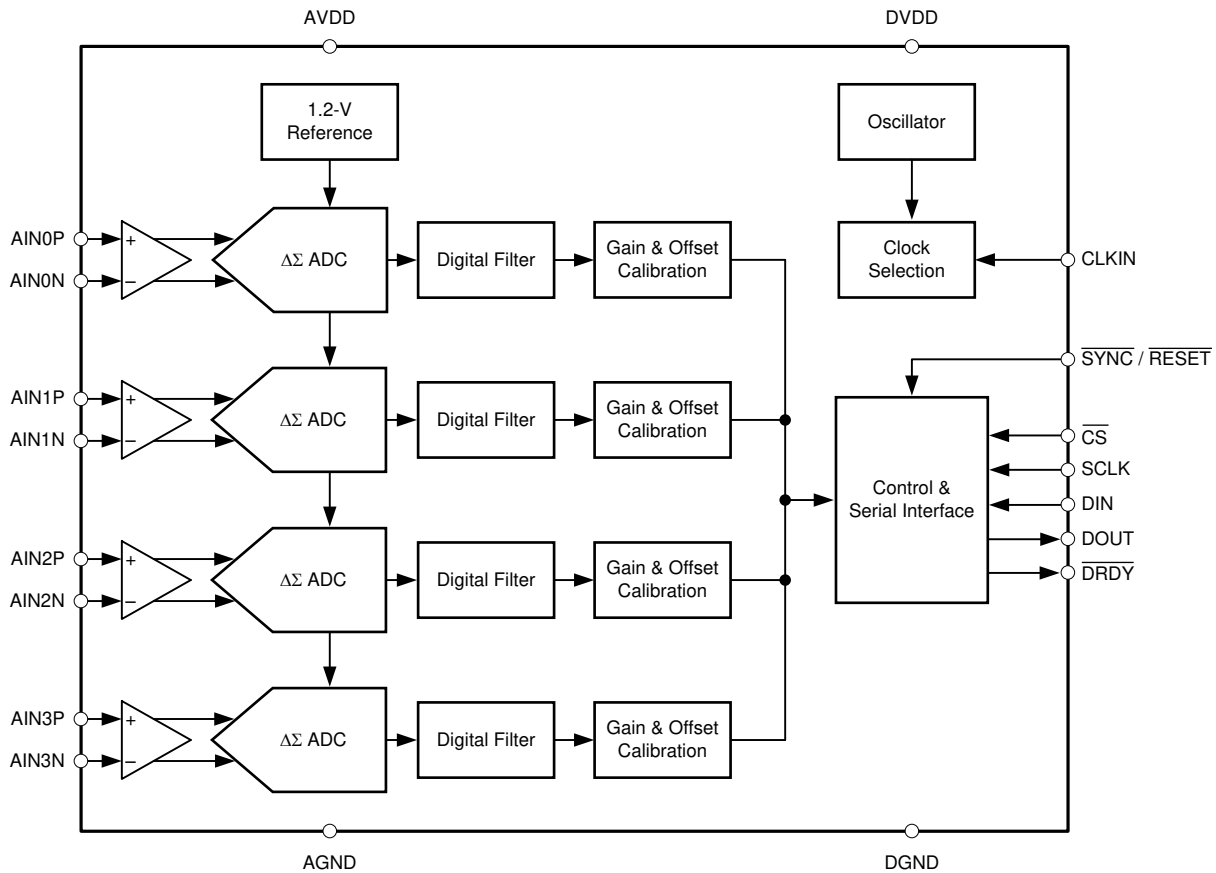
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## 1 Overview

This document contains information for ADS131B04-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



**Figure 1-1. Functional Block Diagram**

ADS131B04-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for ADS131B04-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT Rate	13
Die FIT Rate	2
Package FIT Rate	11

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 28.1 mW
- Climate type: World-wide Table 8
- Package factor ( $\lambda_3$ ): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ADS131B04-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

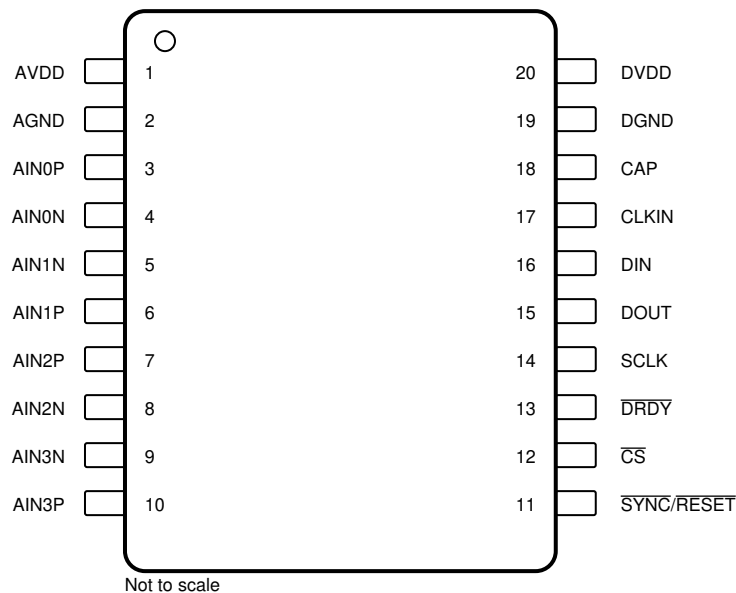
- Pin short-circuited to Ground (see [Table 3-2](#))
- Pin open-circuited (see [Table 3-3](#))
- Pin short-circuited to an adjacent pin (see [Table 3-4](#))
- Pin short-circuited to supply (see [Table 3-5](#))

[Table 3-2](#) through [Table 3-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 3-1](#).

**Table 3-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 3-1](#) shows the ADS131B04-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ADS131B04-Q1 data sheet.



**Figure 3-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same 3.3-V supply voltage.
- 'Short circuit to supply' means short to AVDD = DVDD.
- 'Short circuit to ground' means short to AGND = DGND.
- Differential RC filters on every ADC channel.  
Series resistors are sized to limit the input currents into the analog inputs to <10mA in all circumstances, e.g. also in case device is unpowered and input signal is applied.
- External pulldown resistor ( $\geq 1k\Omega$ ) on CLKIN to DGND in case the device is configured for use with the internal oscillator.
- Device is the only slave on the SPI bus.

**Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	No effect. Normal operation.	D
AIN0P	3	AIN0P stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AGND - V_{AIN0N}$ . Conversion results of ADC0 incorrect.	B
AIN0N	4	AIN0N stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = V_{AIN0P} - AGND$ . Conversion results of ADC0 incorrect.	B
AIN1N	5	AIN1N stuck low. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = V_{AIN1P} - AGND$ . Conversion results of ADC1 incorrect.	B
AIN1P	6	AIN1P stuck low. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = AGND - V_{AIN1N}$ . Conversion results of ADC1 incorrect.	B
AIN2P	7	AIN2P stuck low. $V_{IN2} = V_{AIN2P} - V_{AIN2N} = AGND - V_{AIN2N}$ . Conversion results of ADC2 incorrect.	B
AIN2N	8	AIN2N stuck low. $V_{IN2} = V_{AIN2P} - V_{AIN2N} = V_{AIN2P} - AGND$ . Conversion results of ADC2 incorrect.	B
AIN3N	9	AIN3N stuck low. $V_{IN3} = V_{AIN3P} - V_{AIN3N} = V_{AIN3P} - AGND$ . Conversion results of ADC3 incorrect.	B
AIN3P	10	AIN3P stuck low. $V_{IN3} = V_{AIN3P} - V_{AIN3N} = AGND - V_{AIN3N}$ . Conversion results of ADC3 incorrect.	B
SYNC/RESET	11	SYNC/RESET stuck low. Device held in reset.	B
$\overline{CS}$	12	$\overline{CS}$ stuck low. Normal operation when trying to communicate with ADS131B04-Q1.	B
DRDY	13	$\overline{DRDY}$ stuck low. No data ready indication through $\overline{DRDY}$ pin to host possible. Increase in supply current when DRDY tries to drive high in case bit DRDY_HiZ = 0b. Device damage plausible if $\overline{DRDY}$ drives high for extended period of time.	A
SCLK	14	SCLK stuck low. No SPI communication with device possible.	B
DOUT	15	DOUT stuck low. No SPI communication back to host possible. Increase in supply current when DOUT tries to drive high. Device damage plausible if DOUT drives high for extended period of time.	A
DIN	16	DIN stuck low. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock: CLKIN stuck low. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator: CLKIN stuck low. No effect. Normal operation.	D
CAP	18	Device unpowered. Device not functional.	B
DGND	19	No effect. Normal operation.	D
DVDD	20	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

**Table 3-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device functionality undetermined. Device unpowered and not functional if all external analog pins are held low. Device may power up through internal ESD diodes to AVDD if voltages above the device's power-on reset threshold are present on any of the analog pins.	B
AGND	2	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
AIN0P	3	State of AIN0P input undetermined. Conversion results of ADC0 undetermined.	B
AIN0N	4	State of AIN0N input undetermined. Conversion results of ADC0 undetermined.	B
AIN1N	5	State of AIN1N input undetermined. Conversion results of ADC1 undetermined.	B
AIN1P	6	State of AIN1P input undetermined. Conversion results of ADC1 undetermined.	B
AIN2P	7	State of AIN2P input undetermined. Conversion results of ADC2 undetermined.	B
AIN2N	8	State of AIN2N input undetermined. Conversion results of ADC2 undetermined.	B
AIN3N	9	State of AIN3N input undetermined. Conversion results of ADC3 undetermined.	B
AIN3P	10	State of AIN3P input undetermined. Conversion results of ADC3 undetermined.	B
SYNC/RESET	11	State of SYNC/RESET input undetermined. Device functionality undetermined. Device may operate normally or be held in reset.	B
CS	12	State of CS input undetermined. SPI communication corrupted.	B
DRDY	13	State of DRDY output undetermined. No data ready indication through DRDY pin to host possible.	B
SCLK	14	State of SCLK input undetermined. No SPI communication with device possible.	B
DOUT	15	State of DOUT output undetermined. No SPI communication back to host possible.	B
DIN	16	State of DIN input undetermined. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock: State of CLKIN input undetermined. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator: State of CLKIN input undetermined. No effect. Normal operation.	D
CAP	18	Internal digital LDO unstable. Device functionality undetermined.	B
DGND	19	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
DVDD	20	Device functionality undetermined. Device unpowered and not functional if all external digital pins are held low. Device may power up through internal ESD diodes to DVDD if voltages above the device's power-on reset threshold are present on any of the digital pins.	B

**Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	AGND	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	2	AIN0P	AIN0P stuck low. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AGND - V_{AIN0N}$ . Conversion results of ADC0 incorrect.	B
AIN0P	3	AIN0N	$V_{IN0} = V_{AIN0P} - V_{AIN0N} = 0$ V. Conversion result of ADC0 close to 0 V.	B
AIN0N	4	AIN1N	Conversion results of ADC0 and ADC1 undetermined.	B
AIN1N	5	AIN1P	$V_{IN1} = V_{AIN1P} - V_{AIN1N} = 0$ V. Conversion result of ADC1 close to 0 V.	B
AIN1P	6	AIN2P	Conversion results of ADC1 and ADC2 undetermined.	B
AIN2P	7	AIN2N	$V_{IN2} = V_{AIN2P} - V_{AIN2N} = 0$ V. Conversion result of ADC2 close to 0 V.	B
AIN2N	8	AIN3N	Conversion results of ADC2 and ADC3 undetermined.	B
AIN3N	9	AIN3P	$V_{IN3} = V_{AIN3P} - V_{AIN3N} = 0$ V. Conversion result of ADC3 close to 0 V.	B
AIN3P	10	SYNC/RESET	Not considered. Corner pin.	D
SYNC/RESET	11	$\overline{CS}$	Device behavior dependent on drive strength of control signals driving $\overline{CS}$ and SYNC/RESET pins. In case SYNC/RESET control signal can overdrive $\overline{CS}$ control signal: $\overline{CS}$ stuck high or SPI communication corrupted. No SPI communication with device possible. In case $\overline{CS}$ control signal can overdrive SYNC/RESET control signal: Device will synchronize conversions every time $\overline{CS}$ transitions high. Conversion results are valid but data ready is indicated outside the expected time window. In case the SYNC/RESET pin is held low for longer than the reset time period, then device reset will occur.	B
$\overline{CS}$	12	$\overline{DRDY}$	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when $\overline{DRDY}$ tries to drive low while $\overline{CS}$ is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
$\overline{DRDY}$	13	SCLK	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when $\overline{DRDY}$ tries to drive low while SCLK is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
SCLK	14	DOUT	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DOUT tries to drive low while SCLK is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
DOUT	15	DIN	SPI communication corrupted. No SPI communication with device possible. Increase in supply current possible when DOUT tries to drive low while DIN is driven high and vice versa. Device damage plausible if this condition exists for extended period of time.	A
DIN	16	CLKIN	Device configured for use with external clock: SPI communication corrupted. No SPI communication with device possible. CLKIN signal corrupted. Device behavior undetermined.	B
			Device configured for use with internal oscillator: No effect. Normal operation as long as DIN can drive the pull-down resistor between CLKIN and DGND.	D
CLKIN	17	CAP	Device configured for use with external clock: Device behavior undetermined. Device damage plausible when CLKIN pin drives digital core LDO output on CAP pin to >1.8 V.	A
			Device configured for use with internal oscillator: Digital core LDO output drives external pull-down resistor on CLKIN pin to 1.8 V. Increase in digital supply current. Otherwise normal operation.	D
CAP	18	DGND	Device unpowered. Device not functional.	B
DGND	19	DVDD	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	AVDD	Not considered. Corner pin.	D

**Table 3-5. Pin FMA for Device Pins Short-Circuited to supply**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	No effect. Normal operation.	D
AGND	2	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AIN0P	3	AIN0P stuck high. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = AVDD - V_{AIN0N}$ . Conversion results of ADC0 incorrect.	B
AIN0N	4	AIN0N stuck high. $V_{IN0} = V_{AIN0P} - V_{AIN0N} = V_{AIN0P} - AVDD$ . Conversion results of ADC0 incorrect.	B
AIN1N	5	AIN1N stuck high. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = V_{AIN1P} - AVDD$ . Conversion results of ADC1 incorrect.	B
AIN1P	6	AIN1P stuck high. $V_{IN1} = V_{AIN1P} - V_{AIN1N} = AVDD - V_{AIN1N}$ . Conversion results of ADC1 incorrect.	B
AIN2P	7	AIN2P stuck high. $V_{IN2} = V_{AIN2P} - V_{AIN2N} = AVDD - V_{AIN2N}$ . Conversion results of ADC2 incorrect.	B
AIN2N	8	AIN2N stuck high. $V_{IN2} = V_{AIN2P} - V_{AIN2N} = V_{AIN2P} - AVDD$ . Conversion results of ADC2 incorrect.	B
AIN3N	9	AIN3N stuck high. $V_{IN3} = V_{AIN3P} - V_{AIN3N} = V_{AIN3P} - AVDD$ . Conversion results of ADC3 incorrect.	B
AIN3P	10	AIN3P stuck high. $V_{IN3} = V_{AIN3P} - V_{AIN3N} = AVDD - V_{AIN3N}$ . Conversion results of ADC3 incorrect.	B
$\overline{\text{SYNC/RESET}}$	11	No effect. Normal operation. Device cannot be reset or synchronized using the $\overline{\text{SYNC/RESET}}$ pin anymore.	B
$\overline{\text{CS}}$	12	$\overline{\text{CS}}$ stuck high. No SPI communication with device possible.	B
$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$ stuck high. No data ready indication through $\overline{\text{DRDY}}$ pin to host possible. Increase in supply current when $\overline{\text{DRDY}}$ tries to drive low. Device damage plausible if $\overline{\text{DRDY}}$ drives low for extended period of time.	A
SCLK	14	SCLK stuck high. No SPI communication with device possible.	B
DOUT	15	DOUT stuck high. No SPI communication back to host possible. Increase in supply current when DOUT tries to drive low. Device damage plausible if DOUT drives low for extended period of time.	A
DIN	16	DIN stuck high. No SPI communication with device possible.	B
CLKIN	17	Device configured for use with external clock: CLKIN stuck high. No clock provided to device. Device not functional, but SPI communication with device possible.	B
		Device configured for use with internal oscillator: CLKIN stuck high. No effect. Normal operation.	D
CAP	18	Device may operate normally, but permanent device damage within short period of time is very plausible. Device not functional anymore in case of damage.	A
DGND	19	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
DVDD	20	No effect. Normal operation.	D



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