Errata

AM263x Sitara MCU Silicon Revision 1.0A

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

ADVANCE INFORMATION

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1 Usage Notes and Advisories Matrices

Table 1-1 lists all usage notes and the applicable silicon revision(s). Table 1-2 lists all advisories, modules affected, and the applicable silicon revision(s).

Table 1-1. Usage Notes Matrix

Module	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM263x
		1.0A
CLOCKS	i2324 — No synchronizer present between GCM and GCD status signals	YES

Table 1-2. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM263x
		1.0A
UART	i2310 — USART: Erroneous triggering of timeout interrupt	YES
UART	i2311 — UASRT: Spurious DMA Interrupts	YES
GPMC	i2313 — GPMC: Sub-32-bit read issue with NAND and FPGA/FIFO	YES

2 Silicon Usage Notes

i2324 ***No synchronizer present between GCM and GCD status signals***

Details: There is no synchronizer in between GCM and GCD, so the clock configuration register reads may be incorrect momentarily.

Severity: Minor

Workaround(s): Poll for the status registers change until it reflects the programmed SRC_SEL and DIV values.

3 Silicon Advisories

i2310 ***USART: Erroneous triggering of timeout interrupt***

Details: USART: Erroneous triggering of timeout interrupt

The USART may erroneously trigger the timeout interrupt when RHR/MSR/LSR registers are read.

Severity: Minor

Workaround(s):

For CPU use-case, if timeout interrupt is erroneously set, and the FIFO is empty, use following SW workaround to clear the interrupt

- Set a high value of timeout counter in TIMEOUTH and TIMEOUTL registers
- Set EFR2 bit 6 to 1 to change timeout mode to periodic
- Read the IIR register to clear the interrupt
- Set EFR2 bit 6 back to 0 to change timeout mode back to the original mode

DMA use-case is not affected by this errata because if timeout interrupt is erroneously set, it will cause the DMA to be torn down, and the next incoming data will cause SW to setup the DMA again.

i2311 ***USART Spurious DMA Interrupts***

Details: Spurious DMA interrupts may occur when DMA is used to access TX/RX FIFO with a non-power-of-2 trigger level in the TLR register.

Severity: Minor

Workaround(s):

Use power of 2 values for TX/RX FIFO trigger levels (1, 2, 4, 8, 16, and 32).

i2313 ***GPMC: Sub-32-bit read issue with NAND and FPGA/FIFO***

Details: Sub-32-bit reads on the GPMC interface will miss portions of the data, which will result in incorrect read data. This includes 8-bit or 16-bit reads from a NAND device or from an FPGA or FIFO interface. Note that 3-byte accesses are not allowed on the GPMC interface.

Severity: Major

Workaround(s):

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i2313 (continued) ***GPMC: Sub-32-bit read issue with NAND and FPGA/FIFO***

Read accesses on the GPMC interface must be performed as 32-bit reads. Writes are not affected by this erratum.

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