SN65LV1224A Data Sheet Errata

The SN65LV1224B has been released to fix two design flaws explained below. It is pin compatible with all affected devices, and it covers the frequency range of all affected devices.

1 Device Affected

This erratum applies to the datasheet for the following devices:

- SN65LV1224A (TI Literature No. SLLS570C)
- SN65LV1224 (TI Literature No. SLLS527F)
- SN65LV1212 (TI Literature No. SLLS526F)

2 Problem

There are 2 failure modes that the 1224A/1224/1212 devices can enter. The first mode causes the device to lose synchronization with the incoming serial data periodically for short periods of time. In this mode the LOCK pin will be toggling periodically.

The second mode causes the device to loose synchronization with the incoming serial data permanently. The LOCK pin will remain HIGH always.

3 Symptoms

LOCK pin ‘Toggling’:

When the device enters this failure mode the LOCK pin will begin toggling. This toggling can be viewed with an oscilloscope, and if the oscilloscope is set for a horizontal scale on the order of milliseconds it will show that the toggling pulses are periodic. The period of the unlocking is directly proportional to the frequency variation from the receiver’s clock to the transmitter’s clock. Therefore, if the system were setup in a synchronous state (that is if the transmitter and receiver were driven by the same clock source) this failure would never appear.

LOCK pin ‘HIGH’:

When the device enters the LOCK = HIGH failure mode the receiver is completely unable to synchronize with the incoming serial data. The LOCK pin will be driven to a logic 1 level continuously in this mode.

4 Cause

LOCK pin ‘Toggling’:

This behavior is due to the CDR circuit not responding. The CDR circuit is responsible for tracking the incoming serial data even with a small frequency or phase difference between the receiver’s clock domain and the transmitter’s clock domain. If this circuit stops functioning the device loses is ability to track frequency differences. This is why the period of the LOCK pin toggling is dependant on the frequency variation. In a synchronous system the device is not really using the CDR circuit, and that is why the failure would never be detected in a synchronous system.

The cause of this failure is a digital counter that gets into an invalid state. There is a loop of normal operating states that the counter should stay within. If it somehow enters an invalid state it can get stuck within that state.

LOCK pin ‘HIGH’:

Counter circuits found within the byte-alignment circuitry were previously reset in an asynchronous fashion. This allowed for the possibility of the counters to be initialized into an invalid state to which they could not recover.

5 Resolution

For the LOCK pin toggling failure there is no solution or workaround short of power-cycling the device. High-speed flip-flops within the device must be reinitialized into a valid state for the device to function properly. A reset circuit has been implemented in the SN65LV1224B device to prevent the counter from entering the invalid states.

All experimentation indicates that the device can recover from a LOCK pin HIGH failure mode by resetting the device (PWRDN = LOW). The 1224B device has a synchronous reset for these counters that does not allow an invalid initialization to occur.

Both failure modes have a low chance of occurring. The probability can be affected by the device’s environment. When attempting to recover a device by power-cycling be certain that there is no residual voltage difference between Vdd and ground before switching power back on. Because both failures are due to flip-flop and counter circuit initializations there is no guaranteed solution, and every startup has the same likelihood of failure.

The SN65LV1224B device fixes these issues and should be used to replace the above mentioned receivers.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265