PCI2250

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Errata #1

Brief Description of Issue

ENUM# is NOT an open drain output.

Detailed Description of Issue

According to the Hot Swap CompactPCI specification, the ENUM# signal is an open drain output. It was not implemented as an open drain output on the PCI2250. The PCI2250 will actively drive ENUM# high when a hot swap event has not occurred. This will cause contention on the ENUM# signal if another device is also using this signal.

Impact to Customer & Probability of Bug Occurring in Actual Applications

Will occur in all Hot Swap applications. This is not a problem in non-Hot Swap designs.

SW or HW Workarounds Defined

An external open drain buffer is required to convert the PCI2250's ENUM# signal. Please refer to the application note SCPA027 "Connecting ENUM Terminal to an External Open-Drain Buffer".

Affected Devices

PCI2250 rev. 00, rev. 01, and rev. 02.

Errata #2

Brief Description of Issue

Bridge may not be granted secondary bus when a secondary master asserts FRAME# at the same time that GNT# is de-asserted.

Detailed Description of Issue

The problem occurs when the PCI2250's arbiter removes GNT from a master on the same clock cycle that the master drives FRAME#. When the arbiter detects FRAME# asserted, it updates its internal pointers to indicate that the next master has initiated a transaction.

The condition occurs if a master on the primary bus will not provide the read data to the bridge until the write it is attempting completes. The master on the secondary bus is continuing to perform its read transaction in such a manner that each attempt asserts FRAME# at the same time GNT is being de-asserted. This results in the PCI2250 never being able to complete the write transaction in its FIFO.

This errata will never occur between two masters residing on the same bus.

Impact to Customer & Probability of Bug Occurring in Actual Applications

The condition will occur if a master exhibits the behavior described above. Presently, the only device that is known to exhibit this behavior is the Intel 82559 NIC.

SW or HW Workarounds Defined

The PCI2250 has four available REQ# lines. Connect one of these REQ# lines to GND or connect the REQ# of the master that exhibits the behavior described above to two REQ# pins on the PCI2250.

Affected Devices

PCI2250 rev. 00, rev. 01, and rev. 02.

Errata #3

Brief Description of Issue

Hot Swap Control/Status Register behavior

Detailed Description of Issue

When a CPCI ‘Hot Swap Ready’ board is inserted into the backplane and the ejector handle is closed or when a CPCI Hot swap system is powered up, the INS bit in the Hot Swap Control and Status register is set to ‘1’. Now, if the ejector handle is opened before the software can clear the INS bit, then, according to the CPCI Hot swap specification, the EXT bit must be set to ‘1’ after the INS bit is cleared by writing a ‘1’ to it. This behavior is not observed in PCI2250. When the handle is opened and the INS bit is cleared in PCI2250, the EXT bit remains unchanged. This behavior suggests the PCI2250 only responds to the transitions on the switch and not to the state of the switch when the INS bit is cleared.

The PCI2250 shows the similar behavior for the EXT bit in the Hot Swap Control and Status register. If the user closes the ejector handle while the EXT bit is ‘1’ and clears the EXT bit by writing a ‘1’ to it then the INS bit must be set to ‘1’, according to the CPCI Hot Swap specification. The INS bit remains unchanged in PCI2250.

Please note this problem only exists if the software does not clear the INS or EXT bit in the Hot Swap Control and Status register before the ejector handle is toggled.

Impact to Customer & Probability of Bug Occurring in Actual Applications

Not compliant with the CPCI Hot Swap specification.

SW or HW Workarounds Defined

Wait for software to clear INS/EXT bit before toggling the handle.

Affected Devices

PCI2250 rev. 00, rev. 01, and rev. 02.

Errata #4

Brief Description of Issue

The I/O Window is closed if both I/O limit and I/O Limit Upper 16-bits registers are programmed to zero.

Detailed Description of Issue

According to the PCI-to-PCI bridge specification, a bridge forwards I/O read and I/O write transactions from its primary interface to its secondary interface (downstream) if the address is in the range defined by the I/O base and I/O limit registers (when the base is less than or equal to the limit). The PCI2250 will only forward an I/O transaction downstream if the I/O Limit registers are programmed to a value other than zero.

Impact to Customer & Probability of Bug Occurring in Actual Applications

Only affects customers who want to forward the I/O range 0x000 thru 0xFFF to the secondary interface of the bridge. If the customer wants to pass the I/O range of 0x000 thru 0xFFF to the secondary interface, the range 0x000 thru 0x1FFF has to be used .

SW or HW Workarounds Defined

None.

Affected Devices

PCI2250 rev. 00, rev. 01, and rev. 02.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265