ERRATA
TO THE TSB12LV22 DATA SHEET
(TEXAS INSTRUMENTS LITERATURE NO. SLLS290, July 1998)

This document contains corrections and additions to information in the TSB12LV22 data sheet (TI Literature Number SLLS290, July 1998).

a. The PhyRegRcv event (interrupt) may be set (erroneously) when PHY Register 0 status is received.

   Received status from PHY Register 0 should not create an interrupt event. All other received PHY registers should generate an interrupt.

   When the interrupt routine receives the PhyRegRcv, there may not be any new PHY register read data in the PHY Control register. In this case, software should ignore the interrupt and return.

   Note that if a PHY register was requested, this interrupt might occur and the requested PHY register data may not be available yet. In this case the PHY Control register rdDone bit will not be set. Another PhyRegRcv interrupt will be posted when the requested register data is available.

b. 1394A Ack Accelerations should not be turned on.

   If the Ack Accelerations are turned on, a lockup between the PHY and link might occur. The link logic may miss a cancellation of a 1394 bus request, leaving the link waiting for access to the bus that never occurs.

c. Certain incorrect packets may be received into the FIFO and transferred to the host memory with no error indication.

   The incorrect packets include those with correctly formatted 1, 3, or 4 quadlet packets (i.e. iso, tcode 'hA, with no payload data, quadlet read request, quadlet write request), with extra (erroneous) data after the packet CRC quadlet. These packets will be received and transferred to host memory with no error indication and no extra data transferred; however, no ack will be returned.

   If the packet was a broadcast or received with an ack complete status to the DMA, there is no observable problem at the receive end except that the packet should have been identified as a bad packet. The transmitting node should have bad status (missing ack) if it was not a broadcast.

   Note that this error only exists for incorrectly formatted receive packets, with correct CRC in the normal location.

d. A SelfID Complete interrupt may not be generated if the selfID buffer overflows.

e. (Spec issue) Isochronous transmit interrupt will not occur if the *skip branch address* is taken. This is true even if the skip branch address *Z* value is equal to 0 and can leave the system without an interrupt when it might be expecting a normal termination interrupt from the continue branch with a *Z* value of 0.

f. PCI slave read accesses to registers in the link clock domain (i.e. PHY Control Register, Link Control Register, etc.) may be terminated with a retry. A retry successfully completes. No failure is created by this behavior.

g. When Context.Run is cleared in a transmitting context ATRQ,ATRS,IT while Context.Active is set, the context will stop at a packet boundary with Context.Ptr pointing to the next descriptor block instead of the last one executed as the specification defines.

h. PCI Slave reads of the Cycle Timer register may occasionally get an incorrect value.

   Software may be able to validate value by reading the register multiple times rapidly and evaluating for a reasonable difference.

i. CycleTooLong is erroneously disabled by cycleMaster. CycleTooLong interrupt will not occur on the cycleMaster OHCI controller. However, the CycleTooLong interrupt may occur erroneously when cycleMaster is disabled.

Note that *cycleMaster* in this case is actually *LinkControl.cycleMaster && root_node.*

j. When two or more packets are in the Async Transmit FIFO and it becomes full near the end of a packet, the FIFO control information may be corrupted. This may result in an *evt_unknown* completion status being stored for one of the DMA Async Transmit contexts.

Typically, this also results in the DMA context for which the last packet was transferred to the FIFO being hung. Once the DMA context is hung, a software or hardware (i.e. PCI_RESET) is required to restore operation.

Workarounds:
Limit the payload size of any request or response packet to 512 bytes. Changing the value of the Max Rec field of the Bus Info Block to 0x8 informs other nodes to use payload sizes less than or equal to 512 bytes. Software should enforce the 512 byte limit on all packets it initiates.

k. When the ISO Transmit FIFO becomes full near the end of a packet, the FIFO control information may be corrupted. This may result in some packets being flushed erroneously from the FIFO. It may also result in unreliable operation of the skip processing.

Workaround:
The sum of the packets sizes in the ISO Transmit FIFO must be less than 2048. There can be two cycles-worth of packets in the ISO Transmit FIFO. There are 8 overhead bytes associated with each packet. For example:

– Assuming 8 active contexts of all equal packet sizes, the maximum packet size is:

```
(2048 / (8 * 2)) – 4 – 8 = 116 bytes
 FIFO    C         H   T
```

– Assuming 2 active contexts of all equal packet sizes, the maximum packet size is

```
(2048 / (2 * 2)) – 4 – 8 = 500 bytes
 FIFO    C         H   T
```

– Assuming 1 active context, the maximum packet size is

```
(2048 / (1 * 2)) – 4 – 8 = 1012 bytes
 FIFO    C         H   T
```

Where:
FIFO = Fifo size
C = number of active contexts
H = header bytes
T = token overhead bytes

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