

Errata to TFP510, Datasheet Literature Number SLDS146B

This document describes errata to the TFP510 and its datasheet.

Revision history:

| Revision | Date | Description |
|----------|---------|--|
| A | Initial | DE generator |
| B | 7/2003 | MSEN, V _{IH} , V _{IL} clarification, pad size update, revision history |

1. DE Generator:

The DE generator function has a limitation which limits its use in high pixel count formats. The DE_DLY and DE_CNT values are limited by $DE_DLY + DE_CNT \leq 2047$.

For resolutions where the timing allows, it may be possible to work around this limitation by using the inactive edge of HSYNC as the starting point for DE_DLY. Appropriate timing allowances may be needed for the vertical count starting location.

Changes in the document text:

In the “register descriptions” section, under the pictorial for DE_DLY (Page 20), add after the existing sentence: The value must be less than or equal to $(2047 - DE_CNT)$.

In the “register descriptions” section, under the pictorial for DE_CNT (Page 21), add after the existing sentence: The value must be less than or equal to $(2047 - DE_DLY)$.

2. MSEN output:

The MSEN output description is incorrect in the “Terminal Functions” table. MSEN behavior of the 510 with manual configuration is to output the receiver connected status as a high, receiver not connected as a low.

Changes in the document text:

In the “Terminal Functions” table, page 5, for the MSEN pin, middle paragraph of the “Description” column, change the second paragraph

FROM:

When I2C is disabled (ISEL = low), a low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

TO:

When I2C is disabled (ISEL = low), a high level indicates a powered on receiver is detected at the differential outputs. A low level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

3. Input voltage clarifications

In the DC specification table, V_{IH} and V_{IL} are not clear for signals that are not part of the video input bus.

Changes in the document text:

Sheet 7, in the dc specifications table, change the V_{IH} and V_{IL} specifications to contain the following information:

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|--------------------------|------------------------------------|--------------------------------|-----------------|-----------------|------|
| V_{IH} | High-level input voltage | Data, DE, VSYNC, HSYNC and IDCK+/- | $V_{REF} = DV_{DD}$ | $0.7V_{DD}$ | | V |
| | | | $0.55V \leq V_{REF} \leq 0.9V$ | $V_{REF} + 0.2$ | | V |
| | Other inputs | | $0.7V_{DD}$ | | | V |
| V_{IL} | Low-level input voltage | Data, DE, VSYNC, HSYNC and IDCK+/- | $V_{REF} = DV_{DD}$ | | $0.3V_{DD}$ | V |
| | | | $0.55V \leq V_{REF} \leq 0.9V$ | | $V_{REF} - 0.2$ | V |
| | Other inputs | | | | $0.3V_{DD}$ | V |

4. PowerPad size and routing consideration:

The size of the exposed metal on the PowerPad package figure is shown as larger than on production devices. When providing a thermal land, it may be smaller than assumed from the package drawing. If routing traces under the power pad, some method of protection from shorts between the traces or vias and the PowerPad should be used.

Changes to document:

Sheet 25, change the package figure as described:

- Re-size the thermal pad dashed box from its present size to 5.35mm, centered in the package.
- Note the dimensions and change note D by either:

Add dimensions to re-sized pad showing: $\frac{5.35}{4.25}$ SQ

and

Change note D to read:

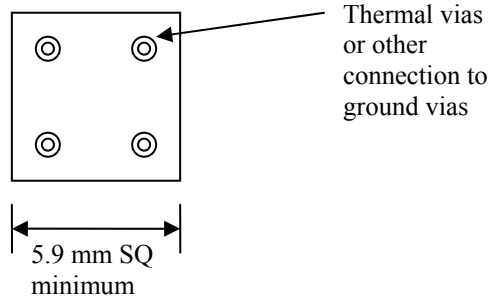
The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is centered on the package and is electrically and thermally connected to the backside of the die.

Sheet 24, add sentence to paragraph 1, revise paragraph 2 and add figure and paragraphs between existing paragraphs 2 & 3 to read:

... soldering the back side of the TFP510 to the application board is not required thermally as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back side pad.

Soldering the backside of the device to thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5.9mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.



More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: <http://www.ti.com>

Table 2 outlines the thermal properties...

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