MSP430I4020 Device Erratasheet

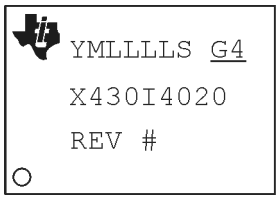
1 Revision History

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
PMM20	✓
USCI36	✓
USCI37	✓

2 Package Markings

DGG48 *(DGG), 48 Pin*



YM = Year and Month Date Code
LLLL = Assembly Lot Code
S = Assembly Site Code
# = Die Revision
○ = Pin 1

3 Detailed Bug Description

PMM20 *PMM Module*

Function Unexpected SVSL/SVML event during wakeup from LPM2/3/4 in fast wakeup mode

Description If PMM low side is configured to operate in fast wakeup mode, during wakeup from LPM2/3/4 the internal VCORE voltage can experience voltage drop below the corresponding SVSL and SVML threshold (recommendation according to User's Guide) leading to an unexpected SVSL/SVML event. Depending on PMM configuration, this event triggers a POR or an interrupt.

NOTE: As soon the SVSL or the SVML is enabled in Normal performance mode the device is in slow wakeup mode and this erratum does not apply.

In addition, this erratum has sporadic characteristic due to an internal asynchronous circuit. The drop of Vcore does not have an impact on specified device performance.

Workaround If SVSL or SVML is required for application (to observe external disruptive events at Vcore pin) the slow wakeup mode has to be used to avoid unexpected SVSL/SVML events. This is achieved if the SVSL or the SVML is configured in "Normal" performance mode (not disabled and not in "Full" Performance Mode).

USCI36 *eUSCI Module*

Function UCLKI not usable in I2C master mode

Description When EUSCIB is configured as I2C Master with the external UCLKI as clock source, the UCLKI signal is not available and cannot be used to source I2C clock.

Workaround Use LFXTCLK via ACLK or HFXTCLK via SMCLK as clock source (BRCLK) for I2C in master mode with external clock source.

USCI37 *eUSCI Module*

Function Reading RXBUF during an active I2C communication might result in unintended bus stalls.

Description The falling edge of SCL bus line is used to set an internal RXBUF-written flag register, which is used to detect a potential RXBUF overflow. If this flag is cleared with a read access from the RXBUF register during a falling edge of SCL, the clear condition might be missed. This could result in an I2C bus stall at the next received byte.

Workaround (1) Execute two consecutive reads of RXBUF, if $t_{SCL} > 4 \times t_{IFCLK}$.

or

(2) Provoke an I2C bus stall before reading RXBUF. A bus stall can be verified by checking if the clock line low status indicator bit UCSCLLOW is set for at least three USCI bit clock cycles i.e. $3 \times t_{BitClock}$.

4 Document Revision History

Changes from device specific erratasheet to document Revision A.

1. Module name for DGG48 was modified.
2. Errata PMM15 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Module name for PMM15 was modified.
2. BSL7 Workaround was updated.
3. PMM15 Description was updated.
4. PMM15 Workaround was updated.
5. Errata PMM18 was removed from the errata documentation.
6. PMM15 Function was updated.

Changes from document Revision B to Revision C.

1. BSL7 Workaround was updated.
2. BSL7 Function was updated.
3. Module name for BSL7 was modified.
4. BSL7 Description was updated.

Changes from document Revision C to Revision D.

1. Errata USCI37 was added to the errata documentation.

Changes from document Revision D to Revision E.

1. Errata USCI36 was added to the errata documentation.

Changes from document Revision E to Revision F.

1. Package Markings section was updated.

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