

UCC5880-Q1 具有适用于汽车应用的高级保护功能的隔离式 20A 可调栅极驱动 IGBT/SiC MOSFET 栅极驱动器

1 特性

- 具有动态可编程驱动强度的双路输出分离驱动器
 - $\pm 15A$ 和 $\pm 5A$ 驱动电流输出
 - 用于在没有 SPI 时进行驱动强度调整的数字输入引脚 (GD*)
 - 3 电阻设置 R1、R2 或 R1||R2
 - 用于米勒钳位晶体管的集成式 4A 有源米勒钳位或可选的外部驱动器
- 支持初级侧和次级侧主动短路 (ASC)
- 内部和外部电源欠压和过压保护
- 驱动器内核温度检测和过热保护
- 短路保护：
 - 75ns 的过流事件响应时间
 - DESAT 保护 - 可承受高达 14V 的电压
 - 基于分流电阻器的过流保护
 - 可配置保护阈值和消隐时间
 - 可编程软关断 (STO) 和两级软关断 (2STO) 电流
- 集成 10 位 ADC
 - 电源开关温度, 驱动器内核温度, DESAT 引脚电压, VCC2 电压, 相电流, 直流链路电压
 - 可编程数字比较器
- 高级 VCE/VDS 钳位电路
- 符合功能安全标准
 - 专为功能安全应用开发
 - 有助于使 ISO 26262 系统设计符合 ASIL D 要求的文档
- 集成型诊断：
 - 针对保护比较器的内置自检 (BIST)
 - 用于功率器件运行状况监测的栅极阈值电压测量
 - INP 至晶体管栅极路径完整性
 - 内部时钟监测
 - 故障警报和警告输出 (nFLT*)
 - ISO 通信数据完整性检查
- 可通过 SPI 对器件进行重新配置、验证、监控和诊断
- 100kV/ μs CMTI
- 安全相关认证：
 - 符合 UL1577 标准且长达 1 分钟的 5kV_{RMS} 隔离 (计划)
 - 符合 DIN VDE 0884-11 的增强型隔离 7070V_{PK}: 2017-01 (计划)
- 具有符合 AEC-Q100 标准的下列结果：
 - 器件温度等级 1: -40°C 至 +125°C 环境工作温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B

2 应用

- 电动汽车和混合动力汽车牵引逆变器
- 电动汽车和混合动力汽车电源模块

3 说明

UCC5880-Q1 器件是一款高度可配置的隔离式可调压摆率栅极驱动器，专用于驱动 EV/HEV 应用中的大功率 SiC MOSFET 和 IGBT。该器件提供功率晶体管保护功能，例如基于分流电阻的过流保护、过热保护 (PTC、NTC 或二极管) 以及 DESAT 检测，包括在这些故障期间可选择的软关断或两级软关断。为了进一步缩小应用尺寸，UCC5880-Q1 集成了可用的有源米勒钳位，以及在驱动器未通电时可用的有源栅极下拉电阻。集成的 10 位 ADC 可用于监控多达 2 个模拟输入、VCC2、DESAT 以及栅极驱动器温度，从而增强系统管理。集成的诊断和检测功能可简化符合 ASIL 标准的系统的设计。这些功能的参数和阈值可使用 SPI 进行配置，因此该器件几乎可与任何 SiC MOSFET 或 IGBT 一同使用。

器件信息

器件型号	封装 (1)	封装尺寸 (标称值)
UCC5880DFC-Q1	SSOP (32)	10.5mm x 7.5mm

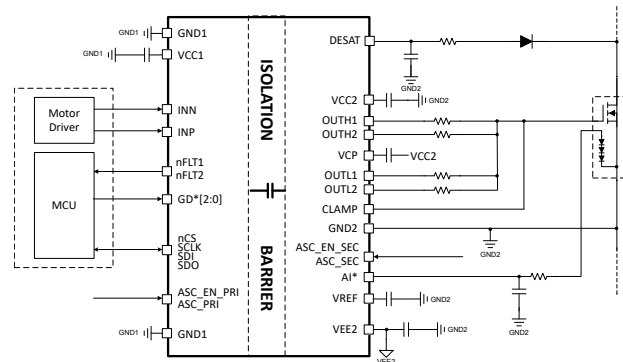


图 3-1. 简化原理图



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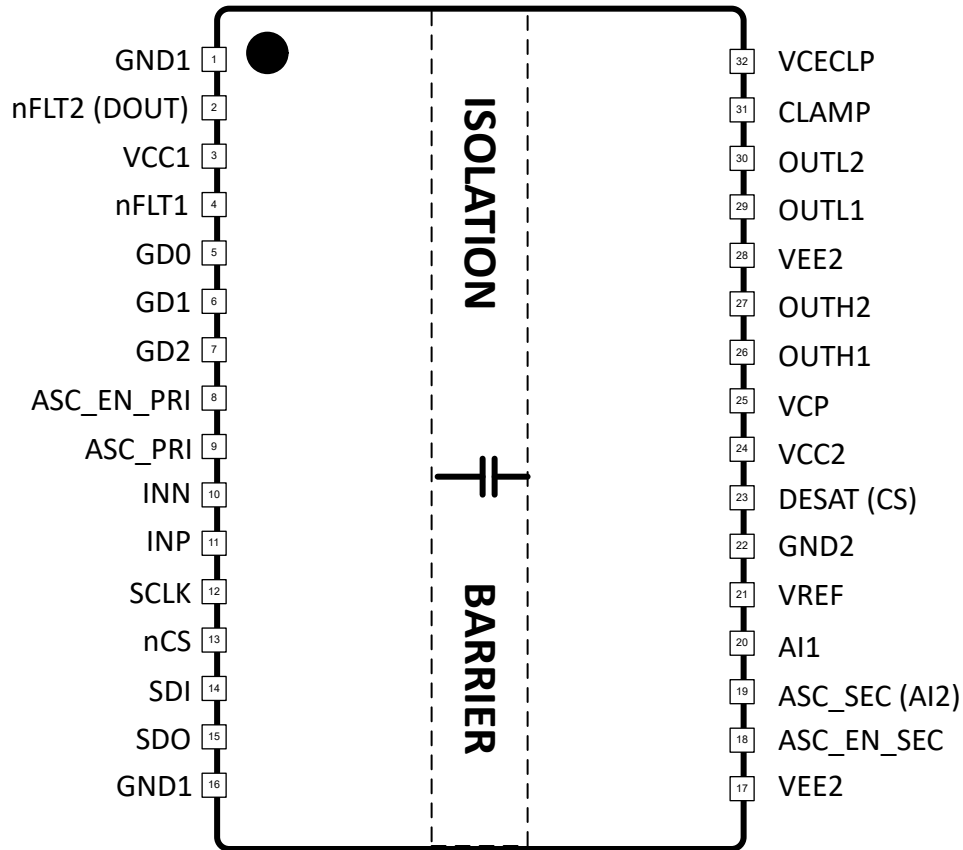
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Advance Information Release

5 Pin Configuration and Functions

32-pin SSOP Top View



ADVANCE INFORMATION

表 5-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND1	1, 16	P	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side. Prioritize pin 1 for supply and input filter decoupling.
nFLT2 (DOUT)	2	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Additionally, nFLT2 may be configured as DOUT to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked.
VCC1	3	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible.
nFLT1	4	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked.
GD0	5	I	OUTL1/2 and OUTH1/2 Selector Inputs. GD* select combinations of OUT*1 and OUT*2 with user-selectable resistors. Drive all GD* high to force the gate of the power transistor low and reset all faults. See Adjustable Gate Drive Outputs (OUTL* OUTH*) for more details. Tie to GND1 if not used.
GD1	6	I	
GD2	7	I	
ASC_EN_PRI	8	I	Primary-side Active Short Circuit Enable Input. ASC_EN_PRI enables the ASC function and forces the output to follow the ASC_PRI pin input state. If ASC_EN_PRI is high, the OUTx pins follow the ASC_PRI pin state. When ASC_EN_PRI is low, the OUT* pins follow the INP and INN pin logical truth table. Tie to GND1 if not used.
ASC_PRI	9	I	Primary-side Active Short Circuit Polarity Input. The OUT* pins follow the logic level at ASC_PRI when the ASC_EN_PRI input is driven high. See the ASC section for more details. Tie to GND1 if not used.
INN	10	I	Negative PWM Input. INN is connected to the INP from the opposite arm of the half-bridge. If INP and INN overlap, the Shoot Through Protection (STP) engages and forces output low. Tie to GND1 if not used.
INP	11	I	Positive PWM Input. INP drives the state of the driver output. With the driver enabled, when INP is high, OUTH* is pulled high. When INP is low, OUTL* is pulled low. Drive INP up to a 50kHz PWM signal, with a logic level determined by the VCC1 voltage. INP is connected to the INN of the opposite arm of the half-bridge. If INP and INN overlap, STP engages and forces output low.
SCLK	12	I	SPI Clock. SCLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz.
nCS	13	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI peripheral device. Drive nCS low during SPI communication. When nCS is high, the CLK and SDI inputs are ignored. Tie to VCC1 if not used.
SDI	14	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication.
SDO	15	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK.
VEE2	17, 28	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of ceramic capacitance as close to pin 28 as possible.
ASC_EN_SEC	18	I	Secondary-side Active Short Circuit Enable Input. ASC_EN_SEC enables the ASC function and forces the output of the driver to the low safe state. If ASC_EN_SEC is high, OUTL* is pulled low. When ASC_EN_SEC is low, the output is controlled by primary side pins. Tie to GND2 if not used.
ASC_SEC	19	I	Analog Input 2/ Secondary-side Active Short Circuit Polarity Input. ASC_SEC (AI2) defaults to Active Short Circuit Polarity Input. When programmed as ASC_SEC, the OUTx pins follow the logic level at ASC_SEC when the ASC_EN_SEC input is driven high. See the ASC section for more details. Tie to GND2 if not used.
AI2		I	Analog Input 2/ Secondary-side Active Short Circuit Polarity Input. ASC_SEC (AI2) can be programmed as an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/ below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.

表 5-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
AI1	20	I	Analog Input 1. AI1 is an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/ below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.
VREF	21	P	Internal ADC Voltage Regulator Output. VREF provides an internal 5V, reference for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance. Loads up to 5mA on VREF are allowed.
GND2	22	P	Gate Drive Supply Reference. Connect GND2 to the power FET source/ IGBT emitter. ASC_EN_SEC, ASC_SEC (AI2), AI1, VREF, and DESAT are referenced to GND2.
DESAT	23	I	Current Sense Input/ Desaturation based Short Circuit Detection Input. DESAT (CS) is configurable to sense over-current conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For DESAT applications, bypass DESAT to GND2 with a ceramic capacitor and, in parallel, connect a Schottky diode with the cathode connected to the DESAT, anode connected to GND2. See the applications section for details on calculating the component values. Additionally, connect DESAT to a resistor to the anode of a diode to the collector of the power FET. DESAT detects a fault when the VDS/VCE voltage of the power FET exceeds the SPI programmable threshold while the power FET is on. Tie to GND2 if not used.
CS		I	Current Sense Positive Input/ Desaturation based Short Circuit Detection Input. CS (DESAT) is configurable to sense over-current and short-circuit conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For sense resistor based applications, connect DESAT (CS) pin to the positive side of the sense element through an RC. The current limit threshold is programmable via SPI. Tie to GND2 if not used.
VCC2	24	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the required drive current.
VCP	25	P	High-side Drive Supply. VCP supplies power for the OUTH* drive. Bypass VCP to VCC2 with a ceramic capacitor between 10nF and 100nF, as close to the VCP pin as possible.
OUTH1	26	O	Gate driver source pins (OUTH1 = 15A _{PK} , OUTH2 = 5A _{PK}). When the driver is active and commanded high, OUTH* pins are used to source current to the gate of the power FET to drive the output high. Connect OUTH* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTH1 and OUTH2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTH1 only, OUTH2 only, and OUTH1 + OUTH2).
OUTH2	27		
OUTL1	29	O	Gate driver sink pins (OUTL1 = 15A _{PK} , OUTL2 = 5A _{PK}). When the driver is active and commanded low, OUTL* pins are used to sink current from the gate of the power FET to drive the gate low. Connect OUTL* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTL1 and OUTL2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTL1 only, OUTL2 only, and OUTL1 + OUTL2).
OUTL2	30		
CLAMP	31	O	Miller Clamp pin. The CLAMP pin is used to hold the gate of the power FET strongly to VEE2 while the power FET is “off”. CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly to the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET. Disable and tie to VEE2 if not used.
VCECLP	32	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth voltage. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. See the applications section for details on calculating the component values. Additionally, connect VCECLP to the anode of a zener diode to the collector/drain of the power FET. Tie to VEE2 if not used.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Documentation Support

6.1.1 Related Documentation

6.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

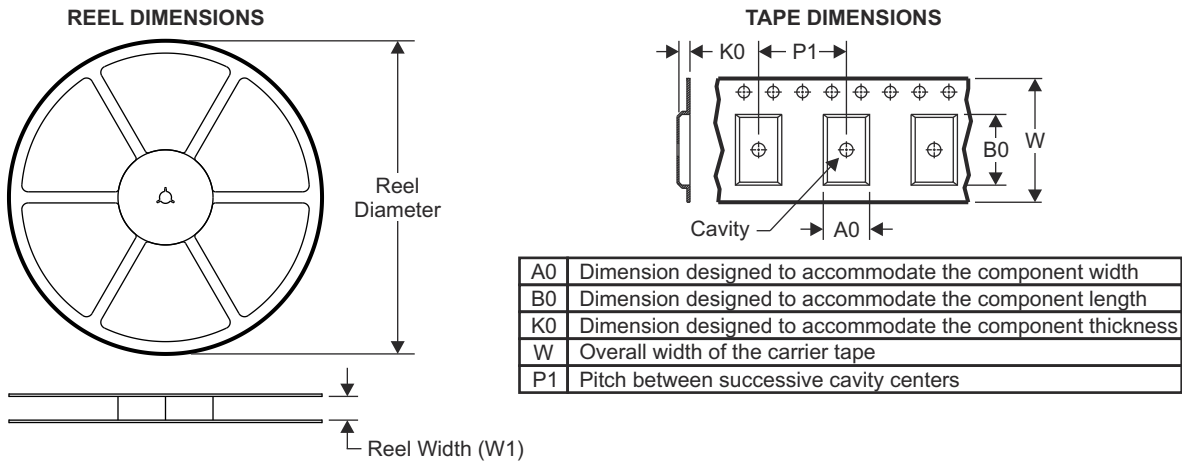
6.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

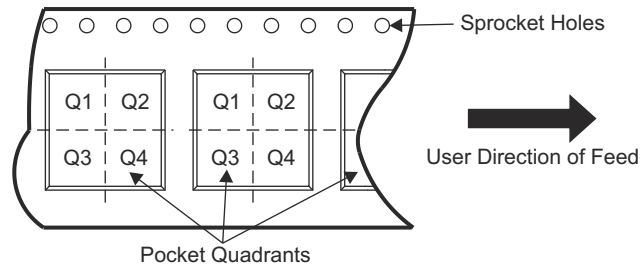
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information

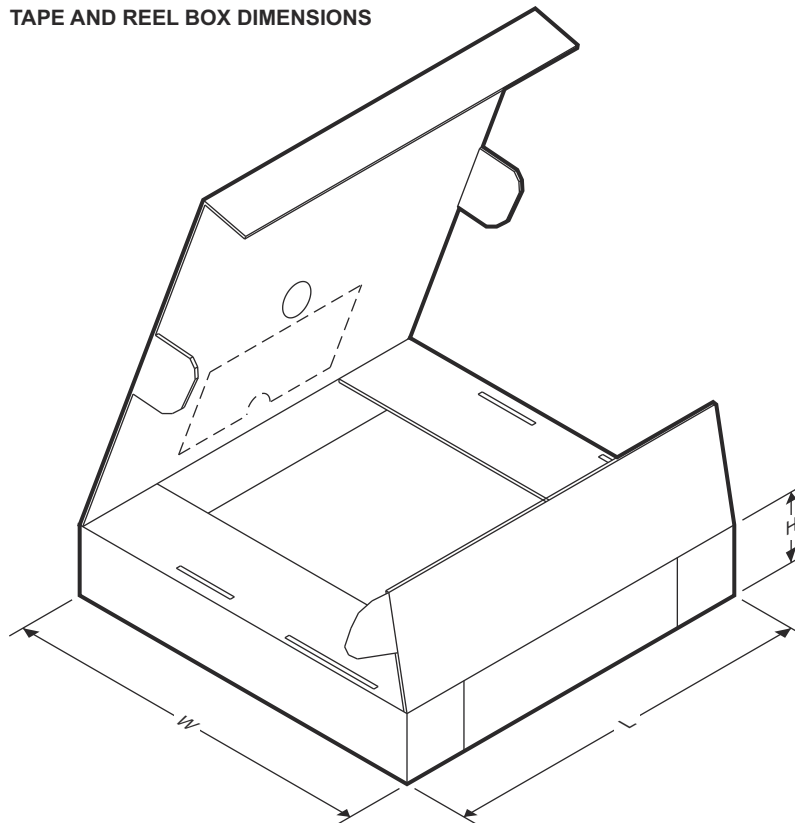


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)

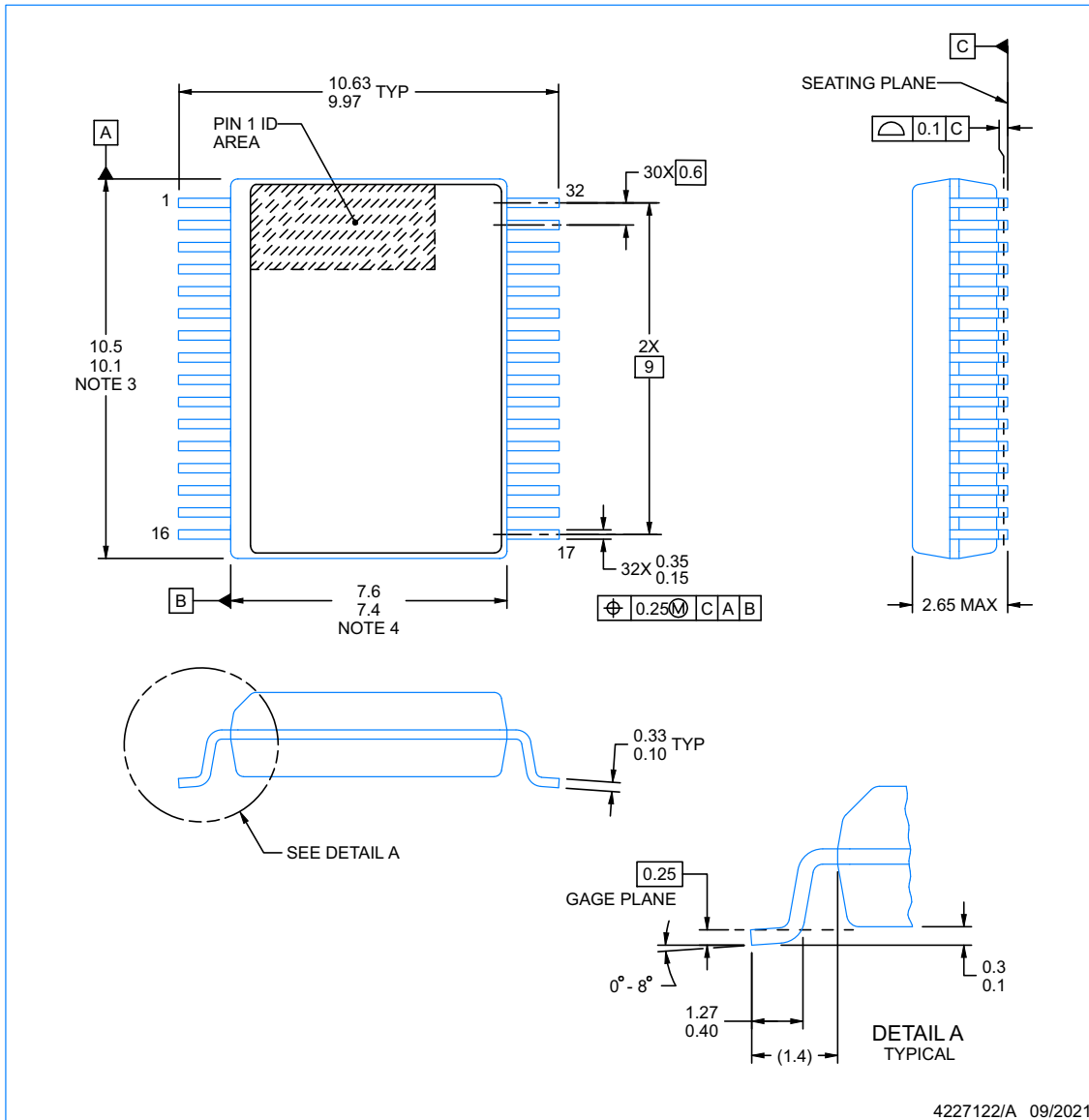
ADVANCE INFORMATION

PACKAGE OUTLINE

DFC0032A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DFC0032A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE

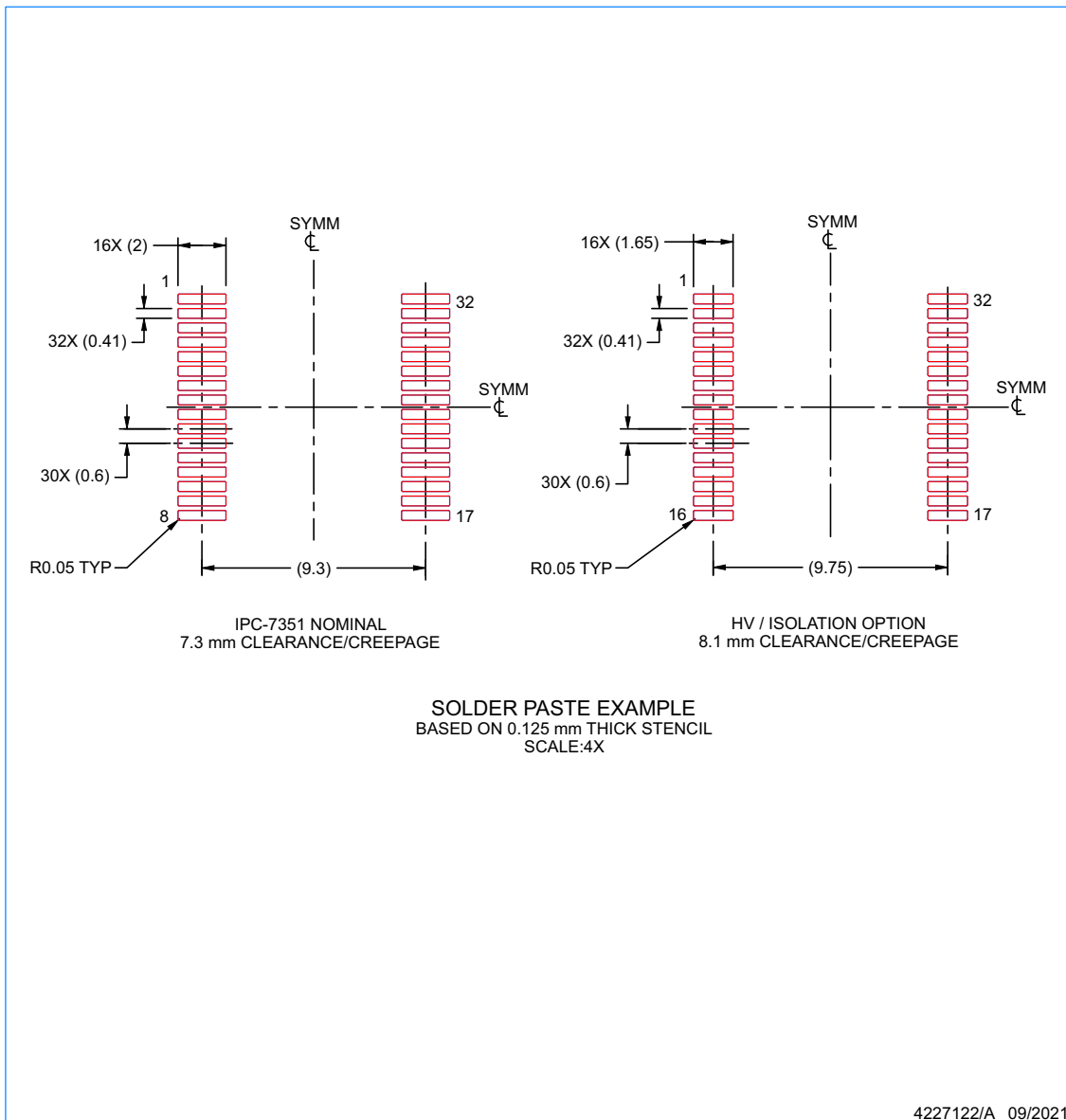
EXAMPLE STENCIL DESIGN

DFC0032A

SSOP - 2.65 mm max height

SAMLL OUTLINE PACKAGE

ADVANCE INFORMATION



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC5880QDFCQ1	ACTIVE	SSOP	DFC	32	40	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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