

## TPS7B69xx-Q1 High-Voltage Ultra-Low $I_Q$ Low-Dropout Regulator

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 4 to 40-V Wide  $V_I$  Input Voltage Range With up to 45-V Transient
- Maximum Output Current: 150 mA
- Low Quiescent Current ( $I_Q$ ):
  - 15  $\mu\text{A}$  Typical at Light Loads
  - 25  $\mu\text{A}$  Maximum Under Full Temperature
- 450-mV Typical Low Dropout Voltage at 100 mA Load Current
- Stable With Low ESR Ceramic Output Capacitor (2.2 to 100  $\mu\text{F}$ )
- Fixed 2.5-V, 3.3-V, and 5-V Output Voltage Options
- Integrated Fault Protection:
  - Thermal Shutdown
  - Short-Circuit Protection
- Packages:
  - 4-Pin SOT-223 Package
  - 5-Pin SOT-23 Package

### 2 Applications

- Automotive
- Infotainment Systems With Sleep Mode
- Always-On Battery Applications
  - Door Modules
  - Remote Keyless-Entry Systems
  - Immobilizers

### 3 Description

The TPS7B69xx-Q1 device is a low-dropout linear regulator designed for up to 40-V  $V_I$  operations. With only 15- $\mu\text{A}$  (typical) quiescent current at light load, the device is suitable for standby microcontrol-unit systems especially in automotive applications.

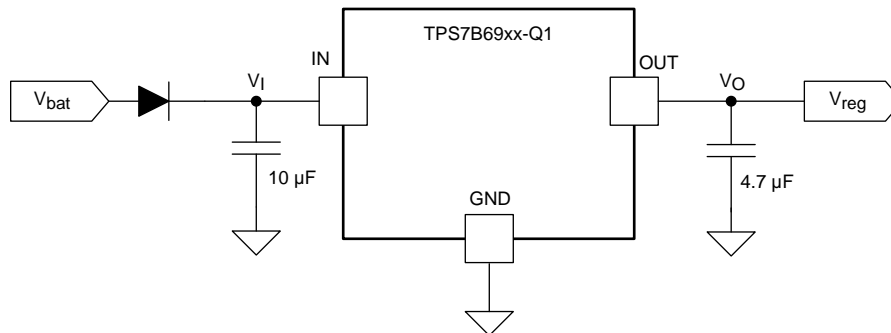
The devices feature an integrated short-circuit and overcurrent protection. The TPS7B69xx-Q1 device operates over a  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  temperature range. Because of these features, the TPS7B6925-Q1, TPS7B6933-Q1, and TPS7B6950-Q1 devices are well suited in power supplies for various automotive applications.

#### Device Information<sup>(1)</sup>

| PART NUMBER  | PACKAGE     | BODY SIZE (NOM)   |
|--------------|-------------|-------------------|
| TPS7B6925-Q1 | SOT-223 (4) | 6.50 mm x 3.50 mm |
| TPS7B6933-Q1 | SOT-23 (5)  | 2.90 mm x 1.60 mm |
| TPS7B6950-Q1 |             |                   |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 Typical Application Schematic



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## 5 Revision History

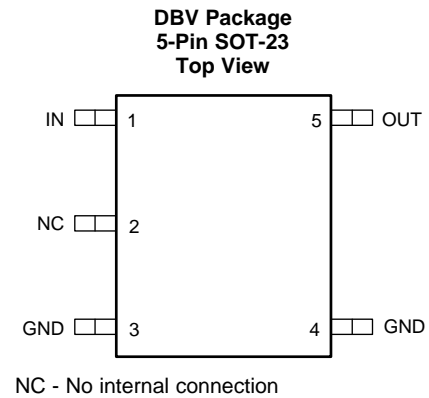
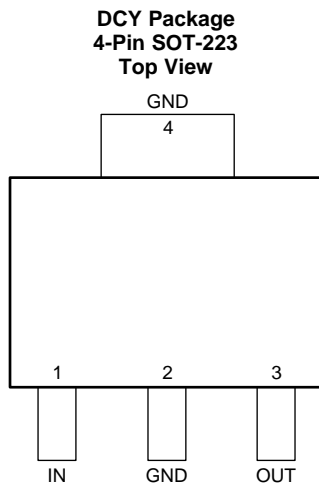
### Changes from Revision A (December 2014) to Revision B Page

- Changed the TPS7B6933-Q1 device status from *Product Preview* to *Production Data* ..... **1**
- Added the TPS7B6933-Q1 device test results to the *Typical Characteristics* section ..... **6**

### Changes from Original (November 2014) to Revision A Page

- Changed the device status from *Product Preview* to *Production Data* ..... **1**

## 6 Pin Configuration and Functions



### Pin Functions

| NAME | PIN NO. |        | TYPE | DESCRIPTION                |
|------|---------|--------|------|----------------------------|
|      | SOT-223 | SOT-23 |      |                            |
| GND  | 2       | 3      | G    | Ground reference           |
|      | 4       | 4      |      |                            |
| IN   | 1       | 1      | P    | Input power-supply voltage |
| NC   | —       | 2      | —    | Not connected pin          |
| OUT  | 3       | 5      | P    | Output voltage             |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  |                         | MIN  | MAX | UNIT |
|--|-------------------------|------|-----|------|
| Unregulated input voltage                            | IN <sup>(2)(3)(4)</sup> | -0.3 | 45  | V    |
| Regulated output voltage                             | OUT <sup>(2)(3)</sup>   | -0.3 | 7   | V    |
| Operating junction temperature range, T <sub>J</sub> |                         | -40  | 150 | °C   |
| Storage temperature, T <sub>stg</sub>                |                         | -65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminal.
- (3) Absolute negative voltage on these pins must not go below -0.3 V.
- (4) Absolute maximum voltage, withstands 45 V for 200 ms.

### 7.2 ESD Ratings

|                    |                         |   | VALUE   | UNIT |      |
|--------------------|-------------------------|---|---|------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> |   | V    |      |
|                    |                         | Charged device model (CDM), per AEC Q100-011            | Other pins  |      | ±500 |
|                    |                         |   | Corner pins (4 pin: 1, 3, and 4; 5 pin: 1, 3, 4, and 5) |      | ±750 |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                   |  | MIN   | MAX | UNIT |
|-------------------|--|-------|-----|------|
| V <sub>I</sub>    | Unregulated input voltage                    | 4     | 40  | V    |
| V <sub>O</sub>    | Output voltage                               | 0     | 5.5 | V    |
| C <sub>O</sub>    | Output capacitor requirements <sup>(1)</sup> | 2.2   | 100 | μF   |
| ESR <sub>CO</sub> | Output ESR requirements <sup>(2)</sup>       | 0.001 | 2   | Ω    |
| T <sub>J</sub>    | Operating junction temperature range         | -40   | 150 | °C   |

- (1) The output capacitance range specified in this table is the effective value.
- (2) Relevant ESR value at  $f = 10$  kHz.

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)(2)</sup> |  | DCY    | DBV    | UNIT |
|----------------------------------|--|--------|--------|------|
|                                  |  | 4 PINS | 5 PINS |      |
| R <sub>θJA</sub>                 | Junction-to-ambient thermal resistance       | 64.2   | 210.4  | °C/W |
| R <sub>θJC(top)</sub>            | Junction-to-case (top) thermal resistance    | 46.8   | 126.1  |      |
| R <sub>θJB</sub>                 | Junction-to-board thermal resistance         | 13.3   | 38.4   |      |
| ψ <sub>JT</sub>                  | Junction-to-top characterization parameter   | 6.3    | 16     |      |
| ψ <sub>JB</sub>                  | Junction-to-board characterization parameter | 13.2   | 37.5   |      |

- (1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, 2s2p four layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$ ,  $1\text{ m}\Omega < \text{ESR} < 2\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                              | TEST CONDITIONS                              | MIN  | TYP  | MAX | UNIT  |                  |
|--|--|--|------|-----|-------|------------------|
| <b>SUPPLY VOLTAGE AND CURRENT (IN)</b> |  |  |      |     |       |                  |
| $V_I$                                  | Input voltage                                | Fixed 2.5-V output, $I_O = 1\text{ mA}$  | 4    |     | 40    | V                |
|  |  | Fixed 3.3-V output, $I_O = 1\text{ mA}$  | 4    |     | 40    |                  |
|  |  | Fixed 5-V output, $I_O = 1\text{ mA}$  | 5.5  |     | 40    |                  |
| $I_Q$                                  | Quiescent current                            | Fixed 2.5-V and 3.3-V version, $V_I = 4$ to $40\text{ V}$ ,<br>Fixed 5-V version, $V_I = 5.5$ to $40\text{ V}$ , $I_O = 0.2\text{ mA}$ |      | 15  | 25    | $\mu\text{A}$    |
| $V_{IN(UVLO)}$                         | IN undervoltage detection                    | Ramp $V_I$ up until the output turns on  | 3.65 |     |       | V                |
|  |  | Ramp $V_I$ down until the output turns OFF   |      |     | 3     |                  |
| <b>REGULATED OUTPUT (OUT)</b>          |  |  |      |     |       |                  |
| $V_O$                                  | Regulated output                             | Fixed 2.5-V version, $V_I = 4$ to $40\text{ V}$ , $I_O = 1$ to $150\text{ mA}$   | -3%  |     | 3%    |                  |
|  |  | Fixed 3.3-V version, $V_I = 5$ to $40\text{ V}$ , $I_O = 1$ to $150\text{ mA}$   | -3%  |     | 3%    |                  |
|  |  | Fixed 5-V version, $V_I = 6.5$ to $40\text{ V}$ , $I_O = 1$ to $150\text{ mA}$   | -3%  |     | 3%    |                  |
| $\Delta V_{O(\Delta V_I)}$             | Line regulation                              | $V_I = 6$ to $40\text{ V}$ , $\Delta V_O$ , $I_O = 10\text{ mA}$   |      |     | 10    | mV               |
| $\Delta V_{O(\Delta I_L)}$             | Load regulation                              | $I_O = 1$ to $150\text{ mA}$ , $\Delta V_O$  |      |     | 20    | mV               |
| $V_{DROPO}$                            | Dropout voltage                              | Fixed 2.5-V version, $V_I - V_O$ , $I_O = 50\text{ mA}$  |      |     | 1.575 | V                |
|  |  | Fixed 2.5-V version, $V_I - V_O$ , $I_O = 100\text{ mA}$   |      |     | 1.575 |                  |
|  |  | Fixed 3.3-V version, $V_I - V_O$ , $I_O = 50\text{ mA}$  |      |     | 799   | mV               |
|  |  | Fixed 3.3-V version, $V_I - V_O$ , $I_O = 100\text{ mA}$   |      |     | 800   |                  |
|  |  | Fixed 5-V version, $V_I - V_O$ , $I_O = 50\text{ mA}$  |      | 220 | 400   |                  |
|  |  | Fixed 5-V version, $V_I - V_O$ , $I_O = 100\text{ mA}$   |      | 450 | 800   |                  |
| $I_O$                                  | Output current                               | $V_O$ in regulation  | 0    |     | 150   | mA               |
| $I_{OCL}$                              | Output current-limit                         | OUT short to ground  | 150  |     | 500   | mA               |
| PSRR                                   | Power supply ripple rejection <sup>(1)</sup> | $V_{rip} = 0.5\text{ V}_{pp}$ , Load = $10\text{ mA}$ , $f = 100\text{ Hz}$ , $C_O = 2.2\ \mu\text{F}$                                 |      | 60  |       | dB               |
| <b>OPERATING TEMPERATURE RANGE</b>     |  |  |      |     |       |                  |
| $T_{sd}$                               | Junction shutdown temperature                |  |      | 175 |       | $^\circ\text{C}$ |
| $T_{hys}$                              | Hysteresis of thermal shutdown               |  |      | 25  |       | $^\circ\text{C}$ |

(1) Design Information—Not tested, ensured by characterization.

## 7.6 Typical Characteristics

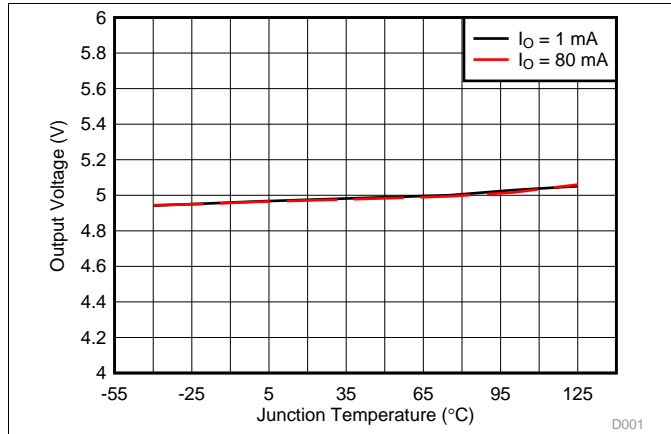


Figure 1. 5-V Output Voltage vs Junction Temperature

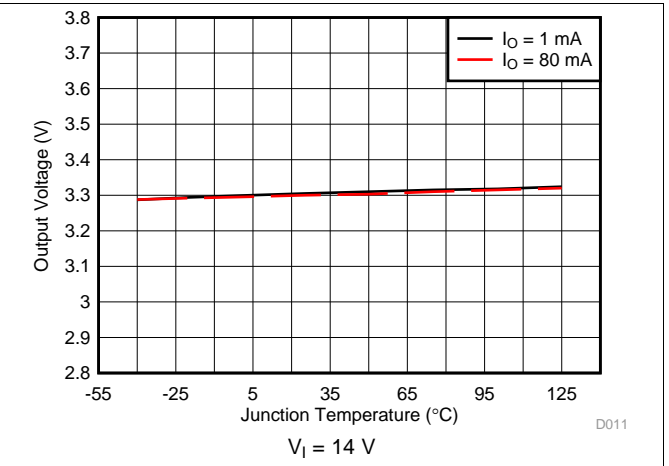


Figure 2. 3.3-V Output Voltage vs Junction Temperature

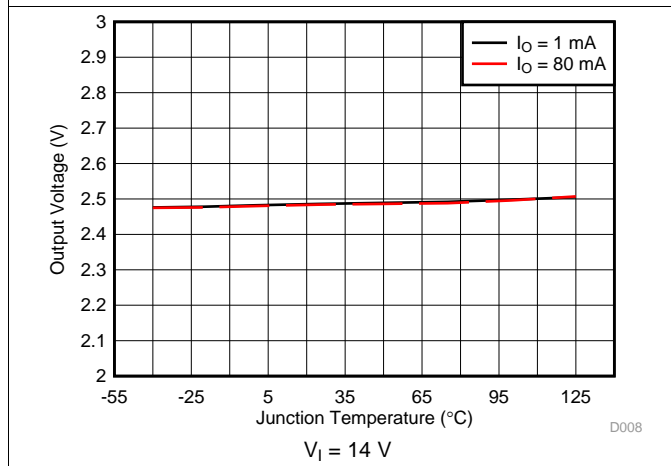


Figure 3. 2.5-V Output Voltage vs Junction Temperature

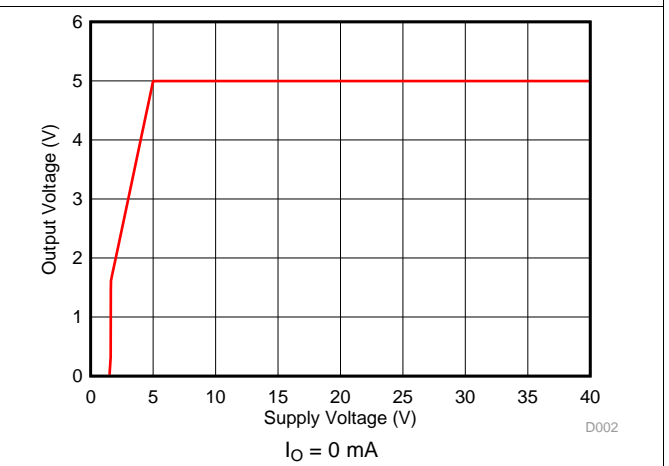


Figure 4. 5-V Output Voltage vs Supply Voltage

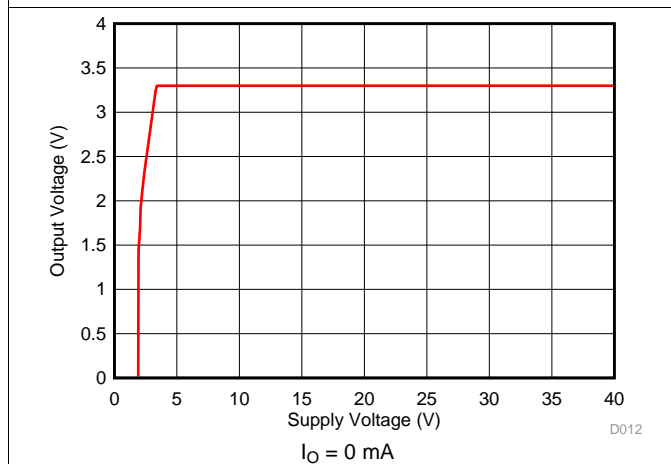


Figure 5. 3.3-V Output Voltage vs Supply Voltage

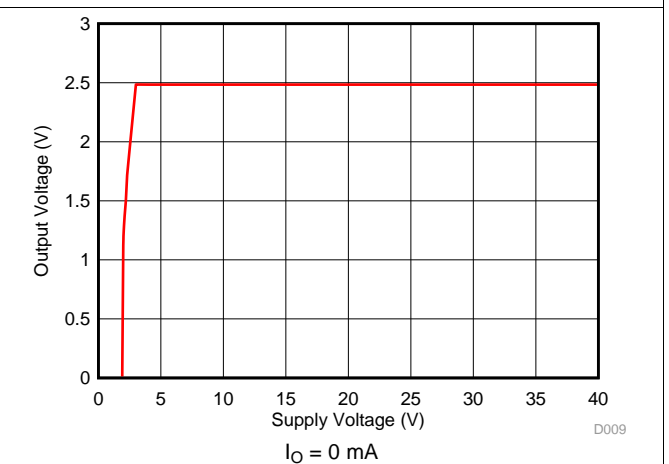


Figure 6. 2.5-V Output Voltage vs Supply Voltage

Typical Characteristics (continued)

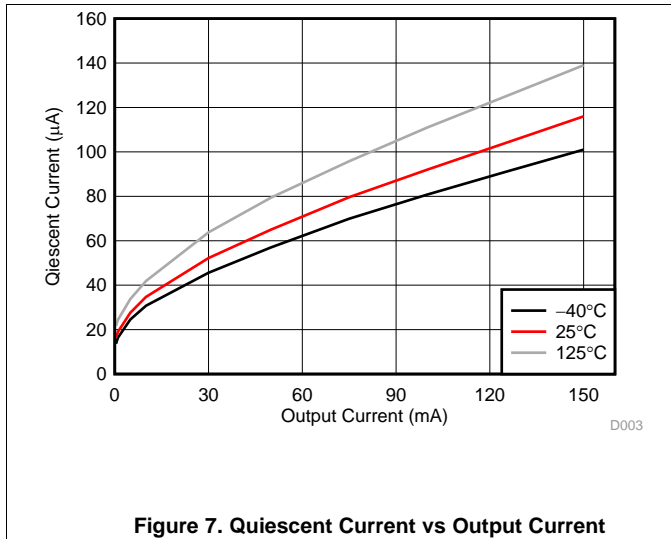


Figure 7. Quiescent Current vs Output Current

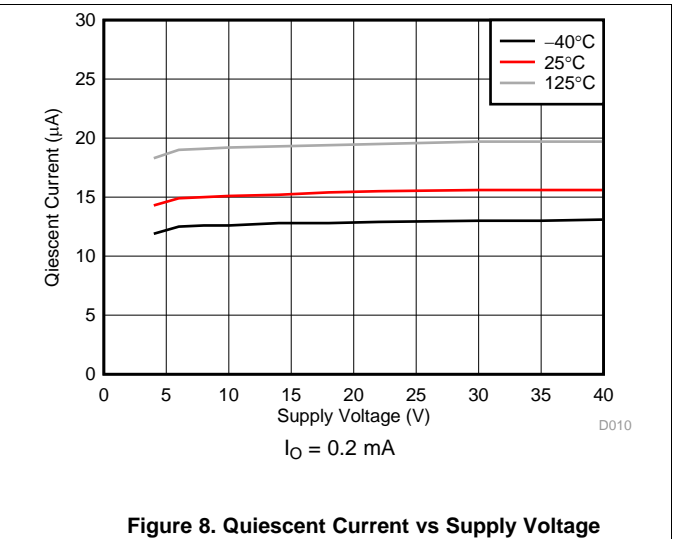


Figure 8. Quiescent Current vs Supply Voltage

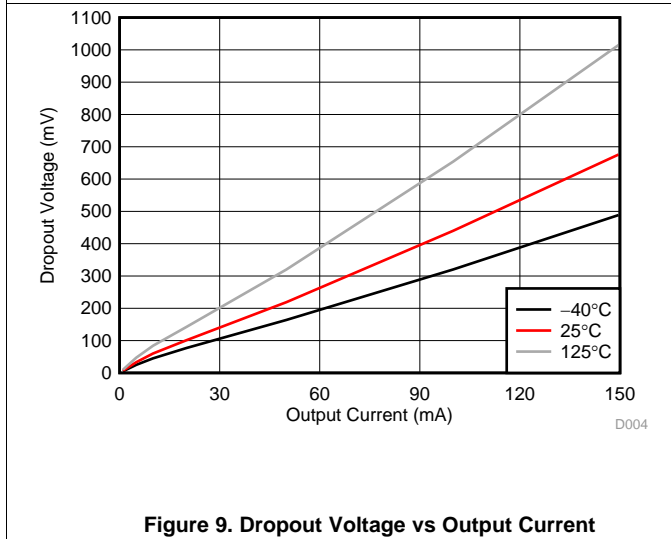


Figure 9. Dropout Voltage vs Output Current

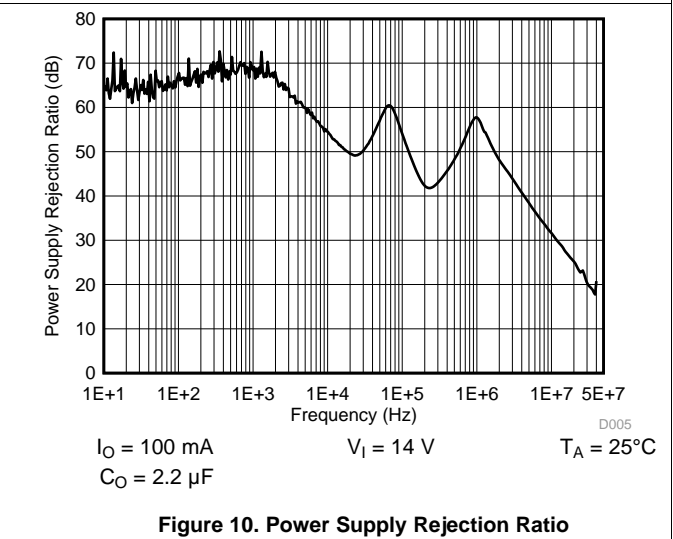


Figure 10. Power Supply Rejection Ratio

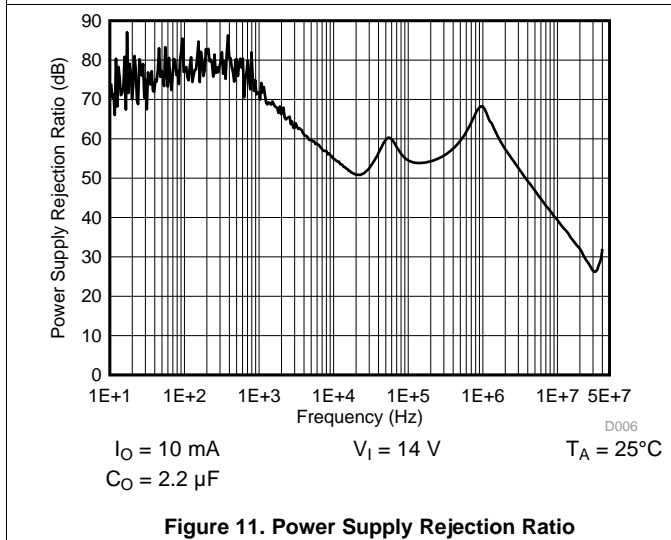


Figure 11. Power Supply Rejection Ratio

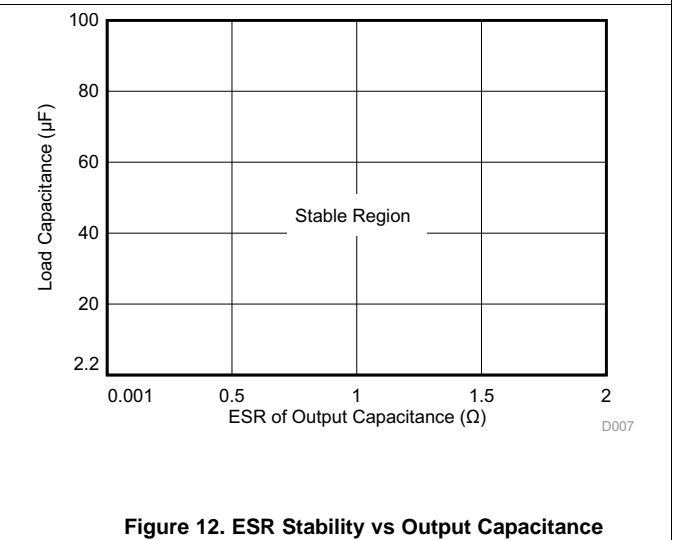
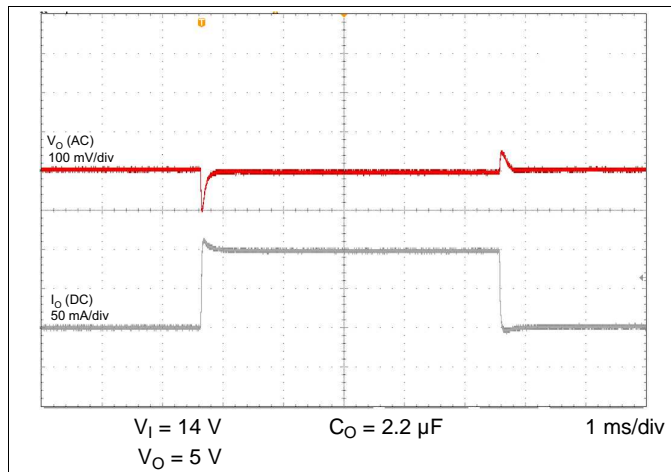
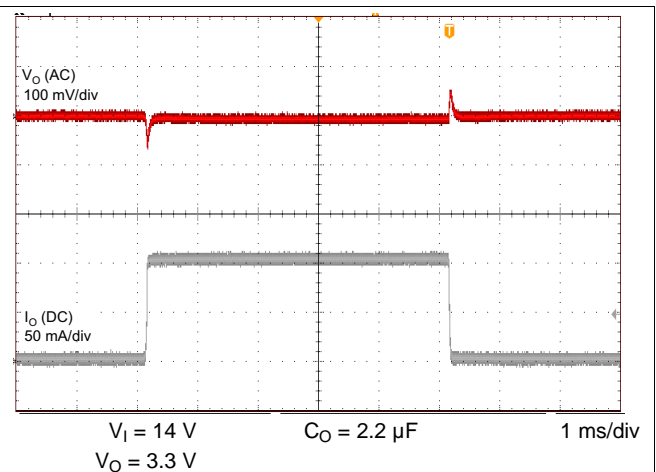
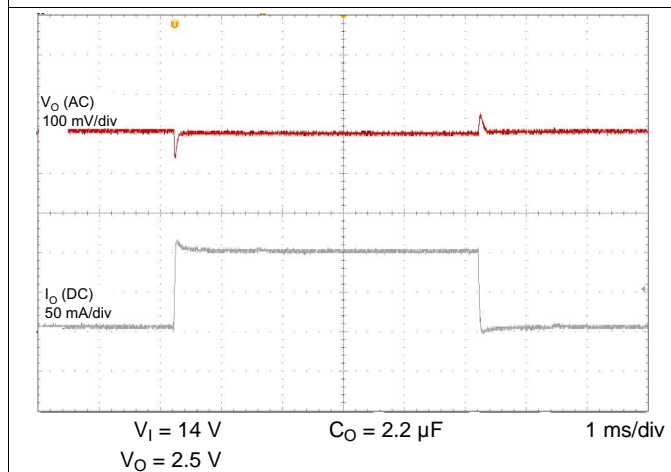
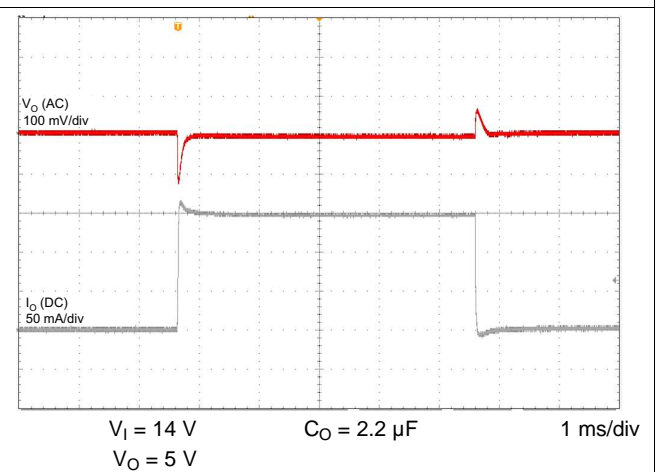
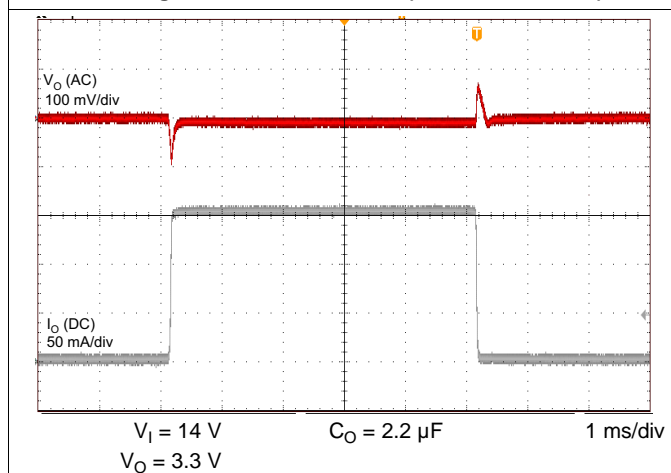
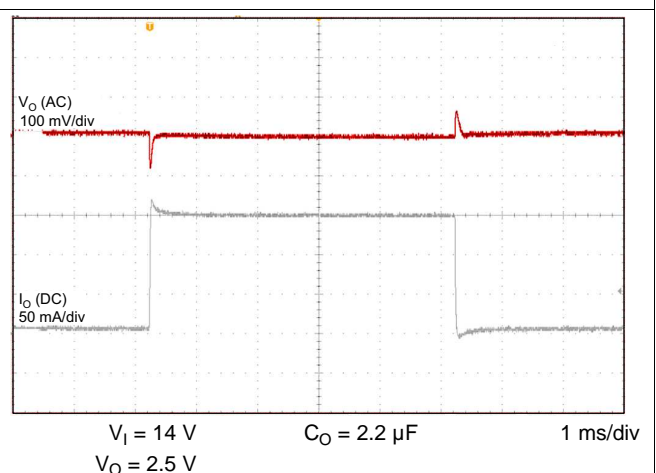


Figure 12. ESR Stability vs Output Capacitance

**Typical Characteristics (continued)**

**Figure 13. Load Transient (1 to 100 mA, 5 V)**

**Figure 14. Load Transient (1 to 100 mA, 3.3 V)**

**Figure 15. Load Transient (1 to 100 mA, 2.5 V)**

**Figure 16. Load Transient (1 to 150 mA, 5 V)**

**Figure 17. Load Transient (1 to 150 mA, 3.3 V)**

**Figure 18. Load Transient (1 to 150 mA, 2.5 V)**



Typical Characteristics (continued)

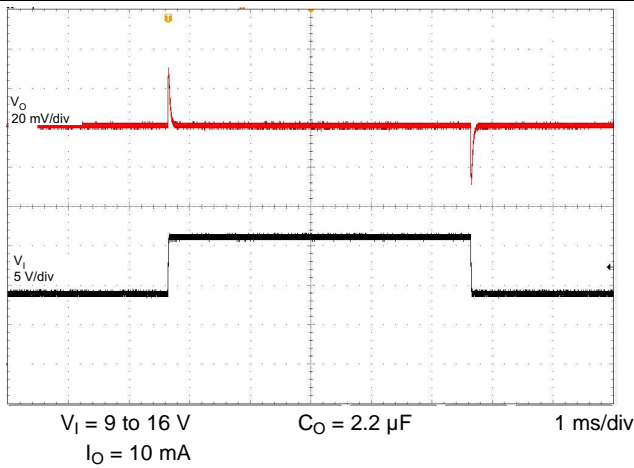


Figure 19. Line Transient ( $V_O = 5\text{ V}$ )

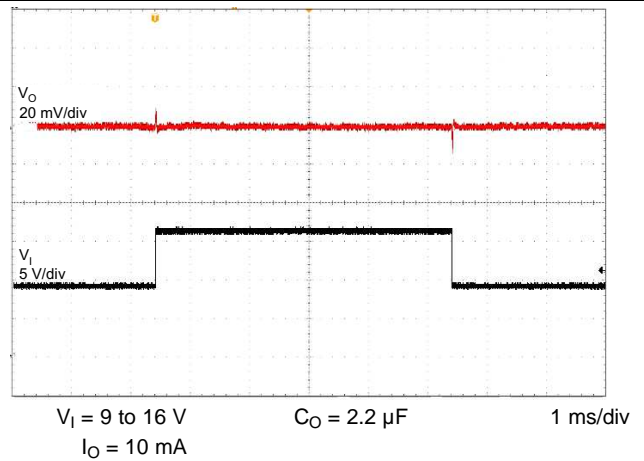


Figure 20. Line Transient ( $V_O = 3.3\text{ V}$ )

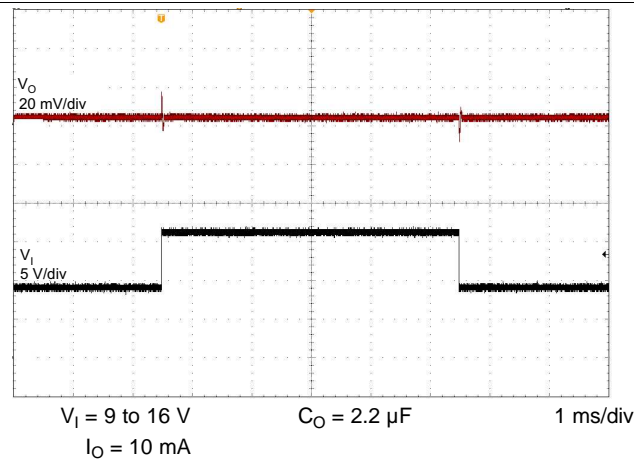


Figure 21. Line Transient ( $V_O = 2.5\text{ V}$ )

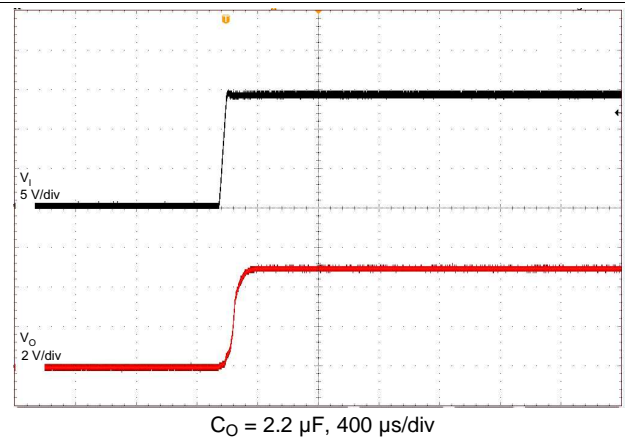


Figure 22. 5-V Power Up

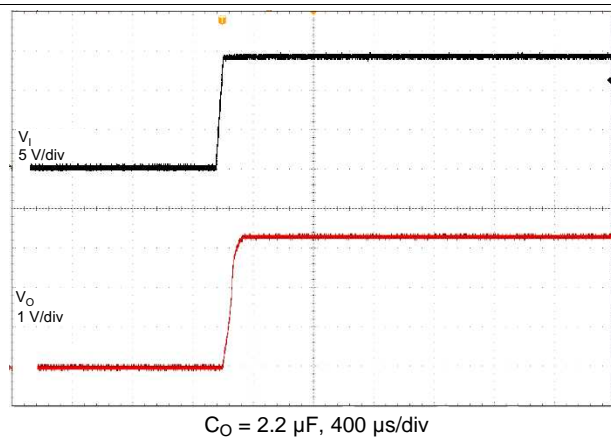


Figure 23. 3.3-V Power Up

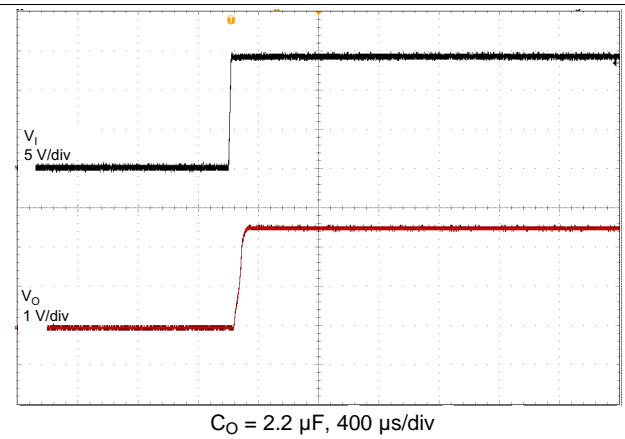


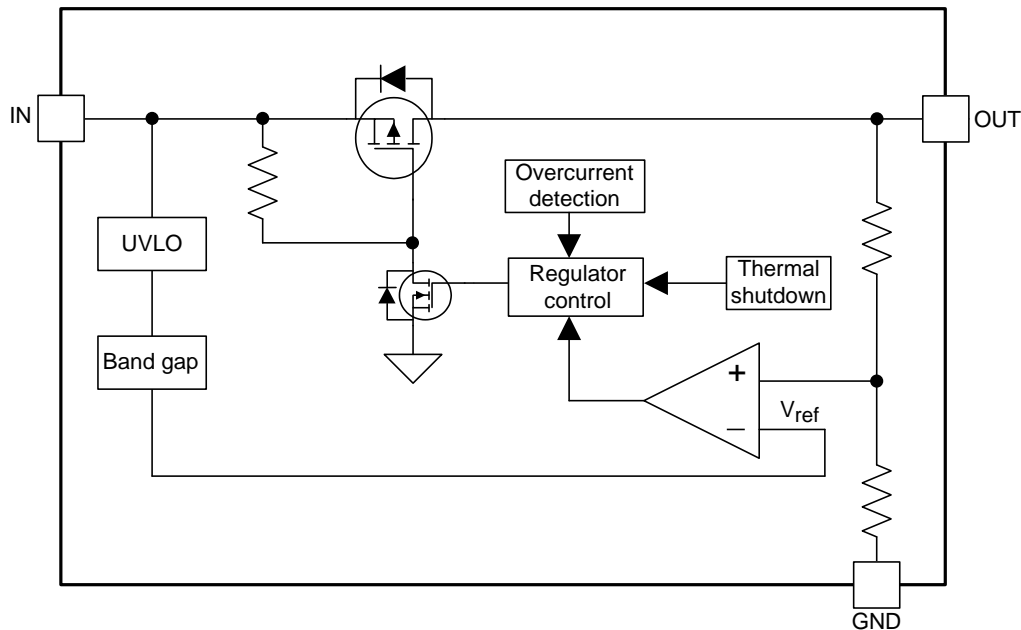
Figure 24. 2.5-V Power Up

## 8 Detailed Description

### 8.1 Overview

The TPS7B69xx-Q1 high-voltage linear regulator operates over a 4-V to 40-V input voltage range. The device has an output current capability of 150 mA and offers fixed output voltages of 2.5 V (TPS7B6925-Q1), 3.3 V (TPS7B6933-Q1) or 5 V (TPS7B6950-Q1). The device features a thermal shutdown and short-circuit protection to prevent damage during over-temperature and overcurrent conditions.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Input (IN)

The IN pin is a high-voltage-tolerant pin. A capacitor with a value higher than 0.1  $\mu\text{F}$  is recommended to be connected close to this pin to better the transient performance.

#### 8.3.2 Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During the initial power up, the regulator has a soft start incorporated to control the initial current through the pass element and the output capacitor.

In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum startup level.

#### 8.3.3 Output Capacitor Selection

For stable operation over the full temperature range and with load currents up to 150 mA, use a capacitor with an effective value between 2.2  $\mu\text{F}$  and 100  $\mu\text{F}$  and ESR smaller than 2  $\Omega$ . To better the load transient performance, an output capacitor, such as a ceramic capacitor with low ESR, is recommended.

#### 8.3.4 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current ( $I_L$ ) and switch resistor. This tracking allows for a smaller input capacitor and can possibly eliminate the need for a boost converter during cold-crank conditions.

## Feature Description (continued)

### 8.3.5 Thermal Shutdown

The TPS7B69xx-Q1 family of devices incorporates a thermal-shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the hysteresis of TSD, the output turns on again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7B69xx-Q1 family of devices is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7B69xx-Q1 family of devices into thermal shutdown degrades device reliability.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $V_I$ Less Than 4 V

The TPS7B69xx-Q1 family of devices operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and the device operates at an input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO, the device shuts down.

### 8.4.2 Operation With $V_I$ Greater Than 4 V

When  $V_I$  is greater than 4 V, if the input voltage is higher than  $V_O$  plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to  $V_I$  minus the dropout voltage.

## 9 Application and Implementation

### NOTE

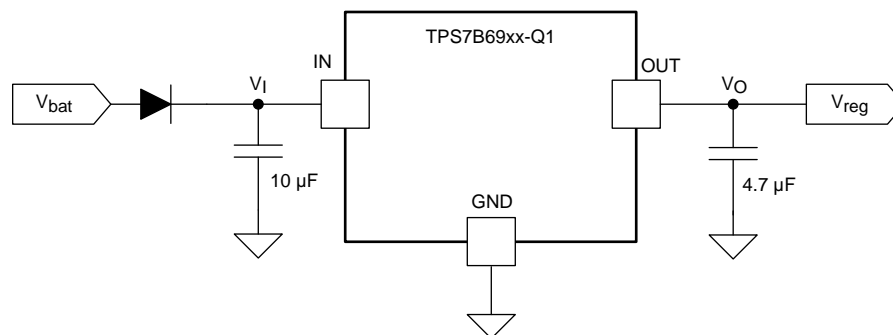
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS7B69xx-Q1 family of devices is a 150-mA low-dropout linear regulator designed for up to 40-V  $V_I$  operation with only 15- $\mu$ A quiescent current at light loads. Use the PSpice transient model to evaluate the base function of the device. To download the PSpice transient model, go to the device product folder on [www.TI.com](http://www.TI.com). In addition to this model, specific evaluation modules (EVM) are available for these devices. For the EVM and the EVM user guide, go to the device product folder.

### 9.2 Typical Application

Figure 25 shows the typical application circuit for the TPS7B69xx-Q1 family of devices. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to achieve better load transient response. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.



**Figure 25. Typical Application Schematic for TPS7B69xx-Q1**

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

| DESIGN PARAMETER           | EXAMPLE VALUES             |
|----------------------------|----------------------------|
| Input voltage range        | 4 to 40 V                  |
| Output voltage             | 2.5 V, 3.3 V, 5 V          |
| Output current rating      | 150 mA                     |
| Output capacitor range     | 2.2 to 100 $\mu$ F         |
| Output capacitor ESR range | 1 m $\Omega$ to 2 $\Omega$ |

#### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output Voltage
- Output current rating

### 9.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommend value for the decoupling capacitor is higher than 0.1  $\mu\text{F}$ . The voltage rating must be greater than the maximum input voltage.

### 9.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The output capacitor value should be between 2.2  $\mu\text{F}$  and 100  $\mu\text{F}$ . The ESR value range should be between 1 m $\Omega$  and 2  $\Omega$ . TI recommends a ceramic capacitor with low ESR to improve the load transient response.

### 9.2.2.3 Power Dissipation and Thermal Considerations

Use [Equation 1](#) to calculate the power dissipated in the device.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- $P_D$  = continuous power dissipation
  - $I_O$  = output current
  - $V_I$  = input voltage
  - $V_O$  = output voltage
- (1)

Because  $I_Q \ll I_O$ , the term  $I_Q \times V_I$  in [Equation 1](#) can be ignored.

For a device under operation at a given ambient air temperature ( $T_A$ ), use [Equation 2](#) to calculate the junction temperature ( $T_J$ ).

$$T_J = T_A + (Z_{\theta JA} \times P_D)$$

where

- $Z_{\theta JA}$  = junction-to-ambient air thermal impedance
- (2)

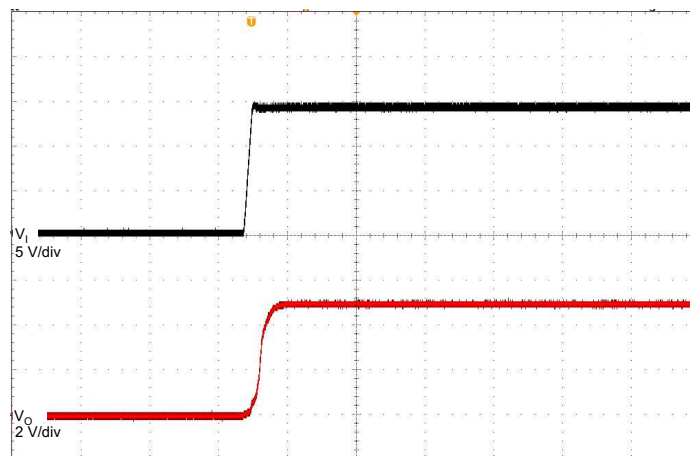
Use [Equation 3](#) to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (Z_{\theta JA} \times P_D)$$
(3)

For a given maximum junction temperature ( $T_{Jmax}$ ), use [Equation 4](#) to calculate the maximum ambient air temperature ( $T_{Amax}$ ) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (Z_{\theta JA} \times P_D)$$
(4)

## 9.2.3 Application Curve



$C_O = 2.2 \mu\text{F}$ , 400  $\mu\text{s}/\text{div}$

**Figure 26. Power Up (5 V)**

## 10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10  $\mu$ F and a ceramic bypass capacitor at the input.

## 11 Layout

### 11.1 Layout Guidelines

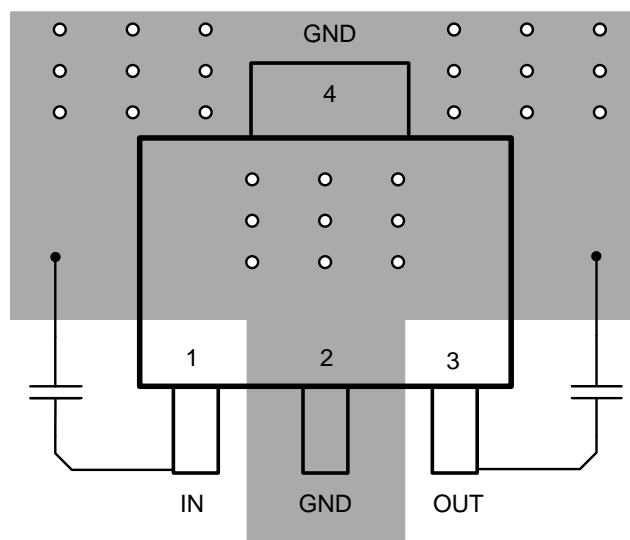
For the layout of TPS7B69xx-Q1 family of devices, place the input and output capacitors close to the devices as shown in [Figure 27](#) and [Figure 28](#). To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of long traces because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7B69xx-Q1 evaluation board.

### 11.2 Layout Example



**Figure 27. Layout Example for SOT-223 Package**

## Layout Example (continued)

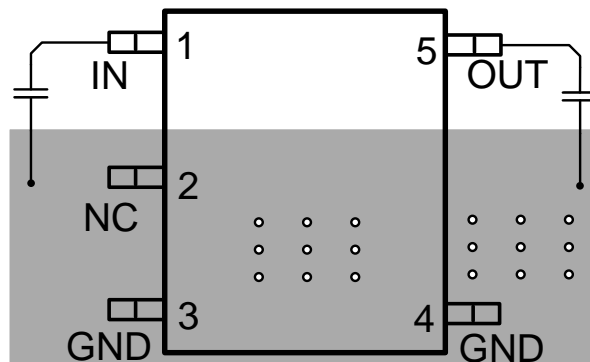


Figure 28. Layout Example for SOT-23 Package

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*TPS7B6950EVM User's Guide*, [SLVUAC0](#).

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS        | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS7B6925-Q1 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS7B6933-Q1 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS7B6950-Q1 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.3 Trademarks

All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS7B6925QDBVRQ1 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | ZBE2                    | <a href="#">Samples</a> |
| TPS7B6925QDCYRQ1 | ACTIVE        | SOT-223      | DCY             | 4    | 2500        | RoHS & Green    | SN                                   | Level-3-260C-168 HR  | -40 to 125   | 7B6925                  | <a href="#">Samples</a> |
| TPS7B6933QDBVRQ1 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | ZBF2                    | <a href="#">Samples</a> |
| TPS7B6933QDCYRQ1 | ACTIVE        | SOT-223      | DCY             | 4    | 2500        | RoHS & Green    | SN                                   | Level-3-260C-168 HR  | -40 to 125   | 7B6933                  | <a href="#">Samples</a> |
| TPS7B6950QDBVRQ1 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 125   | ZAZ2                    | <a href="#">Samples</a> |
| TPS7B6950QDCYRQ1 | ACTIVE        | SOT-223      | DCY             | 4    | 2500        | RoHS & Green    | SN                                   | Level-3-260C-168 HR  | -40 to 125   | 7B6950                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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**OTHER QUALIFIED VERSIONS OF TPS7B69-Q1 :**

- Catalog: [TPS7B69](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS7B6925QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS7B6925QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 330.0              | 12.4               | 7.05    | 7.4     | 1.9     | 8.0     | 12.0   | Q3            |
| TPS7B6933QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS7B6933QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 330.0              | 12.4               | 7.05    | 7.4     | 1.9     | 8.0     | 12.0   | Q3            |
| TPS7B6950QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS7B6950QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 330.0              | 12.4               | 7.05    | 7.4     | 1.9     | 8.0     | 12.0   | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS7B6925QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 190.0       | 190.0      | 30.0        |
| TPS7B6925QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 340.0       | 340.0      | 38.0        |
| TPS7B6933QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 190.0       | 190.0      | 30.0        |
| TPS7B6933QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 340.0       | 340.0      | 38.0        |
| TPS7B6950QDBVRQ1 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TPS7B6950QDCYRQ1 | SOT-223      | DCY             | 4    | 2500 | 340.0       | 340.0      | 38.0        |

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC MO-178.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCY (R-PDSO-G4)

PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters (inches).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC TO-261 Variation AA.

DCY (R-PDSO-G4)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.



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