

# 具有使能端和电源正常指示功能的 TPS7A16A-Q1 60V、5 $\mu$ A I<sub>Q</sub>、100mA、低压降稳压器

## 1 特性

- 适用于汽车 应用
- 下列性能符合 AEC-Q100 标准：
  - 器件温度 1 级：-40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C3B
- 宽输入电压范围：3V 至 60V
- 超低静态电流：5  $\mu$ A
- 停机时静态电流：1 $\mu$ A
- 输出电流：100 mA
- 低压差电压：电流为 20mA 时电压为 60mV
- 精度：2%
- 可提供：
  - 固定输出电压：3.3V、5V
  - 可调节输出电压：大约 1.2 至 18.5V
- 具有可编程延迟的电源正常指示功能
- 电流限制和热关断保护
- 与陶瓷输出电容器一起工作时保持稳定： $\geq 2.2\mu$ F
- 封装：高热性能 HVSSOP-8 PowerPAD™

## 2 应用

- 紧急呼叫 (eCall)
- 电池管理系统 (BMS)
- 车载充电器 (OBC) 和无线充电器
- 直流/直流转换器

## 3 说明

TPS7A16A-Q1 超低功耗、低压降 (LDO) 稳压器具有超低静态电流、高输入电压以及微型高热性能封装等诸多优势。

TPS7A16A-Q1 专为连续或断续（备用电源）电池供电的应用而设计，超低静态电流在此类应用中对于延长系统电池寿命至关重要。

TPS7A16A-Q1 提供了一个与标准互补金属氧化物半导体 (CMOS) 逻辑兼容的使能引脚 (EN) 以及一个具有用户可编程延迟的集成开漏高电平有效电源正常输出 (PG)。这些引脚专用于需要进行电源轨排序、基于微控制器的电池供电类应用。

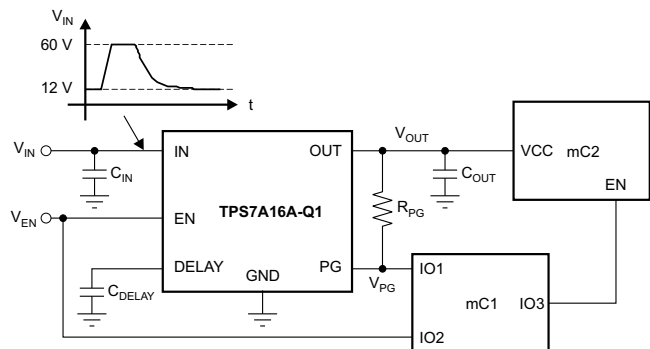
此外，TPS7A16A-Q1 非常适合通过多节电池解决方案生成低电压电源（从高电池节数电动工具组到汽车应用）；TPS7A16A-Q1 器件不但能够提供稳压良好的电压轨，还能够承受瞬态电压并在电压瞬态期间保持稳压状态。这些特性意味着电涌保护电路更加简单且更为经济高效。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS7A16A-Q1	HVSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

### 典型应用原理图



## 目录

<b>1</b>	特性 .....	<b>1</b>	7.4	Device Functional Modes.....	<b>10</b>
<b>2</b>	应用 .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>10</b>
<b>3</b>	说明 .....	<b>1</b>	8.1	Application Information.....	<b>10</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	8.2	Typical Applications .....	<b>11</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>15</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	<b>10</b>	<b>Layout</b> .....	<b>15</b>
6.1	Absolute Maximum Ratings .....	<b>4</b>	10.1	Layout Guidelines .....	<b>15</b>
6.2	ESD Ratings.....	<b>4</b>	10.2	Layout Examples.....	<b>16</b>
6.3	Recommended Operating Conditions.....	<b>4</b>	<b>11</b>	器件和文档支持 .....	<b>18</b>
6.4	Thermal Information .....	<b>4</b>	11.1	接收文档更新通知 .....	<b>18</b>
6.5	Electrical Characteristics.....	<b>5</b>	11.2	社区资源 .....	<b>18</b>
6.6	Typical Characteristics .....	<b>6</b>	11.3	商标 .....	<b>18</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>9</b>	11.4	静电放电警告 .....	<b>18</b>
7.1	Overview .....	<b>9</b>	11.5	术语表 .....	<b>18</b>
7.2	Functional Block Diagram .....	<b>9</b>	<b>12</b>	机械、封装和可订购信息 .....	<b>18</b>
7.3	Feature Description .....	<b>9</b>			

## 4 修订历史记录

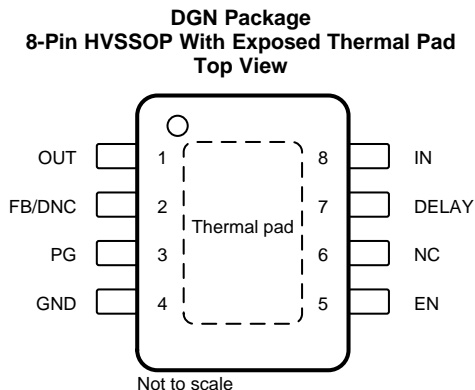
注：之前版本的页码可能与当前版本有所不同。

### Changes from Original (February 2019) to Revision A

Page

• 已更改 将状态从“预告信息”更改为“生产数据” .....	<b>1</b>
---------------------------------	----------

## 5 Pin Configuration and Functions



NC – No internal connection

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ , the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$ , the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	I	For the adjustable version, the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed-voltage versions, <b>do not connect</b> to this pin. Do not route this pin to any electrical net, not even to GND or IN.
GND	4	—	Ground pin
IN	8	I	Regulator input supply pin. A capacitor $> 0.1 \mu\text{F}$ must be tied from this pin to ground to assure stability. TI recommends connecting a $10\text{-}\mu\text{F}$ ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	---	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor $> 2.2 \mu\text{F}$ must be tied from this pin to ground to assure stability. TI recommends connecting a $10\text{-}\mu\text{F}$ ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	O	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad	Pad	---	Solder to the printed circuit board (PCB) to enhance thermal performance. Although the thermal pad can be left floating, TI highly recommends connecting the thermal pad to the GND plane.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	-0.3	62	V
	OUT pin to GND pin	-0.3	20	
	OUT pin to IN pin	-62	0.3	
	FB pin to GND pin	-0.3	3	
	FB pin to IN pin	-62	0.3	
	EN pin to IN pin	-62	0.3	
	EN pin to GND pin	-0.3	62	
	PG pin to GND pin	-0.3	5.5	
	DELAY pin to GND pin	-0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, $T_J$ , absolute maximum <sup>(2)</sup>	-40	150	°C
	Storage, $T_{STG}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

### 6.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	Corner pins (OUT, GND, IN, and EN)		±750
			Other pins		±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	3		60	V
$V_{OUT}$	Output voltage	1.2		18.5	V
EN	EN pin voltage	0		$V_{IN}$	V
	EN pin slew-rate, voltage ramp-up			1.5	V/ $\mu$ s
DELAY	Delay pin voltage	0		5	V
PG	Power-good pin voltage	0		5	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7A16A-Q1	UNIT
		DGN (HVSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	2.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	24.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	10.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and [IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 500\text{ mV}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\text{ }\mu\text{A}$ ,  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $C_{OUT} = 2.2\text{ }\mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range		3		60	V
$V_{REF}$	Internal reference	$T_A = 25^\circ\text{C}$ , $V_{FB} = V_{REF}$ , $V_{IN} = 3\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$	1.169	1.193	1.217	V
$V_{UVLO}$	Undervoltage lockout threshold			2		V
$V_{OUT}$	Output voltage range	$V_{IN} \geq V_{OUT(NOM)} + 0.5\text{ V}$	$V_{REF}$		18.5	V
	Overall $V_{OUT}$ accuracy	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 60\text{ V}^{(1)}$ , $10\text{ }\mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$	-2%		2%	
$\Delta V_{O(\Delta V)}$	Line regulation	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$		$\pm 1$		% $V_{OUT}$
$\Delta V_{O(\Delta I)}$	Load regulation	$10\text{ }\mu\text{A} \leq I_{OUT} \leq 100\text{ mA}$		$\pm 1$		% $V_{OUT}$
$V_{DO}$	Dropout voltage	$V_{IN} = 0.95 \times V_{OUT(NOM)}$ , $I_{OUT} = 20\text{ mA}$		60		mV
		$V_{IN} = 0.95 \times V_{OUT(NOM)}$ , $I_{OUT} = 100\text{ mA}$		265	500	
$I_{LIM}$	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$ , $V_{IN} = V_{OUT(NOM)} + 1\text{ V}^{(2)}$	101	225	400	mA
		$V_{OUT} = 90\% V_{OUT(NOM)}$ , $V_{IN} = 3\text{ V}^{(3)}$	101	225	400	
$I_{GND}$	Ground current	$3\text{ V} \leq V_{IN} \leq 60\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$		5	15	$\mu\text{A}$
		$I_{OUT} = 100\text{ mA}$ , $V_{OUT} = 1.2\text{ V}$		60		
$I_{SHDN}$	Shutdown supply current	$V_{EN} = 0.4\text{ V}$ , $V_{IN} = 12\text{ V}$		0.59	5.0	$\mu\text{A}$
$I_{FB}$	Feedback current <sup>(4)</sup>		-1	0.0	1	$\mu\text{A}$
$I_{EN}$	Enable current	$3\text{ V} \leq V_{IN} \leq 12\text{ V}$ , $V_{IN} = V_{EN}$	-1	0.01	1	$\mu\text{A}$
$V_{EN\_HI}$	Enable high-level voltage		1.2			V
$V_{EN\_LO}$	Enable low-level voltage				0.3	V
$V_{IT}$	PG trip threshold	OUT pin floating, $V_{FB}$ increasing, $V_{IN} \geq V_{IN\_MIN}$	85		95	% $V_{OUT}$
		OUT pin floating, $V_{FB}$ decreasing, $V_{IN} \geq V_{IN\_MIN}$	83		93	
$V_{HYS}$	PG trip hysteresis			2.3		% $V_{OUT}$
$V_{PG\_LO}$	PG output low voltage	OUT pin floating, $V_{FB} = 80\% V_{REF}$ , $I_{PG} = 100\text{ }\mu\text{A}$			0.4	V
$I_{PG\_LKG}$	PG leakage current	$V_{PG} = V_{OUT(NOM)}$	-1		1	$\mu\text{A}$
$I_{DELAY}$	DELAY pin current			1	2	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 3\text{ V}$ , $V_{OUT(NOM)} = V_{REF}$ , $C_{OUT} = 10\text{ }\mu\text{F}$ , $f = 100\text{ Hz}$		50		dB
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		175		$^\circ\text{C}$
		Reset, temperature decreasing		155		

- (1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ( $P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$ ). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
- (2) For fixed output voltages only.
- (3) For adjustable output only, where  $V_{OUT} = 1.2\text{ V}$
- (4)  $I_{FB} > 0\text{ }\mu\text{A}$  flows out of the device.

### 6.6 Typical Characteristics

at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

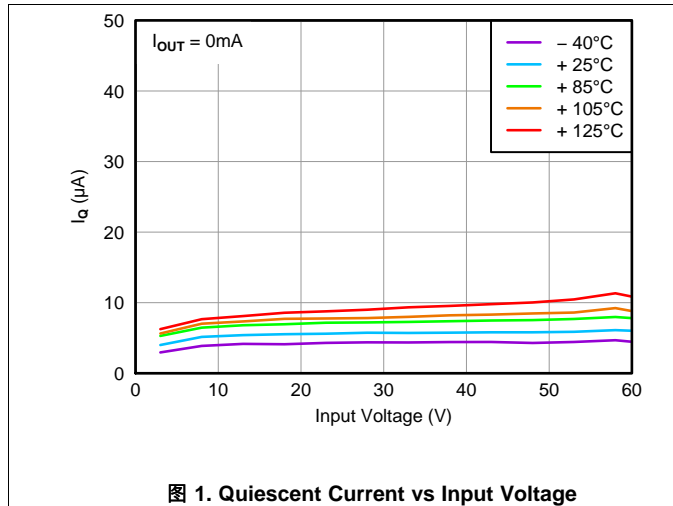


图 1. Quiescent Current vs Input Voltage

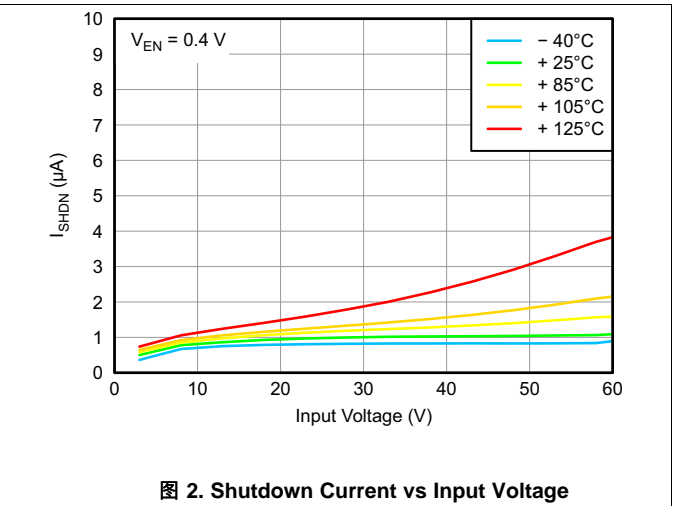


图 2. Shutdown Current vs Input Voltage

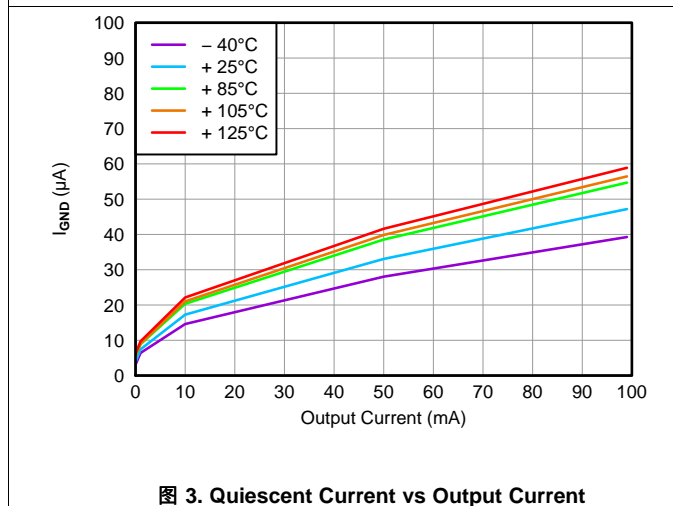


图 3. Quiescent Current vs Output Current

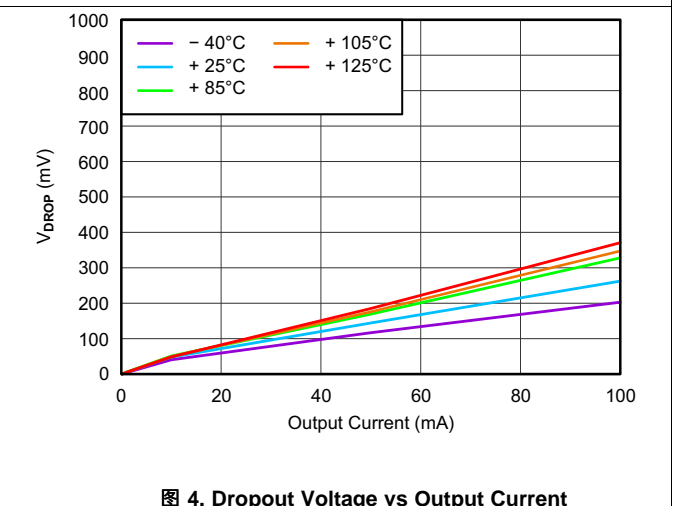


图 4. Dropout Voltage vs Output Current

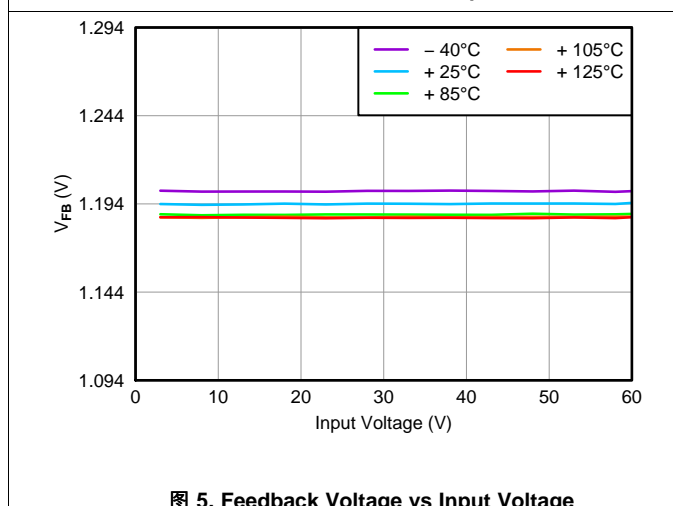


图 5. Feedback Voltage vs Input Voltage

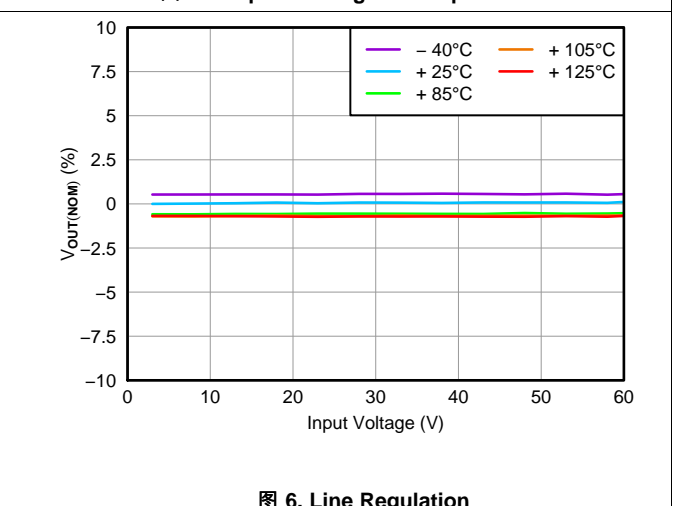


图 6. Line Regulation

Typical Characteristics (接下页)

at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)

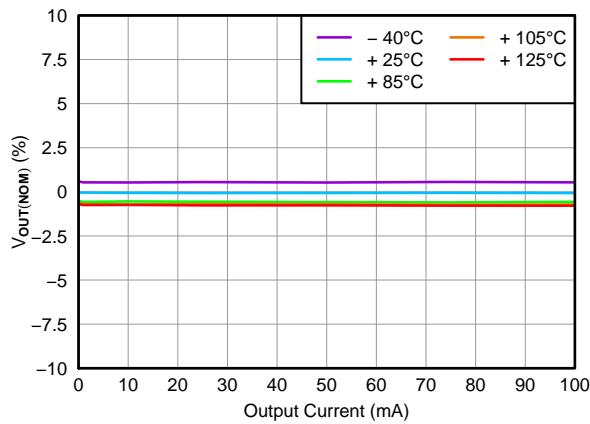


图 7. Load Regulation

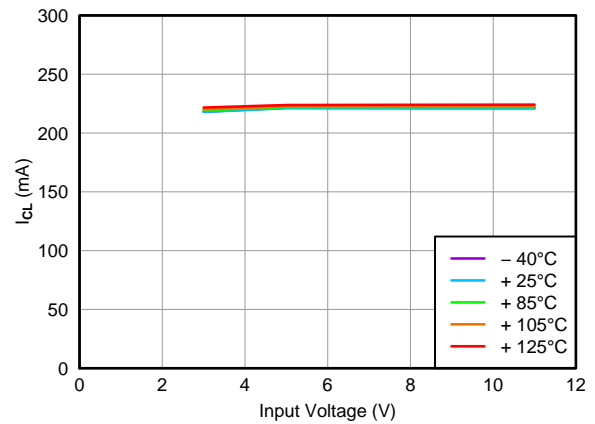


图 8. Current Limit vs Input Voltage

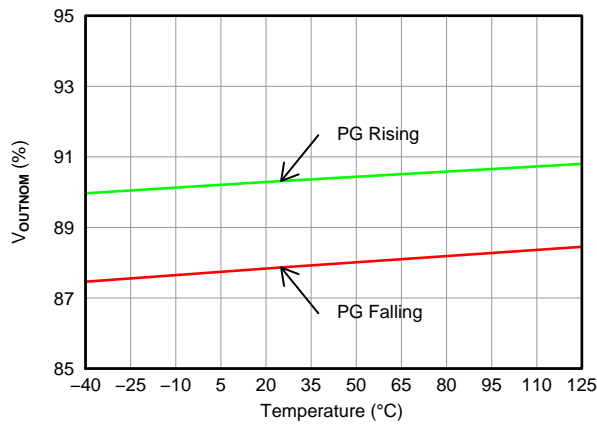


图 9. Power-Good Threshold Voltage vs Temperature

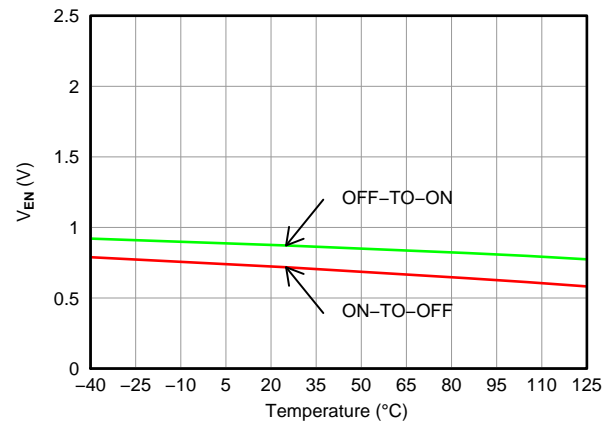


图 10. Enable Threshold Voltage vs Temperature

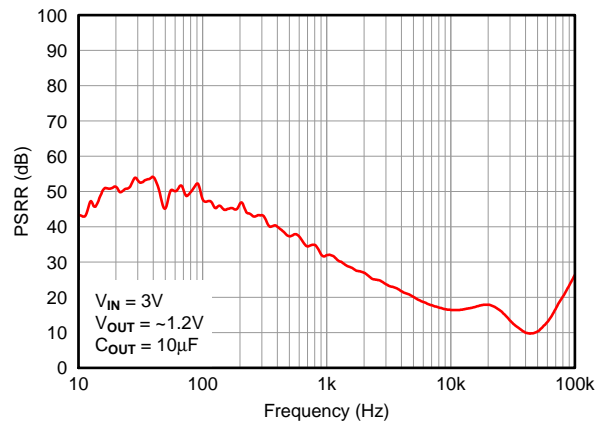


图 11. Power-Supply Rejection Ratio vs Frequency

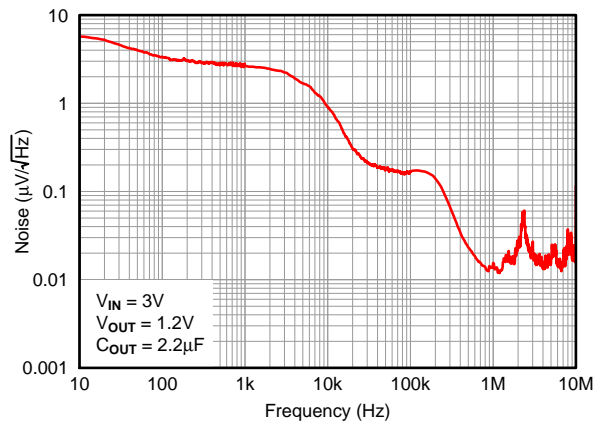
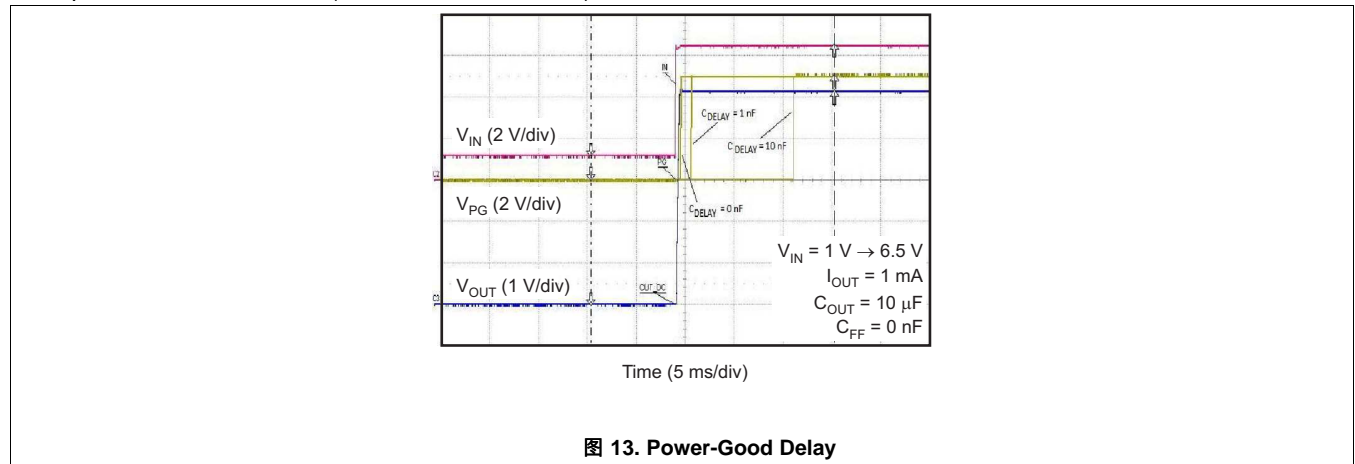


图 12. Output Spectral Noise Density

**Typical Characteristics (接下页)**

at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $V_{IN} = 3\text{ V}$  (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10\ \mu\text{A}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ , and FB tied to OUT (unless otherwise noted)



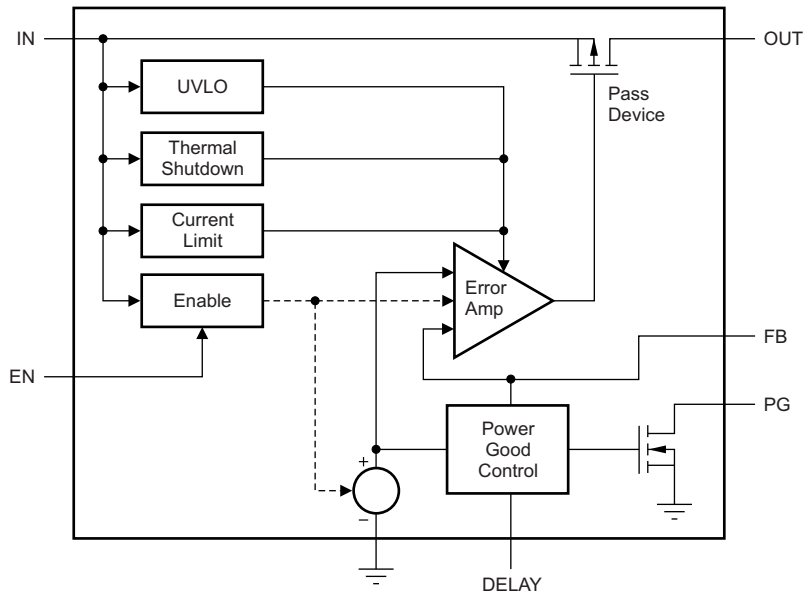


## 7 Detailed Description

### 7.1 Overview

The TPS7A16A-Q1 is an ultra-low-power, low-dropout (LDO) voltage regulator that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16A-Q1 also offers an enable pin (EN) and an integrated open-drain, active-high, power-good output (PG) with a user-programmable delay.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN activates the device and turns on the regulator. For self-bias applications, connect this input to the IN pin. Ensure that  $V_{EN} \leq V_{IN}$  at all times.

When the enable signal is comprised of pulse-width modulation (PWM) pulses, the slew rate of the rising and falling edges must be less than  $1.5 \text{ V}/\mu\text{s}$ . Adding a  $0.1\text{-}\mu\text{F}$  capacitor from the EN pin to GND is recommended.

#### 7.3.2 Regulated Output ( $V_{OUT}$ )

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft-start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the undervoltage lockout (UVLO) threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

#### 7.3.3 PG Delay Timer (DELAY)

The power-good delay time ( $t_{DELAY}$ ) is defined as the time period from when  $V_{OUT}$  exceeds the PG trip threshold voltage ( $V_{IT}$ ) to when the PG output is high. This power-good delay time is set by an external capacitor ( $C_{DELAY}$ ) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current ( $I_{DELAY}$ ) when  $V_{OUT}$  exceeds the PG trip threshold ( $V_{IT}$ ).

## 7.4 Device Functional Modes

### 7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no  $C_{DELAY}$  is used, the PG output is high-impedance when  $V_{OUT}$  is greater than the PG trip threshold ( $V_{IT}$ ). If  $V_{OUT}$  drops below  $V_{IT}$ , the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain  $V_{IN} \geq 3\text{ V}$  ( $V_{IN\_MIN}$ ).

#### 7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time ( $t_{DELAY}$ ) is defined as the time period from when  $V_{OUT}$  exceeds the PG trip threshold voltage ( $V_{IT}$ ) to when the PG output is high. This power-good delay time is set by an external capacitor ( $C_{DELAY}$ ) connected from the DELAY pin to GND; this capacitor is charged from 0 V to up to 1.8 V by the DELAY pin current ( $I_{DELAY}$ ) once  $V_{OUT}$  exceeds the PG trip threshold ( $V_{IT}$ ).

When  $C_{DELAY}$  is used, the PG output is high-impedance when  $V_{OUT}$  exceeds  $V_{IT}$ , and  $V_{DELAY}$  exceeds  $V_{REF}$ .

The power-good delay time can be calculated using:  $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$ . For example, when  $C_{DELAY} = 10\text{ nF}$ , the PG delay time is approximately 12 ms; that is,  $(10\text{ nF} \times 1.193\text{ V}) / 1\text{ }\mu\text{A} = 11.93\text{ ms}$ .

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7A16A-Q1 offers the benefit of ultra-low quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A-Q1 is designed for continuous or sporadic (power backup) battery-operated applications where ultra-low quiescent current is critical to extending system battery life.

## 8.2 Typical Applications

### 8.2.1 TPS7A16A-Q1 Circuit as an Adjustable Regulator

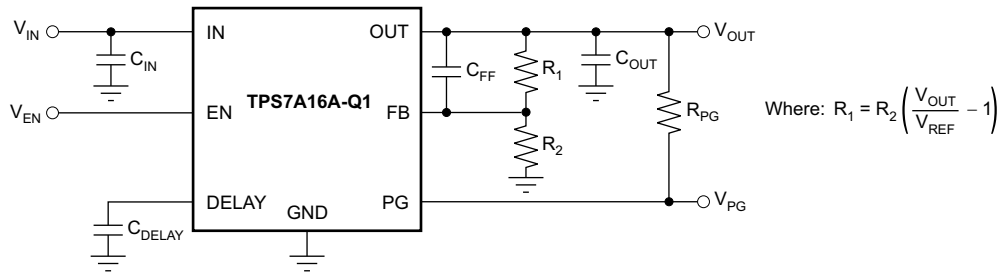


图 14. The TPS7A16A-Q1 Circuit as an Adjustable Regulator Schematic

#### 8.2.1.1 Design Requirements

表 1 lists the design parameters for this application.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Delay capacitor range	100 pF to 100 nF

#### 8.2.1.2 Detailed Design Procedure

##### 8.2.1.2.1 Adjustable Voltage Operation

The TPS7A16A-Q1 has an output voltage range from 1.194 V to 20 V. As shown in 图 15, the nominal output of the device is set by two external resistors.

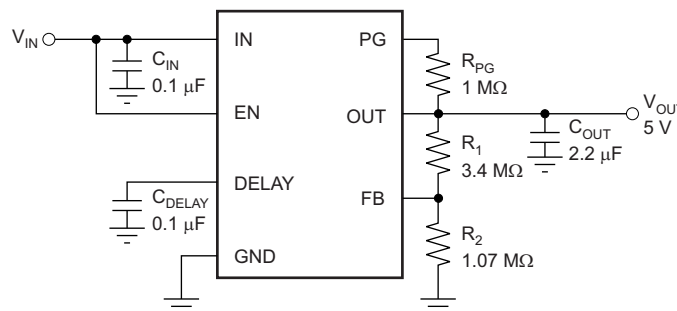


图 15. Adjustable Operation

公式 1 can calculate  $R_1$  and  $R_2$  for any output voltage range:

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

##### 8.2.1.2.1.1 Resistor Selection

Use resistors in the order of  $M\Omega$  to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

表 2 shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in 公式 1.

**表 2. Selected Resistor Combinations**

V <sub>OUT</sub>	R <sub>1</sub>	R <sub>2</sub>	V <sub>OUT</sub> /(R <sub>1</sub> + R <sub>2</sub> ) « I <sub>Q</sub>	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 μA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2.5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants can significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16A-Q1 or using resistors in the order of hundreds or tens of kΩ.

#### 8.2.1.2.2 Capacitor Recommendations

Use low equivalent-series-resistance (ESR) capacitors for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, but ceramic X5R capacitors are the most cost-effective and are available in higher values.

However, high-ESR capacitors can degrade PSRR.

#### 8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16A-Q1 ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 μF and output capacitance of 2.2 μF; however, TI recommends using a 10-μF ceramic capacitor to maximize ac performance.

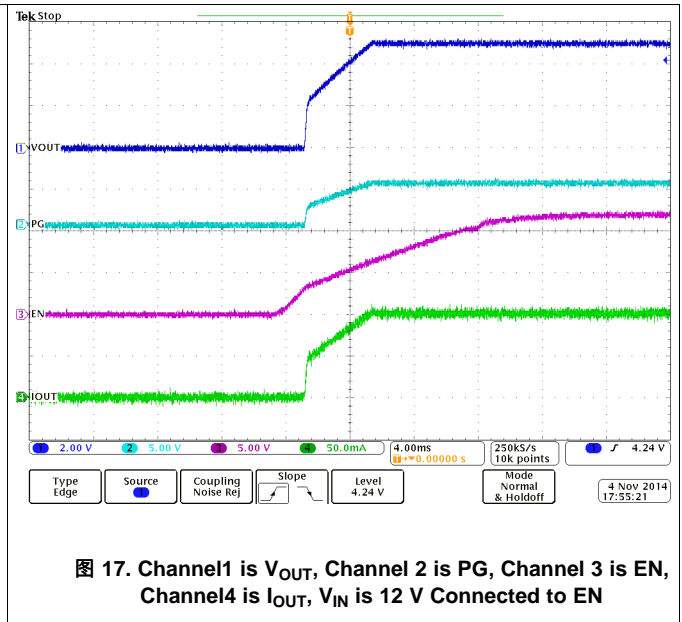
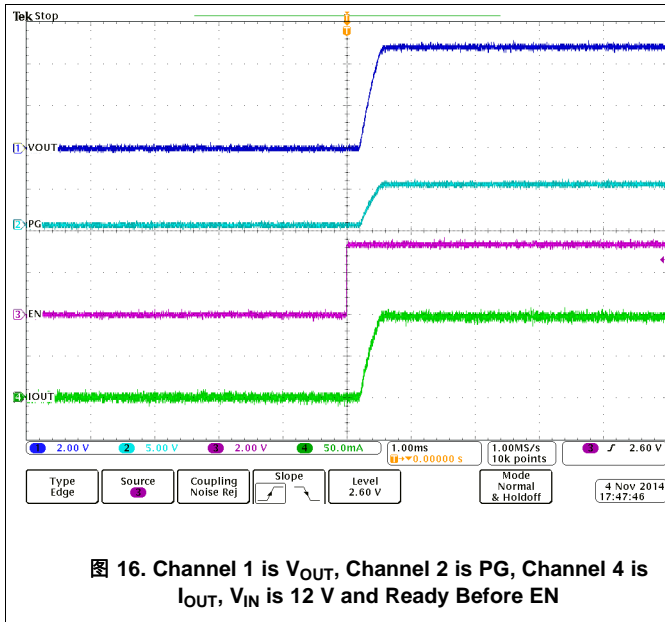
#### 8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C<sub>FF</sub>) from OUT to FB is not needed to achieve stability, TI recommends using a 0.01-μF feed-forward capacitor to maximize ac performance.

#### 8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

### 8.2.1.3 Application Curves



## 8.2.2 Automotive Applications

The TPS7A16A-Q1 maximum input voltage of 60 V makes the device ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) can cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16A-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity. 图 18 shows a circuit diagram of an example automotive application.

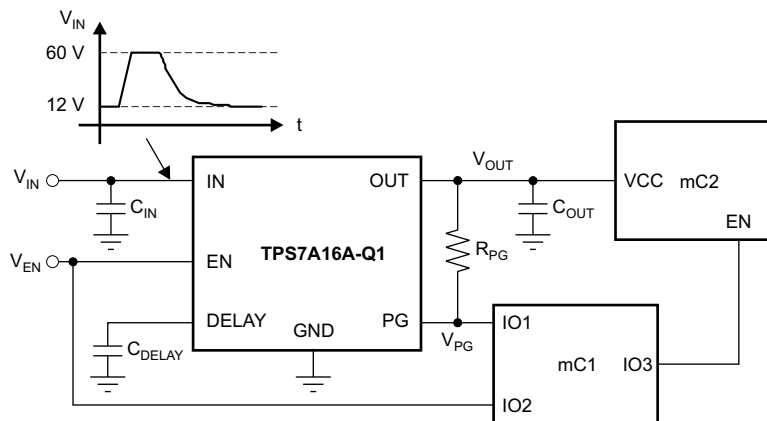


图 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

### 8.2.2.1 Design Requirements

表 3 lists the design parameters for this application.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Delay capacitor range	100 pF to 100 nF

### 8.2.2.2 Detailed Design Procedure

See the [Capacitor Recommendations](#) and [Input and Output Capacitor Requirements](#) sections.

#### 8.2.2.2.1 Device Recommendations

The output is fixed, so choose the TPS7A16A-Q1.

### 8.2.2.3 Application Curves

See 图 16 and 图 17.

## 9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. The TPS7A16A-Q1 ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1  $\mu\text{F}$  and output capacitance of 2.2  $\mu\text{F}$ ; however, TI recommends using a 10- $\mu\text{F}$  ceramic capacitor to maximize AC performance.

## 10 Layout

### 10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, the board is recommended to be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. This grounding scheme is commonly referred to as *star grounding*. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

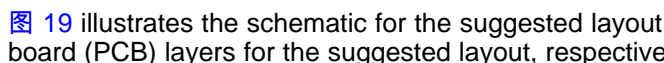

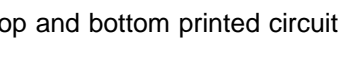

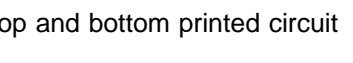
Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this document, use the same layout pattern used for the TPS7A16A-Q1 evaluation board, available at [www.ti.com](http://www.ti.com).

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Acceptable performance can be obtained with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

   illustrates the schematic for the suggested layout.  and  depict the top and bottom printed circuit board (PCB) layers for the suggested layout, respectively.

#### 10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitively-coupled signals can produce undesirable output voltage transients. In these cases, use a fixed-voltage version of the TPS7A16A-Q1, or isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

#### 10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. As [公式 2](#) shows, power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

## Layout Guidelines (接下页)

### 10.1.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, limit junction temperature to a maximum of 125°C at the worst-case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16A-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A16A-Q1 into thermal shutdown degrades device reliability.

### 10.2 Layout Examples

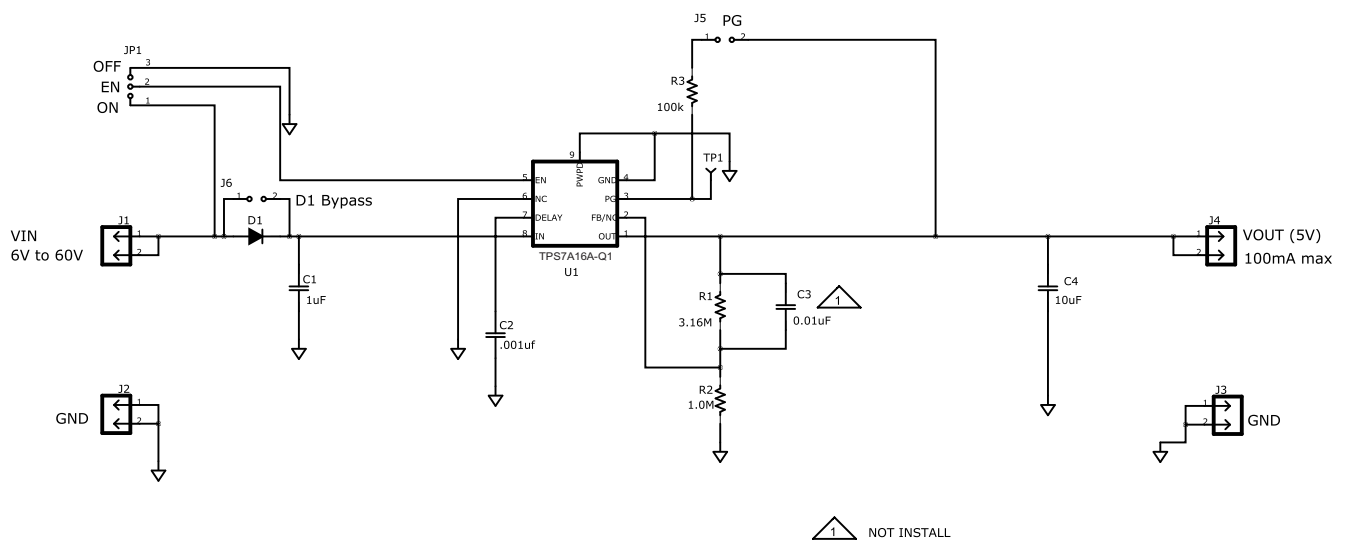


图 19. Schematic for Suggested Layout



Layout Examples (接下页)

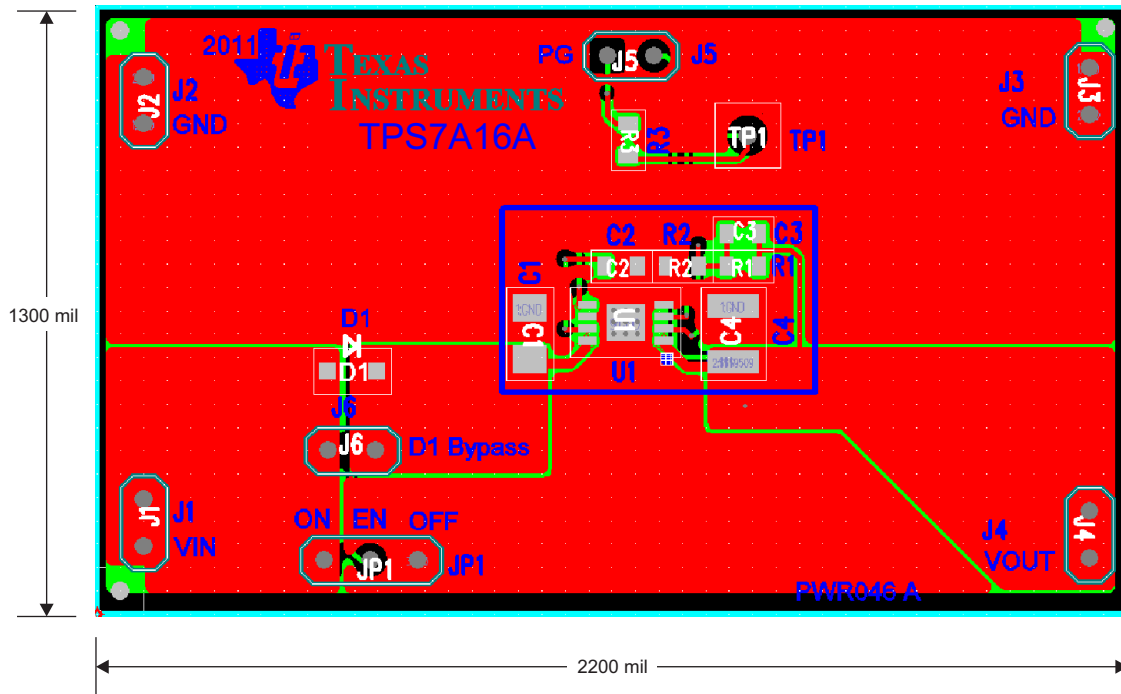


图 20. Suggested Layout: Top Layer

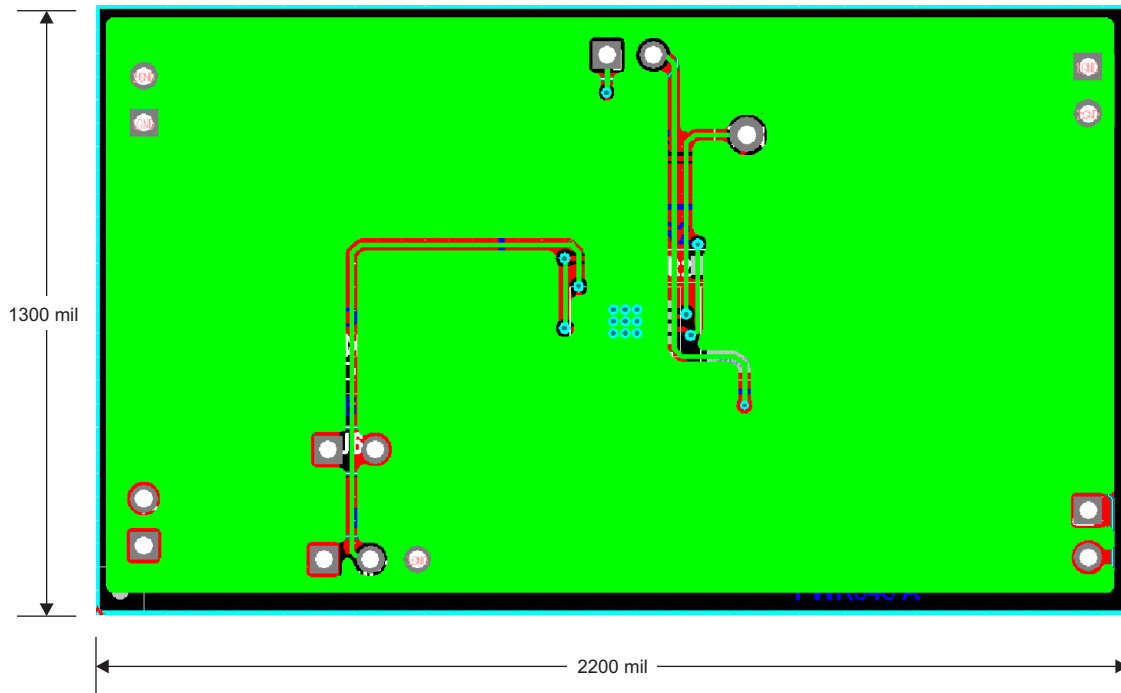


图 21. Suggested Layout: Bottom Layer

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A1601AQDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NT1	<a href="#">Samples</a>
TPS7A1633AQDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NU1	<a href="#">Samples</a>
TPS7A1650AQDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NV1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

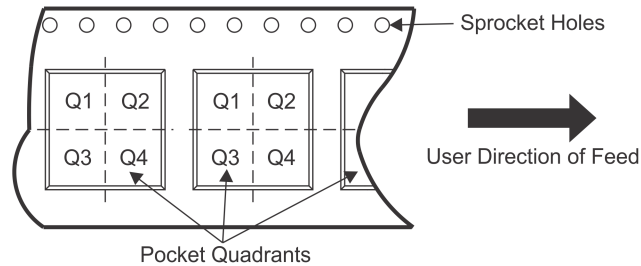
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1633AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1650AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0

## GENERIC PACKAGE VIEW

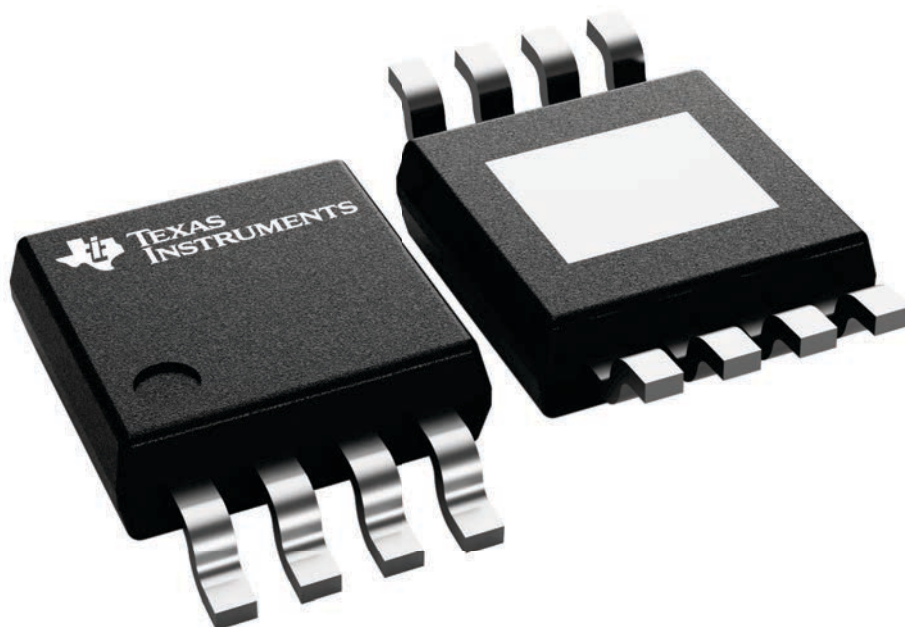
**DGN 8**

**PowerPAD™ HVSSOP - 1.1 mm max height**

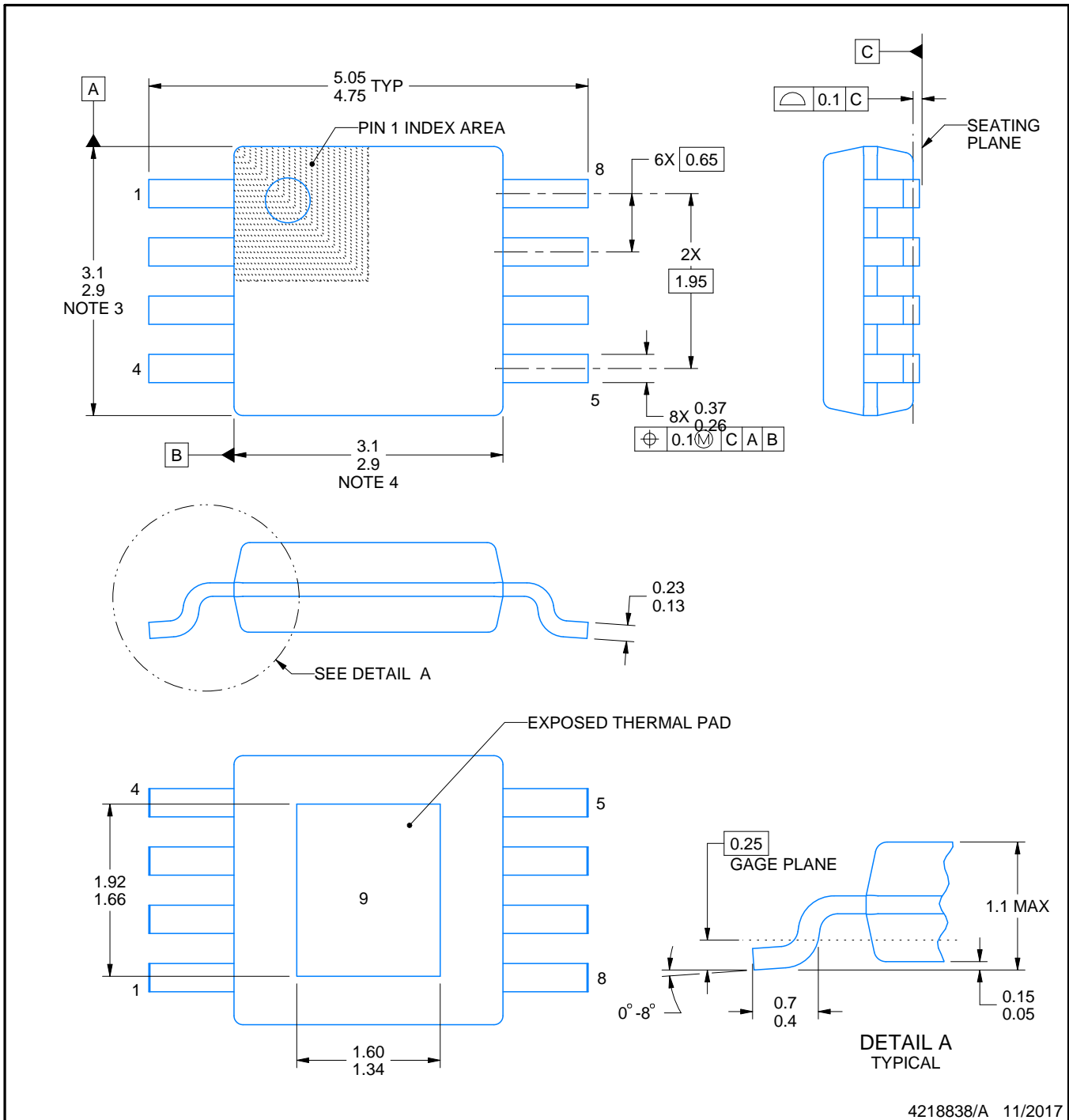
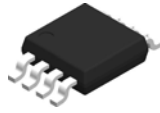
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/B



4218838/A 11/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



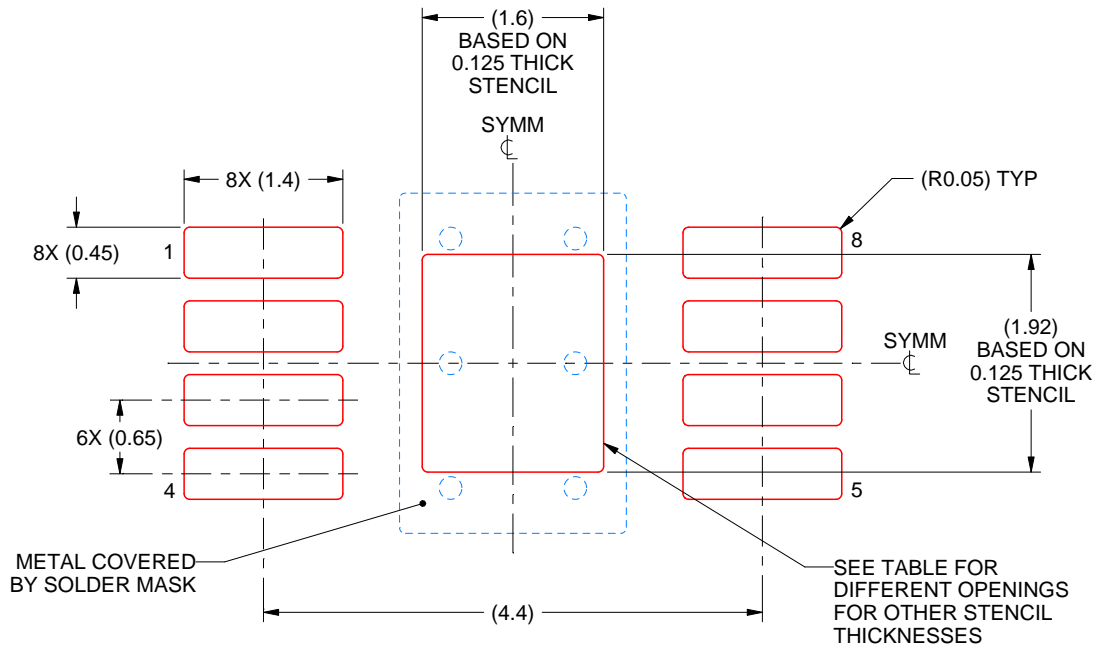


# EXAMPLE STENCIL DESIGN

DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 EXPOSED PAD 9:  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024，德州仪器 (TI) 公司