TPS63901 采用 WCSP 封装、具有输入电流限制和 DVS 的 1.8V 至 5.5V、75nA I_Q 降压/升压转换器

1 特性

- 输入电压范围为 1.8V 至 5.5V
- 1.8V 至 5V 输出电压范围（100mV 阶跃）
  - 可使用外部电阻器进行编程
  - SEL 引脚用于在两个输出电压预设之间切换
- $V_I \geq 2.0V$、$V_O = 3.3V$ 时，输出电流大于 400mA
  - 可堆叠：并联多个器件以获得更高的输出电流
- 负载电流为 10µA 时，效率 > 90%
  - 静态电流为 75nA
  - 60nA 关断电流
- 单模式运行
  - 无需在降压、降压/升压和升压模式之间转换
  - 低输出波纹
  - 出色的瞬态性能
- 可靠运行的特性
  - 集成软启动
  - 可编程输入电流限制，具有八个设置（1mA 至 100mA 和无限制）
  - 输出短路和过热保护
- 微型解决方案尺寸
  - 小型 2.2µH 电感器，单个 22µF 输出电容器
  - 12 焊球、1.5mm × 1.15mm、0.35mm 间距 WCSP 封装

2 应用

- 智能手表
- 智能追踪器
- 可穿戴电子产品
- 医疗传感器贴片和患者监护仪
- 智能仪表和传感器节点
- 电子智能锁
- 工业物联网（智能传感器）和窄带物联网

3 说明

TPS63901 器件是一款具有超低静态电流（典型值为 75nA）的高效同步降压/升压转换器。该器件具有 32 个用户可编程的输出电压设置，范围为 1.8V 至 5V。

动态电压调节特性使各项应用可于运行期间在两个输出电压之间进行切换；例如，在待机运行期间，可通过降低系统电源电压来降低功耗。

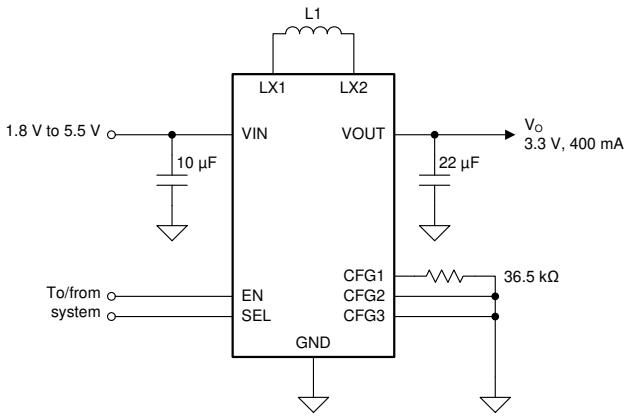
凭借其宽电源电压范围和可编程的输入电流限制（1mA 至 100mA 和无限制），该器件非常适合与 3 芯串联碱性电池、1 芯锂二氧化锰 (Li-MnO_2) 或 1 芯锂亚硫酰氯 (Li-$SOCl_2$) 等各种一次电池以及二次电池搭配使用。

高输出电流功能支持 sub-1GHz、BLE、LoRa、wM-Bus 和 NB-IoT 等常用射频标准。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TPS63901	WCSP (12)	1.50 mm × 1.15 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2021) to Revision A (June 2022)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

5 Pin Configuration and Functions

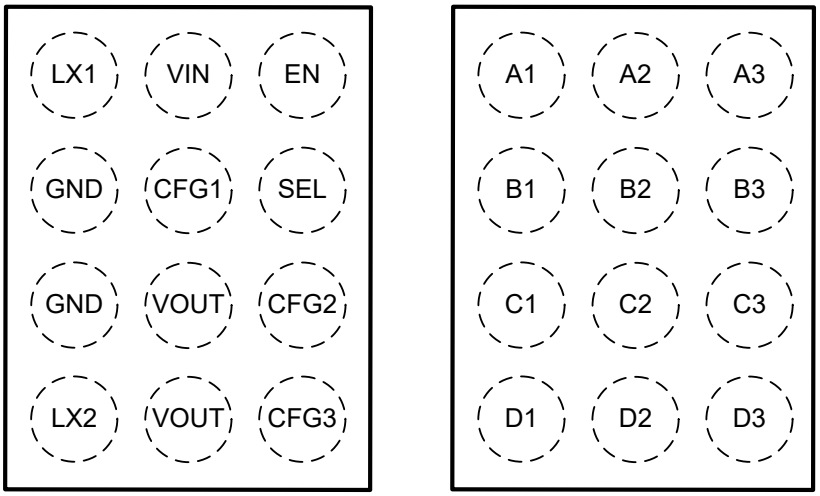


图 5-1. 12-Ball WCSP Package (Top View)

表 5-1. Pin Functions

Pin		Type	Description
Name	No.		
LX1	A1	—	Switching node of the buck stage
VIN	A2	—	Supply voltage
EN	A3	I	Device enable. A high level applied to this pin enables the device and a low level disables it. It must not be left open.
GND	B1,C1	—	Ground
CFG1	B2	I	Configuration pin 1. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit. Must not be left open.
SEL	B3	I	Output voltage select. Selects $V_{O(2)}$ when a high level is applied to this pin. Selects $V_{O(1)}$ when a low level is applied to this pin. It must not be left open.
VOUT	C2,D2	—	Output voltage. The C2 and D2 pins must be connected together.
CFG2	C3	I	Configuration pin 2. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit. Must not be left open.
LX2	D1	—	Switching node of the boost stage
CFG3	D3	I	Configuration pin 3. Connect a resistor between this pin and ground to set $V_{O(1)}$. Must not be left open.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, EN, CFG1, CFG2, CFG3, SEL)[2]	–0.3	5.9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.8		5.5	V
V_O	Output voltage		1.8		5.0	V
C_I	Input capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)[1]		5			µF
C_O	Output capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)[1]		10			µF
$C_{(CFG)}$	Capacitance (CFG1, CFG2, CFG3)				10	pF
L	Inductance			2.2		µH
I_{SAT}	Inductor saturation current rating	Unlimited current setting	2			A
		≤ 100-mA current settings	1			
T_A	Operating ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

(1) Effective capacitance after DC bias effects have been considered.

6.4 Thermal Information

THERMAL METRIC[1]		YCJ (WCSP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_I = 3.0 V, V_O = 2.5 V . Typical values are at T_J = 25°C (unless otherwise noted).

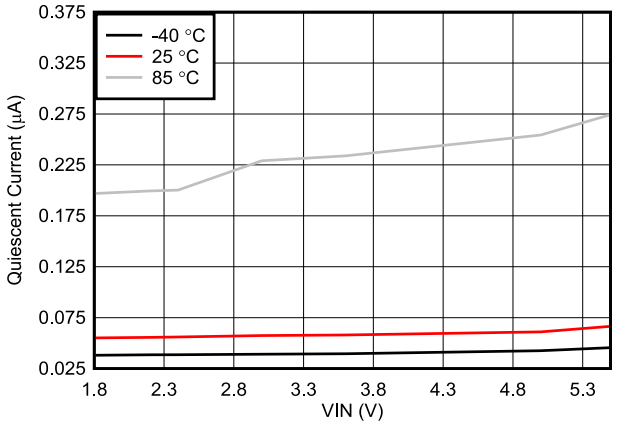
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
I_Q	Quiescent current into VIN		V(EN) = 3 V, no load, not switching, "unlimited" current setting; T_J = –40°C to 85°C			0.075	1	µA
I_{SD}	Shutdown current into VIN		V(EN) = 0 V ; T_J = –40°C to 85°C			60		nA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage				1.73	1.75	1.77	V
$V_{hys(UVLO)}$	UVLO threshold voltage hysteresis				90	100	110	mV
$V_{IT+(POR)}$	Positive-going POR threshold voltage				1.37		1.74	V
I/O SIGNALS								
V_{IH}	High-level input voltage (EN, SEL)						1.2	V
V_{IL}	Low-level input voltage (EN, SEL)				0.4			V
	Input current (EN, SEL)		$V_{(EN)}$, $V_{(SEL)}$ = 1.8 V or 0 V			±1	±10	nA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3 V, V_O = 5 V, test current = 1 A			140		mΩ
		Q2	V_I = 3 V, V_O = 3 V, test current = 1 A			95		
		Q3	V_I = 3 V, V_O = 3 V, test current = 1 A			95		
		Q4	V_I = 5 V, V_O = 3 V, test current = 1 A			140		
CURRENT LIMIT								
	Peak current limit during start-up (Q1)		V_I = 3.6 V, unlimited current limit setting		0.35		0.83	A
	Peak current limit (Q1)		V_I = 1.8 V, V_O = 3.6 V, unlimited current limit setting		1.33	1.45	1.6	A
			V_I = 3.6 V, V_O = 3.3 V, 100-mA current limit setting		0.15	0.29	0.51	
	Average input current limit		T_J = –40°C to 85°C	1-mA setting		1		mA
				2.5-mA setting		2.5		
				5-mA setting		5		
				10-mA settting		10		
				25-mA setting		25		
				50-mA setting		50		
				100-mA setting		100		
OUTPUT								
	Output voltage DC accuracy		I_O = 1 mA, $C_{O(eff)}$ = 10 µF, $L_{(eff)}$ = 2.2 µH				±1.5%	
CONTROL								
	Internal reference resistor					33		kΩ

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_I = 3.0 V, V_O = 2.5 V . Typical values are at T_J = 25°C (unless otherwise noted).

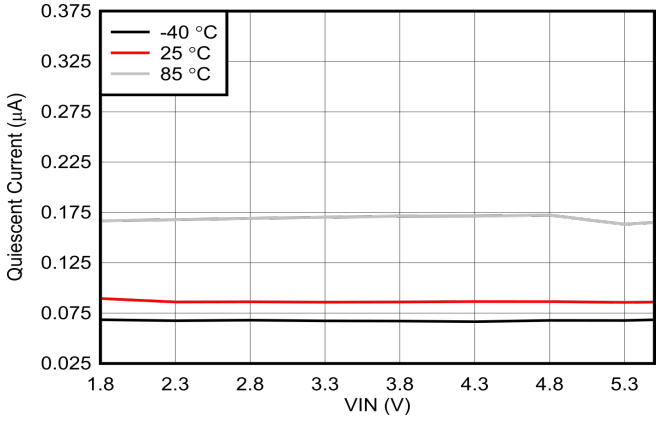
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CFG}	R2D setting #0			0	0.1	kΩ
	R2D setting #1		–3%	0.511	+3%	
	R2D setting #2		–3%	1.15	+3%	
	R2D setting #3		–3%	1.87	+3%	
	R2D setting #4		–3%	2.74	+3%	
	R2D setting #5		–3%	3.83	+3%	
	R2D setting #6		–3%	5.11	+3%	
	R2D setting #7		–3%	6.49	+3%	
	R2D setting #8		–3%	8.25	+3%	
	R2D setting #9		–3%	10.5	+3%	
	R2D setting #10		–3%	13.3	+3%	
	R2D setting #11		–3%	16.2	+3%	
	R2D setting #12		–3%	20.5	+3%	
	R2D setting #13		–3%	24.9	+3%	
	R2D setting #14		–3%	30.1	+3%	
	R2D setting #15		–3%	36.5	+3%	
PROTECTION FEATURES						
	Thermal shutdown threshold temperature		140	150	160	°C
	Thermal shutdown hysteresis		15	20	25	°C
TIMING PARAMETERS						
$t_{d(POR)}$	POR signal delay after reaching POR threshold			3.8		ms
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	Supply voltage stable before EN pin goes high			1.5	ms
$t_{w(SS)}$	Soft-start step duration	V_O > 1.8 V	100	125	150	µs
$t_{d(SEL)}$	Delay between a change in the state of the SEL pin and the first step change in the output voltage			30	40	µs
$t_{w(DVS)}$	Dynamic voltage scaling step duration		100	125	150	µs
$t_{d(RESTART)}$	Restart delay after protection			10	11	ms

6.6 Typical Characteristics



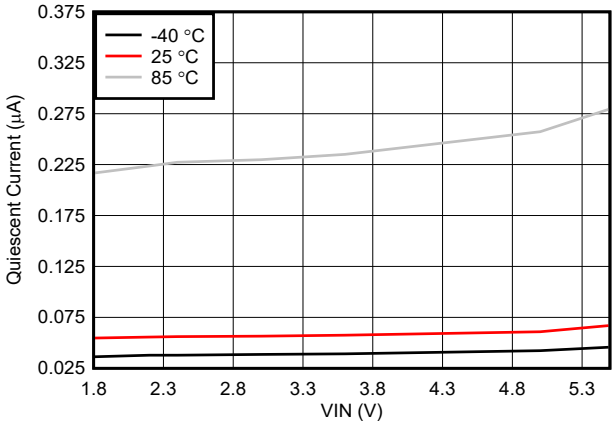
V_O = 5.1 V EN = HIGH I_O = 0 mA, device not switching

图 6-1. Quiescent Current into VIN vs Input Voltage



V_O = 5.1 V EN = HIGH I_O = 0 mA, device not switching

图 6-2. Quiescent Current into VOUT vs Input Voltage



V_O = 5.1 V EN = LOW

图 6-3. Shutdown Current vs Input Voltage

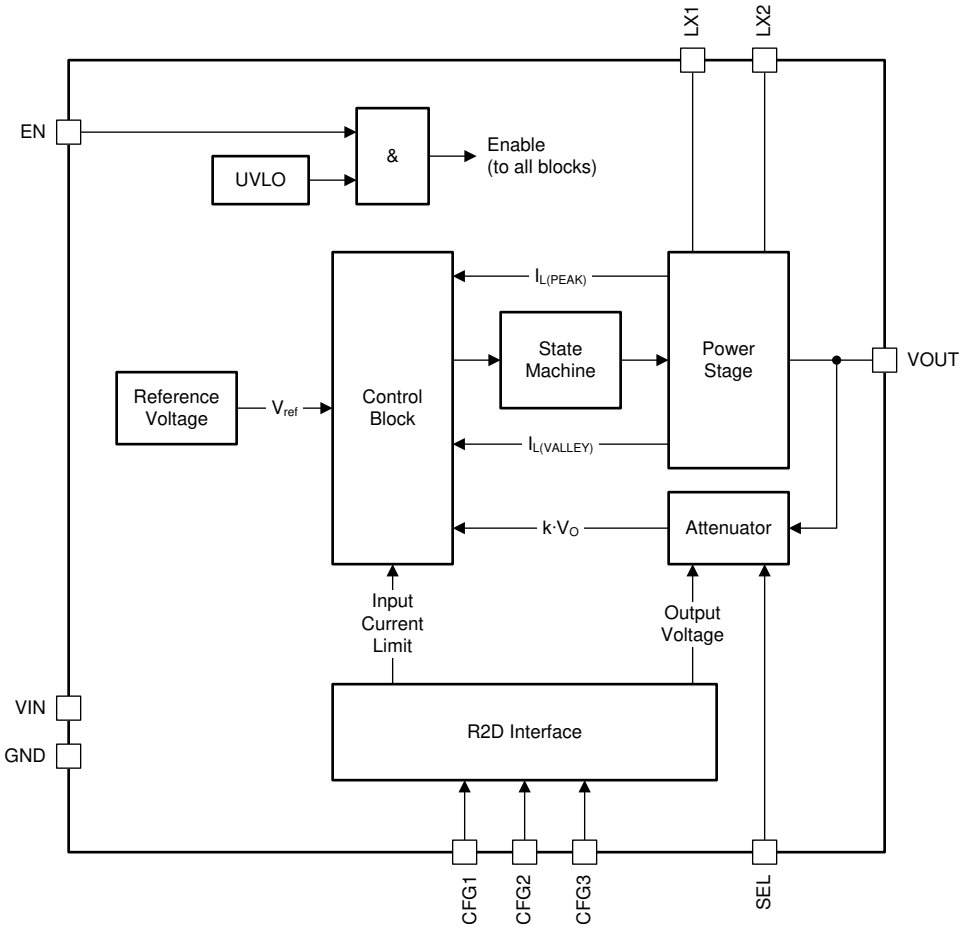
7 Detailed Description

7.1 Overview

The TPS63901 device is a four-switch synchronous buck-boost converter with a maximum output current of 400 mA. The device has a single-mode operation that allows the device to regulate the output voltage to a level above, below, or equal to the input voltage without displaying the mode-switching transients and unpredictable inductor current ripple from which many other buck-boost devices suffer.

The switching frequency of the TPS63901 device varies with the operating conditions: it is lowest when I_O is low and increases smoothly as I_O increases.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Trapezoidal Current Control

图 7-1 shows a simplified block diagram of the power stage of the device. Inductor current is sensed in series with Q1 (the peak current) and Q4 (the valley current).

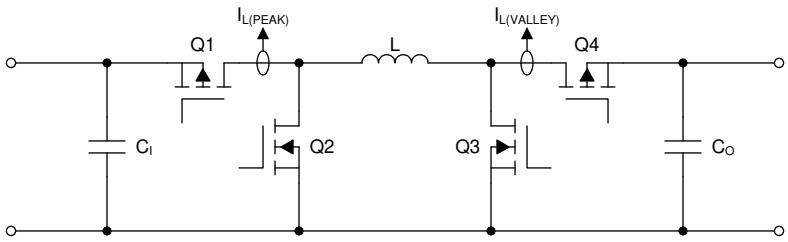


图 7-1. Power Stage Simplified Block Diagram

The device uses a trapezoidal inductor current to regulate its output under all operating conditions. Thus, the device only has one operating mode and does not display any of the mode-change transients or unpredictable switching displayed by many other buck-boost devices.

There are four phases of operation:

- Phase A – Q1 and Q3 are on and Q2 and Q4 are off.
- Phase B – Q1 and Q4 are on and Q2 and Q3 are off.
- Phase C – Q2 and Q4 are on and Q1 and Q3 are off.
- Phase D – Q2 and Q3 are on and Q1 and Q4 are off.

图 7-2 shows the inductor current waveform when $V_I > V_O$, 图 7-3 shows the current waveform when $V_I = V_O$, and 图 7-4 shows the current waveform when $V_I < V_O$.

图 7-2 through 图 7-4 show the typical waveforms during continuous conduction mode (CCM) switching for three operating conditions. During discontinuous conduction mode (DCM), the typical inductor current waveforms look similar to CCM with Phase D at 0-A inductor current. In deep boost mode, where $V_I << V_O$, Phase C length gradually decreases to zero until the switching waveform becomes triangular.

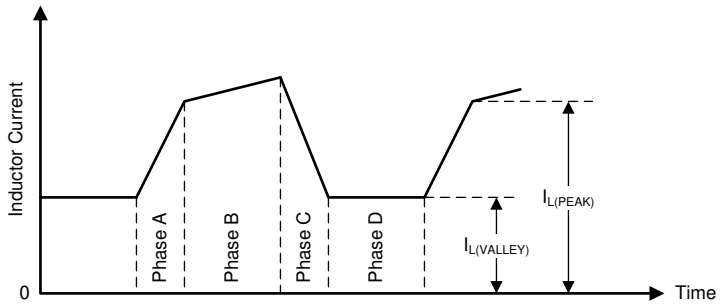


图 7-2. Inductor Current Waveform when $V_I > V_O$ (CCM)

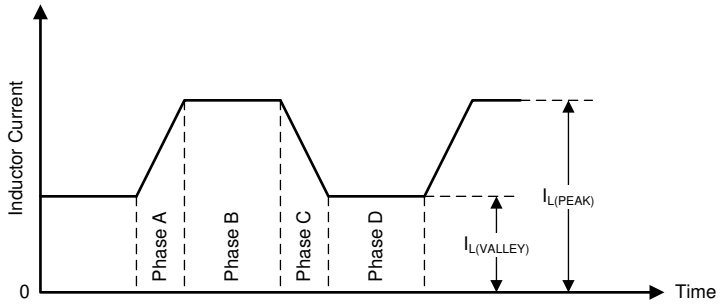


图 7-3. Inductor Current Waveform when $V_I = V_O$ (CCM)

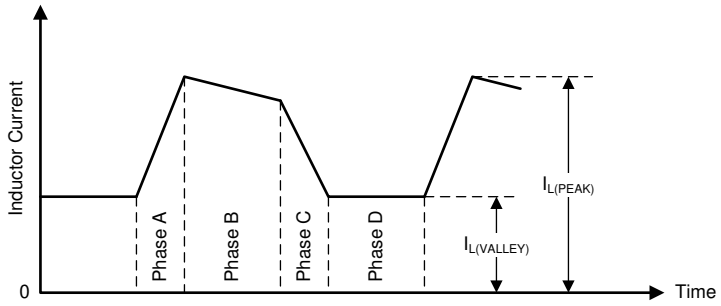


图 7-4. Inductor Current Waveform when $V_I < V_O$ (CCM)

The ideal relationship between V_I and V_O (that is, assuming no losses) is:

$$V_O = V_I \left(\frac{t_{w(A)} + t_{w(B)}}{t_{w(B)} + t_{w(C)}} \right) \quad (1)$$

where

- V_I is the input voltage.
- V_O is the output voltage.
- $t_{w(A)}$ is the duration of phase A.
- $t_{w(B)}$ is the duration of phase B.
- $t_{w(C)}$ is the duration of phase C.

By varying relative duration of each phase, the device can regulate V_O to be less than, equal to, or greater than V_I.

7.3.2 Device Enable and Disable

The device turns on when *all* of the following conditions are true:

- The supply voltage is greater than the positive-going undervoltage lockout (UVLO) threshold.
- The EN pin is high.

The device turns off when *at least one* of the following conditions is true:

- The supply voltage is less than the negative-going UVLO threshold.
- The EN pin is low.

图 7-13 shows a complete state diagram.

After the device turns on, the internal reference system starts, then the trimming information and the CFG pins are read out. The device ignores any further changes to the CFG pins during device operation.

图 7-5 shows the internal start-up sequence.

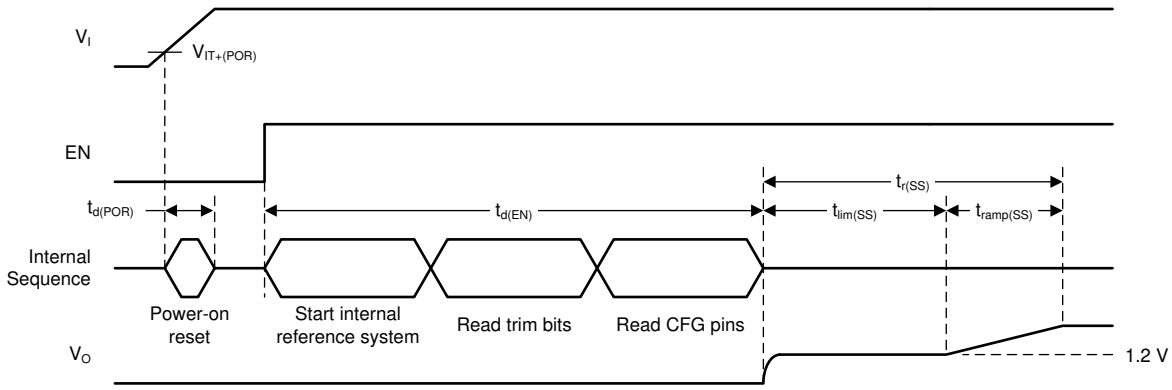


图 7-5. Internal Start-Up Sequence

7.3.3 Soft Start

The device has a soft-start feature that starts the device typically with 500-mA peak current limit until V_O = 1.8 V and 500 µs elapsed when the input current limit is set to unlimited (see 节 7.3.4). Afterward, the output voltage ramps in a series of discrete steps (see 图 7-6).

- When $V_O \leqslant$ 1.8 V, peak current is limited to 500 mA typical for 500 µs.
- When V_O > 1.8 V, each step is 100 mV high and has a duration of 125 µs.

The total soft-start ramp-up time can be calculated with Equation 2.

$$t_{r(SS)} = V_O \times 1.25 \left[ms/V\right] - 1.75[ms] \quad (2)$$

where

- $t_{r(SS)}$ is the rise time of the output voltage in milliseconds.
- V_O is the output voltage in volts.

图 7-6 shows a typical start-up case.

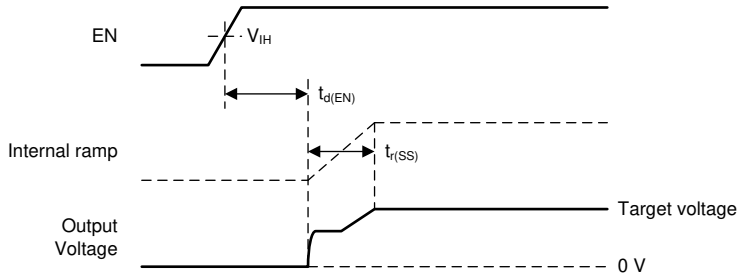


图 7-6. Start-Up Behavior

图 7-7 illustrates the start-up step size behavior.

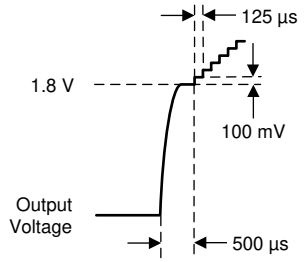


图 7-7. Typical Soft-Start Ramp Step Size

表 7-1 shows the typical start-up time for a number of standard output voltages.

表 7-1. Typical Start-Up Times

Output Voltage	Soft-Start Ramp-Up Time ($t_{r(SS)}$)	Start-Up Time ($t_{d(EN)}$ + $t_{r(SS)}$)
1.8 V	0.5 ms	2 ms
2.5 V	1.375 ms	2.875 ms
3.3 V	2.375 ms	3.875 ms
5 V	4.5 ms	6 ms

If the output is prebiased – that is, the initial output voltage is not zero – the start-up behavior is as follows:

- If the prebias voltage is *lower* than the target voltage, the device does not start switching until the ramping output voltage is greater than the prebias voltage (see 图 7-8).
- If the prebias voltage is *higher* than the target voltage, the device does not start to switch until the output voltage has decreased to the target voltage (see 图 7-9). The device cannot actively discharge the output to the target voltage and relies on the load current to discharge the output capacitor and decrease the output voltage to the target value.

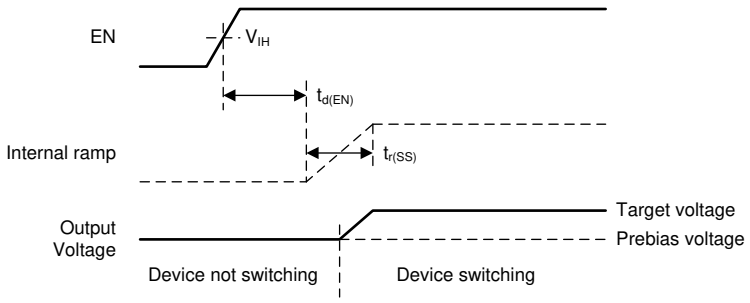


图 7-8. Start-Up Behavior into Prebiased (Low) Output

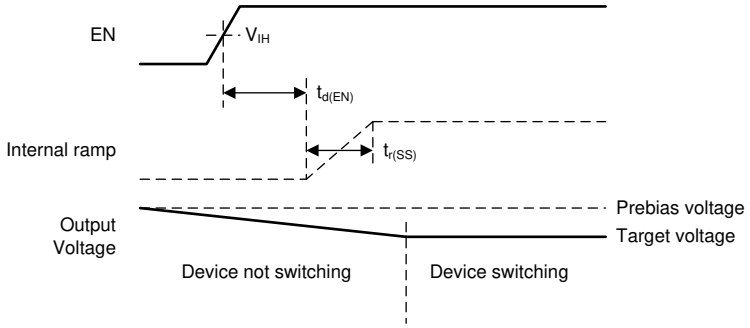


图 7-9. Start-Up Behavior into Prebiased (High) Output

7.3.4 Input Current Limit

The device can limit the current drawn from its supply, so that it can be used with batteries that do not support high peak currents. The input current limit is active during normal operation and at start-up to avoid high inrush current. The device has eight current limit settings:

- 1 mA
- 2.5 mA
- 5 mA
- 10 mA
- 25 mA
- 50 mA
- 100 mA
- Unlimited

CFG1 and CFG2 pins select which setting is active (see 节 7.3.6).

7.3.5 Dynamic Voltage Scaling

The device has a dynamic voltage scaling function to switch between the two output voltage settings. When the SEL pin changes state, the output voltage ramps to the new value in 100-mV steps. The duration of each step is 125 µs (see 图 7-10).

The device does not actively discharge the output capacitor when the output voltage ramps to a lower level. This leads to a longer output voltage settling time when light load is applied (see 图 7-11). The settling time can be calculated with Equation 3.

$$t_{settle} = C_O \times \frac{V_{O(HIGH)} - V_{O(LOW)}}{I_O} \quad (3)$$

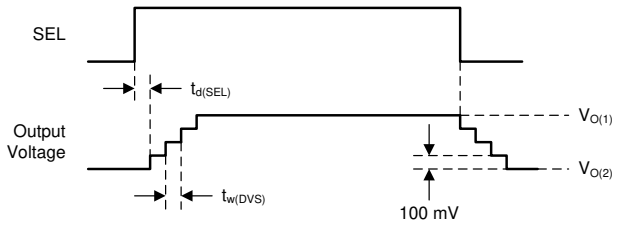


图 7-10. Dynamic Voltage Scaling with High Load

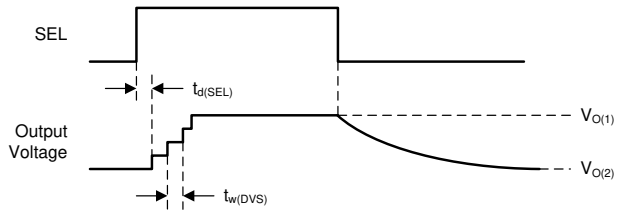


图 7-11. Dynamic Voltage Scaling with Light Load

7.3.6 Device Configuration (Resistor-to-Digital Interface)

The device has three configuration pins (CFG1, CFG2, and CFG3) that control its operation. When the device starts up, a resistor-to-digital (R2D) interface reads the values of the configuration resistors on the CFG pins and transfers the setting to an internal configuration register (see 图 7-12).

- CFG1 and CFG2 set $V_{O(2)}$ level and the input current limit.
- CFG3 sets $V_{O(1)}$ level.

To reduce power consumption, the device reads the value of the resistors connected to the configuration pins during start-up and then disables these pins. Once the device has started to operate, changes to the configuration pins have no effect.

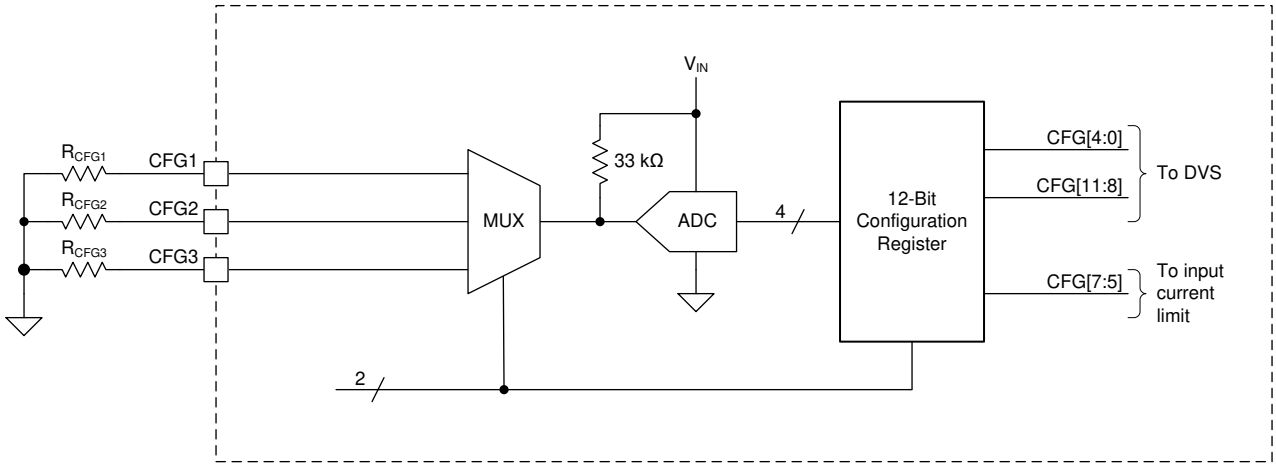


图 7-12. Resistor-to-Digital Interface Block Diagram

表 7-2 summarizes the resistor values needed to configure the device for different input current limit and output voltage (SEL = high) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of ±200 ppm or better.

备注

For correct operation, TI recommends that the total RMS error of the configuration resistors – including initial tolerance, temperature drift, and aging – is less than ±3%.

表 7-2. Input Current Limit and Output Voltage (SEL = High) Settings

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
1.8 V	R_{CFG1}	0 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
1.9 V	R_{CFG1}	511 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ

表 7-2. Input Current Limit and Output Voltage (SEL = High) Settings (continued)

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
2.0 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.1 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.2 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.3 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.4 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.5 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.6 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.7 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.8 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.9 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.0 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.1 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.2 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.3 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.4 V	R_{CFG1}	0 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.5 V	R_{CFG1}	511 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.6 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.7 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.8 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.9 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.0 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

表 7-2. Input Current Limit and Output Voltage (SEL = High) Settings (continued)

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
4.1 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.2 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.3 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.4 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.5 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.6 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.7 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.8 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
5.0 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

表 7-3 summarizes the resistor values needed to configure the device for different output voltage (SEL = low) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of better than ±200 ppm.

表 7-3. Output Voltage (SEL Pin = Low) Settings

Output Voltage – $V_{O(1)}$ (SEL = LOW)	R_{CFG3}
1.8 V	0 Ω
2.0 V	511 Ω
2.1 V	1.15 kΩ
2.2 V	1.87 kΩ
2.3 V	2.74 kΩ
2.4 V	3.83 kΩ
2.5 V	5.11 kΩ
2.6 V	6.49 kΩ
2.7 V	8.25 kΩ
2.8 V	10.5 kΩ
3.0 V	13.3 kΩ
3.3 V	16.2 kΩ
3.6 V	20.5 kΩ
4.0 V	24.9 kΩ
4.5 V	30.1 kΩ
5.0 V	36.5 kΩ

7.3.7 SEL Pin

The SEL pin selects which configuration bits control the output voltage.

- When SEL = high, the output voltage $V_{O(2)}$ is set.
- When SEL = low, the output voltage $V_{O(1)}$ is set.

7.3.8 Short-Circuit Protection

7.3.8.1 Current Limit Setting = 'Unlimited'

The device has a built-in short circuit protection function to limit the current through Q1. The maximum current that flows is limited by the peak current limit. The output voltage decreases if the load is higher than the peak current limit. If the output voltage falls below 1.25 typically, the short circuit protection is activated. With short circuit protection activated, the input current is limited to 26 mA on average.

The device automatically restarts to normal operation after the short condition is removed.

7.3.8.2 Current Limit Setting = 1 mA to 100 mA

The input current limiting function automatically limits current during a short-circuit condition. The device regulates the average input current for as long as the short-circuit condition exists. If the output voltage falls below 1.25 V typically, the short circuit protection is activated. For input current limit settings of 100 mA, 50 mA, and 25 mA, the short circuit protection limits the input current to 26 mA on average. For input current limit setting of 10 mA, 5 mA, 2.5 mA, and 1 mA, the short circuit protection limits the input current to slightly above the typical values for each setting. 表 7-4 shows the typical short circuit currents for each input current limit setting.

The device automatically restarts to previous operation after the short condition is removed.

表 7-4. Typical Input Current During Short Circuit Condition (V_O < 1.25 V Typically) for All Input Current Limit Settings

Input Current Limit Setting	Typical Short Circuit Input Current
1 mA	1.2 mA
2.5 mA	2.8 mA
5 mA	5.2 mA
10 mA	12 mA
25 mA	26 mA
50 mA	26 mA
100 mA	26 mA
Unlimited	26 mA

7.3.9 Thermal Shutdown

The device has a thermal shutdown function that disables the device if it gets too hot for correct operation. When the device cools down, it automatically restarts operation after a typical delay of $t_{d(RESTART)}$ = 10 ms. The device starts with the soft-start feature (see 节 7.3.3) and keeps the previously read CFG pin setting.

7.4 Device Functional Modes

The device has two functional modes: on and off. The device enters on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

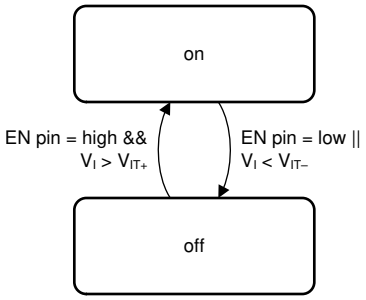


图 7-13. Device Functional Modes

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS63901 is a high-efficiency, non-inverting buck-boost converter with an extremely low quiescent current, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. The input current limit and output voltage are set through resistors connected to the three CFGx pins.

8.2 Typical Application

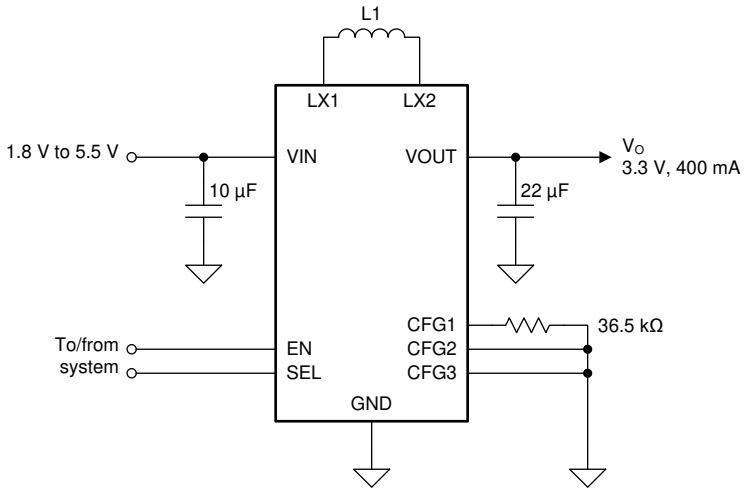


图 8-1. 3.3-V_{OUT} Typical Application

8.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions*.

表 8-1. Matrix of Output Capacitor and Inductor Combinations

Nominal Inductor Value [µH](1)	Nominal Output Capacitor Value [µF](2)				
	10	22	47	100	⩾ 300
2.2	+(3)	+ (4)	+	+	+(5)

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and – 30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and – 50%.
(3) Output voltage ripple increases versus typical application.
(4) Typical application. Other check marks indicate possible filter combinations.
(5) Start-up time increased

8.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, the *Recommended Operating Conditions* outlines minimum and maximum values for inductance and capacitance. Tolerance and derating must be taken into account when selecting nominal inductance and capacitance.

8.2.2.1 Inductor Selection

The inductor selection is affected by several parameters such as inductor ripple current, output voltage ripple, transition point into power save mode, and efficiency. See 表 8-2 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses, which needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the core and conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using 方程式 5. Only the equation that defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{4}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{5}$$

where

- D is duty cycle in boost mode.
- *f* is the converter switching frequency.
- L is the inductor value.
- η is the estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption).

备注

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends choosing an inductor with a saturation current 20% higher than the value calculated using 方程式 5. Possible inductors are listed in 表 8-2.

表 8-2. List of Recommended Inductors

Inductor Value [µH](1)	Saturation Current [A]	DCR [mΩ]	Part Number	Manufacturer	Size (L × W × H mm)
2.2	3.5	21	XFL4020-222ME	Coilcraft	4 × 4 × 2
2.2	1.7	72	SRN3015TA-2R2M	Bourns	3 × 3 × 1.5
2.2	3.3	82	DFE252012F-2R2M	Murata	2.5 × 2 × 1.2
2.2	2.4	116	DFE201612E-2R2M	Murata	2.0 × 1.6 × 1.2
2.2	2.0	190	DFE201210U-2R2M	Murata	2.0 × 1.2 × 1.0

(1) See the *Third-party Products Disclaimer*.

8.2.2.2 Output Capacitor Selection

For the output capacitor, use of small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. The recommended nominal output capacitor value is a single 22 µF. If, for any reason, the application requires the use of large capacitors, which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor must be placed as close as possible to the VOUT and GND pins of the IC.

It is important that the effective capacitance is given according to the recommended value in the *Recommended Operating Conditions*. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Possible output capacitors are listed in 表 8-3.

There is no upper limit for the output capacitance value.

At light load currents, the output voltage ripple is dependent on the output capacitor value. Larger output capacitors reduce the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

表 8-3. List of Recommended Capacitors

Capacitor Value [µF](1)	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)
22	6.3	GRM219R60J476ME44	Murata	0805 (3210)
47	6.3	GRM188R60J476ME15	Murata	0603 (1608)

(1) See the *Third-party Products Disclaimer*.

8.2.2.3 Input Capacitor Selection

A 10-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63901 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

When operating from a high impedance source, a larger input buffer capacitor is recommended to avoid voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current.

表 8-4. List of Recommended Capacitors

Capacitor Value [µF](1)	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
10	6.3	GRM188R60J106ME47	Murata	0603 (1608)
10	10	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)

(1) See the *Third-party Products Disclaimer*.

8.2.2.4 Setting The Output Voltage

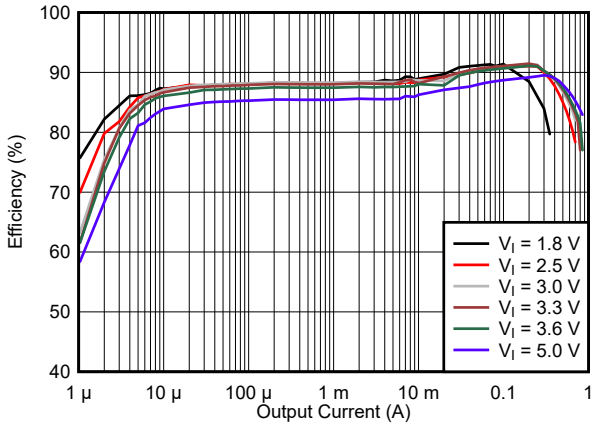
The output voltage is set with the CFGx pins (see 节 7.3.6).

8.2.3 Application Curves

表 8-5. Components for Application Characteristic Curves for V_{OUT} = 3.3 V

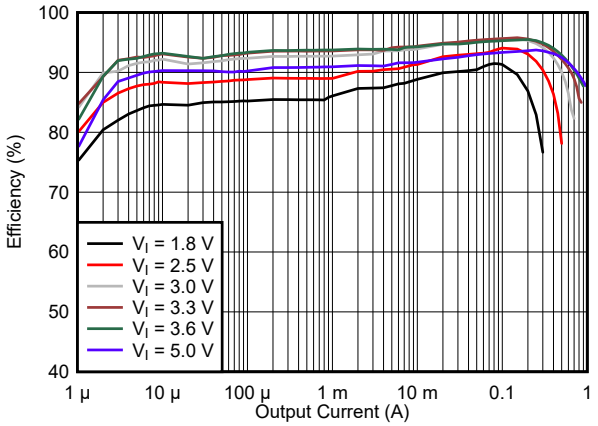
Reference(1)	Description(2)	Part Number	Manufacturer
U1	400-mA ultra low I_Q buck-boost converter (1.5 mm × 1.15 mm)	TPS63901YCJ	Texas Instruments
L1	2.2 µH, 2.5 mm × 2 mm 3.3 A, 82 mΩ	DFE252012F-2R2M	Murata
C1	10 µF, 0603, ceramic capacitor, ±20%, 6.3 V	GRM188R60J106ME47	Murata
C2	22 µF, 0603, ceramic capacitor, ±20%, 6.3 V	GRM187R60J226ME15	Murata
CFG1	36.5 kΩ, 0603 resistor, 1%, 100 mW	Standard	Standard
CFG2	0 Ω, 0603 resistor, 1%, 100 mW	Standard	Standard
CFG3	0 Ω, 0603 resistor, 1%, 100 mW	Standard	Standard

(1) See the *Third-Party Products Discalimer*
(2) For other output voltages, refer to 表 8-1 for resistor values.



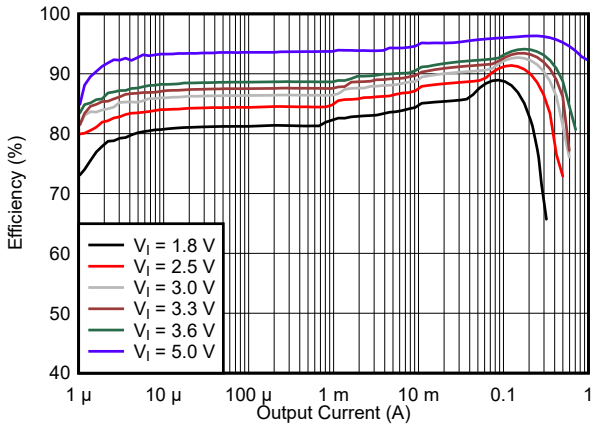
V_O = 1.8 V T_A = 25°C

图 8-2. Efficiency vs Output Current



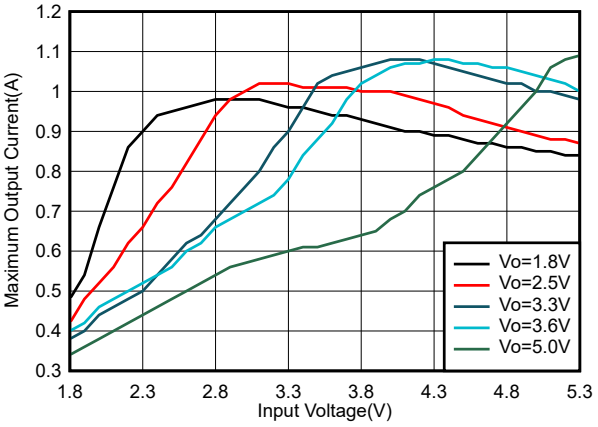
V_O = 3.3 V T_A = 25°C

图 8-3. Efficiency vs Output Current



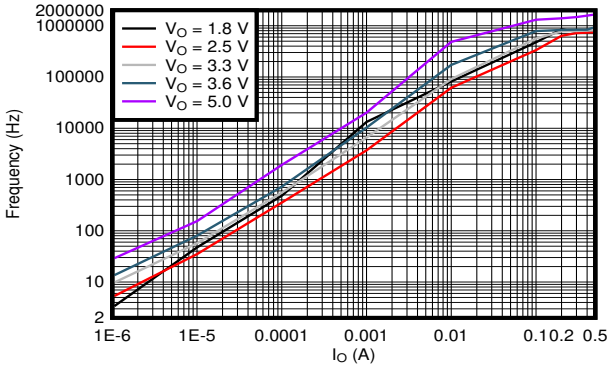
V_O = 5.0 V T_A = 25°C

图 8-4. Efficiency vs Output Current



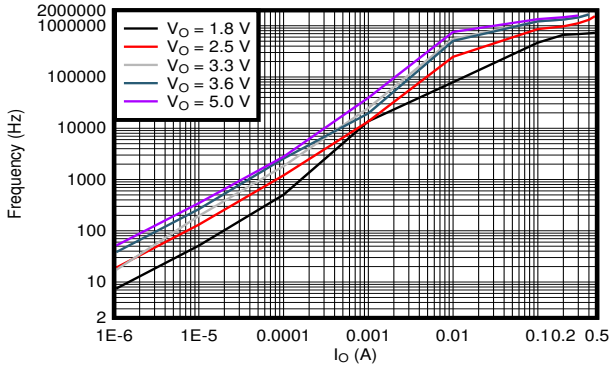
T_A = 25°C

图 8-5. Typical Output Current Capability vs Input Voltage



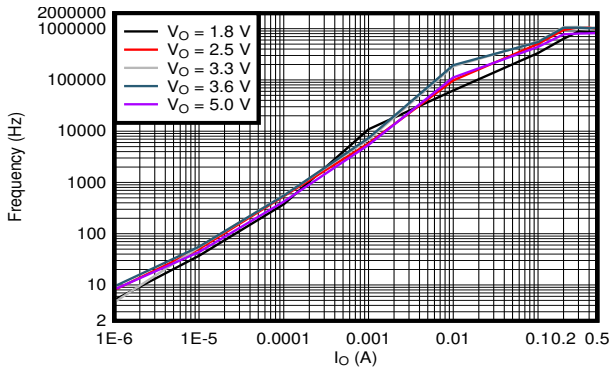
V_I = 3.3 V T_A = 25°C

图 8-6. Typical Burst Switching Frequency vs Output Current



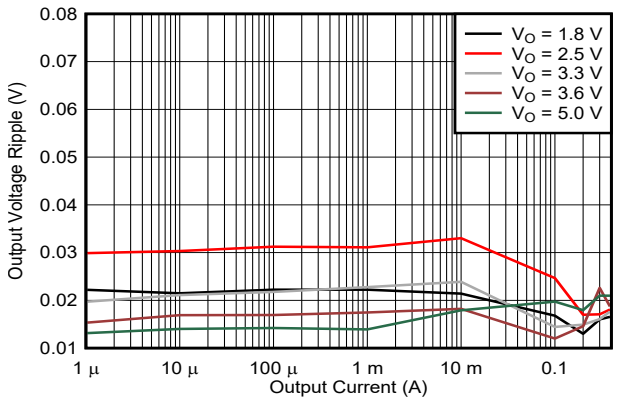
V_I = 2.0 V T_A = 25°C

图 8-7. Typical Burst Switching Frequency vs Output Current



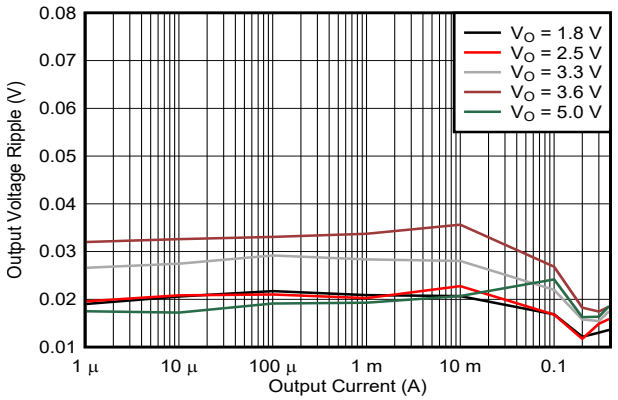
V_I = 5.2 V T_A = 25°C

图 8-8. Typical Burst Switching Frequency vs Output Current



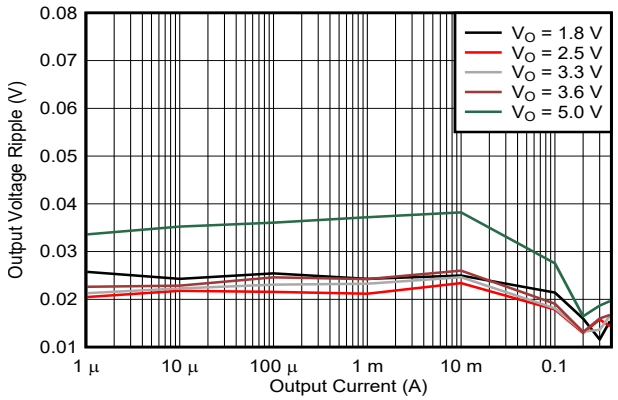
V_I = 3.3 V T_A = 25°C

图 8-9. Output Voltage Ripple



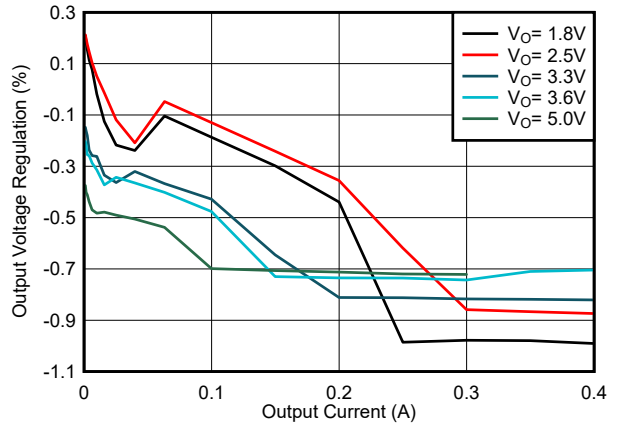
V_I = 4.4 V T_A = 25°C

图 8-10. Output Voltage Ripple



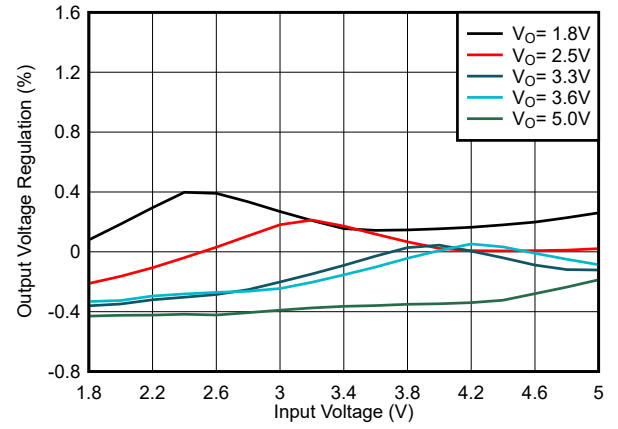
V_I = 5.2 V T_A = 25°C

图 8-11. Output Voltage Ripple



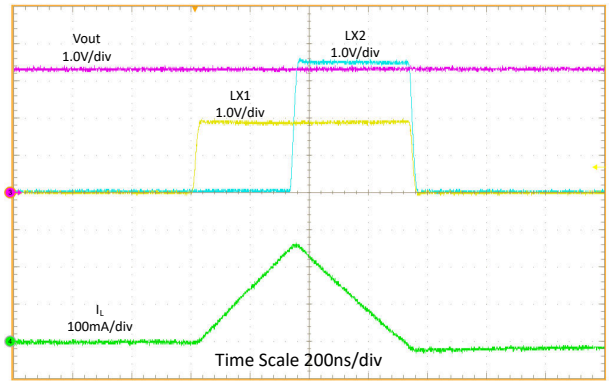
V_I = 3.3 V T_A = 25°C

图 8-12. Load Regulation



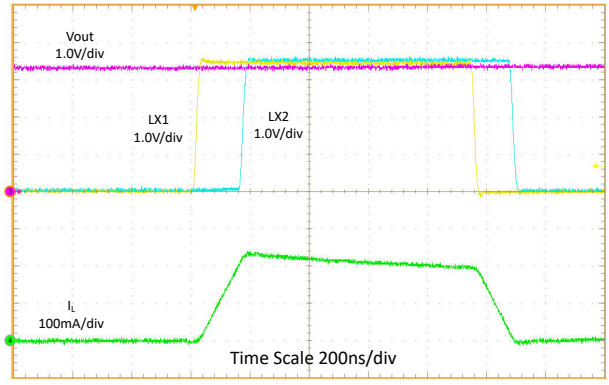
V_I = 1.8 V to 5.0 V Load = 1 mA, T_A = 25°C

图 8-13. Line Regulation



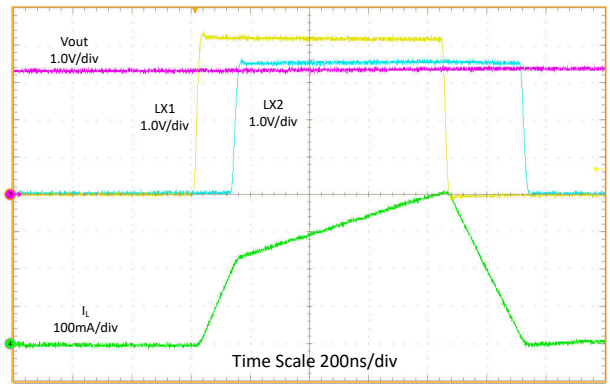
V_I = 1.8 V, V_O = 3.3 V No load

图 8-14. Switching Waveforms, Boost Operation



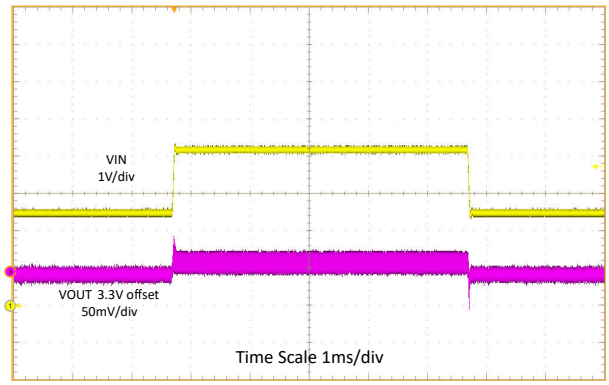
V_I = 3.3 V, V_O = 3.3 V No load

图 8-15. Switching Waveforms, Buck-Boost Operation



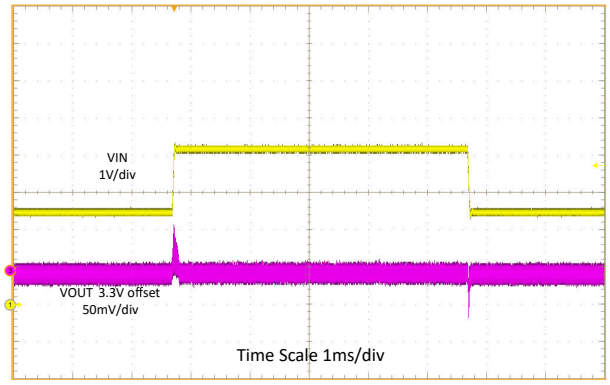
V_I = 4.0 V, V_O = 3.3 V No load

图 8-16. Switching Waveforms, Buck Operation



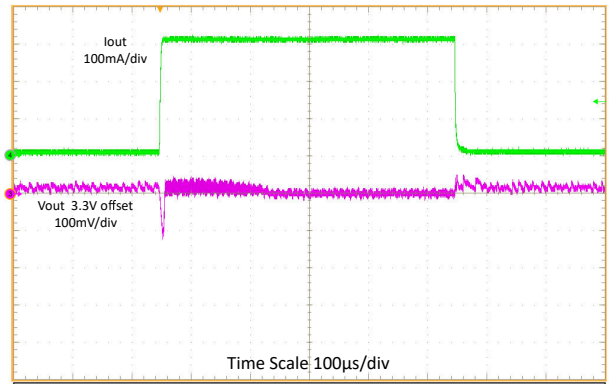
V_I = 2.5 V to 4.2 V, V_O = 3.3 V Load = 200-mA resistive load

图 8-17. Line Transient, 200-mA Load



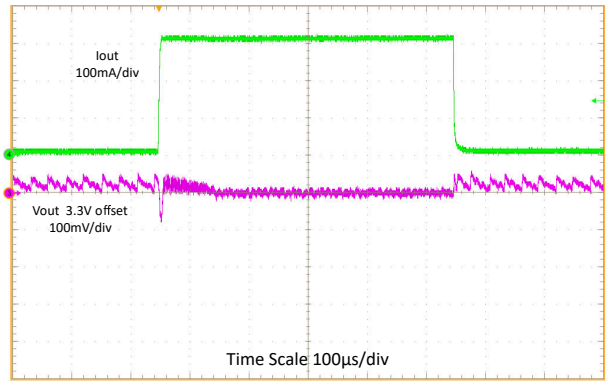
V_I = 2.5 V to 4.2 V, V_O = 3.3 V Load = 400-mA resistive load

图 8-18. Line Transient, 400-mA Load



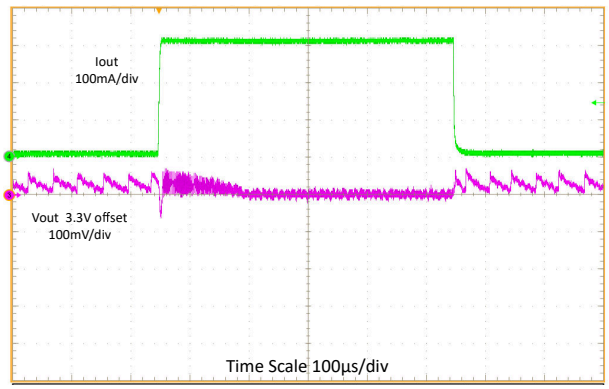
V_I = 2.7 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

图 8-19. Load Transient, 300-mA Step



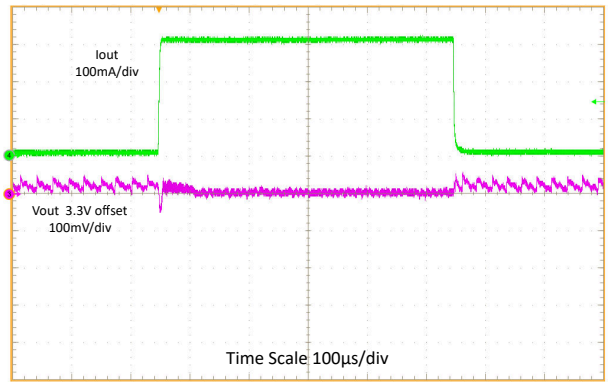
V_I = 3.3 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

图 8-20. Load Transient, 300-mA Step



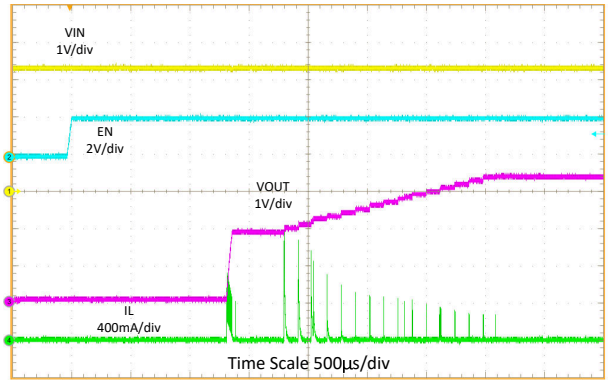
V_I = 4.2 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

图 8-21. Load Transient, 300-mA Step



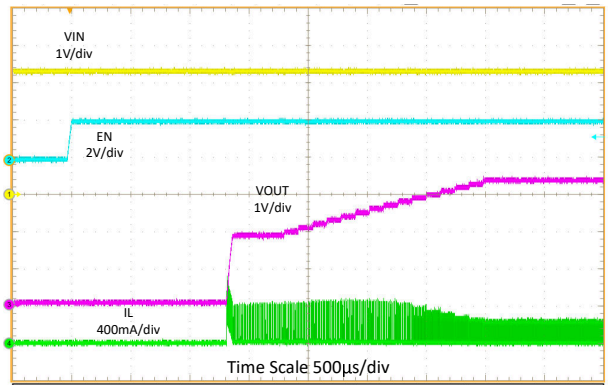
V_I = 5.5 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

图 8-22. Load Transient, 300-mA Step



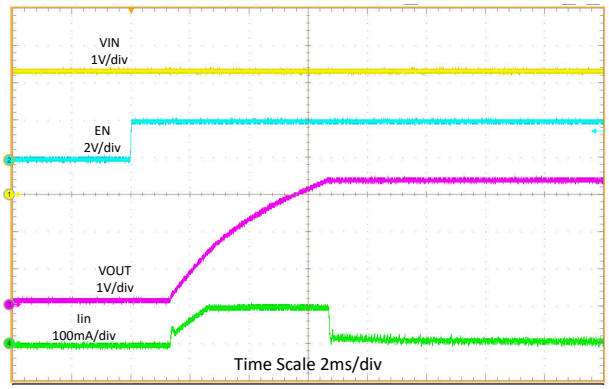
V_I = 3.3 V, V_O = 3.3 V 10- µA resistive load

图 8-23. Start-Up Behavior from Rising Enable



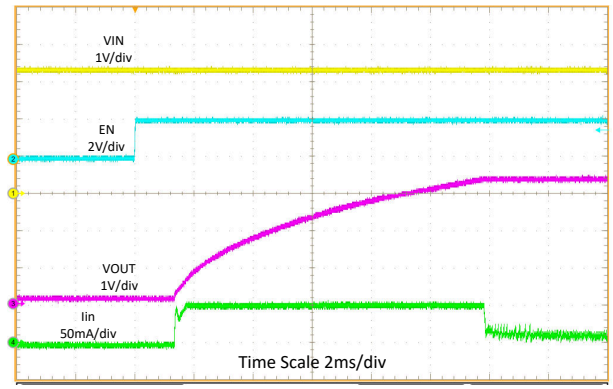
V_I = 3.3 V, V_O = 3.3 V 100-mA resistive load

图 8-24. Start-Up Behavior from Rising Enable



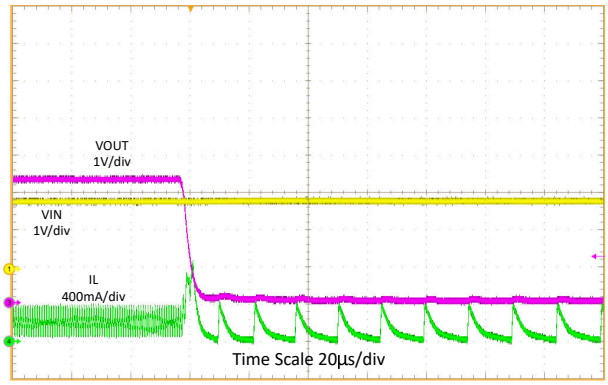
V_I = 3.3 V, V_O = 3.3 V C_I = 32 µF, C_O = 300 µF

图 8-25. Start-Up with 100-mA ICL



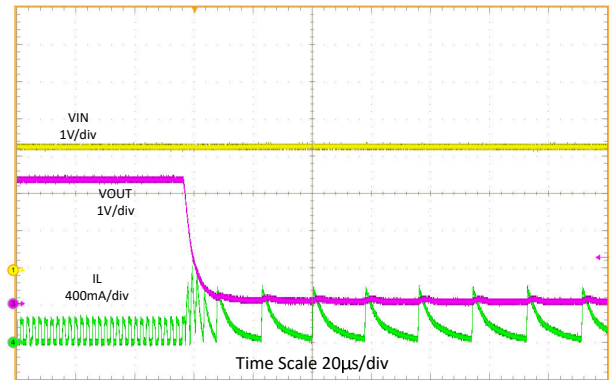
V_I = 3.3 V, V_O = 3.3 V C_I = 32 µF, C_O = 300 µF

图 8-26. Start-Up with 50-mA ICL



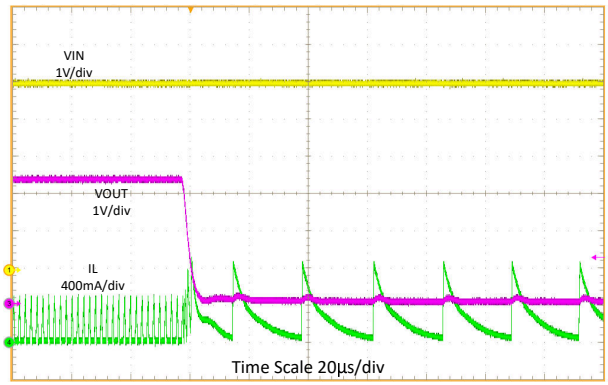
V_I = 1.8 V, V_O = 3.3 V T_A = 25°C

图 8-27. Short Circuit Behavior



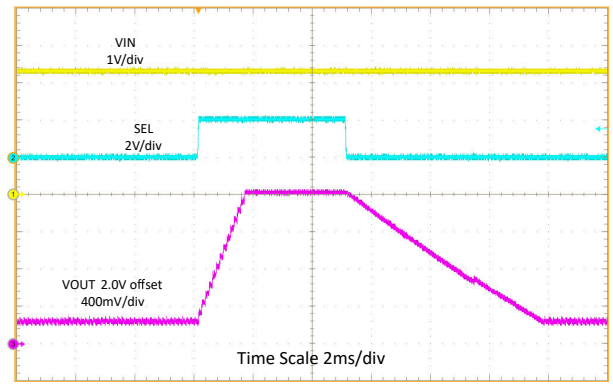
V_I = 3.3 V, V_O = 3.3 V T_A = 25°C

图 8-28. Short Circuit Behavior



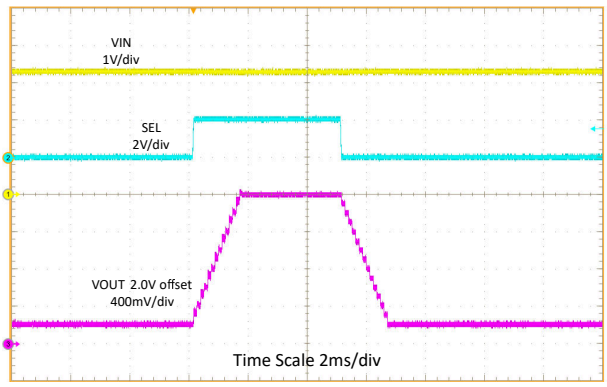
V_I = 5.0 V, V_O = 3.3 V T_A = 25°C

图 8-29. Short Circuit Behavior



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V 0.1-mA resistive load

图 8-30. DVS Behavior at Light Load



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V 400-mA resistive load

图 8-31. DVS Behavior at High Load

9 Power Supply Recommendations

The TPS63901 device is designed to operate with input supplies from 1.8 V to 5.5 V. The input supply must be stable and free of noise to achieve the full performance of the device. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance can be required. The input capacitance shown in the application schematics in this data sheet is sufficient for typical applications.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of any switching power supply design. A poor layout can cause unstable operation, load regulation problems, increased ripple and noise, and EMI issues.

The following PCB layout design guidelines are recommended:

- Place the input and output capacitors close to the device.
- Minimize the area of the input loop, and use short, wide traces on the top layer to connect the input capacitor to the VIN and GND pins.
- Minimize the area of the output loop, and use short, wide traces on the top layer to connect the output capacitor to the VOUT and GND pins.
- The location of the inductor on the PCB is less important than the location of the input and output capacitors. Place the inductor after the input and output capacitors have been placed close to the device. Route the traces to the inductor on an inner layer if necessary.

10.2 Layout Example

图 10-1 shows an example of a PCB layout that follows the recommendations of the previous section.

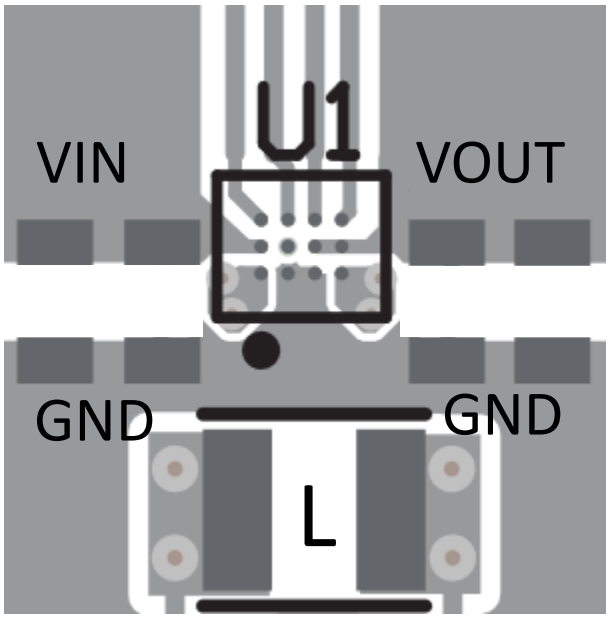


图 10-1. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS63901 EVM User Guide*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63901YCJR	ACTIVE	DSBGA	YCJ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3901	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

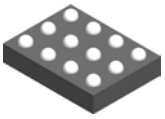
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

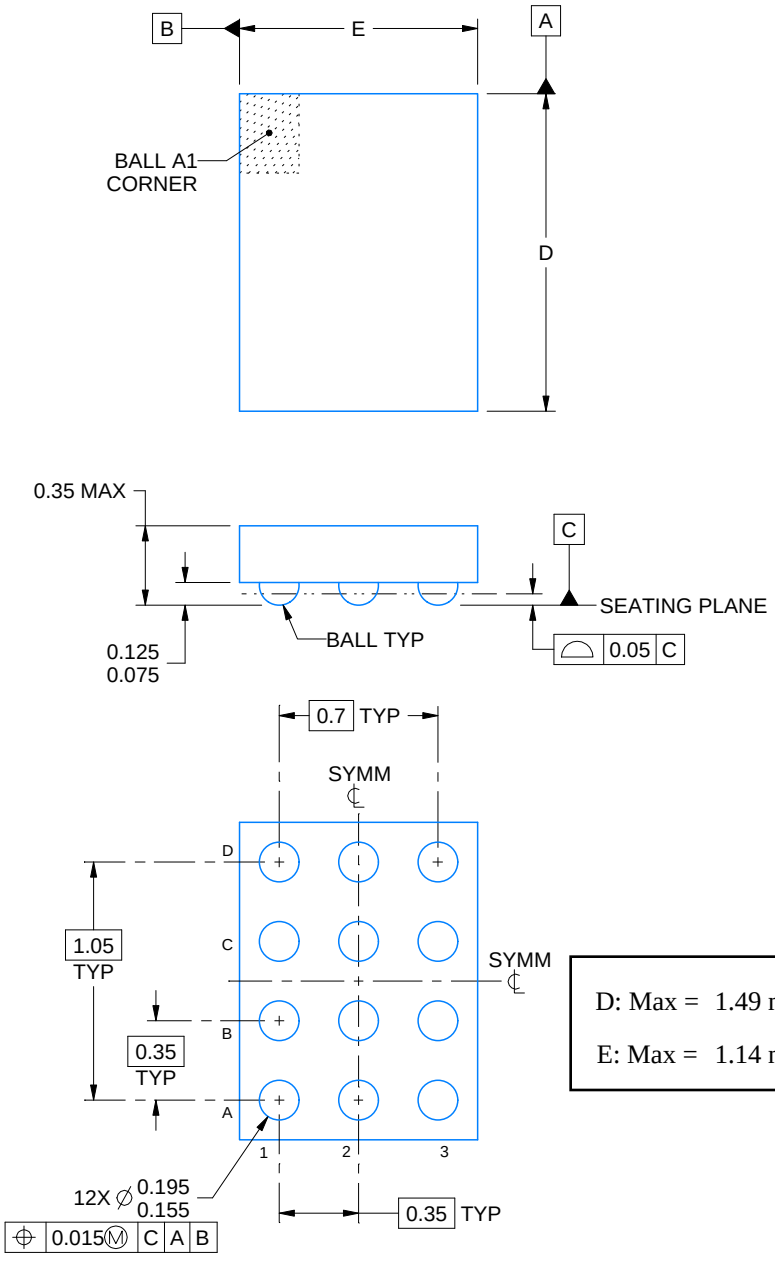
YCJ0012



PACKAGE OUTLINE

DSBGA - 0.35 mm max height

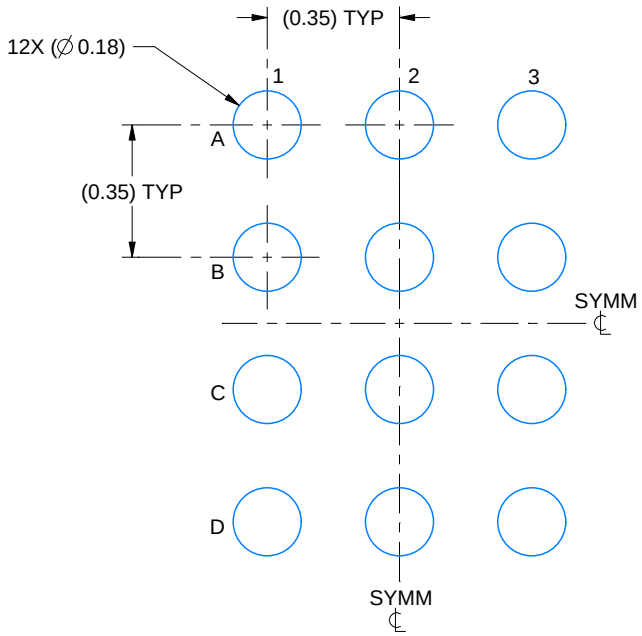
DIE SIZE BALL GRID ARRAY



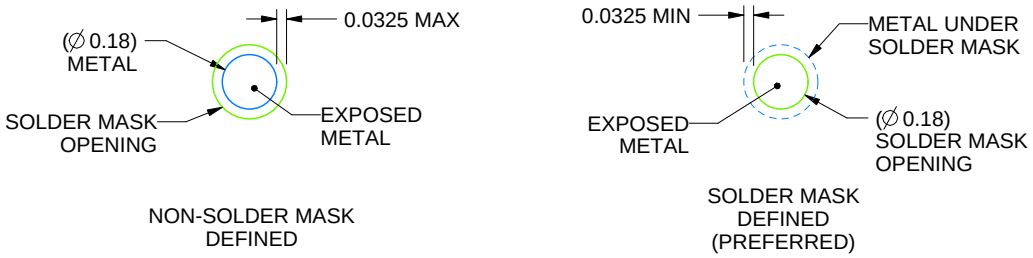
4224964/A 04/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4224964/A 04/2019

NOTES: (continued)

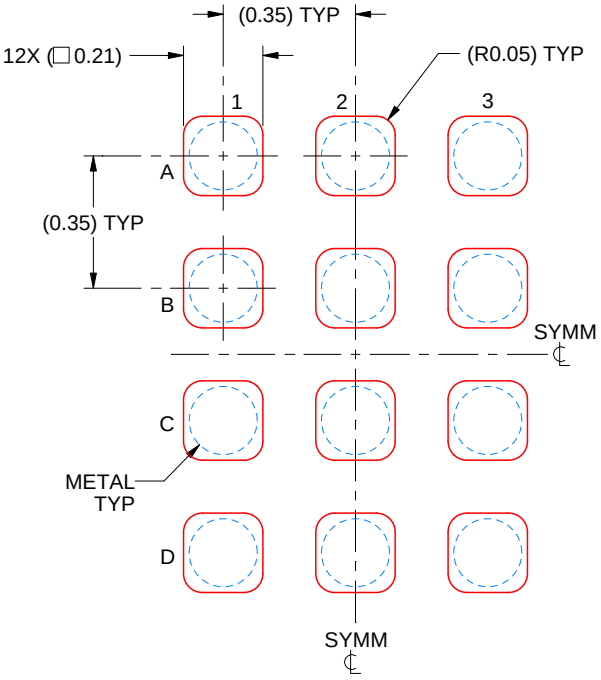
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0012

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4224964/A 04/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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