具有 Eco-mode™ 的 0.5A，60V 降压直流/直流转换器

查询样品: **TPS54060A**

特性

- **3.5V** 至 **60V** 输入电压范围
- **200mΩ** 高侧金属氧化物半导体场效应晶体管 **(MOSFET)**
- 在带有脉冲跳跃的轻负载条件上的高效率 **Eco-mode™**
- 比 **TPS54060** 更严密的使能阀值以获得更精确的欠压闭锁 **(UVLO)** 电压
- 可调的 **UVLO** 电压和滞后
- 运行静态电流 **116μA**
- 关断电流 **1.3μA**
- **100kHz** 至 **2.5MHz** 的开关频率
- 同步至外部时钟
- 可调节的缓起动/排序
- 欠压 **(UV)** 和过流 **(OV)** 电源正常输出
- **0.8V** 内部电压基准
- 微型小外形尺寸 **(MSOP)** 和 **3mm x 3mm** 超薄小外形尺寸 **(VSON)-10** 封装，这些封装具有 **PowerPAD™**
- 由 **WEBENCH®** 和 **SwitcherPro™** 软件工具

应用范围

- **12V**，**24V** 和 **48V** 工业及商用低功耗系统
- 汽车售后加装配件：视频、全球卫星定位 **(GPS)**、娱乐

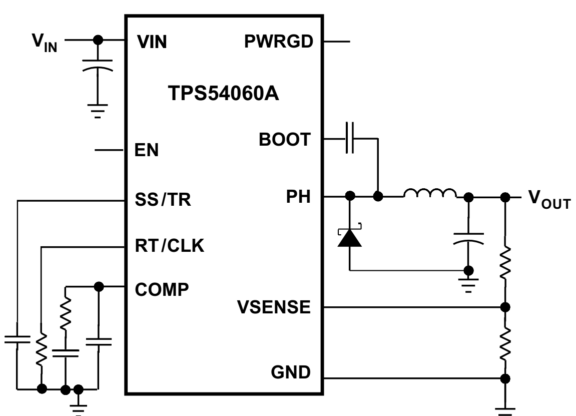
说明

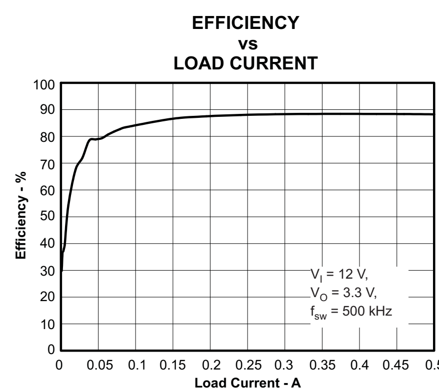
TPS54060A 器件是一款带有集成型高侧 MOSFET 的 60V，0.5A，降压稳压器。 电流模式控制提供了简单的外部补偿和组件选择的灵活性。 一个低纹波脉冲跳跃模式将无负载的稳定输出电源电流减小至 116μA。 采用使能引脚可将停机模式的电源电流降低至 1.3μA（此时，使能引脚为低电平）。

欠压闭锁在内部设定为 2.5V，但可采用使能引脚将之提高。 输出电压启动斜坡受控于缓慢起动引脚，该引脚还可以通过配置来控制排序/跟踪。 一个开漏电源正常信号表示说明第二段中的输出 94% 至 107% 的范围内。

宽开关频率范围允许对效率及外部组件尺寸进行优化。 频率折返和热关断功能在过载情况下对部件实施保护。

简化的原理图





English Data Sheet: SLVSB57

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_J	PACKAGE	PART NUMBER(2)
–40°C to 150°C	MSOP-10	TPS54060ADGQ
	VSON-10	TPS54060ADRC

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DGQ package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54060ADGQR).

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN	–0.3	65	V
	EN	–0.3	5	
	BOOT		73	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-PH		8	V
	PH	–0.6	65	
	PH, 10-ns Transient	–2	65	
Voltage Difference	PAD to GND		±200	mV
Source current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH	Current Limit		A
	RT/CLK		100	µA
Sink current	VIN	Current Limit		A
	COMP		100	µA
	PWRGD		10	mA
	SS/TR		200	µA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating junction temperature		–40	150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS54060A		UNITS
		DGQ (10 PINS)	DRC (10 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance (standard board)	62.5	40	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	0.6	
ψ_{JB}	Junction-to-board characterization parameter	20.1	7.5	
θ_{JCtop}	Junction-to-case(top) thermal resistance	83	65	
θ_{JCbot}	Junction-to-case(bottom) thermal resistance	21	7.8	
θ_{JB}	Junction-to-board thermal resistance	28	8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) Power rating at a specific ambient temperature TA should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 3.5 to 60V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		3.5		60	V
Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 60 V		1.3	4	μA
Operating : nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V, 25°C		116	136	
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	1.11	1.25	1.36	V
Input current	Enable threshold +50 mV		–3.8		μA
	Enable threshold –50 mV		–0.9		
Hysteresis current		1.91	2.95	3.99	μA
VOLTAGE REFERENCE					
Voltage reference	T_J = 25°C	0.792	0.8	0.808	V
		0.784	0.8	0.816	
HIGH-SIDE MOSFET					
On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
	VIN = 12 V, BOOT-PH = 6 V		200	410	
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (g_M)	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V		97		μMhos
Error amplifier transconductance (g_M) during slow start	–2 μA < I_{COMP} < 2 μA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		μMhos
Error amplifier dc gain	V_{VSENSE} = 0.8 V		10,000		V/V
Error amplifier bandwidth			2700		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±7		μA
COMP to switch current transconductance			1.9		A/V

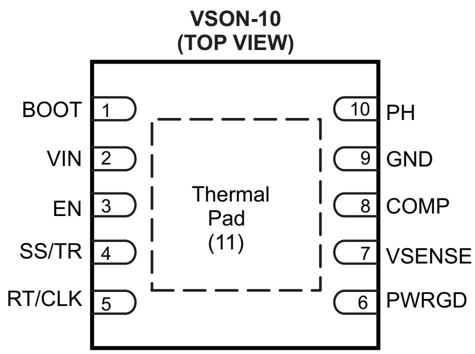
ELECTRICAL CHARACTERISTICS (continued)

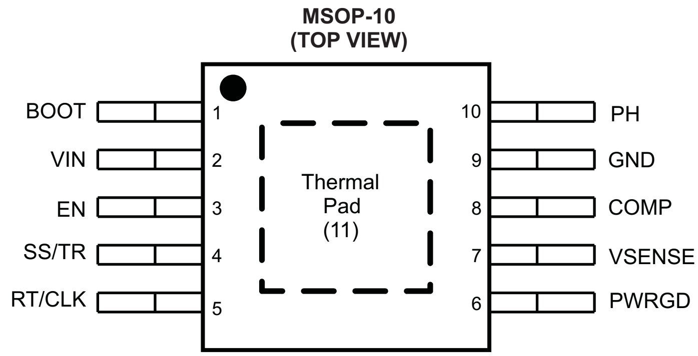
T_J = –40°C to 150°C, VIN = 3.5 to 60V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	Current limit threshold	VIN = 12 V, T_J = 25°C	0.6	0.94		A
THERMAL SHUTDOWN						
	Thermal shutdown			182		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching Frequency Range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	581	720	kHz
	Switching Frequency Range using CLK mode		300		2200	kHz
	Minimum CLK input pulse width			40		ns
	RT/CLK high threshold			1.9	2.2	V
	RT/CLK low threshold		0.5	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	PLL lock in time	Measured at 500 kHz		100		μs
SLOW START AND TRACKING (SS/TR)						
	Charge current	$V_{SS/TR}$ = 0.4 V		2		μA
	SS/TR-to-VSENSE matching	$V_{SS/TR}$ = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1.0		V
	SS/TR discharge current (overload)	VSENSE = 0 V, V(SS/TR) = 0.4 V		112		μA
	SS/TR discharge voltage	VSENSE = 0 V		54		mV
POWER GOOD (PWRGD PIN)						
V_{VSENSE}	VSENSE threshold	VSENSE falling		92%		
		VSENSE rising		94%		
		VSENSE rising		109%		
		VSENSE falling		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
	Minimum VIN for defined output	V(PWRGD) < 0.5 V, II(PWRGD) = 100 μA		0.95	1.5	V

DEVICE INFORMATION

PIN CONFIGURATION

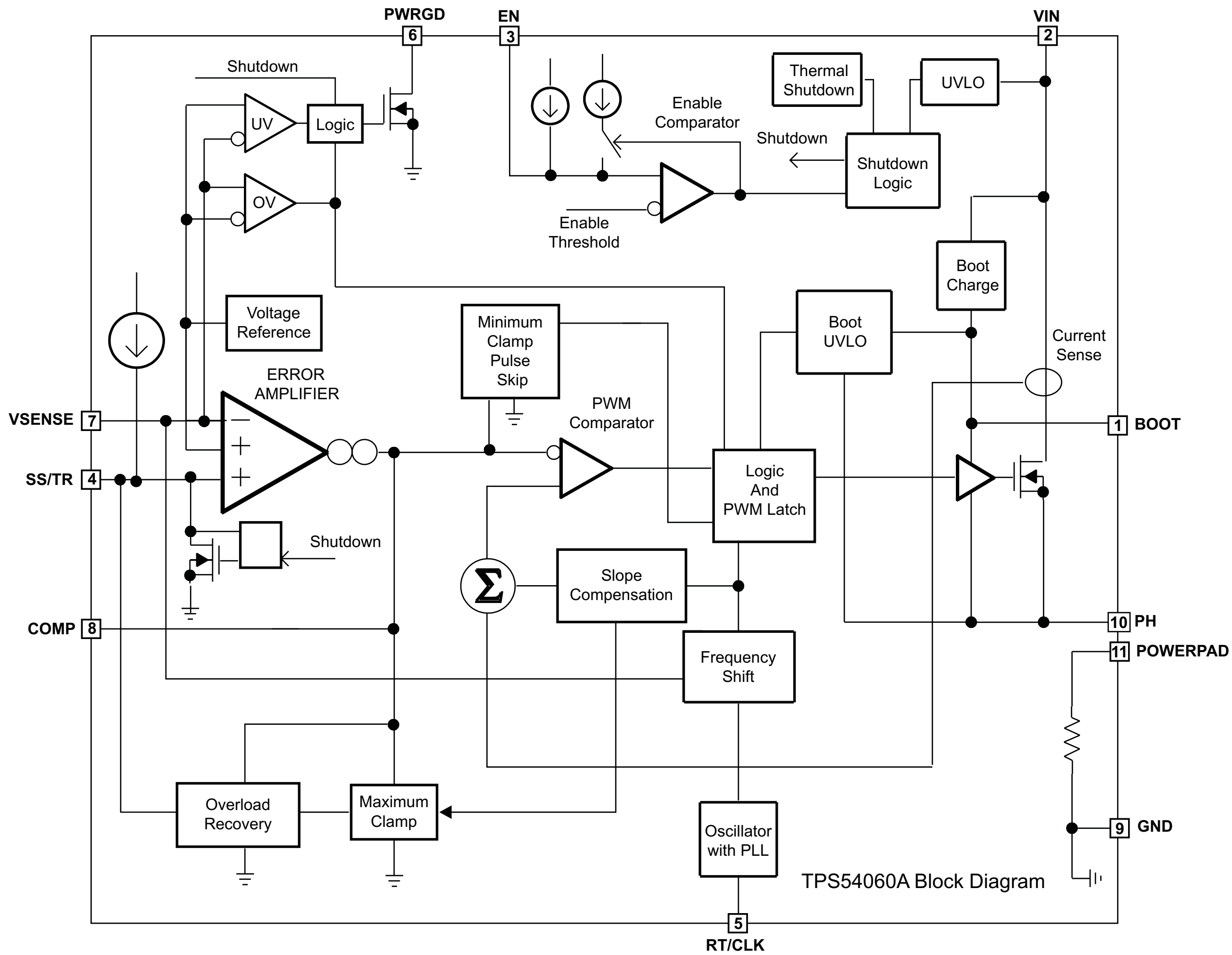




PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	–	Ground
PH	10	I	The source of the internal high-side power MOSFET.
THERMAL PAD	11	–	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.
PWRGD	6	O	An open drain output, asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS/TR	4	I	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 60 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

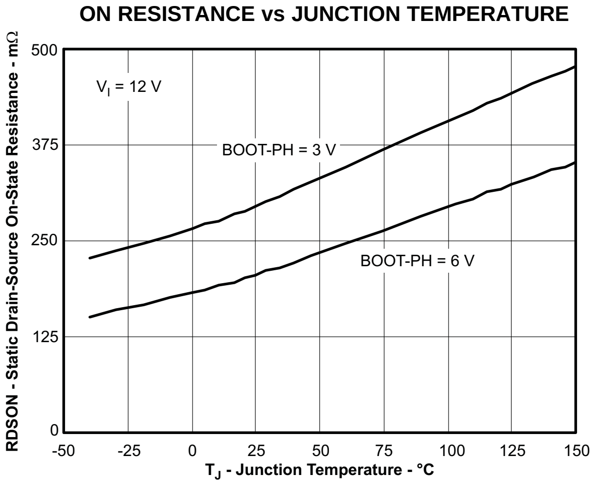


Figure 1.

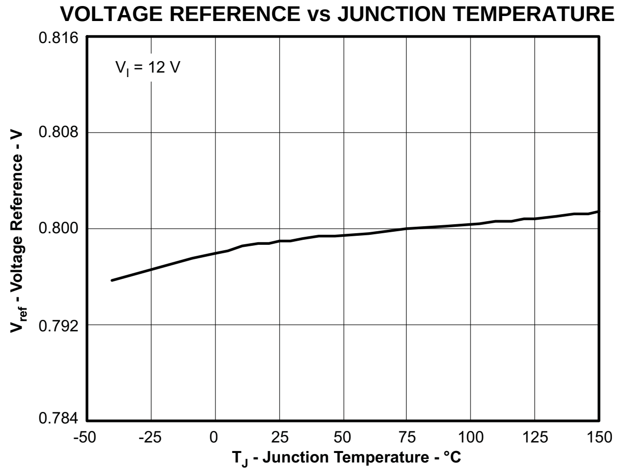
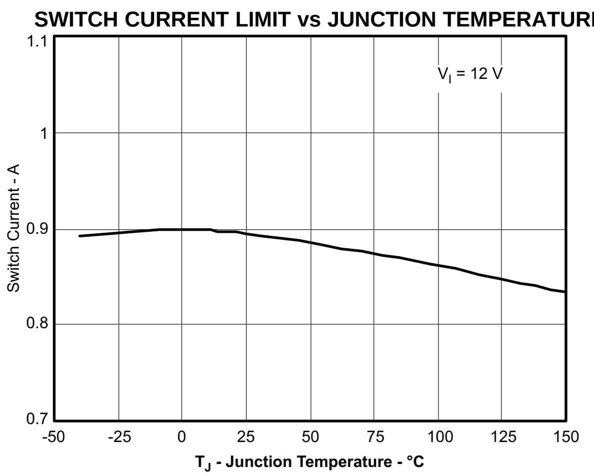


Figure 2.



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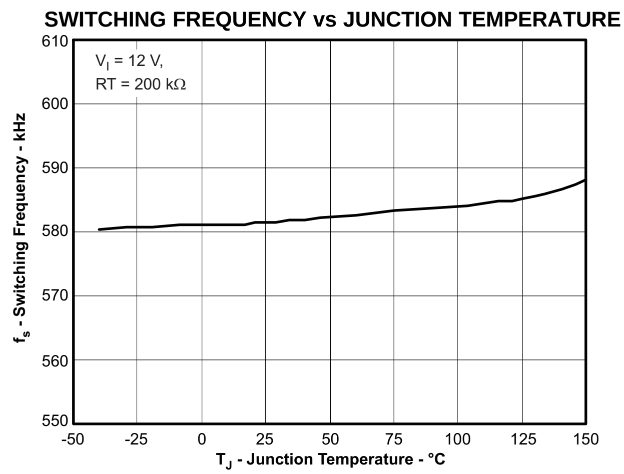

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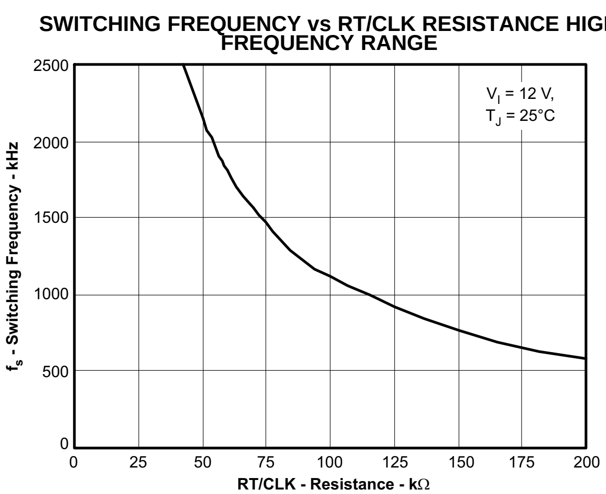


Figure 5.

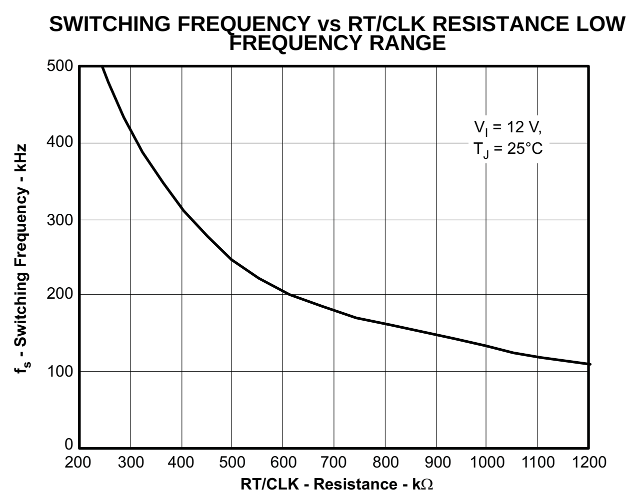


Figure 6.

TYPICAL CHARACTERISTICS (continued)

EA TRANSCONDUCTANCE DURING SLOW START vs JUNCTION TEMPERATURE

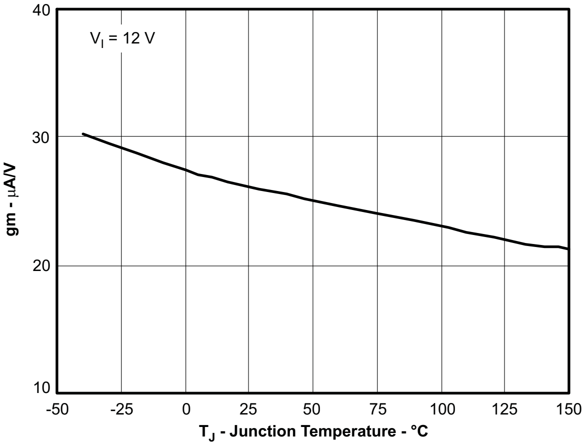


Figure 7.

EA TRANSCONDUCTANCE vs JUNCTION TEMPERATURE

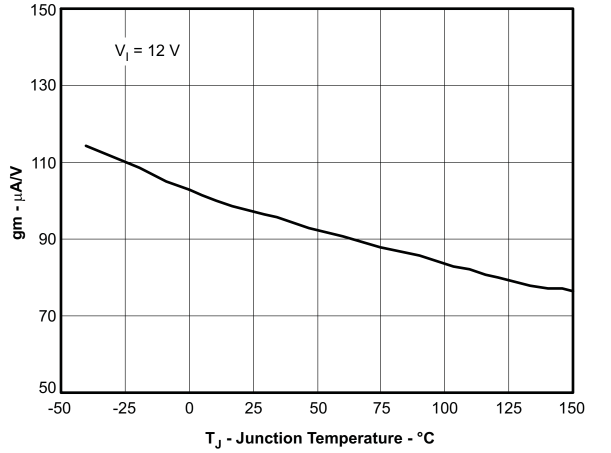


Figure 8.

EN PIN VOLTAGE vs JUNCTION TEMPERATURE

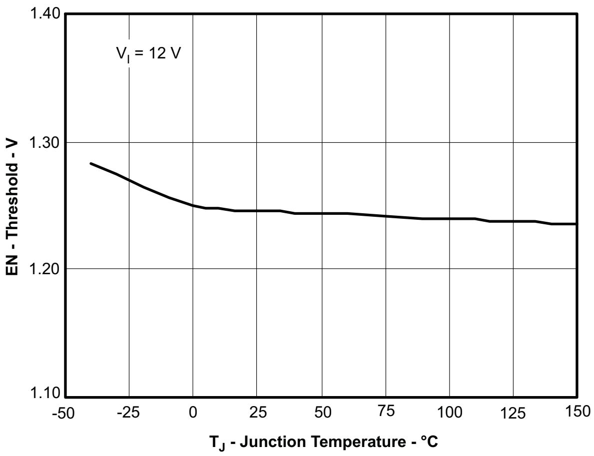


Figure 9.

EN PIN CURRENT vs JUNCTION TEMPERATURE

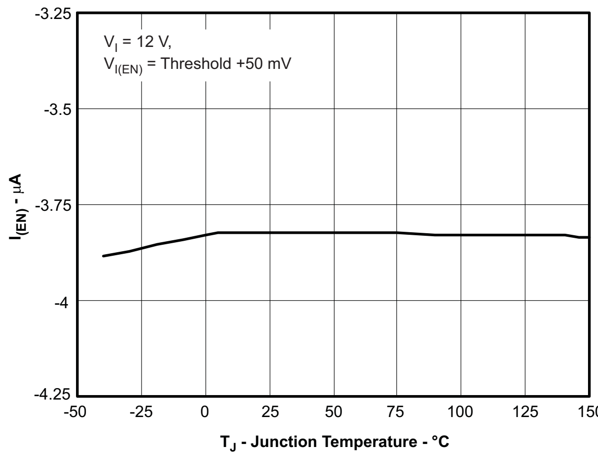


Figure 10.

EN PIN CURRENT vs JUNCTION TEMPERATURE

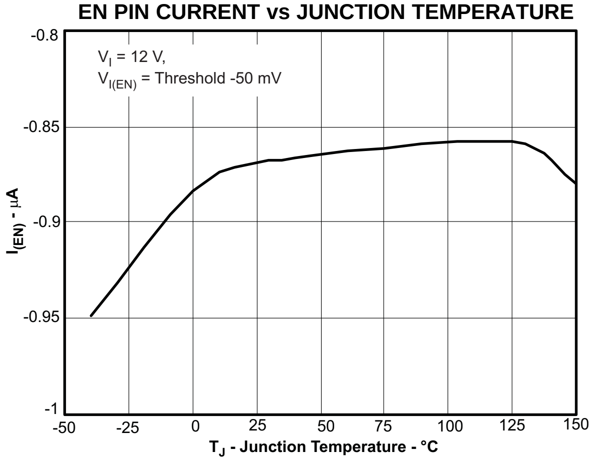


Figure 11.

SS/TR CHARGE CURRENT vs JUNCTION TEMPERATURE

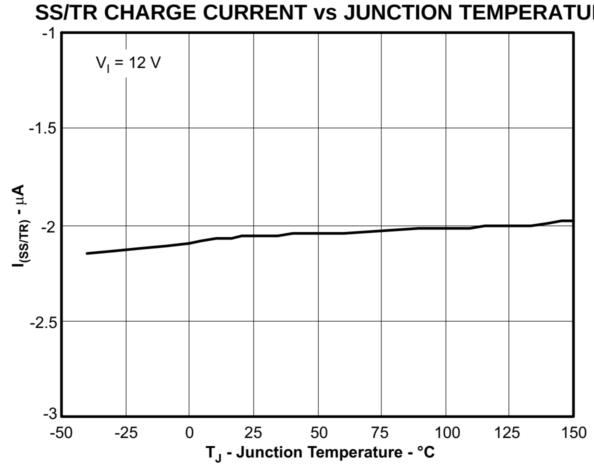


Figure 12.

TYPICAL CHARACTERISTICS (continued)

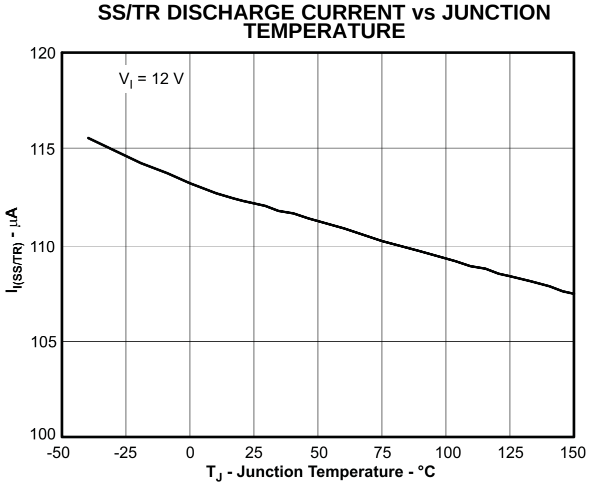


Figure 13.

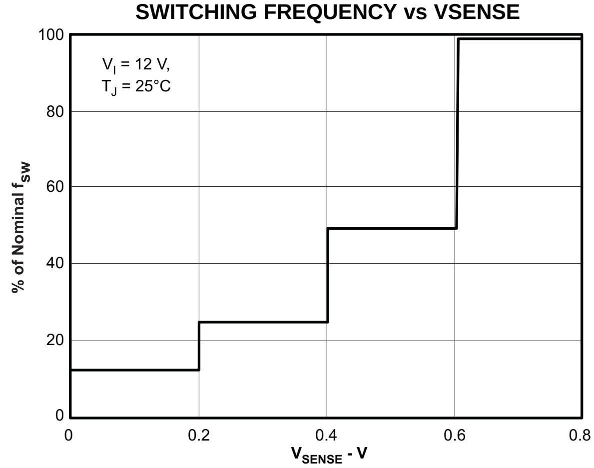


Figure 14.

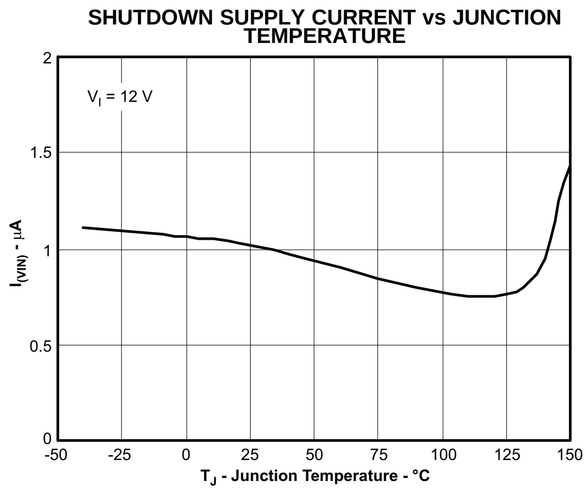


Figure 15.

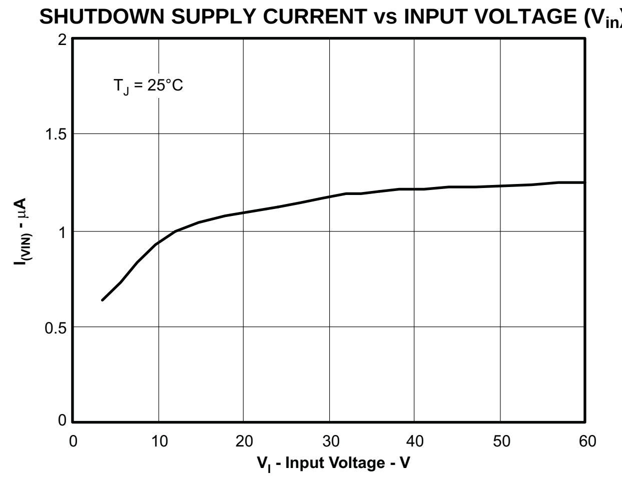


Figure 16.

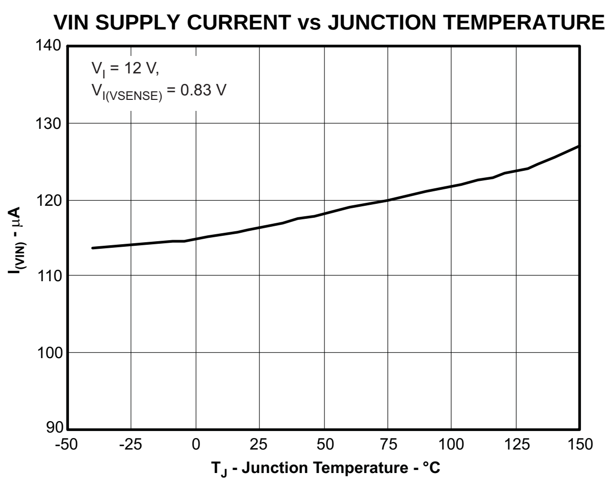


Figure 17.

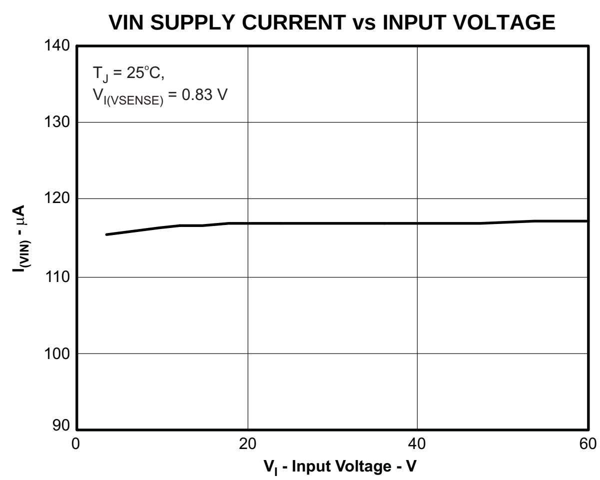


Figure 18.

TYPICAL CHARACTERISTICS (continued)

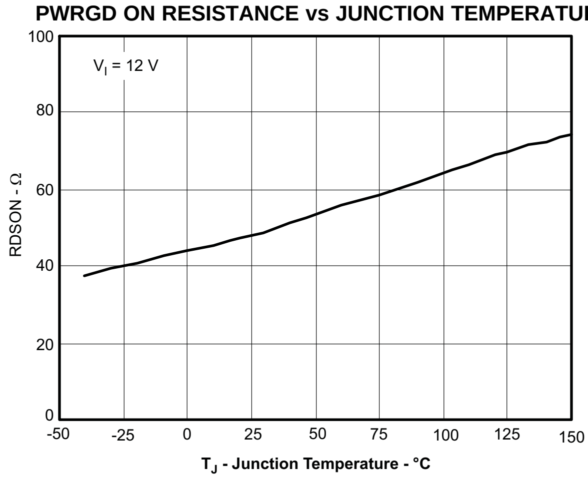
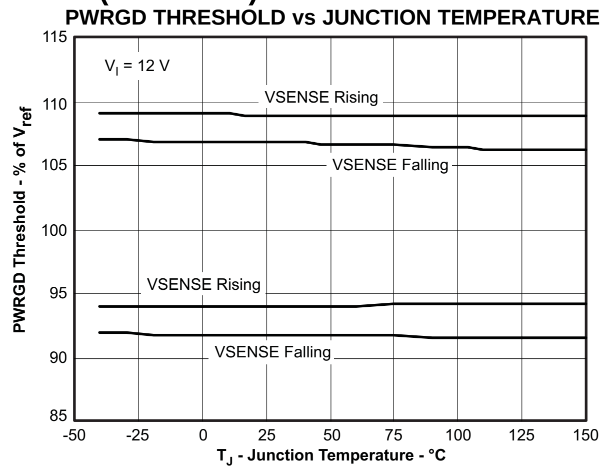


Figure 19.



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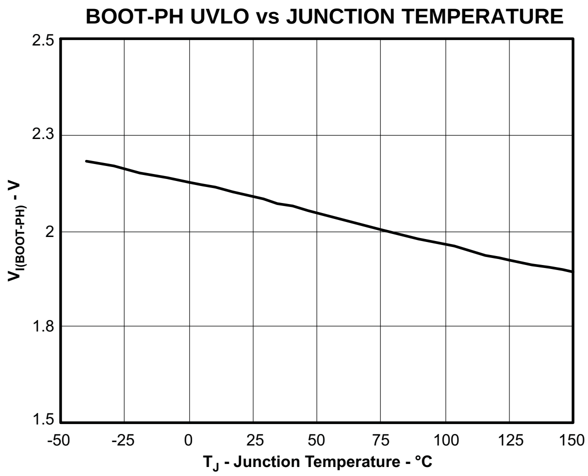


Figure 21.

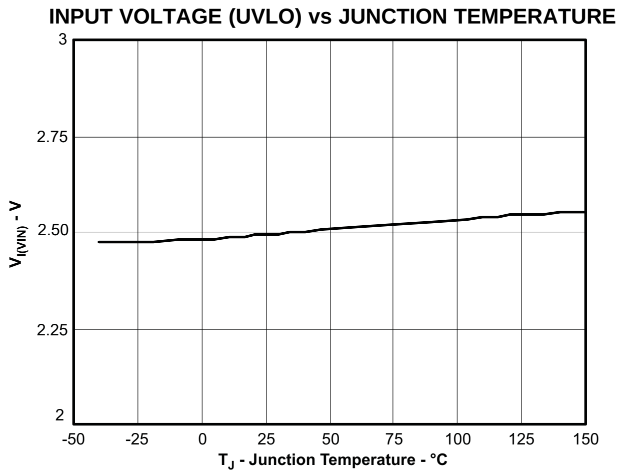


Figure 22.

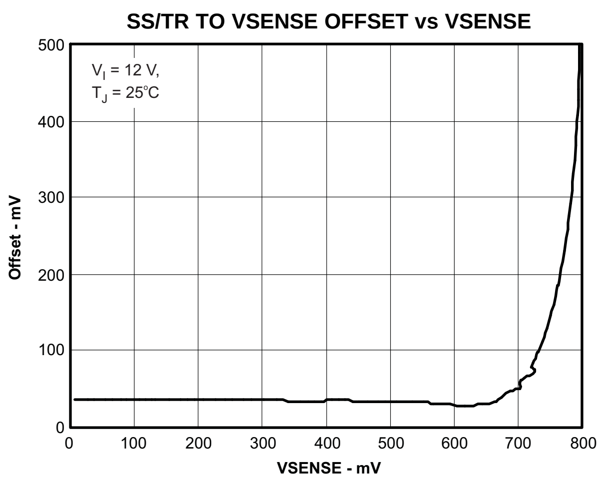


Figure 23.

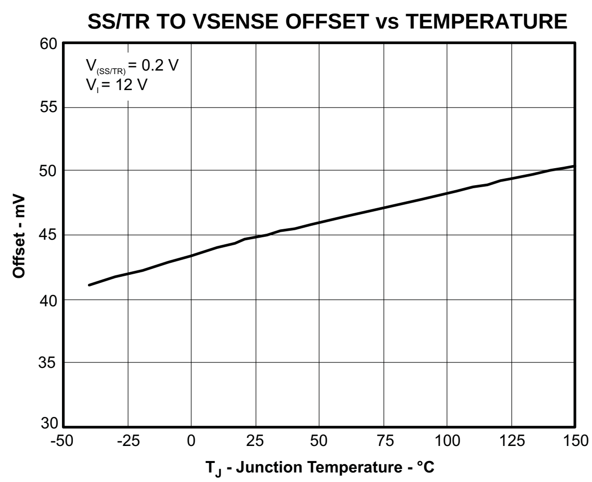


Figure 24.

OVERVIEW

The TPS54060A device is a 60-V, 0.5-A, step-down (buck) regulator with an integrated high side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100kHz to 2500kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54060A has a default start up voltage of approximately 2.5V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN pin is floating the device will operate. The operating current is 116μA when not switching and under no load. When the device is disabled, the supply current is 1.3μA.

The integrated 200mΩ high side MOSFET allows for high efficiency power supply designs capable of delivering 0.5 amperes of continuous current to a load. The TPS54060A reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The TPS54060A can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8V reference.

The TPS54060A has a power good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pull-up resistor is used.

The TPS54060A minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power good comparator. When the OV comparator is activated, the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault, UVLO fault or a disabled condition.

The TPS54060A, also, discharges the slow start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54060A uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the COMP voltage, the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-Mode™ is implemented with a minimum clamp on the COMP pin.

Slope Compensation Output Current

The TPS54060A adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

Pulse Skip Eco-mode

The TPS54060A operates in a pulse skip Eco mode at light load currents to improve efficiency by reducing switching and gate drive losses. The TPS54060A is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco mode. This current threshold is the current level corresponding to a nominal COMP voltage or 500mV.

When in Eco-mode, the COMP pin voltage is clamped at 500mV and the high side MOSFET is inhibited. Further decreases in load current or in output voltage can not drive the COMP pin below this clamp voltage level.

Since the device is not switching, the output voltage begins to decay. As the voltage control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high side MOSFET is enabled and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP pin voltage. The output voltage re-charges the regulated value (see Figure 25), then the peak switch current starts to decrease, and eventually falls below the Eco mode threshold at which time the device again enters Eco mode.

For Eco-mode operation, the TPS54060A senses peak current, not average or load current, so the load current where the device enters Eco mode is dependent on the output inductor value. For example, the circuit in Figure 51 enters Eco mode at about 20 mA of output current. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 116μA input quiescent current. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse skip mode, the switching transitions occur synchronously with the external clock signal.

DETAILED DESCRIPTION (continued)

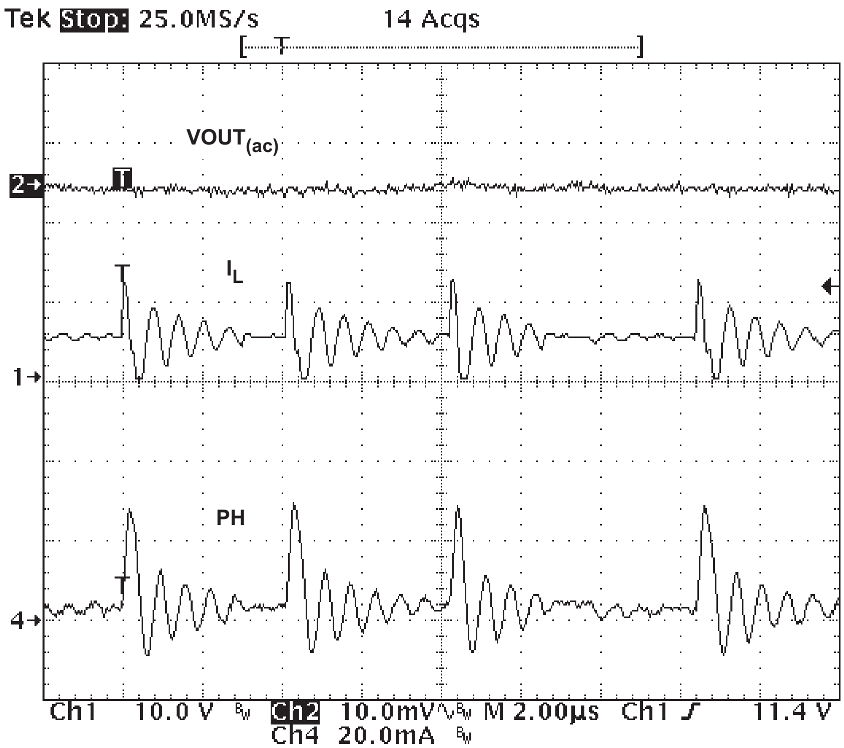


Figure 25. Pulse Skip Mode Operation

Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54060A has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high side MOSFET. The BOOT capacitor is refreshed when the high side MOSFET is off and the low side diode conducts. The value of this ceramic capacitor should be 0.1μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics overtemperature and voltage.

To improve drop out, the TPS54060A is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1V. When the voltage from BOOT to PH drops below 2.1V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the BOOT capacitor. Since the supply current sourced from the BOOT capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low side diode and printed circuit board resistance. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high side MOSFET can remain on for 100% of the duty cycle to maintain output regulation, until the BOOT to PH voltage falls below 2.1V.

Attention must be taken in maximum duty cycle applications which experience extended time periods with light loads or no load. When the voltage across the BOOT capacitor falls below the 2.1V UVLO threshold, the high side MOSFET is turned off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1V. The output capacitor then decays until the difference in the input voltage and output

DETAILED DESCRIPTION (continued)

voltage is greater than 2.1V, at which point the BOOT UVLO threshold is exceeded, and the device starts switching again until the desired output voltage is reached. This operating condition persists until the input voltage and/or the load current increases. It is recommended to adjust the VIN stop voltage greater than the BOOT UVLO trigger condition at the minimum load of the application using the adjustable VIN UVLO feature with resistors on the EN pin.

The start and stop voltages for typical 3.3V and 5V output applications are shown in Figure 26 and Figure 27. The voltages are plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output within 1%. The stop voltage is defined as the input voltage at which the output drops by 5% or stops switching.

During high duty cycle conditions, the inductor current ripple increases while the BOOT capacitor is being recharged resulting in an increase in ripple voltage on the output. This is due to the recharge time of the boot capacitor being longer than the typical high side off time when switching occurs every cycle.

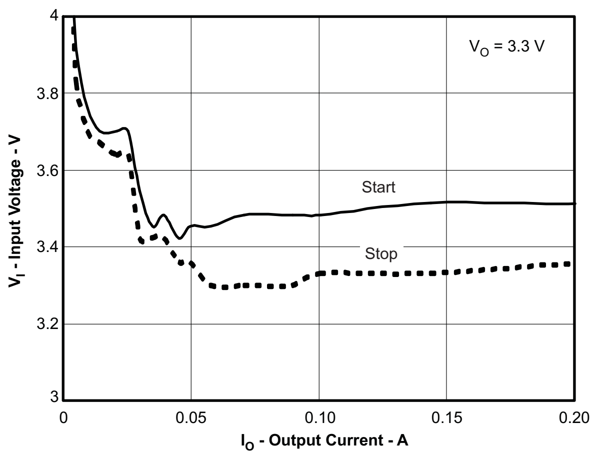


Figure 26. 3.3V Start/Stop Voltage

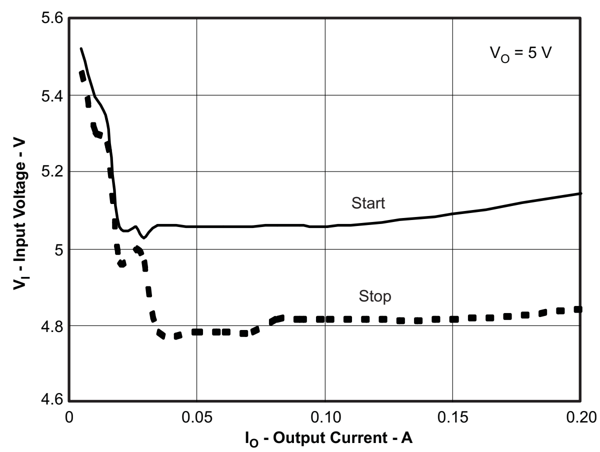


Figure 27. 5.0V Start/Stop Voltage

Error Amplifier

The TPS54060A has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8V voltage reference. The transconductance (gm) of the error amplifier is 97μA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8V and the device is regulating using the SS/TR voltage, the gm is 25μA/V.

The frequency compensation components (capacitor, series resistor and capacitor) are added to the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

DETAILED DESCRIPTION (continued)

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for the R2 resistor and use the Equation 1 to calculate R1. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator will be more susceptible to noise and voltage errors from the VSENSE input current will be noticeable

$$R1 = R2 \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \tag{1}$$

Enable and Adjusting Undervoltage Lockout

The TPS54060A is disabled when the VIN pin voltage falls below 2.5 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 28 to adjust the input voltage UVLO by using the two external resistors. Though it is not necessary to use the UVLO adjust registers, for operation it is highly recommended to provide consistent power up behavior. The EN pin has an internal pull-up current source, I1, of 0.9μA that provides the default condition of the TPS54060A operating when the EN pin floats. Once the EN pin voltage exceeds 1.25V, an additional 2.9μA of hysteresis, Ihys, is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input start voltage.

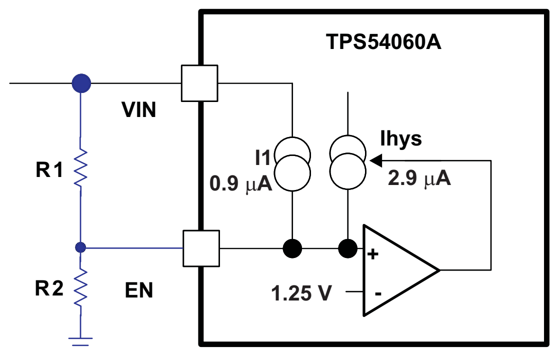


Figure 28. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{2}$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \tag{3}$$

Another technique to add input voltage hysteresis is shown in Figure 29. This method may be used, if the resistance values are high from the previous method and a wider voltage hysteresis is needed. The resistor R3 sources additional hysteresis current into the EN pin.

DETAILED DESCRIPTION (continued)

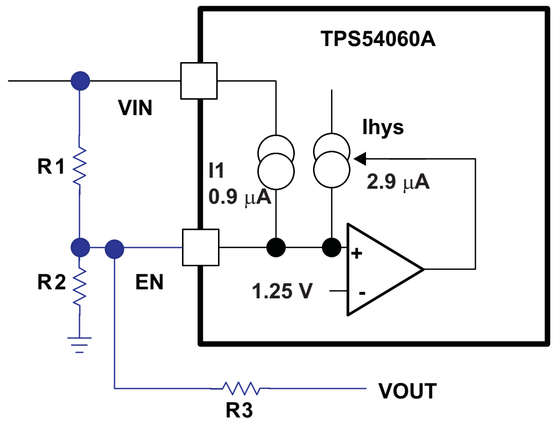


Figure 29. Adding Additional Hysteresis

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \tag{4}$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \tag{5}$$

Do not place a low-impedance voltage source with greater than 5 V directly on the EN pin. Do not place a capacitor directly on the EN pin if V_{EN} > 5 V when using a voltage divider to adjust the start and stop voltage. The node voltage, (see Figure 30) must remain equal to or less than 5.8 V. The zener diode can sink up to 100 µA. The EN pin voltage can be greater than 5 V if the V_{IN} voltage source has a high impedance and does not source more than 100 µA into the EN pin.

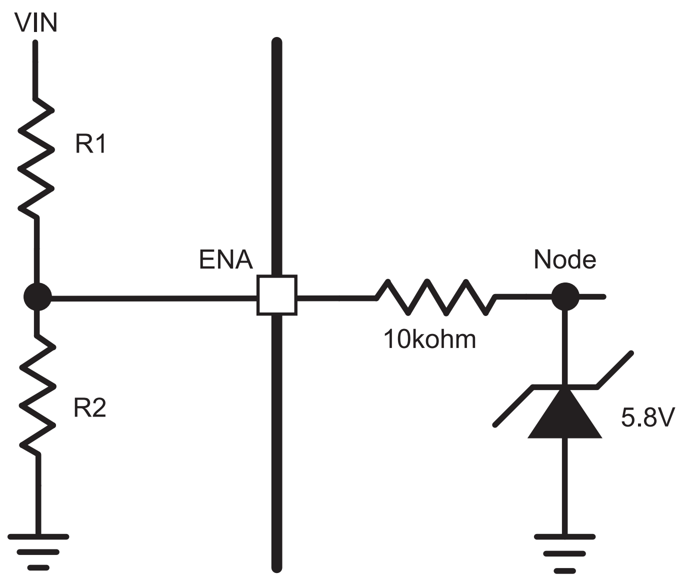


Figure 30. Node Voltage

DETAILED DESCRIPTION (continued)

Slow Start/Tracking Pin (SS/TR)

The TPS54060A effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply's reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow start time. The TPS54060A has an internal pull-up current source of 2μA that charges the external slow start capacitor. The calculations for the slow start time (10% to 90%) are shown in Equation 6. The voltage reference (V_{REF}) is 0.8 V and the slow start current (I_{SS}) is 2μA. The slow start capacitor should remain lower than 0.47μF and greater than 0.47nF.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref\ (V) \times 0.8} \tag{6}$$

At power up, the TPS54060A will not start switching until the slow start pin is discharged to less than 40 mV to ensure a proper power up, see Figure 31.

Also, during normal operation, the TPS54060A will stop switching and the SS/TR must be discharged to 40 mV, the voltage at the VIN pin is below the VIN UVLO, EN pin pulled below 1.25V, or a thermal shutdown event occurs.

The VSENSE voltage will follow the SS/TR pin voltage with a 45mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage will ramp linearly until clamped at 1.7V.

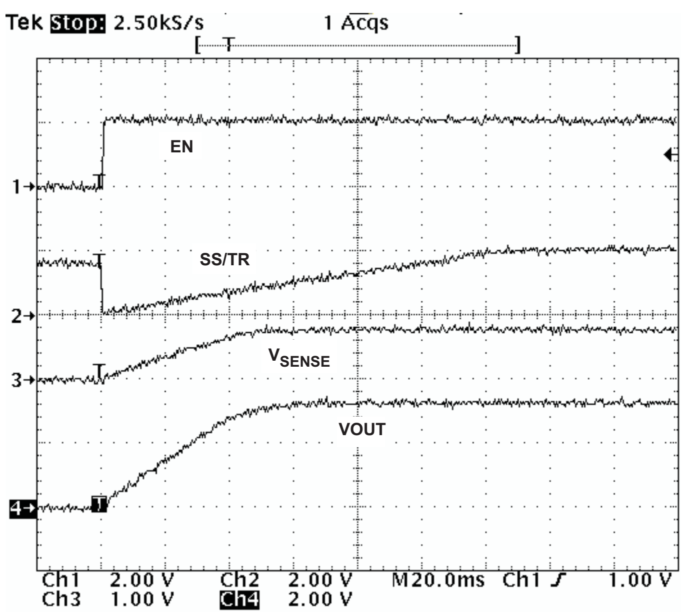


Figure 31. Operation of SS/TR Pin when Starting

Overload Recovery Circuit

The TPS54060A has an overload recovery (OLR) circuit. The OLR circuit will slow start the output from the overload voltage to the nominal regulation voltage once the fault condition is removed. The OLR circuit will discharge the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pull down of 100μA when the error amplifier is changed to a high voltage from a fault condition. When the fault condition is removed, the output will slow start from the fault voltage to nominal output voltage.

DETAILED DESCRIPTION (continued)

Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open drain output of a power on reset pin of another device. The sequential method is illustrated in Figure 32 using two TPS54060A devices. The power good is coupled to the EN pin on the TPS54060A which will enable the second power supply once the primary supply reaches regulation. If needed, a 1nF ceramic capacitor on the EN pin of the second power supply will provide a 1ms start up delay. Figure 33 shows the results of Figure 32.

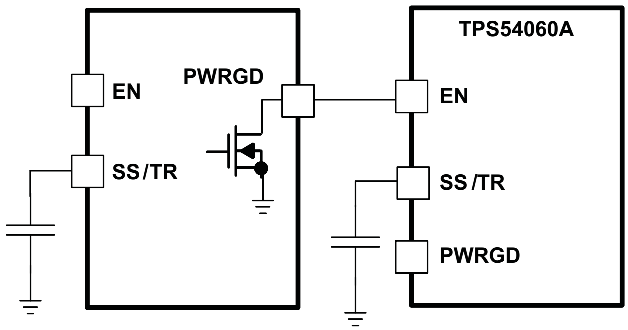


Figure 32. Schematic for Sequential Start-Up Sequence

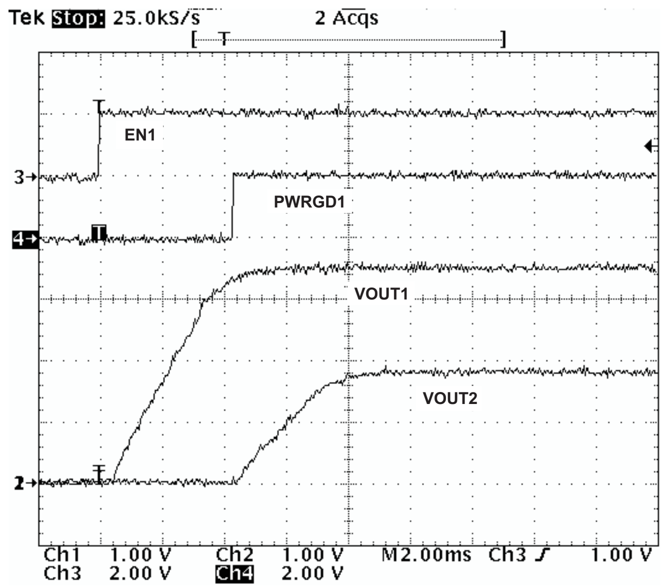


Figure 33. Sequential Startup using EN and PWRGD

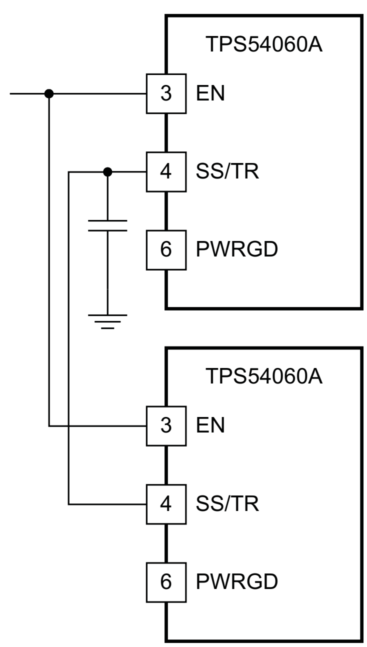


Figure 34. Schematic for Ratiometric Start-Up Sequence

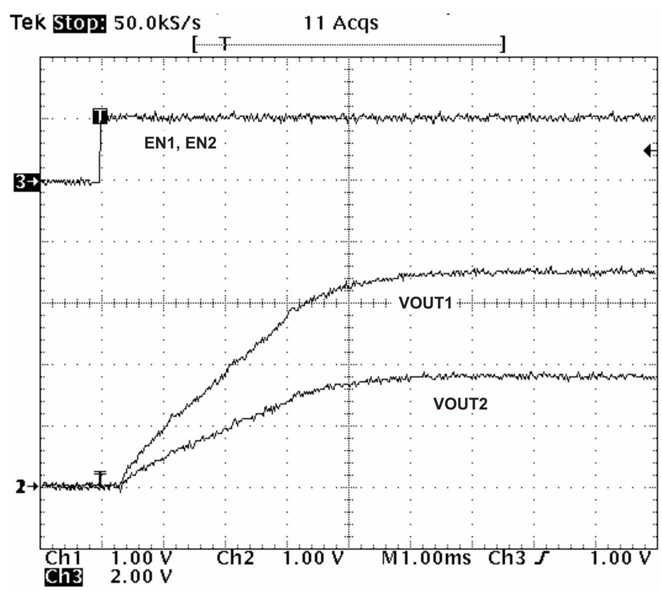


Figure 35. Ratio-Metric Startup using Coupled SS/TR pins

DETAILED DESCRIPTION (continued)

Figure 34 shows a method for ratio-metric start up sequence by connecting the SS/TR pins together. The regulator outputs will ramp up and reach regulation at the same time. When calculating the slow start time the pull up current source must be doubled in Equation 6. Figure 35 shows the results of Figure 34.

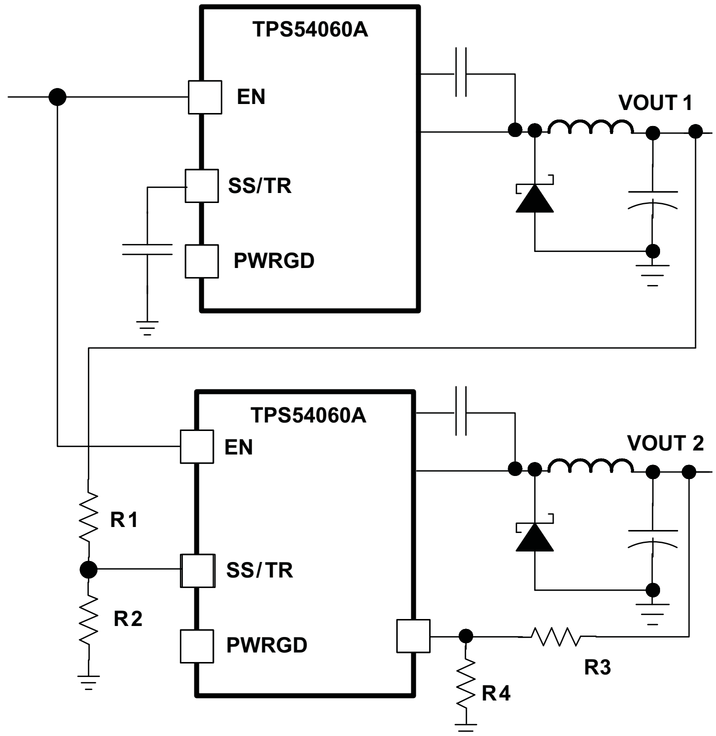


Figure 36. Schematic for Ratiometric and Simultaneous Start-Up Sequence

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 36 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 7 and Equation 8, the tracking resistors can be calculated to initiate the Vout2 slightly before, after or at the same time as Vout1. Equation 9 is the voltage difference between Vout1 and Vout2 at the 95% of nominal output regulation.

The deltaV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset) in the slow start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the Vssoffset and Iss are included as variables in the equations.

To design a ratio-metric start up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 7 through Equation 9 for deltaV. Equation 9 will result in a positive number for applications which the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved.

Since the SS/TR pin must be pulled below 40mV before starting after an EN, UVLO or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device will restart after a fault. Make sure the calculated R1 value from Equation 7 is greater than the value calculated in Equation 10 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage the Vssoffset becomes larger as the slow start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 1.3V for a complete handoff to the internal voltage reference as shown in Figure 23.

DETAILED DESCRIPTION (continued)

$$R1 = \frac{Vout2 + deltaV}{VREF} \times \frac{Vssoffset}{Iss} \quad (7)$$

$$R2 = \frac{VREF \times R1}{Vout2 + deltaV - VREF} \quad (8)$$

$$deltaV = Vout1 - Vout2 \quad (9)$$

$$R1 > 2800 \times Vout1 - 180 \times deltaV \quad (10)$$

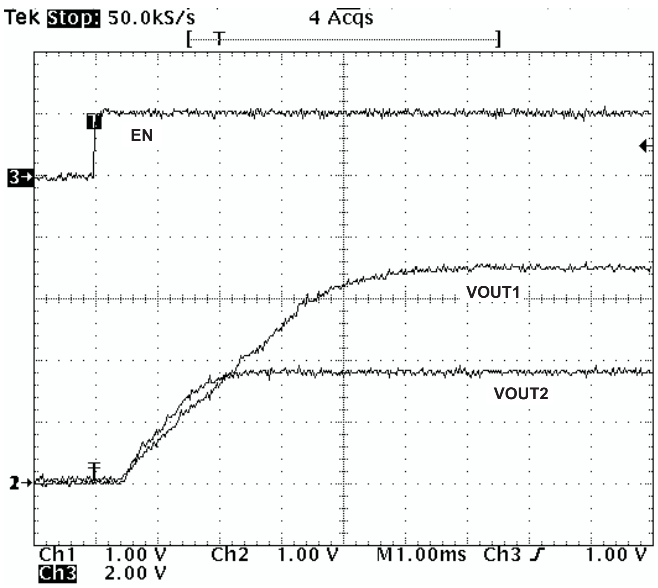


Figure 37. Ratio-metric Startup with Tracking Resistors

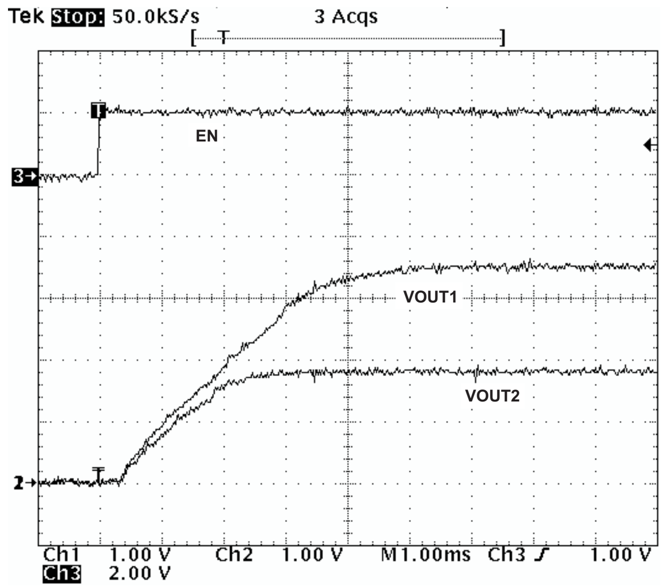


Figure 38. Ratiometric Startup with Tracking Resistors

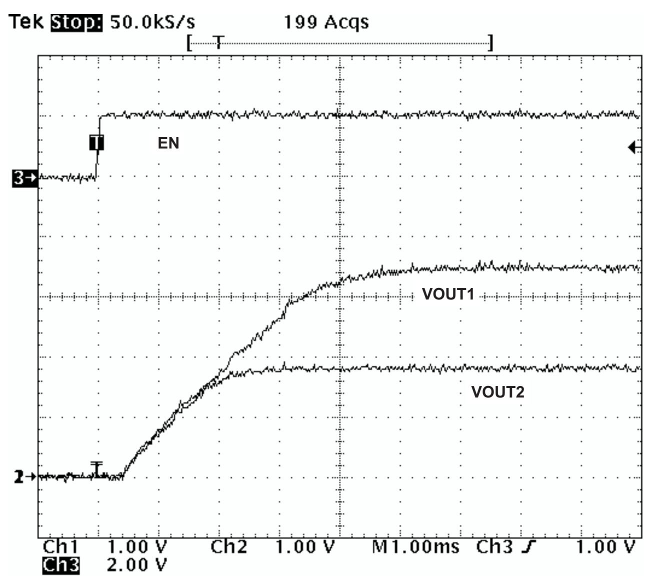


Figure 39. Simultaneous Startup With Tracking Resistor

DETAILED DESCRIPTION (continued)

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54060A is adjustable over a wide range from approximately 100kHz to 2500kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 11 or the curves in Figure 40 or Figure 41. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 130ns and limits the maximum operating input voltage.

The maximum switching frequency is also limited by the frequency shift circuit. More discussion on the details of the maximum switching frequency is located below.

$$\text{RT (kOhm)} = \frac{206033}{f\text{sw (kHz)}^{1.0888}} \tag{11}$$

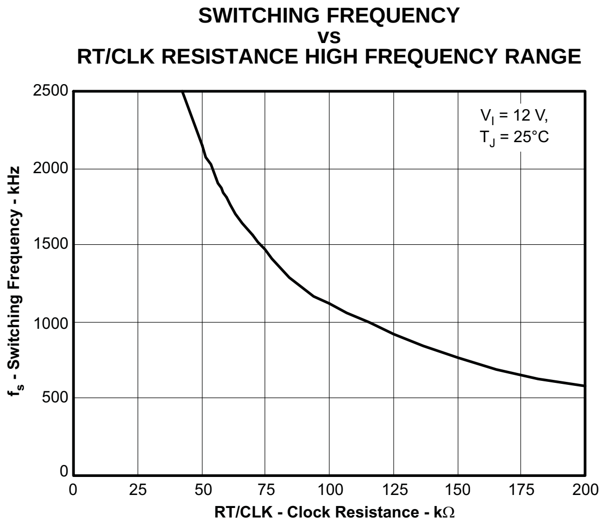


Figure 40. High Range RT

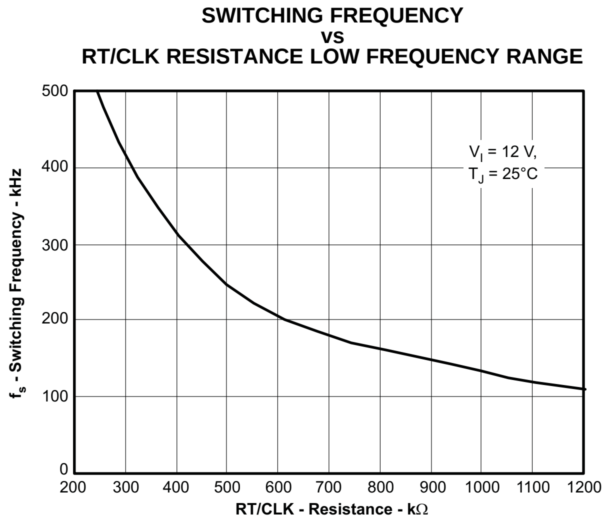


Figure 41. Low Range RT

Overcurrent Protection and Frequency Shift

The TPS54060A implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET on a cycle by cycle basis. Each cycle the switch current and COMP pin voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

To increase the maximum operating switching frequency at high input voltages the TPS54060A implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Since the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still have frequency shift protection.

During short-circuit events (particularly with high input voltage applications), the control loop has a finite minimum controllable on time and the output has a low voltage. During the switch on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time allowing the current to ramp down.

DETAILED DESCRIPTION (continued)

Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the two equations, Equation 12 and Equation 13. Equation 12 is the maximum switching frequency limitation set by the minimum controllable on time. Setting the switching frequency above this value will cause the regulator to skip switching pulses.

Equation 13 is the maximum switching frequency limit set by the frequency shift protection. To have adequate output short circuit protection at high input voltages, the switching frequency should be set to be less than the fsw(maxshift) frequency. In Equation 13, to calculate the maximum switching frequency one must take into account that the output voltage decreases from the nominal voltage to 0 volts, the fdiv integer increases from 1 to 8 corresponding to the frequency shift.

In Figure 42, the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, and the resistance of the inductor is 0.130Ω, FET on resistance of 0.2Ω and the diode voltage drop is 0.5V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software or use the SwitcherPro design software to determine the switching frequency.

$$f_{SW(max\,skip)} = \left(\frac{1}{t_{ON}}\right) \times \left(\frac{(I_L \times Rdc + V_{OUT} + Vd)}{(V_{IN} - I_L \times Rhs + Vd)}\right) \tag{12}$$

$$f_{SW(shift)} = \frac{f\text{div}}{t_{ON}} \times \left(\frac{(I_L \times Rdc + V_{OUTSC} + Vd)}{(V_{IN} - I_L \times Rhs + Vd)}\right) \tag{13}$$

I_L	inductor current
Rdc	inductor resistance
V_{IN}	maximum input voltage
V_{OUT}	output voltage
V_{OUTSC}	output voltage during short
Vd	diode voltage drop
$R_{DS(on)}$	switch on resistance
t_{ON}	controllable on time
f_{DIV}	frequency divide equals (1, 2, 4, or 8)

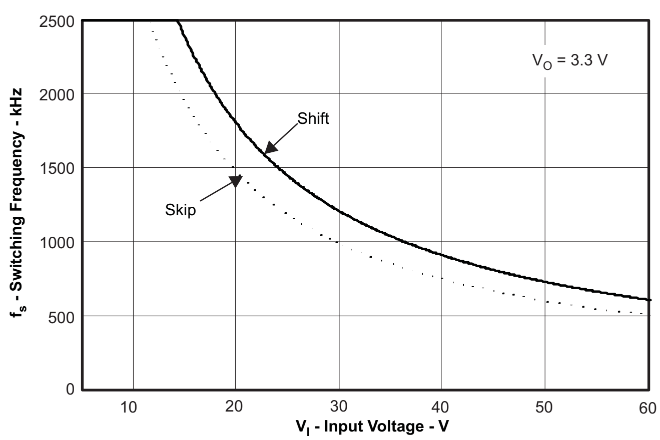


Figure 42. Maximum Switching Frequency vs. Input Voltage

DETAILED DESCRIPTION (continued)

How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through the circuit network shown in Figure 43. The square wave amplitude must transition lower than 0.5V and higher than 2.2V on the RT/CLK pin and have an on time greater than 40 ns and an off time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed in such a way that the device will have the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 43 through a 50Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10 pF ceramic capacitor to RT/CLK pin and a 4kΩ series resistor. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then will increase or decrease the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

When the device transitions from the PLL to resistor mode the switching frequency will slow down from the CLK frequency to 150 kHz, then reapply the 0.5V voltage and the resistor will then set the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Figure 44, Figure 45 and Figure 46 show the device synchronized to an external system clock in continuous conduction mode (ccm) discontinuous conduction (dcm) and pulse skip mode (psm).

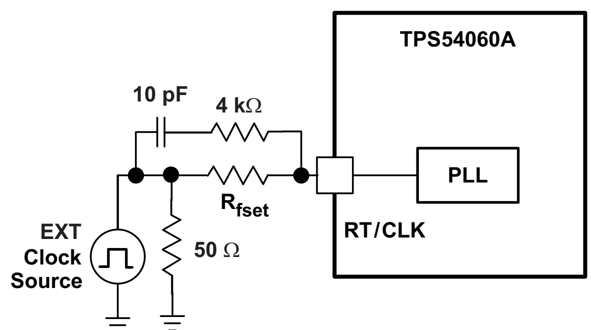


Figure 43. Synchronizing to a System Clock

DETAILED DESCRIPTION (continued)

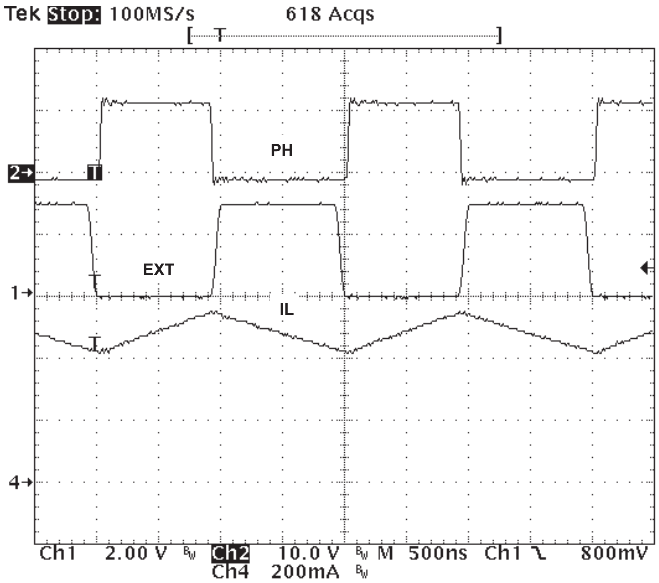


Figure 44. Plot of Synchronizing in ccm

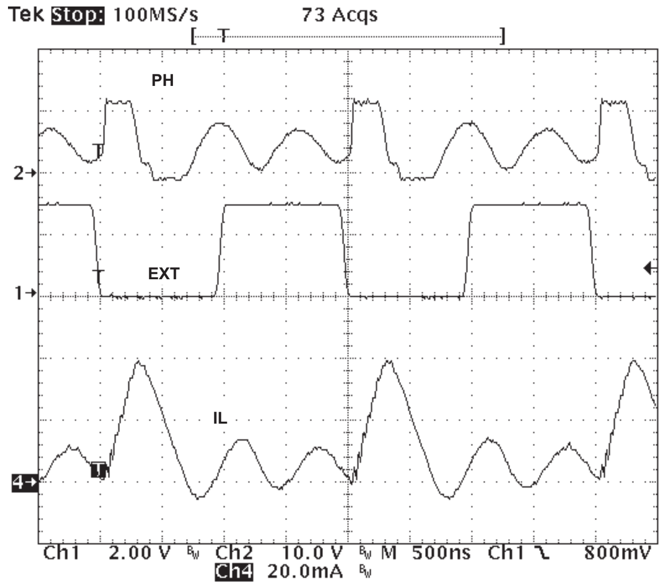


Figure 45. Plot of Synchronizing in dcm

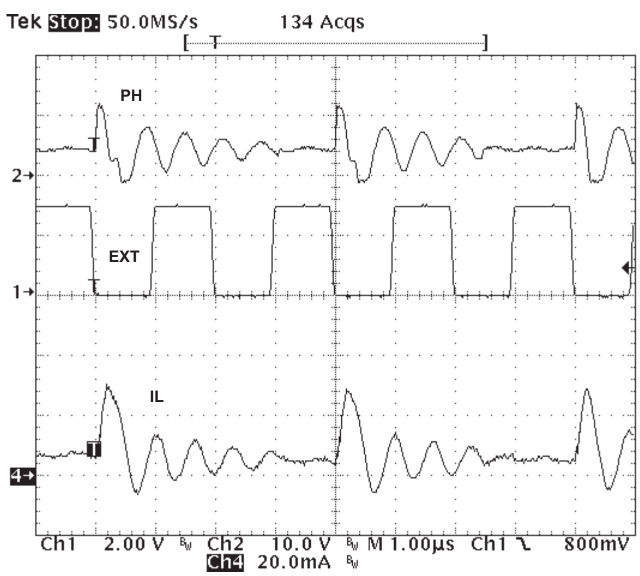


Figure 46. Plot of Synchronizing in PSM

Power Good (PWRGD Pin)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10 and 100kΩ to a voltage source that is 5.5V or less. The PWRGD is in a defined state once the VIN input voltage is greater than 1.5V but with reduced current sinking capability. The PWRGD will achieve full current sinking capability as VIN input voltage approaches 3V.

The PWRGD pin is pulled low when the VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the UVLO or thermal shutdown are asserted or the EN pin pulled low.

DETAILED DESCRIPTION (continued)

Overvoltage Transient Protection

The TPS54060A incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power up sequence by discharging the SS/TR pin.

Small Signal Model for Loop Response

Figure 47 shows an equivalent model for the TPS54060A control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 97 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode designs.

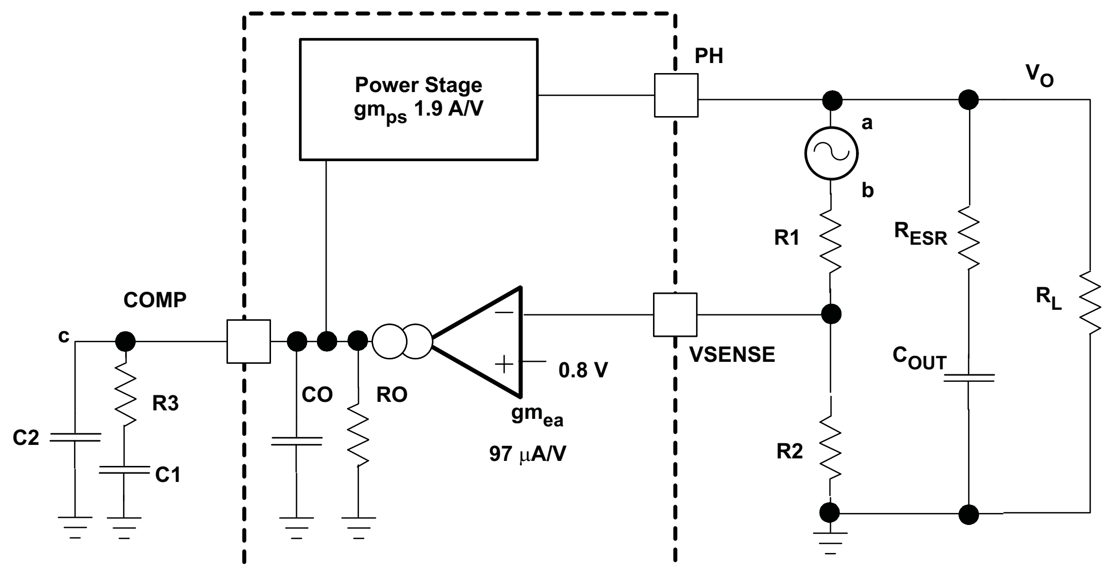


Figure 47. Small Signal Model for Loop Response

DETAILED DESCRIPTION (continued)

Simple Small Signal Model for Peak Current Mode Control

Figure 48 describes a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54060A power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 14 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 47) is the power stage transconductance. The gm_{PS} for the TPS54060A is 1.9A/V. The low-frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 48. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 17).

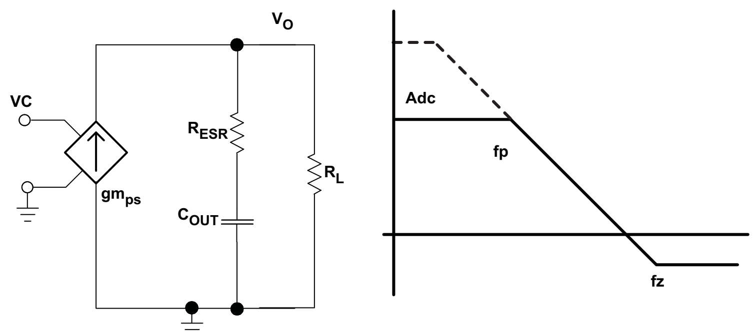


Figure 48. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

Small Signal Model for Frequency Compensation

The TPS54060A uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 49. Type 2 circuits most likely implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors.. Equation 18 and Equation 19 show how to relate the frequency response of the amplifier to the small signal model in Figure 49. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 49. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

DETAILED DESCRIPTION (continued)

Equation 18 through Equation 27 are provided as a reference for those who prefer to compensate using the preferred methods. Those who prefer to use prescribed method use the method outlined in the application section or use switched information.

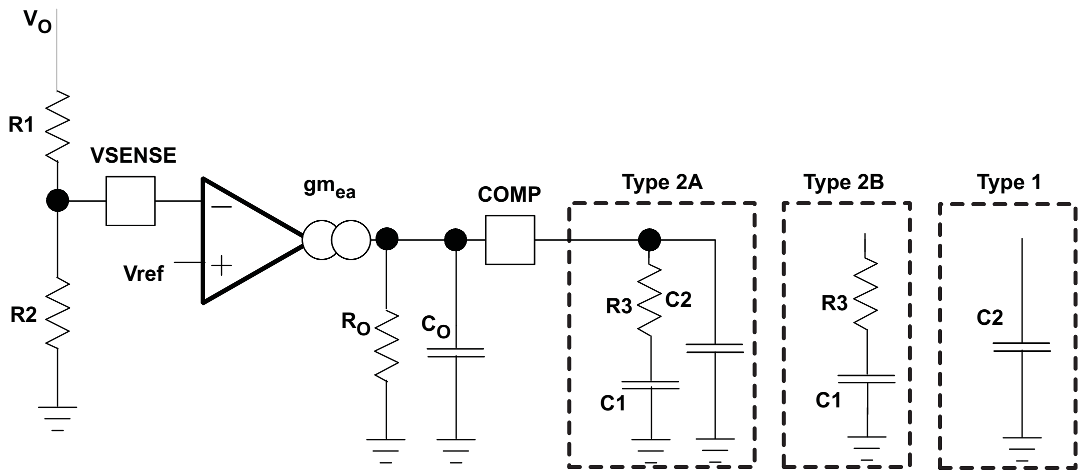


Figure 49. Types of Frequency Compensation

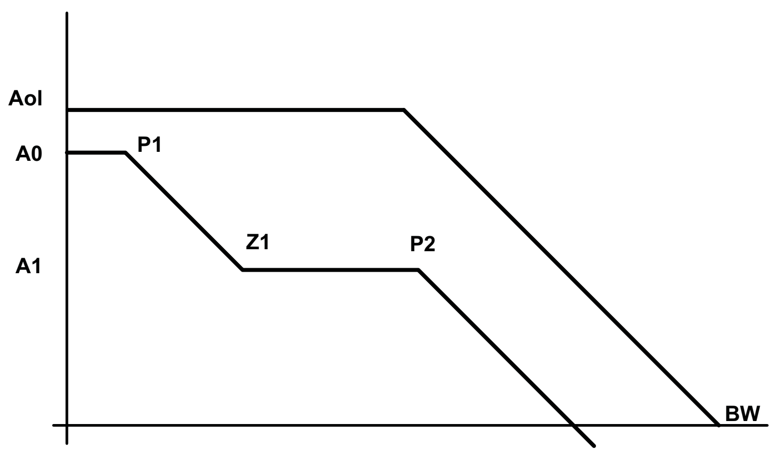


Figure 50. Frequency Response of the Type 2A and Type 2B Frequency Compensation

DETAILED DESCRIPTION (continued)

$$Ro = \frac{Aol(V/V)}{gm_{ea}} \tag{18}$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \tag{19}$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \tag{20}$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \tag{21}$$

$$A1 = gm_{ea} \times Ro|\,|\,R3 \times \frac{R2}{R1 + R2} \tag{22}$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \tag{23}$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \tag{24}$$

$$P2 = \frac{1}{2\pi \times R3\,|\,|\,R_O \times (C2 + C_O)} \text{ type 2a} \tag{25}$$

$$P2 = \frac{1}{2\pi \times R3\,|\,|\,R_O \times C_O} \text{ type 2b} \tag{26}$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ type 1} \tag{27}$$

APPLICATION INFORMATION

Design Guide — Step-By-Step Design Procedure

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	3.3 V
Transient Response 0 to 0.5A load step	ΔVout = 4%
Maximum Output Current	0.5 A
Input Voltage	34 V nom. 12V to 48 V
Output Voltage Ripple	1% of Vout
Start Input Voltage (rising VIN)	8.9 V
Stop Input Voltage (falling VIN)	7.9 V

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation.

Equation 12 and Equation 13 must be used to find the maximum switching frequency for the regulator, choose the lower value of the two equations. Switching frequencies higher than these values will result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 130 ns for the TPS54060A. For this example, the output voltage is 3.3 V and the maximum input voltage is 48 V, which allows for a maximum switch frequency up to 616 kHz when including the inductor resistance, on resistance and diode voltage in Equation 12. To ensure overcurrent runaway is not a concern during short circuits in your design use Equation 13 or the solid curve in Figure 42 to determine the maximum switching frequency. With a maximum input voltage of 48 V, assuming a diode voltage of 0.5 V, inductor resistance of 130mΩ, switch resistance of 400mΩ, a current limit value of 0.94 A and a short circuit output voltage of 0.1V. The maximum switching frequency is approximately 923 kHz.

Choosing the lower of the two values and adding some margin a switching frequency of 500kHz is used. To determine the timing resistance for a given switching frequency, use Equation 11 or the curve in Figure 40.

The switching frequency is set by resistor R_3 shown in Figure 51.

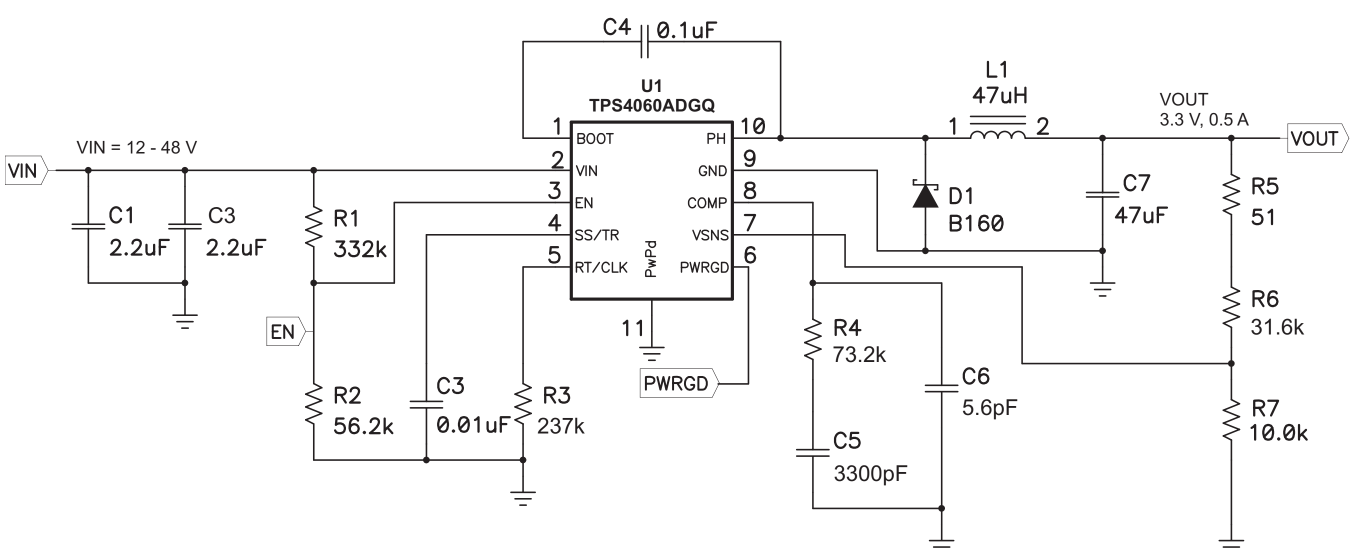


Figure 51. High Frequency, 3.3V Output Power Supply Design with Adjusted UVLO.

Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 28.

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Since the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 30 mA for dependable operation. In a wide input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated to be 39.7 μH. For this design, a nearest standard value was chosen: 47μH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 30 and Equation 31.

For this design, the RMS inductor current is 0.501 A and the peak inductor current is 0.563 A. The chosen inductor is a MSS1048-473ML. It has a saturation current rating of 1.44 A and an RMS current rating of 1.83A.

As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$Lo\ min = \frac{Vinmax - Vout}{Io \times K_{IND}} \times \frac{Vout}{Vinmax \times fsw} \tag{28}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (Vinmax - V_{OUT})}{Vinmax \times L_O \times f_{SW}} \tag{29}$$

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (Vinmax - V_{OUT})}{Vinmax \times L_O \times f_{SW}}\right)^2} \tag{30}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{31}$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulators responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also will temporarily not be able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 32 shows the minimum output capacitance necessary to accomplish this.

Where ΔIout is the change in output current, $f$sw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in Vout for a load step from 0A (no load) to 0.5 A (full load). For this example, ΔIout = 0.5-0 = 0.5 A and ΔVout = 0.04 × 3.3 = 0.132 V. Using these numbers gives a minimum capacitance of 15.2μF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The catch diode of the regulator can not sink current so any stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases, see Figure 52. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 33 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, VF is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 0.5 A to 0 A. The output voltage will increase during this load transition and the stated maximum in our specification is 4% of the output voltage. This will make Vf = 1.04 × 3.3 = 3.432. Vi is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 33 yields a minimum capacitance of 13.2μF.

Equation 34 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. Equation 34 yields 1μF.

Equation 35 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 35 indicates the ESR should be less than 248mΩ.

The most stringent criteria for the output capacitor is 15.2μF of capacitance to keep the output voltage in regulation during an load transient.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, a 47 μF 10V X5R ceramic capacitor with 5 mΩ of ESR will be used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 36 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 36 yields 37.7 mA.

$$\text{Cout} > \frac{2 \times \Delta\text{Iout}}{f\text{sw} \times \Delta\text{Vout}} \tag{32}$$

$$\text{Cout} > \text{Lo} \times \frac{\left(\text{Ioh}^2 - \text{Iol}^2\right)}{\left(\text{V}f^2 - \text{Vi}^2\right)} \tag{33}$$

$$\text{Cout} > \frac{1}{8 \times f\text{sw}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \tag{34}$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \tag{35}$$

$$\text{Icorms} = \frac{\text{Vout} \times (\text{Vin max} - \text{Vout})}{\sqrt{12} \times \text{Vin max} \times \text{Lo} \times f\text{sw}} \tag{36}$$

Catch Diode

The TPS54060A requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than Vinmax. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage will be. Since the design example has an input voltage up to 48V, a diode with a minimum of 60V reverse voltage will be selected.

For the example design, the B160A Schottky diode is selected for its lower forward voltage and it comes in a larger package size which has good thermal characteristics over small devices. The typical forward voltage of the B160A is 0.50 volts.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode which equals the conduction losses of the diode. At higher switch frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Equation 37 is used to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B160A has a junction capacitance of 110pF. Using Equation 37, the selected diode will dissipate 0.297 Watts. This power dissipation, depending on mounting techniques, should produce a 5.9°C temperature rise in the diode when the input voltage is 48V and the load current is 0.5A.

If the power supply spends a significant amount of time at light load currents or in sleep mode consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$\text{Pd} = \frac{(\text{Vin max} - \text{Vout}) \times \text{Iout} \times \text{V}f\text{d}}{\text{Vin max}} + \frac{\text{Cj} \times f\text{sw} \times (\text{Vin} + \text{V}f\text{d})^2}{2} \tag{37}$$

Input Capacitor

The TPS54060A requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3 μF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54060A. The input ripple current can be calculated using Equation 38.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 60V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4V, 6.3V, 10V, 16V, 25V, 50V or 100V so a 100V capacitor should be selected. For this example, two 2.2μF, 100V capacitors in parallel have been selected. Table 1 shows a selection of high voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 39. Using the design example values, Ioutmax = 0.5 A, Cin = 4.4μF, $f$sw = 500 kHz, yields an input voltage ripple of 57 mV and a rms input ripple current of 0.223A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vin min}} \times \frac{(\text{Vin min} - \text{Vout})}{\text{Vin min}}} \quad (38)$$

$$\Delta\text{Vin} = \frac{\text{Iout max} \times 0.25}{\text{Cin} \times f\text{sw}} \quad (39)$$

Table 1. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE	DIALECTRIC	COMMENTS
Murata	1.0 to 2.2	1210	100 V	X7R	GRM32 series
	1.0 to 4.7		50 V		
	1.0	1206	100 V		GRM31 series
	1.0 to 2.2		50 V		
Vishay	1.0 10 1.8	2220	50 V		VJ X7R series
	1.0 to 1.2		100 V		
	1.0 to 3.9	2225	50 V		
	1.0 to 1.8		100 V		
TDK	1.0 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1.0. to 2.2	1210	100 V		C series C3225
	1.0 to 3.3		50 V		
AVX	1.0 to 4.7	1210	50 V		X7R dielectric series
	1.0		100 V		
	1.0 to 4.7	1812	50 V		
	1.0 to 2.2		100 V		

Slow Start Capacitor

The slow start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54060A reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 40 can be used to find the minimum slow start time, tss, necessary to charge the output capacitor, Cout, from 10% to 90% of the output voltage, Vout, with an average slow start current of Issavg. In the example, to charge the 47μF output capacitor up to 3.3V while only allowing the average input current to be 0.125A would require a 1 ms slow start time.

Once the slow start time is known, the slow start capacitor value can be calculated using Equation 6. For the example circuit, the slow start time is not too critical since the output capacitor value is 47μF which does not require much current to charge to 3.3V. The example circuit has the slow start time set to an arbitrary value of 3.2ms which requires a 0.01 μF capacitor.

$$\text{Tss} > \frac{\text{Cout} \times \text{Vout} \times 0.8}{\text{Issavg}} \quad (40)$$

Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10V or higher voltage rating.

Under Voltage Lock Out Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54060A. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 8.9V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 7.9V (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, a 332kΩ between Vin and EN and a 56.2kΩ between EN and ground are required to produce the 8.9 and 7.9 volt start and stop voltages.

Output Voltage and Feedback Resistors Selection

For the example design, 10.0 kΩ was selected for R2. Using Equation 1, R1 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 μA in order to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 kΩ. Choosing higher resistor values will decrease quiescent current and improve efficiency at low output currents but may introduce noise immunity problems.

Compensation

There are several methods used to compensate DC/DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the cross over frequency used in the calculations. This method assume the crossover frequency is between the modulator pole and the esr zero and the esr zero is at least 10 times greater the modulator pole. Use SwitcherPro software for a more accurate design.

To get started, the modulator pole, fpmod, and the esr zero, fz1 must be calculated using Equation 41 and Equation 42. For Cout, use a derated value of 40 μf. Use equations Equation 43 and Equation 44, to estimate a starting point for the crossover frequency, fco, to design the compensation. For the example design, fpmod is 603 Hz and fzmod is 796 kHz. Equation 43 is the geometric mean of the modulator pole and the esr zero and Equation 44 is the mean of modulator pole and the switching frequency. Equation 43 yields 21.9 kHz and Equation 44 gives 12.3 kHz. Use the lower value of Equation 43 or Equation 44 for an initial crossover frequency. For this example, fco is 12.3kHz. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f\text{p mod} = \frac{\text{Ioutmax}}{2 \times \pi \times \text{Vout} \times \text{Cout}} \tag{41}$$

$$f\text{z mod} = \frac{1}{2 \times \pi \times \text{Resr} \times \text{Cout}} \tag{42}$$

$$f_{\text{co}} = \sqrt{f_p\text{mod} \times f_z\text{mod}} \tag{43}$$

$$f_{\text{co}} = \sqrt{f_p\text{mod} \times \frac{f_{sw}}{2}} \tag{44}$$

To determine the compensation resistor, R4, use Equation 45. Assume the power stage transconductance, gmps, is 1.9A/V. The output voltage, Vo, reference voltage, VREF, and amplifier transconductance, gmea, are 3.3V, 0.8V and 97μA/V, respectively. R4 is calculated to be 72.6 kΩ, use the nearest standard value of 73.2kΩ. Use Equation 46 to set the compensation zero to the modulator pole frequency. Equation 46 yields 3600pF for compensating capacitor C7, a 3300pF is used on the board.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{out}}{gmps}\right) \times \left(\frac{V_{out}}{V_{ref} \times gmea}\right) \quad (45)$$

$$C7 = \frac{1}{2 \times \pi \times R4 \times f_{p}\ \text{mod}} \quad (46)$$

Use the larger value of Equation 47 and Equation 48 to calculate the C8, to set the compensation pole. Equation 48 yields 8.7pF so the nearest standard of 10pF is used.

$$C8 = \frac{C_o \times Resr}{R4} \quad (47)$$

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} \quad (48)$$

Discontinuous Mode and Eco-mode Boundary

With an input voltage of 34V, the power supply enters discontinuous mode when the output current is less than 60mA. The power supply enters EcoMode when the output current is lower than 38mA.

The input current draw at no load is 228μA.

APPLICATION CURVES

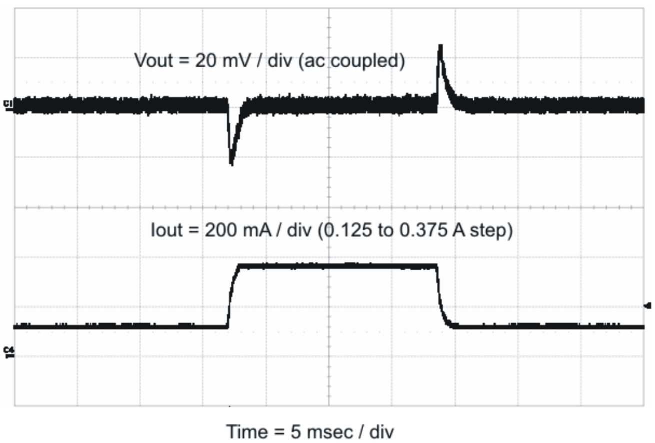


Figure 52. Load Transient

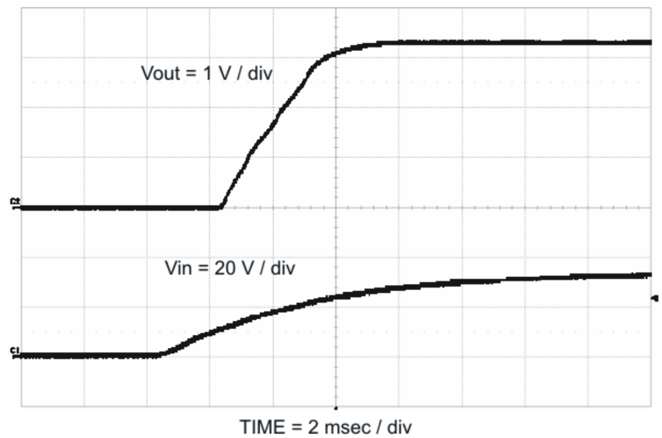


Figure 53. Startup With VIN

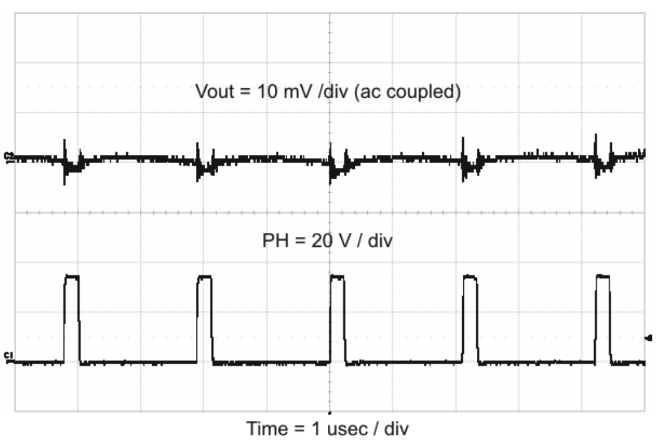


Figure 54. Output Ripple CCM

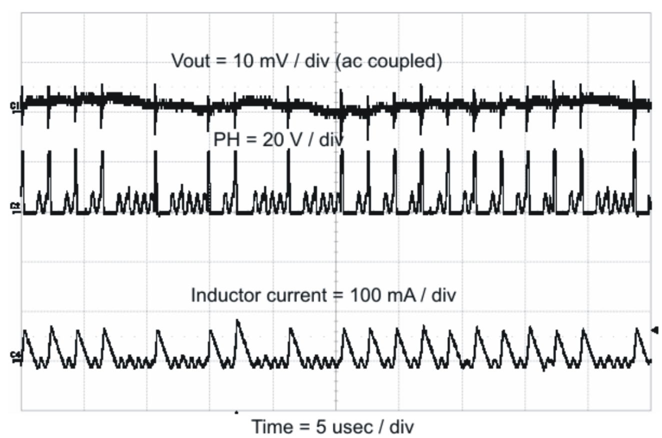


Figure 55. Output Ripple, DCM

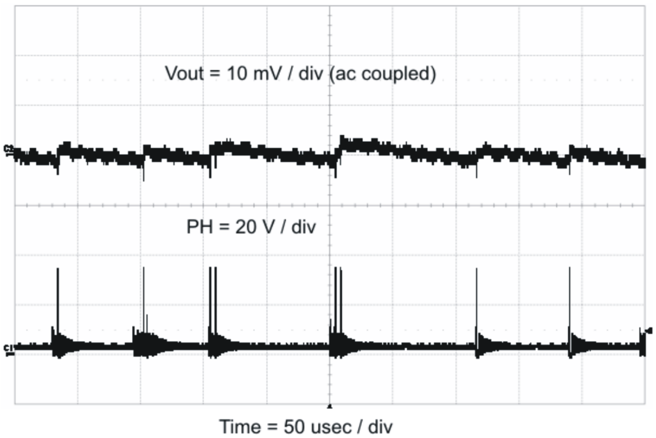


Figure 56. Output Ripple, PSM

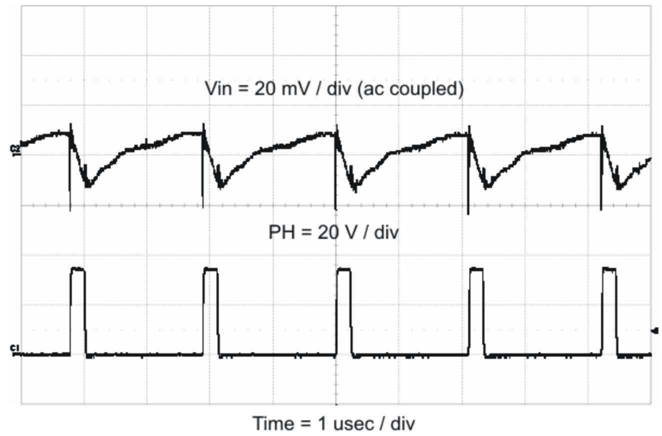


Figure 57. Input Ripple CCM

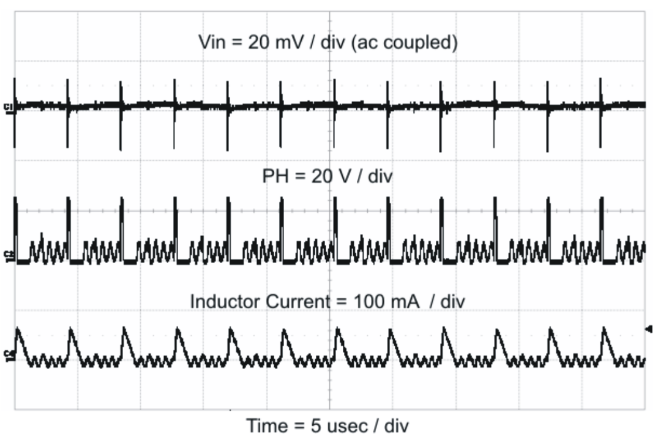


Figure 58. Input Ripple DCM

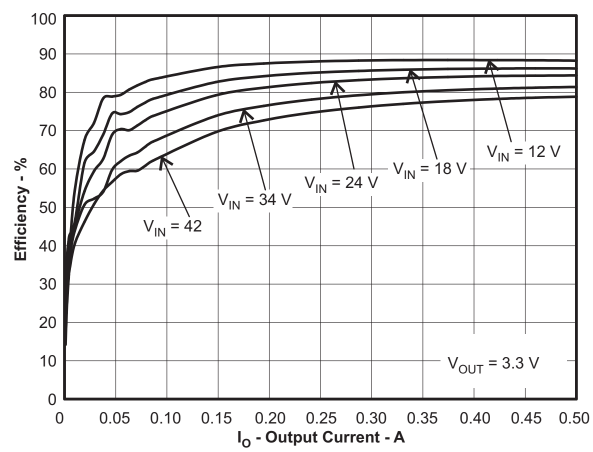


Figure 59. Efficiency vs Load Current

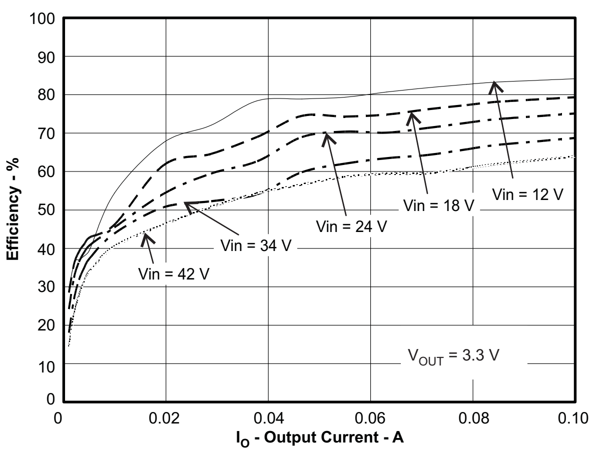


Figure 60. Light Load Efficiency

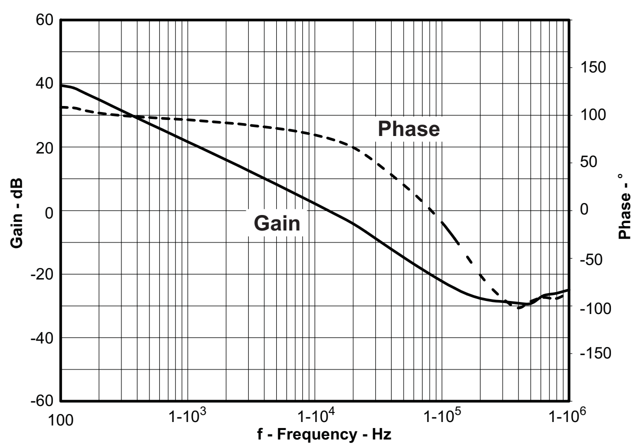


Figure 61. Overall Loop Frequency Response

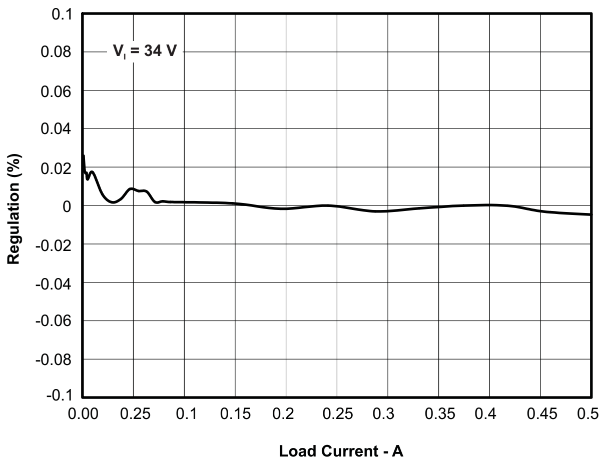


Figure 62. Regulation vs Load Current

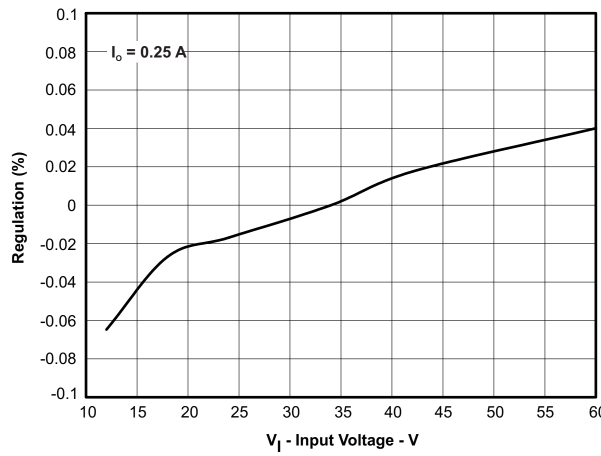


Figure 63. Regulation vs Input Voltage

Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is working in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (Pcon), switching loss (Psw), gate drive loss (Pgd) and supply current (Pq).

$$Pcon = Io^2 \times R_{DS(on)} \times \frac{Vout}{Vin} \tag{49}$$

$$Psw = Vin^2 \times f sw \times Io \times 0.25 \times 10^{-9} \tag{50}$$

$$Pgd = Vin \times 3 \times 10^{-9} \times f sw \tag{51}$$

$$Pq = 116 \times 10^{-6} \times Vin \tag{52}$$

Where:

Io is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
VOUT is the output voltage (V).
VIN is the input voltage (V).
fsw is the switching frequency (Hz).

So

$$Ptot = Pcon + Psw + Pgd + Pq \tag{53}$$

For given T_A,

$$TJ = TA + Rth \times Ptot \tag{54}$$

For given T_{JMAX} = 150°C

$$TAmax = TJmax - Rth \times Ptot \tag{55}$$

Where:

Ptot is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
Rth is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There will be additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and trace resistance that will impact the overall efficiency of the regulator.

Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 64 for a PCB layout example. The GND pin should be tied directly to the power pad under the IC and the power pad.

The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

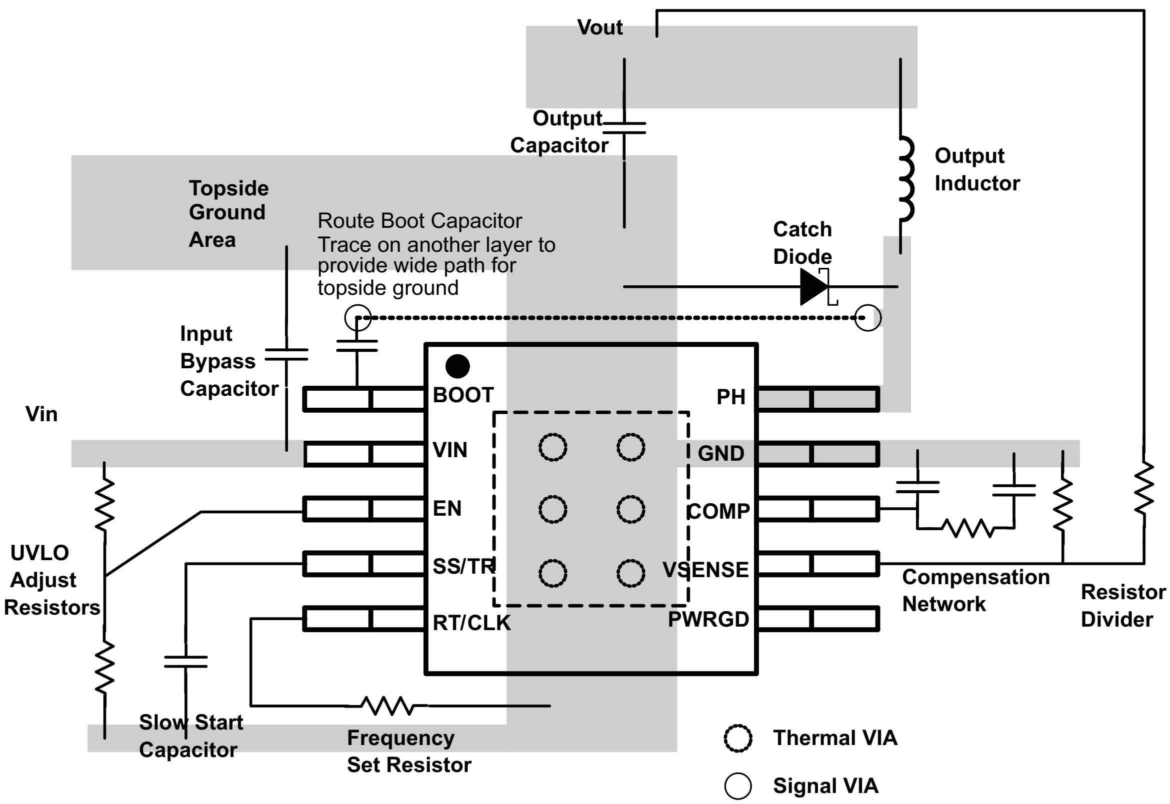


Figure 64. PCB Layout Example

Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 51 is 0.55 in^2. This area does not include test points or connectors.

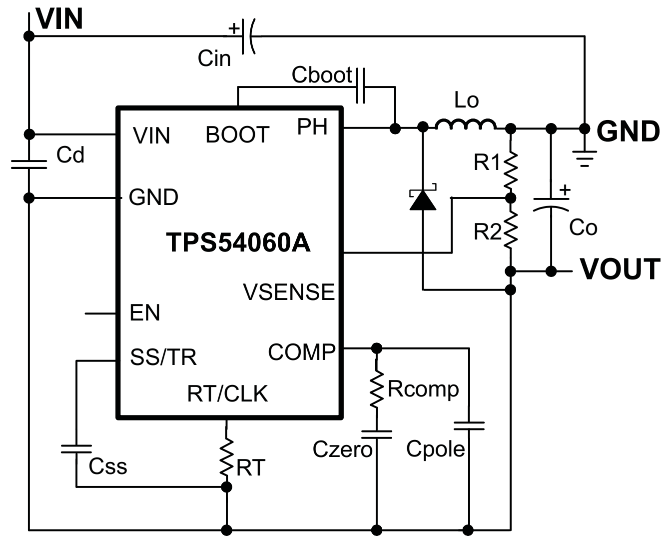


Figure 65. Inverting Power Supply from the SLVA317 Application Note

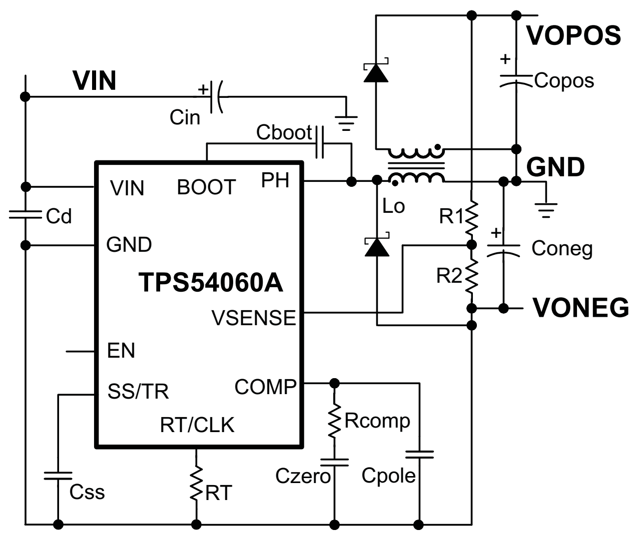


Figure 66. Split Rail Power Supply Based on the SLVA369 Application Note

REVISION HISTORY

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54060ADGQ	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5406A
TPS54060ADGQR	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5406A
TPS54060ADRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5406A
TPS54060ADRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5406A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

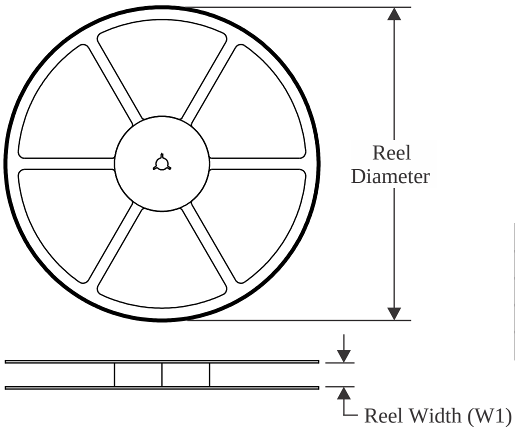
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

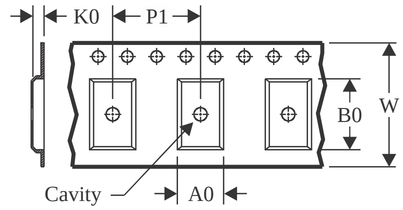
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

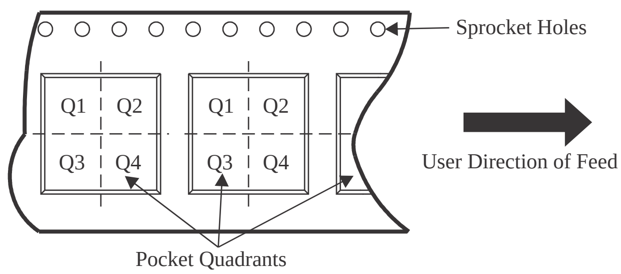
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





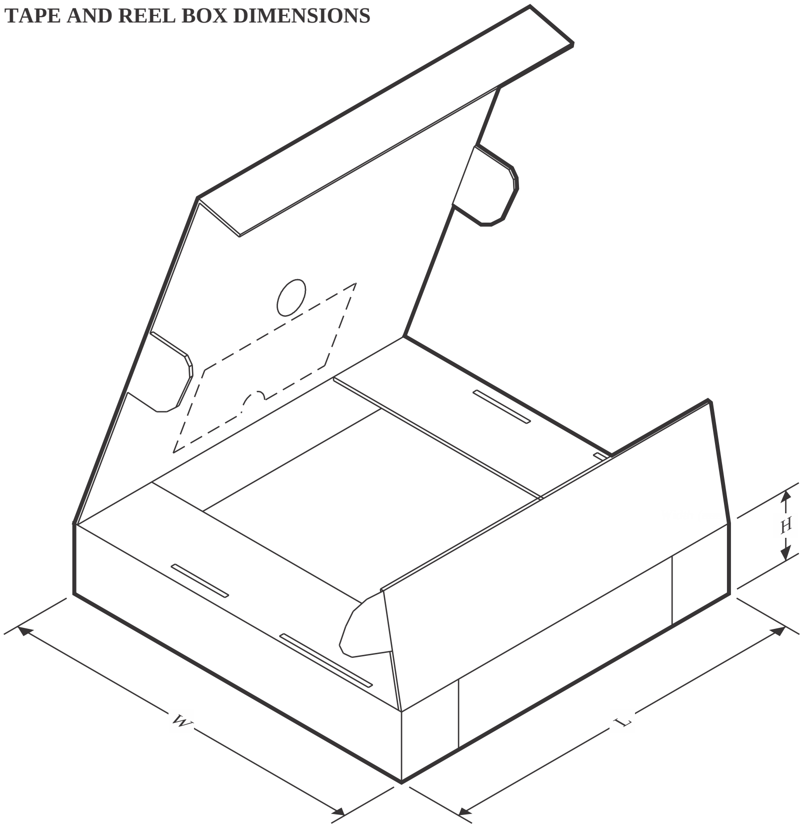
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54060ADGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TPS54060ADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54060ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54060ADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

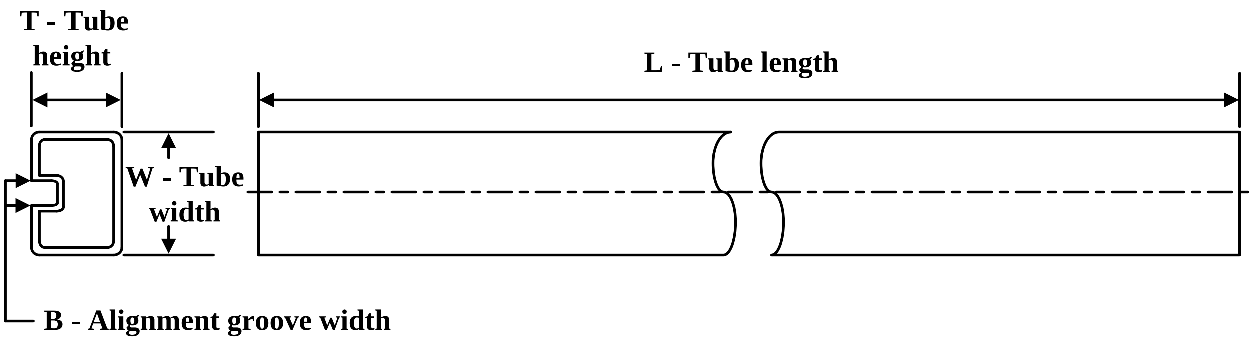
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54060ADGQR	HVSSOP	DGQ	10	2500	366.0	364.0	50.0
TPS54060ADRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS54060ADRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS54060ADRCT	VSON	DRC	10	250	200.0	183.0	25.0

TUBE



*All dimensions are nominal

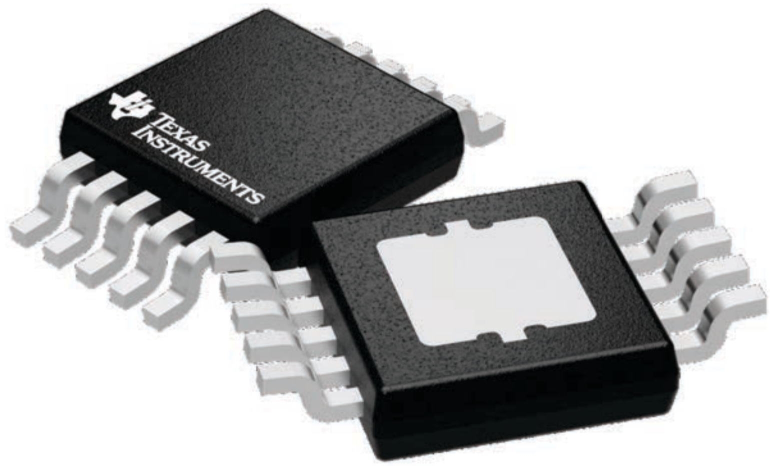
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54060ADGQ	DGQ	HVSSOP	10	80	322	6.55	1000	3.01

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

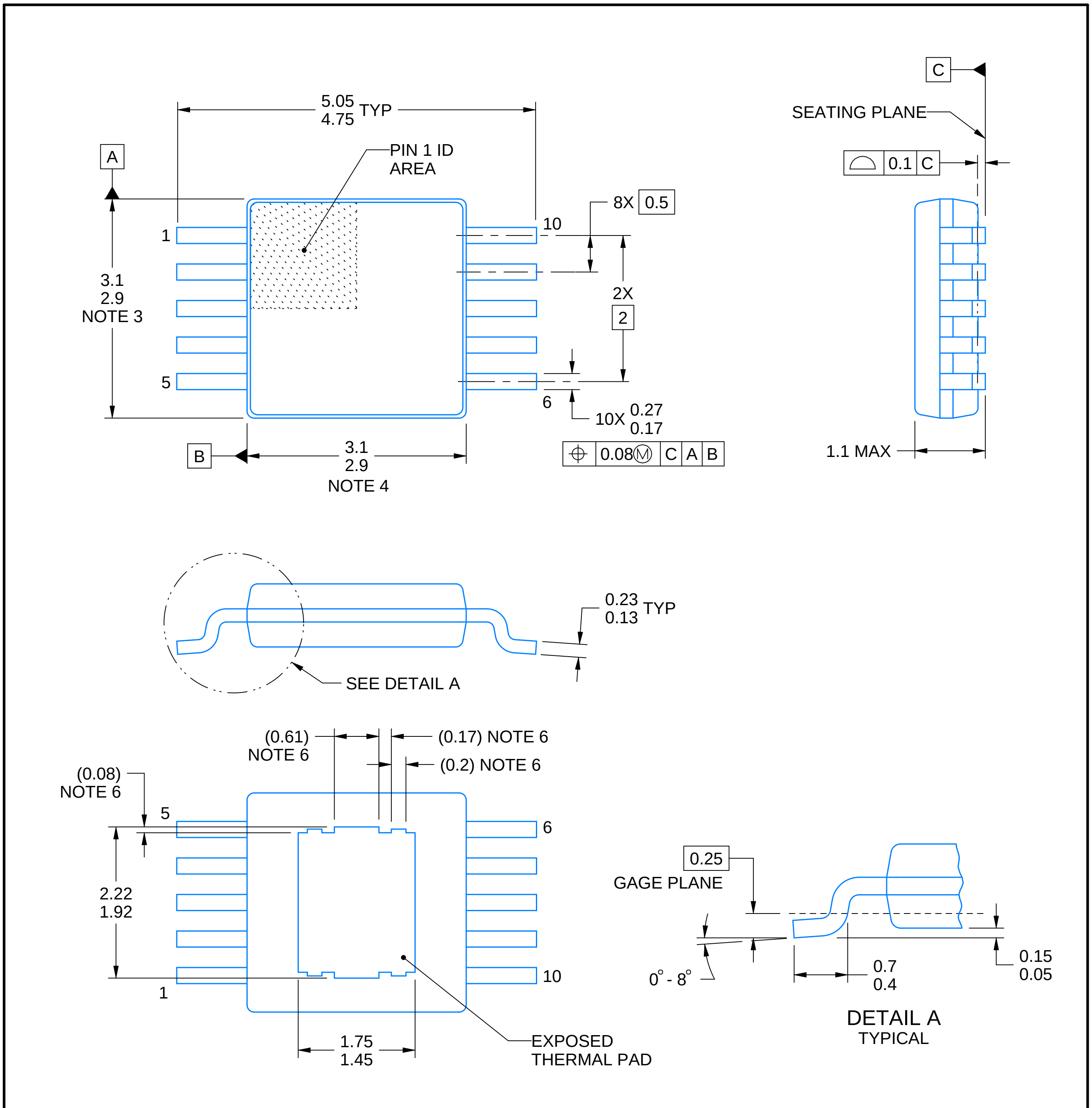
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224775/A

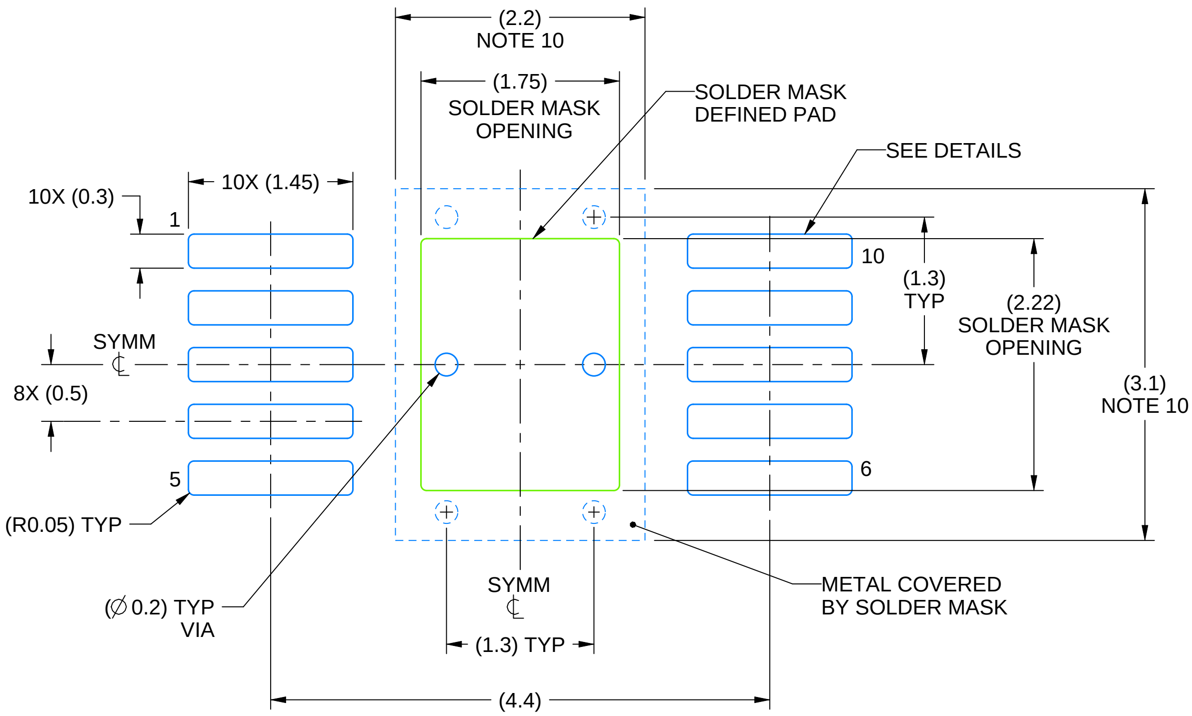


4226735/C 04/2024

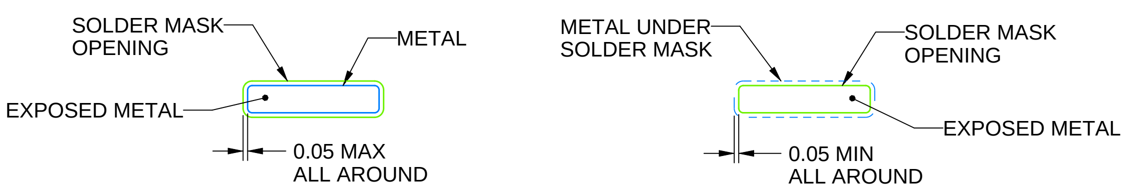
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

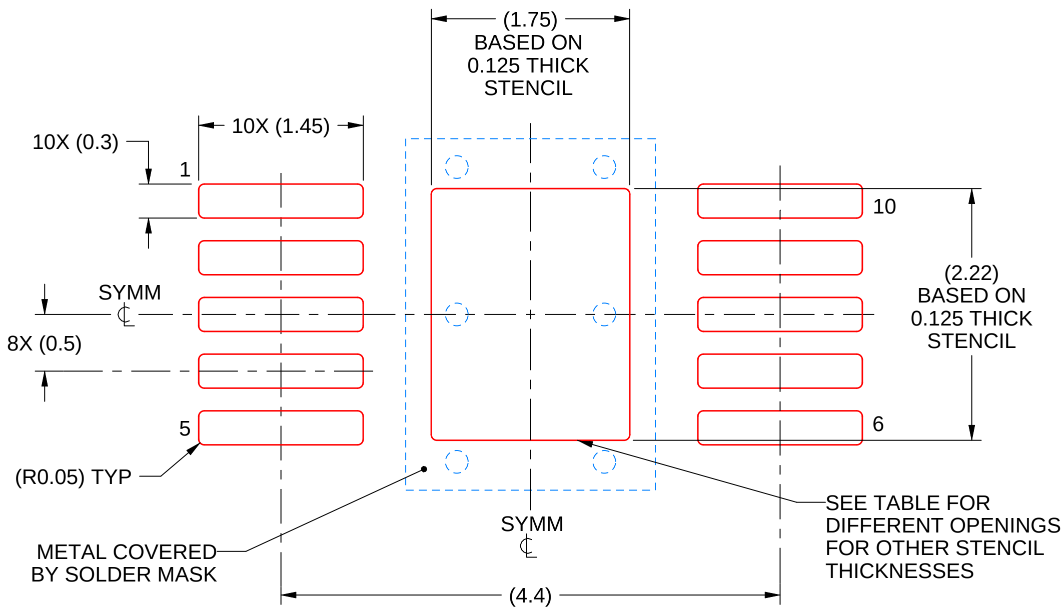
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226735/C 04/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.



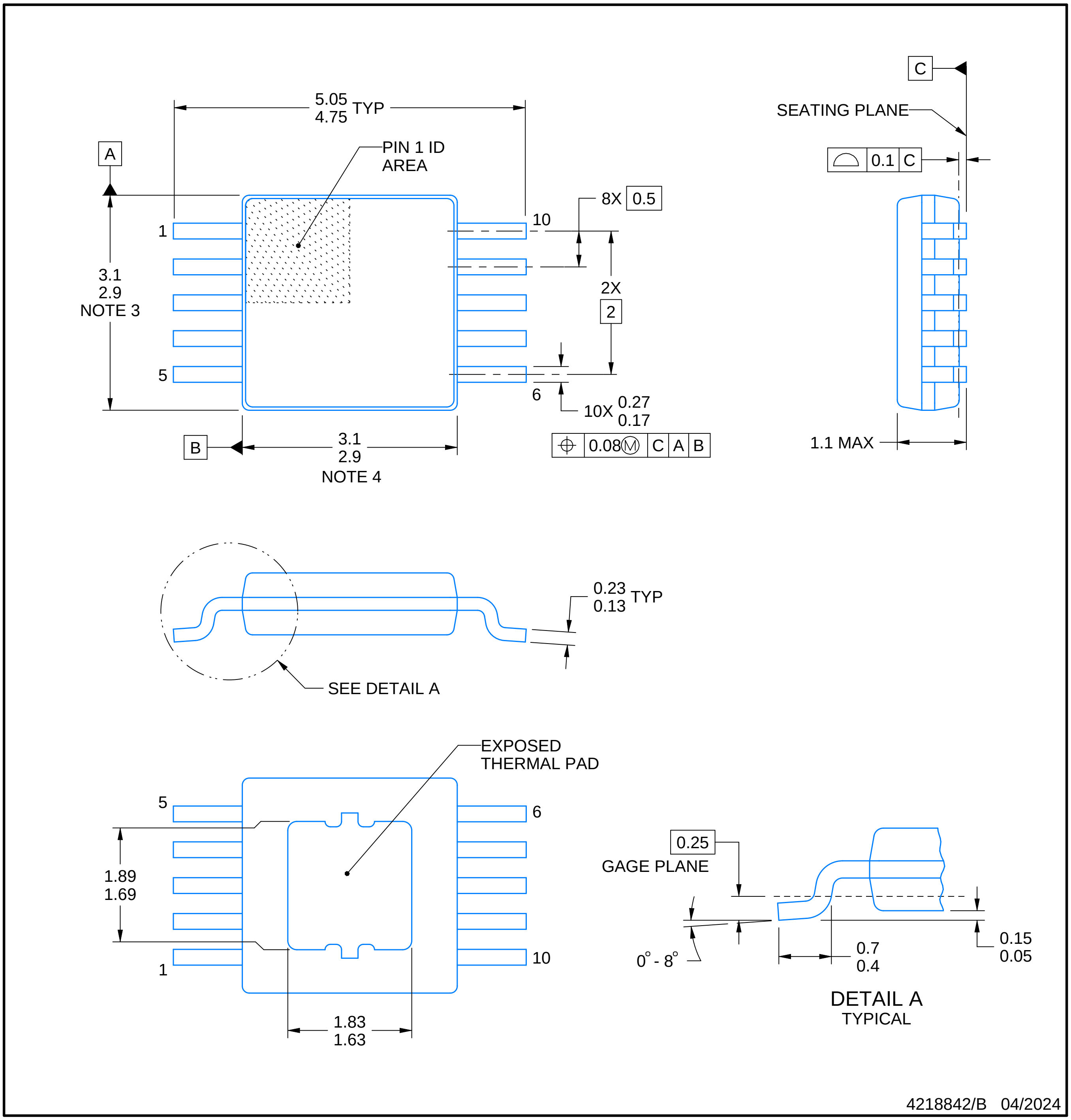
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.96 X 2.48
0.125	1.75 X 2.22 (SHOWN)
0.150	1.6 X 2.03
0.175	1.48 X 1.88

4226735/C 04/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

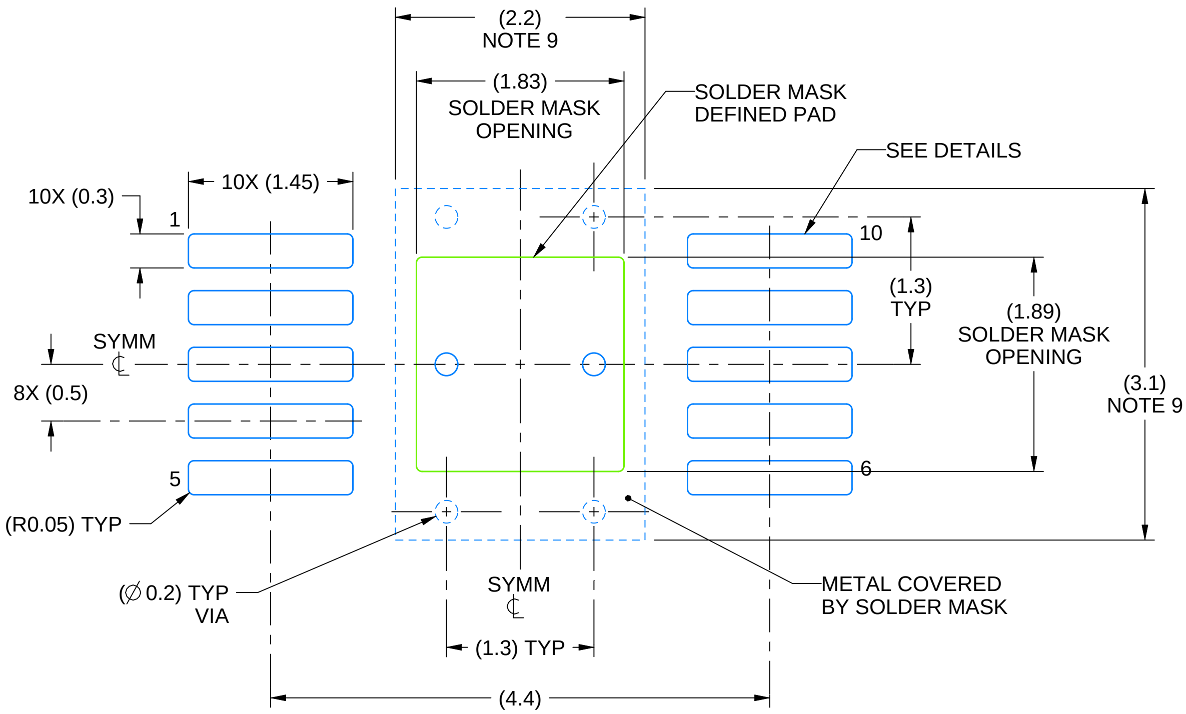


4218842/B 04/2024

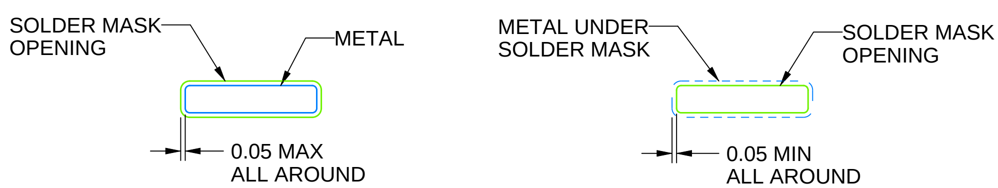
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK DEFINED

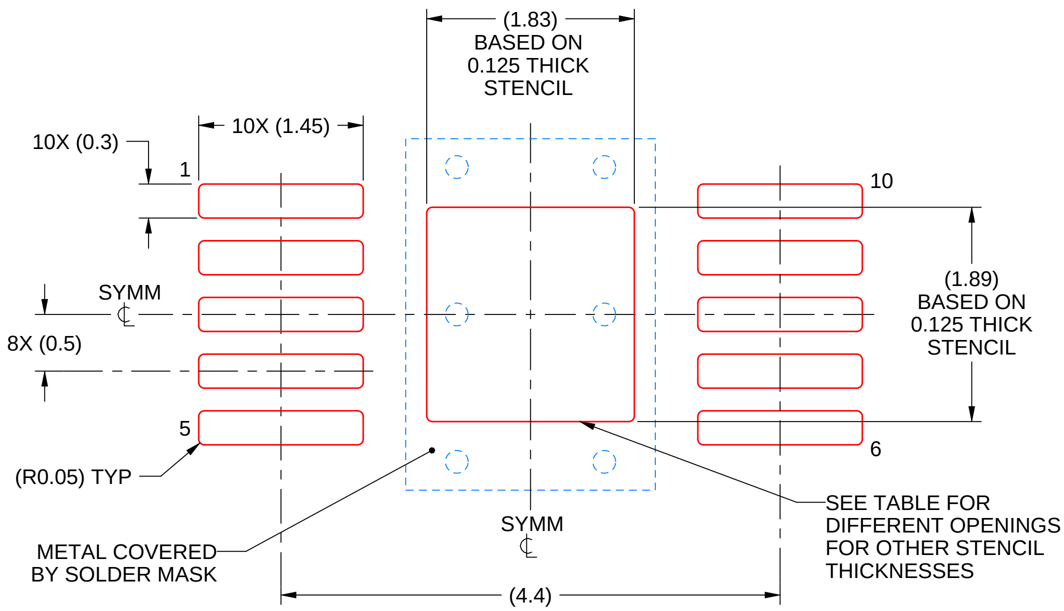
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218842/B 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

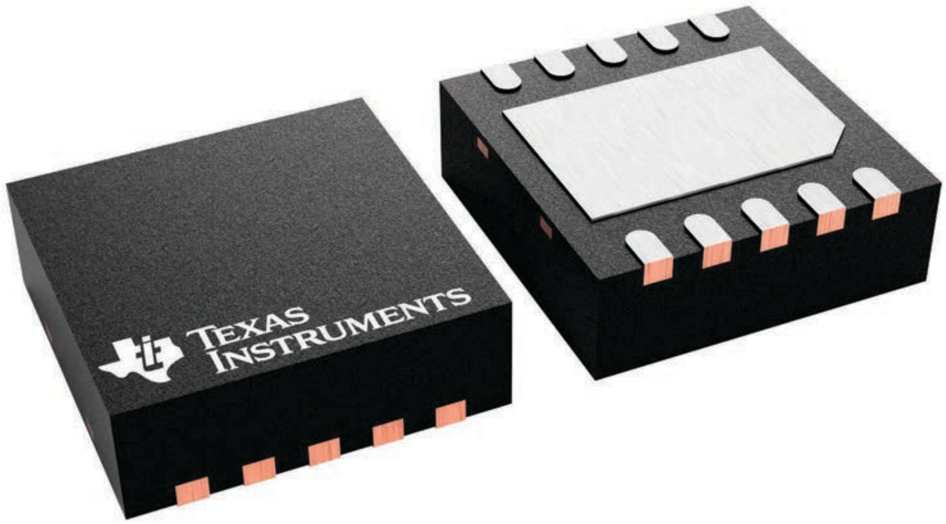
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

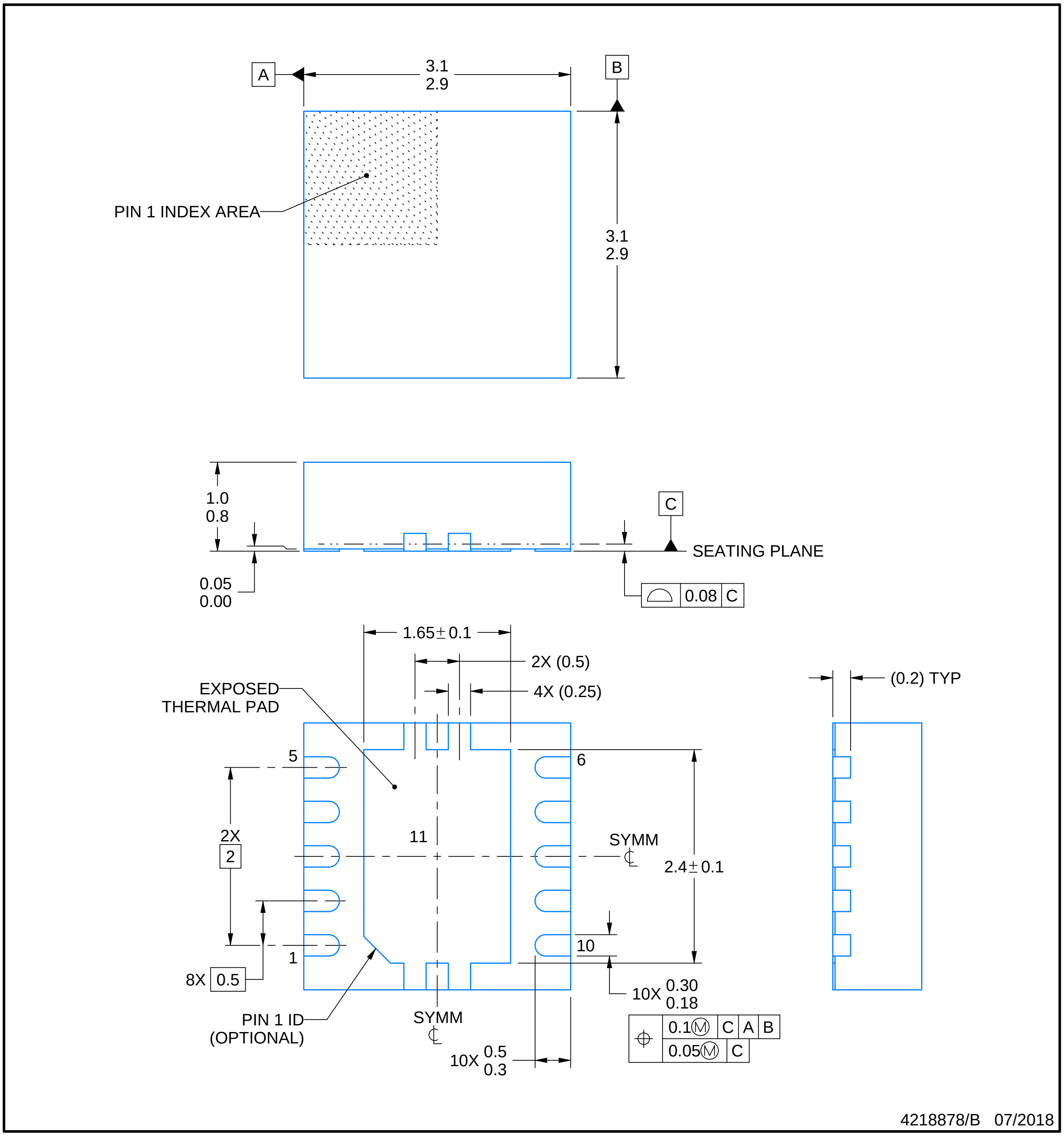
4218842/B 04/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

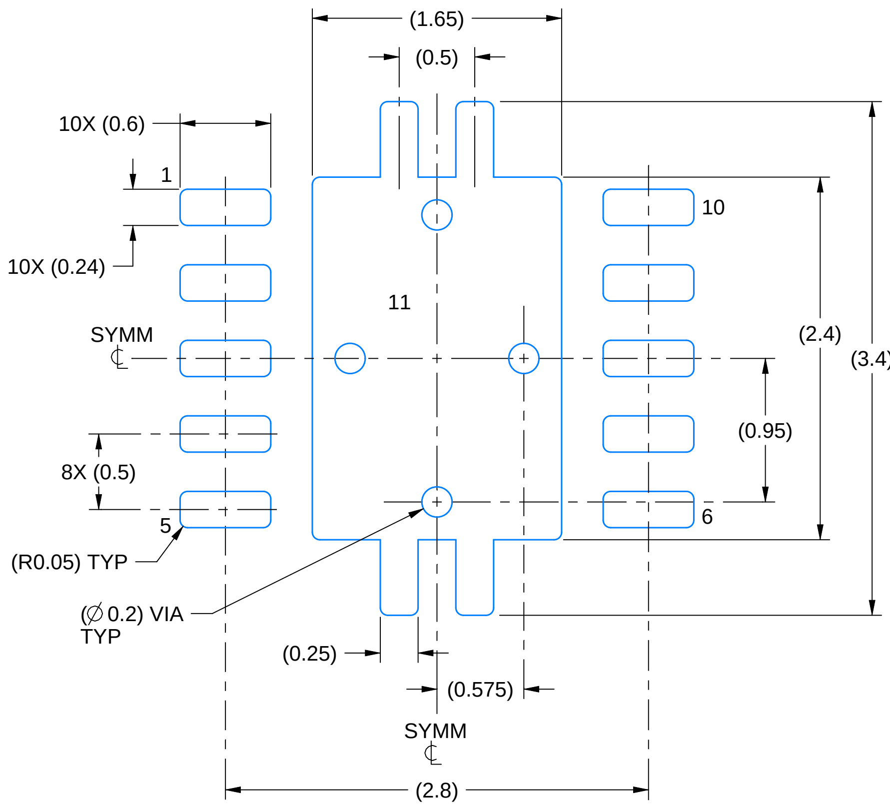
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



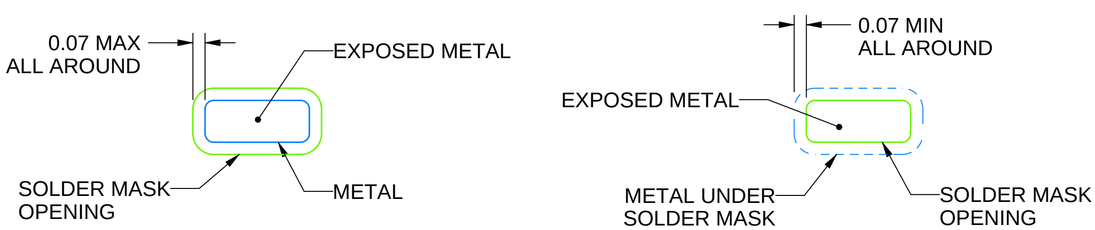


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

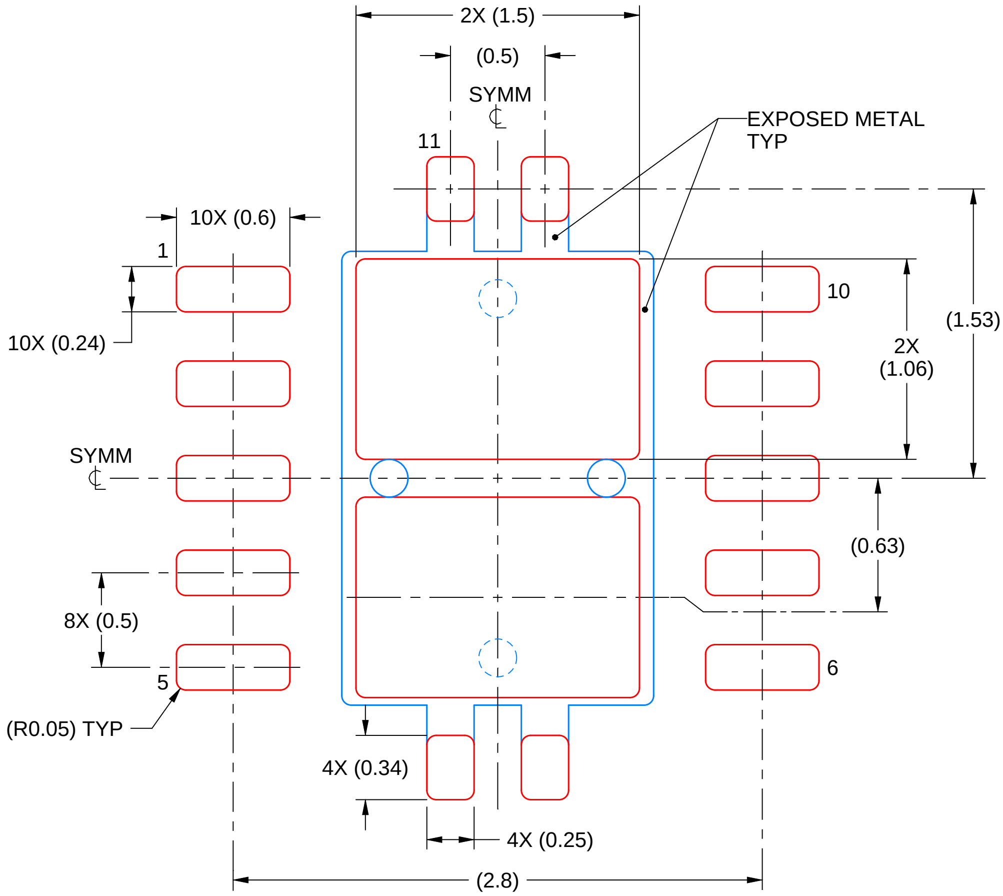
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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