TPS2041B, TPS2042B, TPS2043B, TPS2044B
TPS2051B, TPS2052B, TPS2053B, TPS2054B
ZHCSSK0P – APRIL 2004 – REVISED AUGUST 2024

TPS20xxB 限流、配电开关

1 特性

- 70mΩ 高侧 MOSFET
- 500mA 持续电流
- 过热和短路保护
- 精确电流限制
  （最小值 0.75A，最大值 1.25A）
- 工作电压范围：2.7V 至 5.5V
- 0.6ms 典型上升时间
- 欠压锁定
- 抗尖峰脉冲故障报告 ($\overline{OC}$)
- 上电期间无 $\overline{OC}$ 尖峰脉冲
- 最大待机电源电流：
  1μA（单、双通道）或 2μA（三、四通道）
- 环境温度范围：-40°C 至 85°C
- 通过 UL 认证，文件编号 E169910
- 针对成组配置的 TPS2042B 和 TPS2052B 的其他 UL 认证

2 应用

- 大电容负载
- 短路保护

3 说明

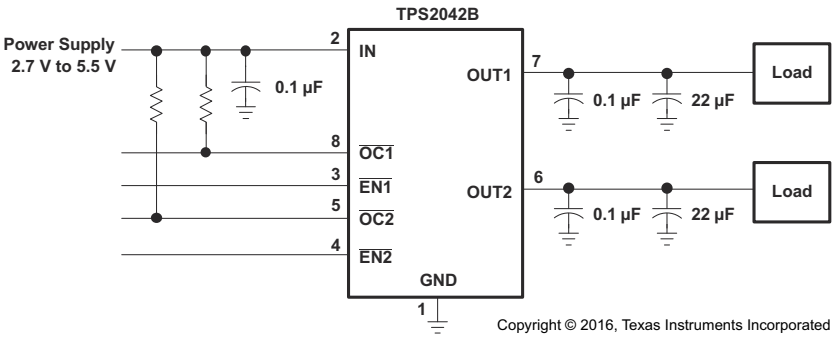
TPS20xxB 配电开关适用于可能具有高容性负载和发生短路的应用。此系列器件包含 70mΩ N 沟道 MOSFET 电源开关，适用于需要在单个封装内包含多个电源开关的配电系统。每个开关由一个逻辑使能输入控制。栅极驱动由一个内部电荷泵提供，此电荷泵设计用于控制电源开关上升时间和下降时间以大大减少切换期间的电流涌入。电荷泵无需外部组件并可在低至 2.7V 的电源电压下工作。

当输出负载超过限流阈值或者短路出现时，该器件通过切换至恒定电流模式，并通过将过流 ($\overline{OCx}$) 下拉至逻辑输出低电平来将输出电流限制在安全水平上。如果持续重过载和短路增加了开关内的功率耗散，则将引起结温上升，此时，过热保护电路将关闭此开关以避免器件损坏。一旦器件充分冷却，此器件将自动从热关断中恢复。内部电路确保此开关在有效输入电压出现前保持关闭状态。此配电开关旨在将电流限制设置为 1A（典型值）。

器件信息

器件型号	封装(1)	本体尺寸（标称值）
TPS20xxB	SOIC (8)	4.90mm × 3.91mm
	SOIC (16)	9.90mm × 3.91mm
	SOT-23 (5)	2.90mm × 1.60mm
	HVSSOP (8)	3.00mm × 3.00mm
	SON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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典型应用原理图

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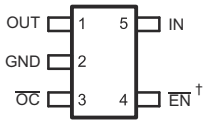
4 General Switch Catalog

GENERAL SWITCH CATALOG

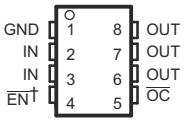
33 mΩ, Single		80 mΩ, Single		80 mΩ, Dual		80 mΩ, Dual		80 mΩ, Triple		80 mΩ, Quad		80 mΩ, Quad	
TPS201xA	0.2 A to 2 A	TPS2014	600 mA	TPS2042B	500 mA	TPS2080	500 mA	TPS2043B	500 mA	TPS2044B	500 mA	TPS2085	500 mA
TPS202x	0.2 A to 2 A	TPS2015	1 A	TPS2052B	500 mA	TPS2081	500 mA	TPS2053B	500 mA	TPS2054B	500 mA	TPS2086	500 mA
TPS203x	0.2 A to 2 A	TPS2041B	500 mA	TPS2046B	250 mA	TPS2082	500 mA	TPS2047B	250 mA	TPS2048A	250 mA	TPS2087	500 mA
		TPS2051B	500 mA	TPS2056	250 mA	TPS2090	250 mA	TPS2057A	250 mA	TPS2058	250 mA	TPS2095	250 mA
		TPS2045A	250 mA	TPS2062	1 A	TPS2091	250 mA	TPS2063	1 A			TPS2096	250 mA
		TPS2049	100 mA	TPS2066	1 A	TPS2092	250 mA	TPS2067	1 A			TPS2097	250 mA
		TPS2055A	250 mA	TPS2060	1.5 A								
		TPS2061	1 A	TPS2064	1.5 A								
		TPS2065	1 A										
		TPS2068	1.5 A										
		TPS2069	1.5 A										

5 Pin Configuration and Functions



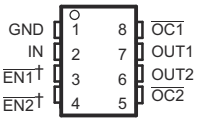
† All enable outputs are active high for the TPS205xB series.

图 5-1. TPS2041B and TPS2051B: DBV Package 5-Pin SOT-23 Top View



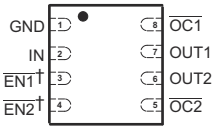
† All enable outputs are active high for the TPS205xB series.

图 5-2. TPS2041B and TPS2051B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View



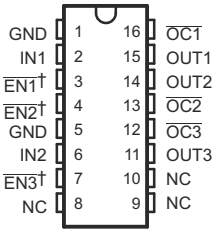
† All enable outputs are active high for the TPS205xB series.

图 5-3. TPS2042B and TPS2052B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View



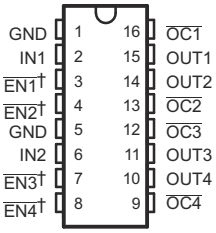
† All enable outputs are active high for the TPS205xB series.

图 5-4. TPS2042B and TPS2052B: DRB Package 8-Pin SON Top View



† All enable outputs are active high for the TPS205xB series.

图 5-5. TPS2043B and TPS2053B: D Package 16-Pin SOIC Top View



† All enable outputs are active high for the TPS205xB series.

图 5-6. TPS2044B and TPS2054B: D Package 16-Pin SOIC Top View

表 5-1. Pin Functions (TPS2041B and TPS2051B)

NAME	PIN				I/O	DESCRIPTION
	TPS2041B	TPS2051B	TPS2041B	TPS2051B		
	SOIC AND DGN		SOT-23			
$\overline{EN}$	4	—	4	—	I	Enable input, logic low turns on power switch
EN	—	4	—	4	I	Enable input, logic high turns on power switch
GND	1	1	2	2	—	Ground
IN	2, 3	2, 3	5	5	I	Input voltage
$\overline{OC}$	5	5	3	3	O	Overcurrent open-drain output, active-low

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表 5-1. Pin Functions (TPS2041B and TPS2051B)（续）

PIN					I/O	DESCRIPTION
NAME	TPS2041B	TPS2051B	TPS2041B	TPS2051B		
	SOIC AND DGN		SOT-23			
OUT	6, 7, 8	6, 7, 8	1	1	O	Power-switch output

表 5-2. Pin Functions (TPS2042B and TPS2052B)

PIN			I/O	DESCRIPTION
NAME	TPS2042B	TPS2052B		
	SOIC, HVSSOP, SON			
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN-OUT2
EN1	—	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1	—	Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
PowerPAD™	—	—	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Must be connected to GND pin.

表 5-3. Pin Functions (TPS2043B and TPS2053B)

PIN			I/O	DESCRIPTION
NAME	TPS2043B	TPS2053B		
	SOIC	SOIC		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	—	I	Enable input, logic low turns on power switch IN2-OUT3
EN1	—	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	—	7	I	Enable input, logic high turns on power switch IN2-OUT3
GND	1, 5	1, 5	—	Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3
NC	8, 9, 10	8, 9, 10	—	No connection
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

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表 5-4. Pin Functions (TPS2044B and TPS2054B)

PIN			I/O	DESCRIPTION
NAME	TPS2044B	TPS2054B		
	SOIC	SOIC		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	—	I	Enable input, logic low turns on power switch IN2-OUT3
$\overline{EN4}$	8	—	I	Enable input, logic low turns on power switch IN2-OUT4
EN1	—	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	—	7	I	Enable input, logic high turns on power switch IN2-OUT3
EN4	—	8	I	Enable input, logic high turns on power switch IN2-OUT4
GND	1, 5	1, 5	—	Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3 and OUT4
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent, open-drain output, active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{I(IN)}$, $V_{I(INx)}$	Input voltage (2)	–0.3	6	V
$V_{O(OUT)}$, $V_{O(OUTx)}$ (2)	Output voltage	–0.3	6	V
$V_{I(\overline{EN})}$, $V_{I(\overline{ENx})}$, $V_{I(EN)}$, $V_{I(ENx)}$	Input voltage	–0.3	6	V
$V_{I(/OC)}$, $V_{I(\overline{OCx})}$	Voltage range	–0.3	6	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current	Internally limited		
T_J	Operating virtual junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{I(IN)}$, $V_{I(INx)}$	Input voltage	2.7		5.5	V
$V_{I(\overline{EN})}$, $V_{I(\overline{ENx})}$, $V_{I(EN)}$, $V_{I(ENx)}$	Input voltage	0		5.5	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current	0		500	mA
T_J	Operating virtual junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)		DBV (SOT-23)	DGN (HVSSOP)	DRB (SON)	UNIT
		8 PINS	16 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.3	81.6	208.6	53.6	47.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	42.7	122.9	58.7	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	39.1	37.8	35.5	14.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.3	10.4	14.6	2.7	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.1	38.8	36.9	35.3	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	6.7	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 0.5 A, -40°C ≤ T_J ≤ 125°C		D and DGN packages		70	135	mΩ
				DBV package only		95	140	
	Static drain-source on-state resistance, 2.7-V operation	$V_{I(IN)}$ = 2.7 V, I_O = 0.5 A, –40°C ≤ T_J ≤ 125°C		D and DGN packages		75	150	mΩ
	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, I_O = 1 A, OUT1 and OUT2 connected, 0°C ≤ T_J ≤ 70°C		DGN package, TPS2042B/52B			49	mΩ
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 10 Ω	T_J = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V				0.4	1	
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V			0.05		0.5	
		$V_{I(IN)}$ = 2.7 V			0.05		0.5	
ENABLE INPUT $\overline{EN}$ AND $\overline{ENx}$								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V					0.8	
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V			–0.5		0.5	µA
t_{on}	Turnon time	C_L = 100 µF, R_L = 10 Ω					3	ms
t_{off}	Turnoff time	C_L = 100 µF, R_L = 10 Ω					10	
CURRENT LIMIT								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit		T_J = 25°C	0.75	1	1.25	A
				–40°C ≤ T_J ≤ 125°C	0.7	1	1.3	
		$V_{I(IN)}$ = 5 V, OUT1 and OUT2 connected to GND, device enabled into short-circuit, measure at IN		0°C ≤ T_J ≤ 70°C TPS2042B/52B	1.5			
I_{OC} [2]	Overcurrent trip threshold	V_{IN} = 5 V, 100 A/s	TPS2042B TPS2052B (DRB package only)		I_{OS}	1.55	2	A
SUPPLY CURRENT (TPS2041B, TPS2051B)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	1	µA
				-40°°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		75	95	µA
				–40°C ≤ T_J ≤ 125°C		75	95	
Leakage current		OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0		µA
SUPPLY CURRENT (TPS2042B, TPS2052B)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V		T_J = 25°C		0.5	1	µA
				–40°C ≤ T_J ≤ 125°C		0.5	5	

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6.5 Electrical Characteristics（续）

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V	TPS20x2B (DRB package only)	T_J = 25°C		50	70	µA
			–40°C ≤ T_J ≤ 125°C		50	90	
		TPS20x2B (D and DGN packages)	T_J = 25°C		95	120	uA
			–40°C ≤ T_J ≤ 125°C		95	120	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2043B, TPS2053B)							
Supply current, low-level output	No load on OUT, $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	2	µA
			–40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		65	90	µA
			–40°C ≤ T_J ≤ 125°C		65	110	
Leakage current	OUT connected to ground, $V_{I(ENx)}$ = 0 V		–40°C≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground		T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2044B, TPS2054B)							
Supply current, low-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	2	µA
			–40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		75	110	µA
			–40°C ≤ T_J ≤ 125°C		75	140	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		–40°C≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground		T_J = 25°C		0.2		µA
UNDERVOLTAGE LOCKOUT (TPS20x3BD, TPS20x4BD, & TPS20x2BDRB)							
Low-level input voltage, IN, INx				2		2.5	V
Hysteresis, IN, INx	T_J = 25°C				75		mV
UNDERVOLTAGE LOCKOUT (TPS20x1B & TPS20x2B; D/DBV/DGN packages)							
Low-level input voltage, IN, INx				2		2.6	V
Hysteresis, IN, INx	T_J = 25°C				75		mV
OVERCURRENT $\overline{OC}$ and $\overline{OCx}$							
Output low voltage, $V_{OL(/OCx)}$	$I_{O(\overline{OCx})}$ = 5 mA					0.4	V
Off-state current	$V_{O(\overline{OCx})}$ = 5 V or 3.3 V					1	µA
$\overline{OC}$ deglitch	$\overline{OCx}$ assertion or deassertion			4	8	15	ms
THERMAL SHUTDOWN[3]							
Thermal shutdown threshold				135			°C
Recovery from thermal shutdown				125			°C

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6.5 Electrical Characteristics（续）

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Hysteresis			10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) TPS20x1B and TPS20x2B devices in the D, DGN, and DBV packages do not have overcurrent trip thresholds. Current is limited to I_{OS} under different test condition. Check 节 8.3.7 for more details.
(3) The thermal shutdown only reacts under overcurrent conditions.

6.6 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD)

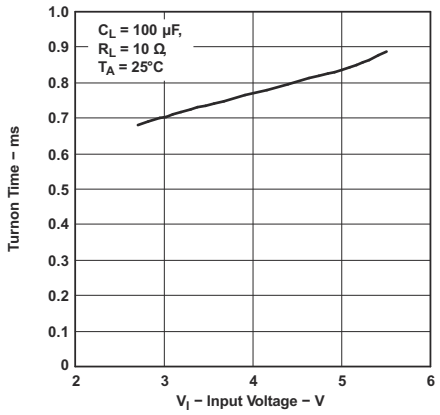

图 6-1. Turnon Time vs Input Voltage

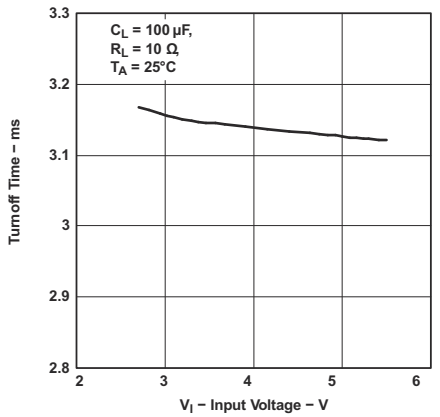

图 6-2. Turnoff Time vs Input Voltage

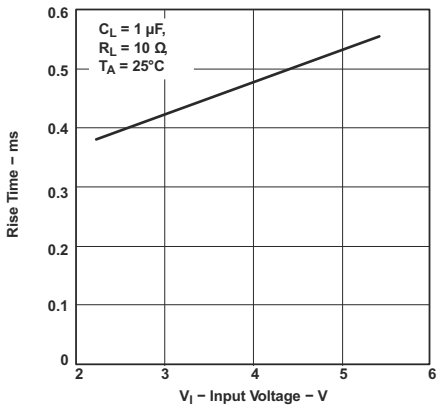

图 6-3. Rise Time vs Input Voltage

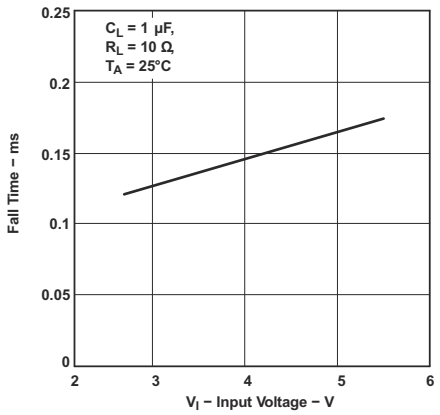

图 6-4. Fall Time vs Input Voltage

6.6 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

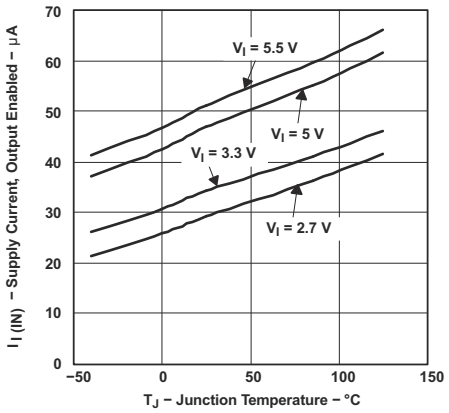

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图 6-5. TPS20x2BDRB Supply Current, Output Enabled vs Junction Temperature

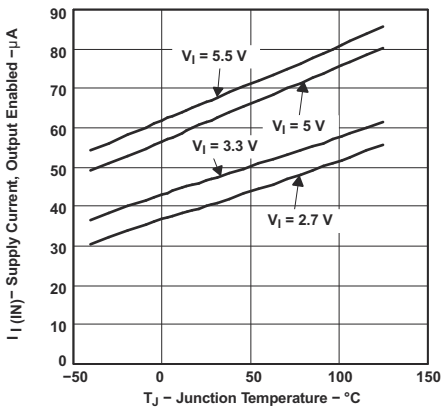

图 6-6. TPS2043B and TPS2053B Supply Current, Output Enabled vs Junction Temperature

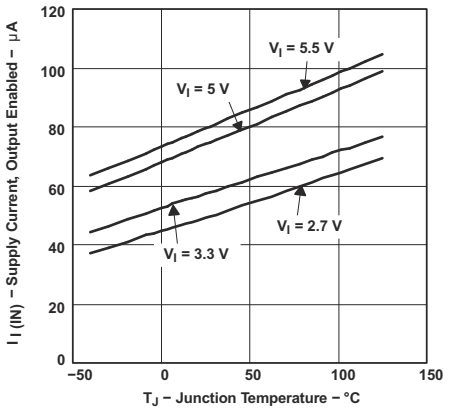

图 6-7. TPS2044B TPS2054B Supply Current, Output Enabled vs Junction Temperature

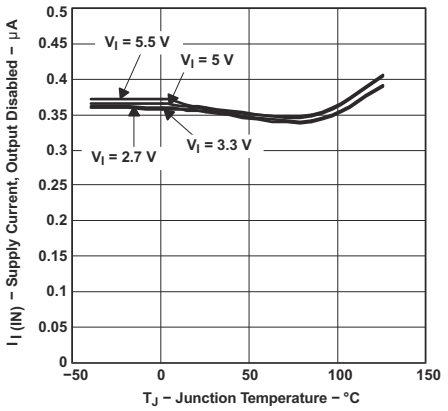

图 6-8. TPS20x2BDRB Supply Current, Output Disabled vs Junction Temperature

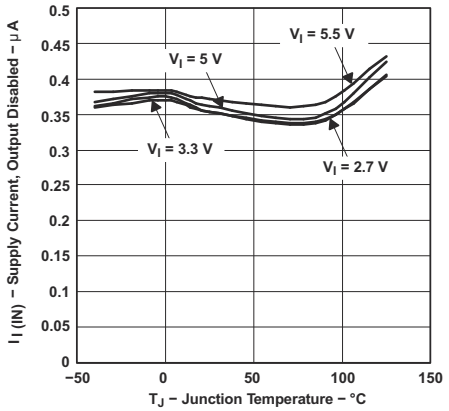

图 6-9. TPS2043B and TPS2053B Supply Current, Output Disabled vs Junction Temperature

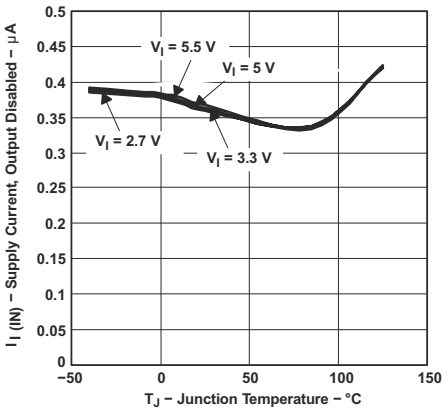

图 6-10. TPS2044B and TPS2054B Supply Current, Output Disabled vs Junction Temperature

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6.6 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

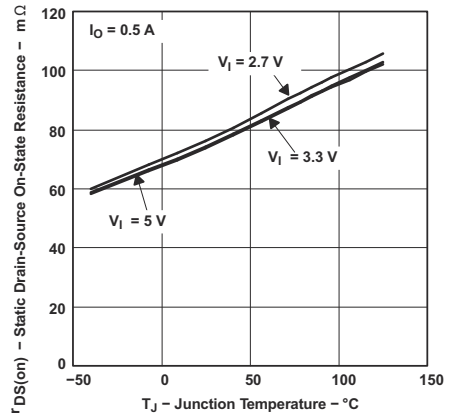

图 6-11. Static Drain-Source on-State Resistance vs Junction Temperature

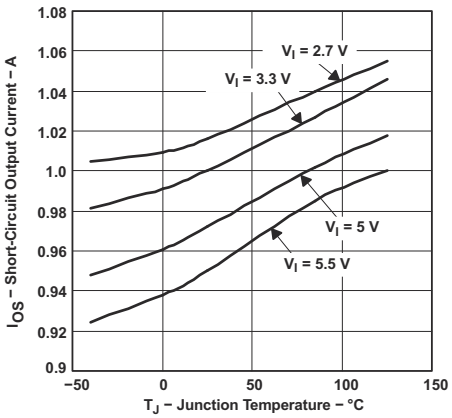

图 6-12. Short-Circuit Output Current vs Junction Temperature

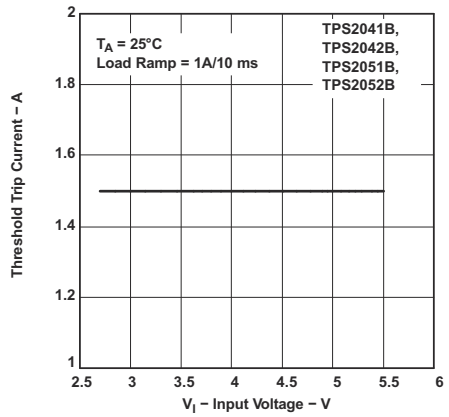

图 6-13. Threshold Trip Current vs Input Voltage

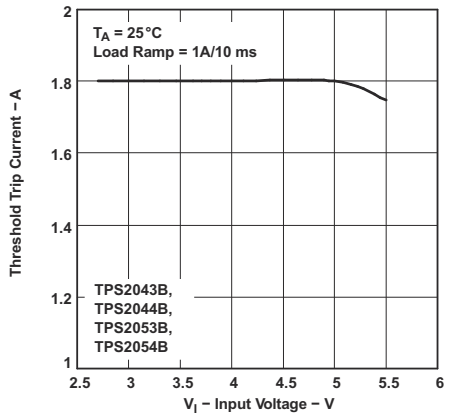

图 6-14. Threshold Trip Current vs Input Voltage

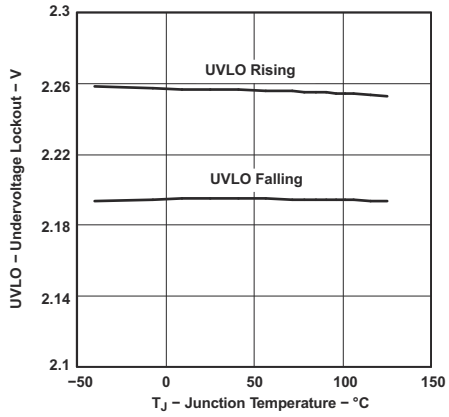

图 6-15. Undervoltage Lockout vs Junction Temperature

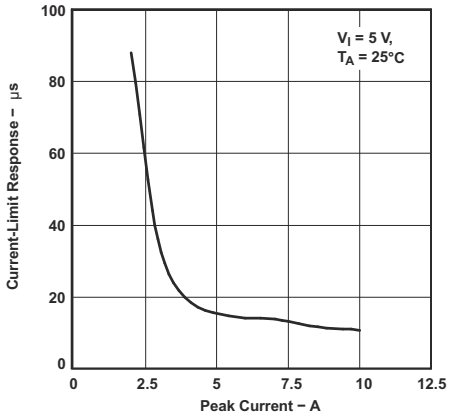

图 6-16. Current-Limit Response vs Peak Current

6.6 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

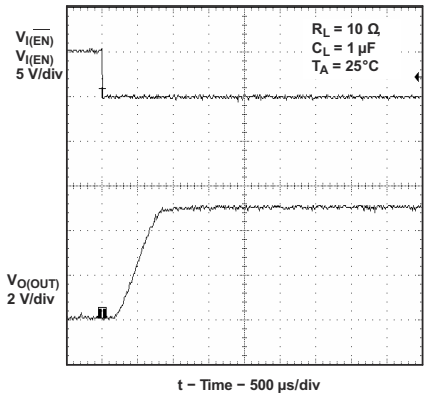

图 6-17. Turnon Delay and Rise Time With 1-µF Load

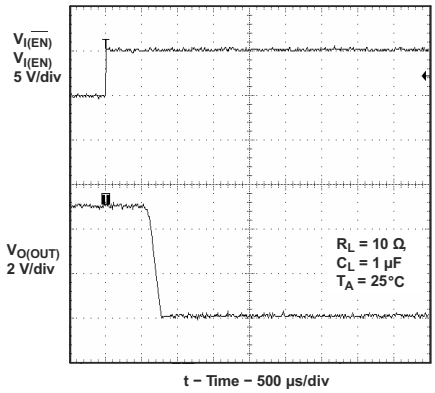

图 6-18. Turnoff Delay and Fall Time With 1-µF Load

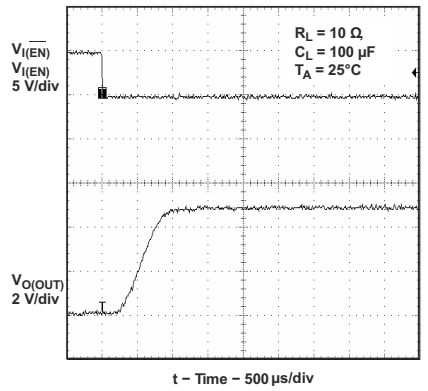

图 6-19. Turnon Delay and Rise Time With 100-µF Load

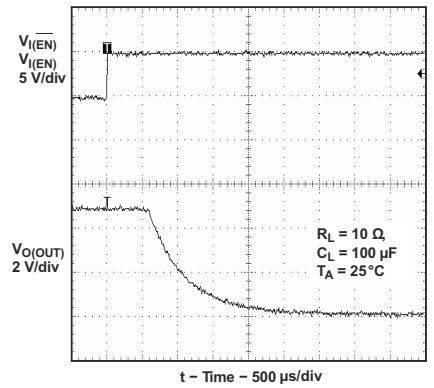

图 6-20. Turnoff Delay and Fall Time With 100-µF Load

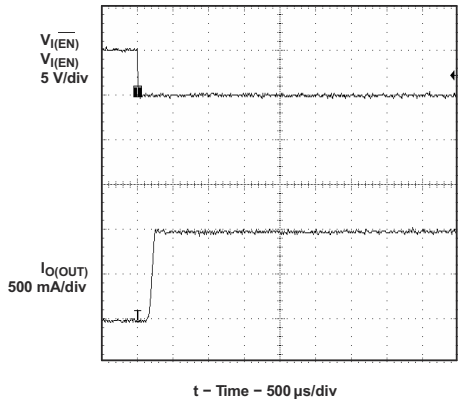

图 6-21. Short-Circuit Current, Device Enabled Into Short

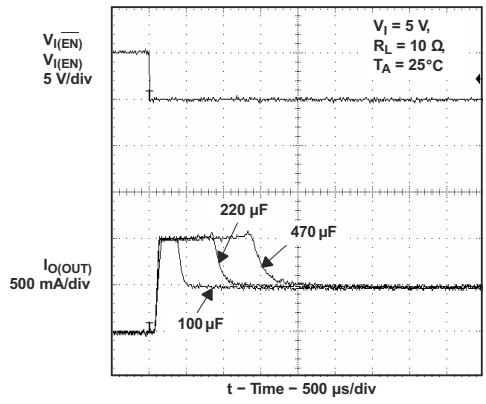

图 6-22. Inrush Current With Different Load Capacitance

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6.6 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

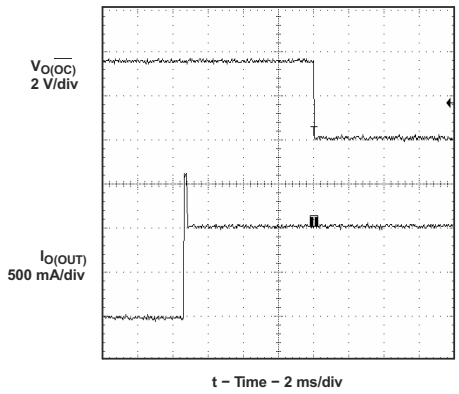

图 6-23. 3-Ω Load Connected to Enabled Device

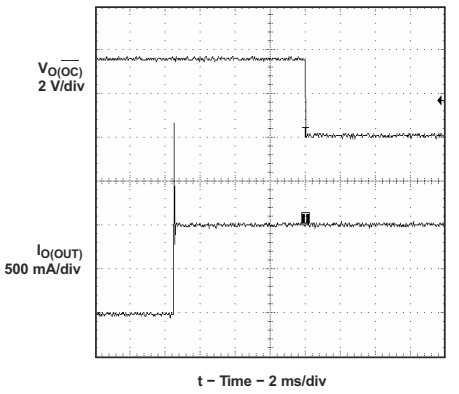

图 6-24. 2-Ω Load Connected to Enabled Device

6.7 Typical Characteristics (TPS2051BDBV and TPS2052BD)

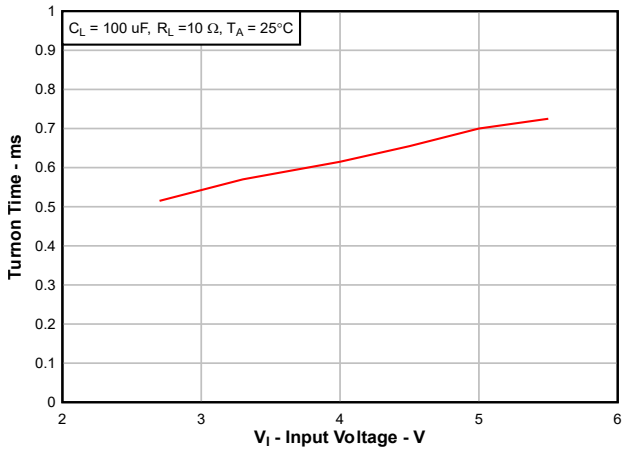

图 6-25. Turnon Time vs Input Voltage

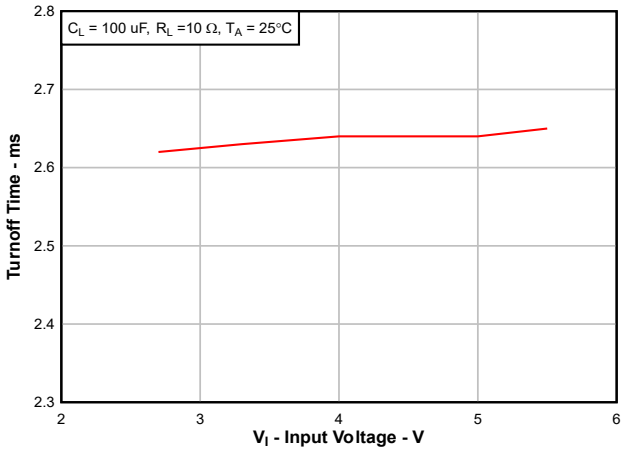

图 6-26. Turnoff Time vs Input Voltage

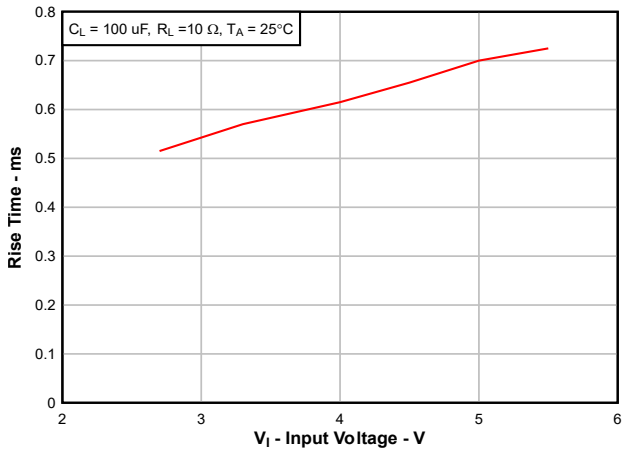

图 6-27. Rise Time vs Input Voltage

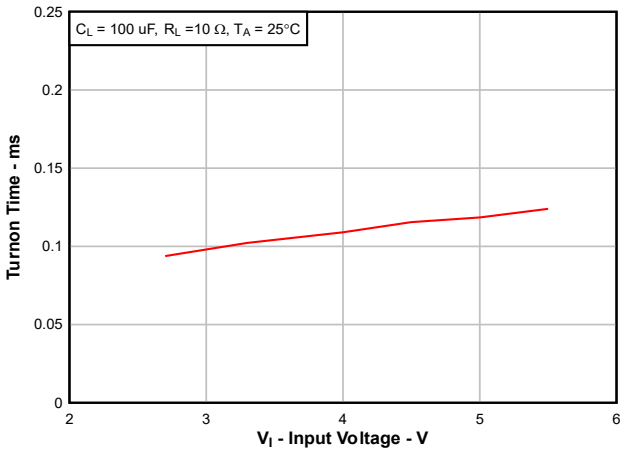

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图 6-28. Fall Time vs Input Voltage

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6.7 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)

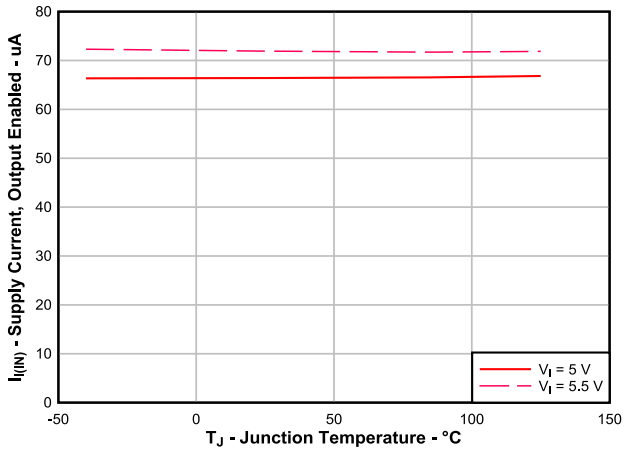

图 6-29. TPS2051BDBV Supply Current, Output Enabled vs Junction Temperature

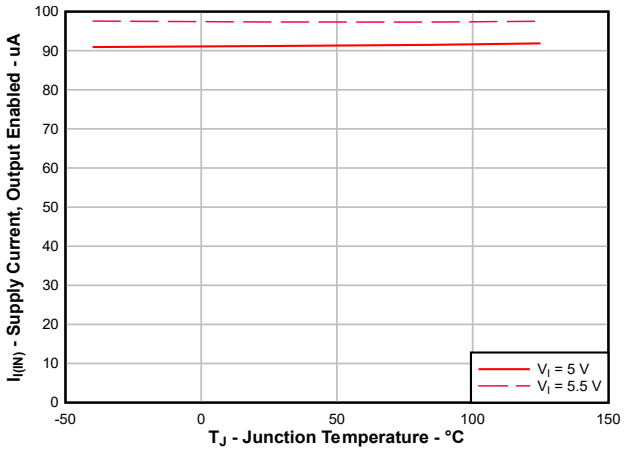

图 6-30. TPS2052BD Supply Current, Output Enabled vs Junction Temperature

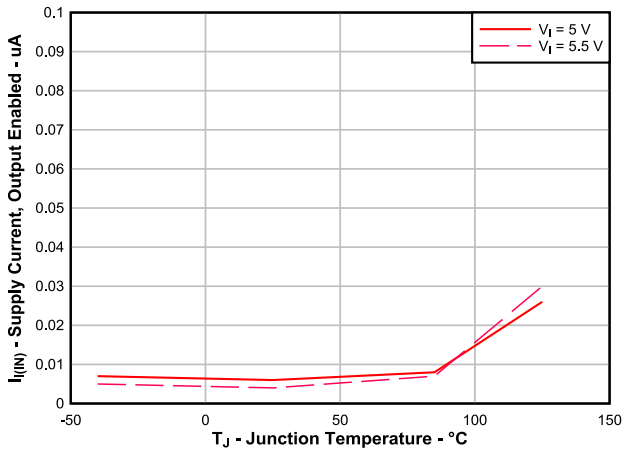

图 6-31. TPS2051BDBV Supply Current, Output Disabled vs Junction Temperature

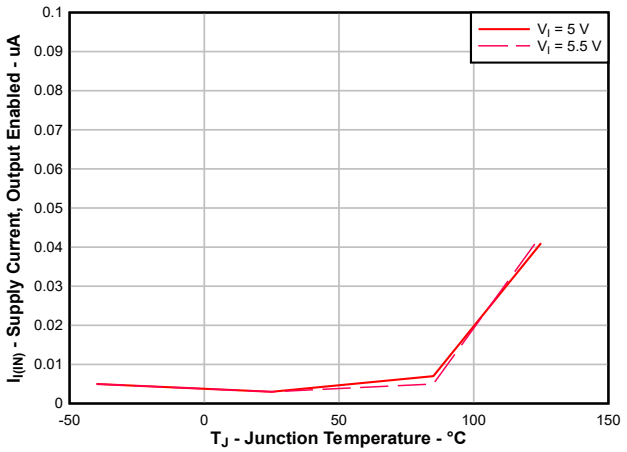

图 6-32. TPS2052BD Supply Current, Output Disabled vs Junction Temperature

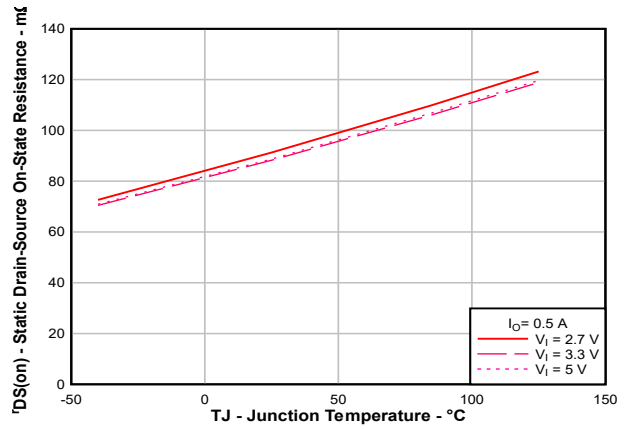

图 6-33. DBV Package Static Drain-Source on-State Resistance vs Junction Temperature

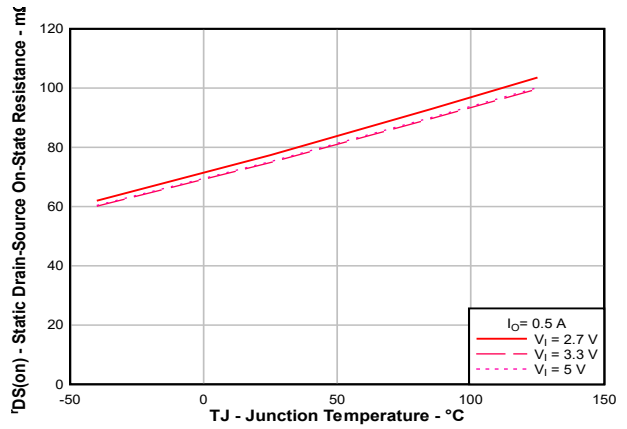

图 6-34. D Package Static Drain-Source on-State Resistance vs Junction Temperature

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6.7 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)

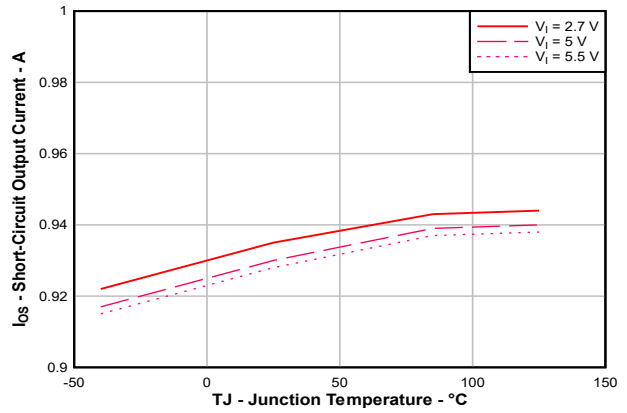

图 6-35. Short-Circuit Output Current vs Junction Temperature

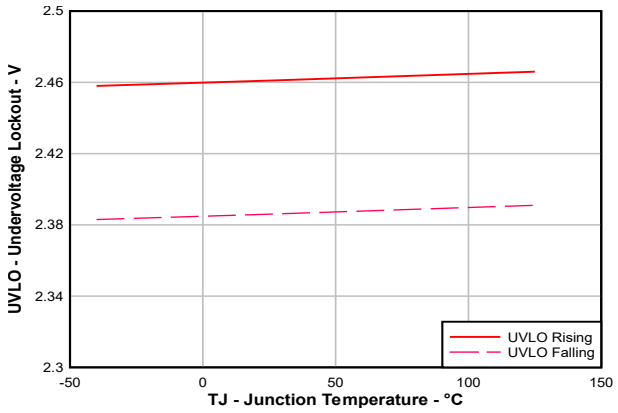

图 6-36. Undervoltage Lockout vs Junction Temperature

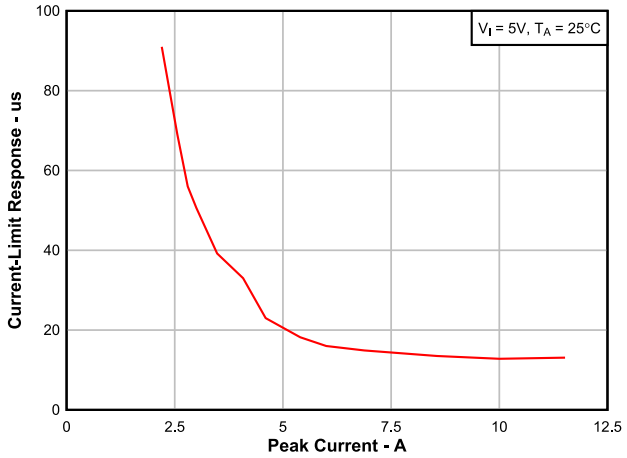

图 6-37. Current-Limit Response vs Peak Current

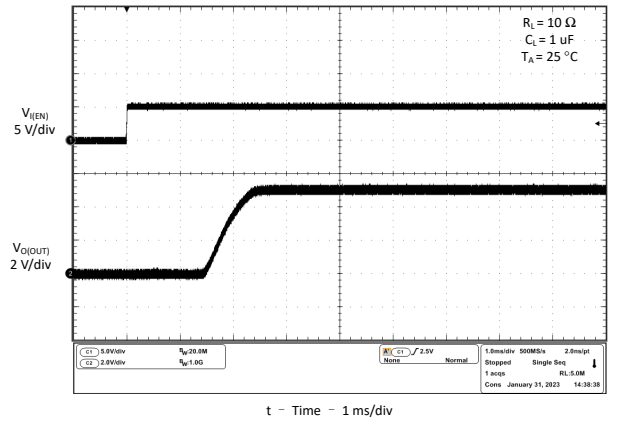

图 6-38. Turnon Delay and Rise Time With 1-µF Load

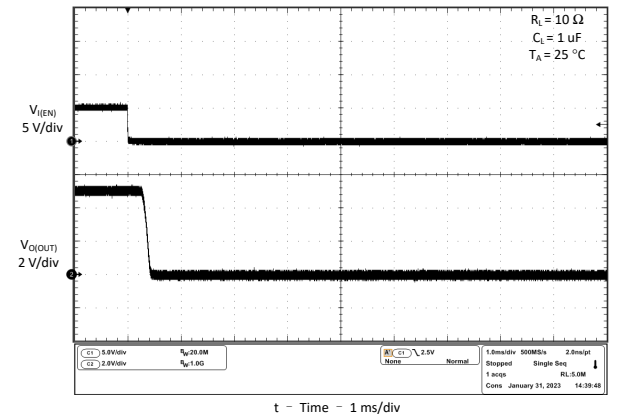

图 6-39. Turnoff Delay and Fall Time With 1-µF Load

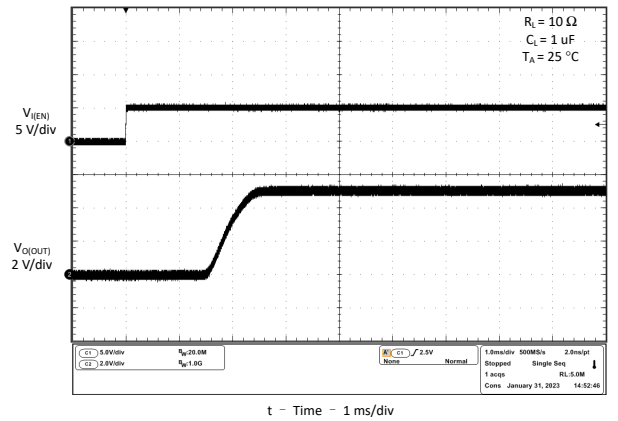

图 6-40. Turnon Delay and Rise Time With 100-µF Load

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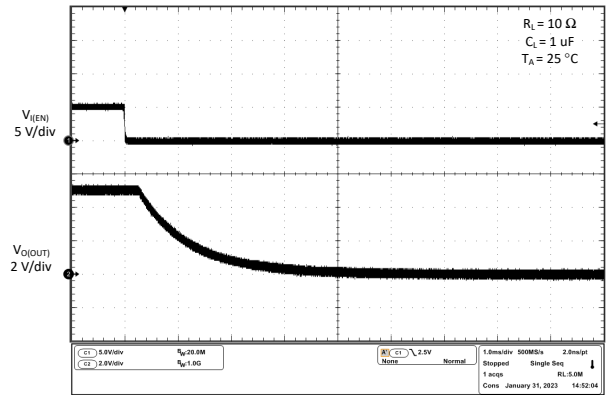
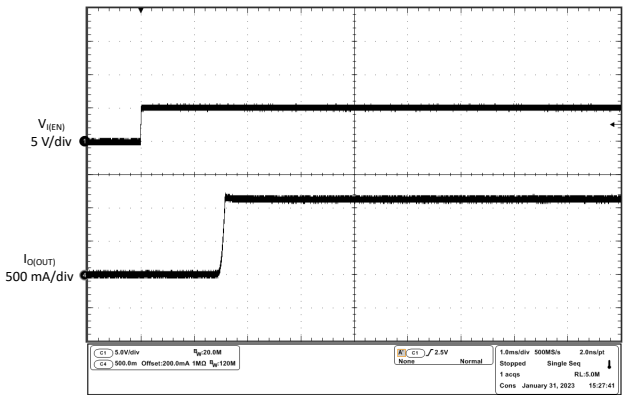
6.7 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)



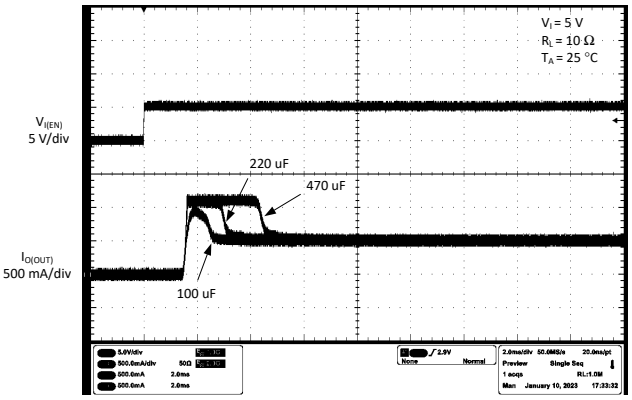
t – Time – 1 ms/div

图 6-41. Turnoff Delay and Fall Time With 100-µF Load



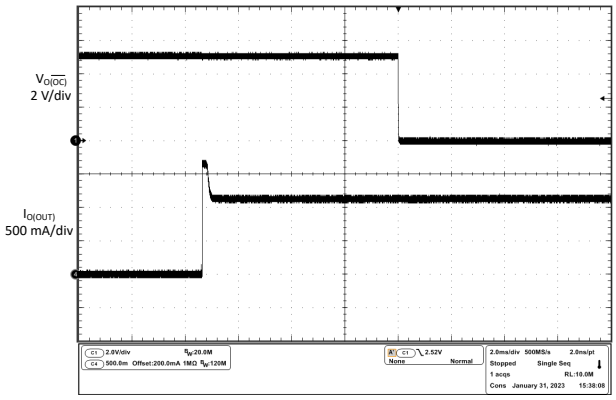
t – Time – 1 ms/div

图 6-42. Short-Circuit Current, Device Enabled Into Short



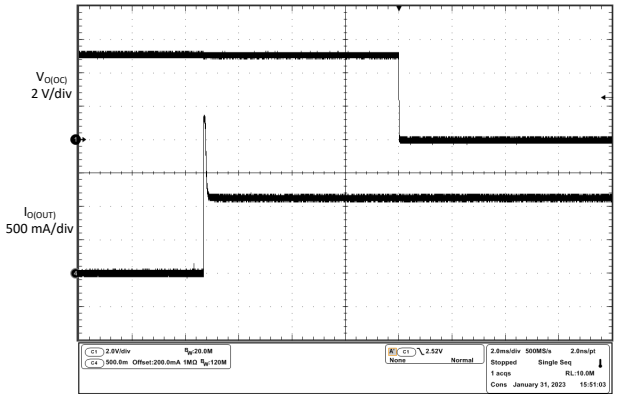
t – Time – 2 ms/div

图 6-43. Inrush Current With Different Load Capacitance



t – Time – 2 ms/div

图 6-44. 3-Ω Load Connected to Enabled Device



t – Time – 2 ms/div

图 6-45. 2-Ω Load Connected to Enabled Device

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7 Parameter Measurement Information

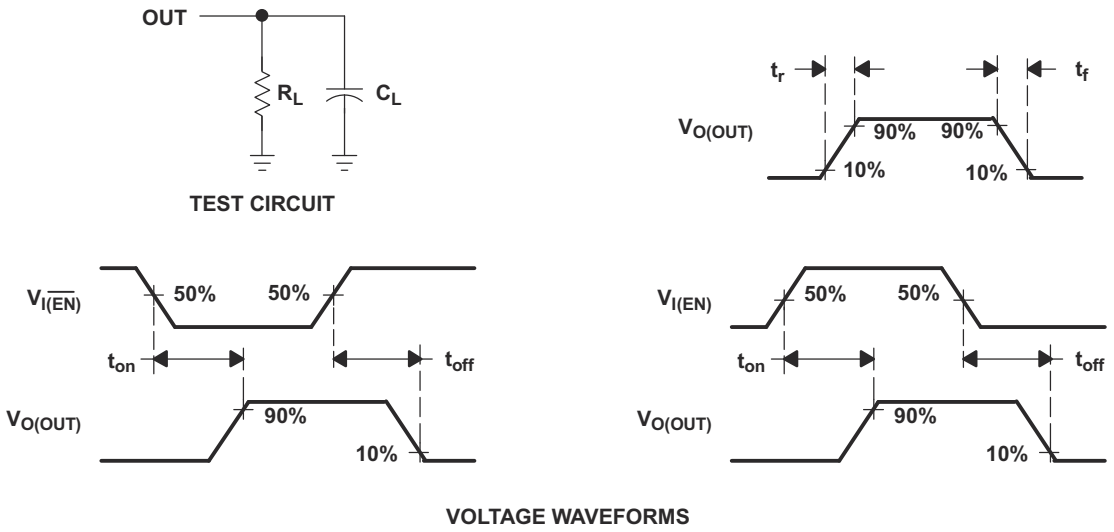


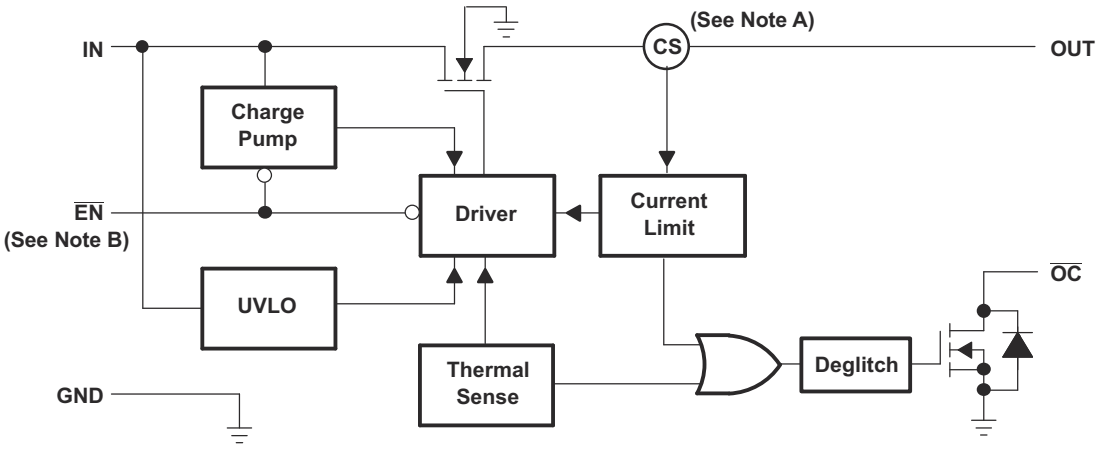
图 7-1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TPS20xxB are current-limited, power-distribution switches providing 0.5-A continuous load current. These devices incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Gate driver is provided by an internal charge pump designed to minimize current surges during switching. The charge pump requires no external components and allows operation supplies as low as 2.7 V.

8.2 Functional Block Diagrams



Note A: Current sense
Note B: Active low ($\overline{EN}$) for TPS2041B; Active high (EN) for TPS2051B

图 8-1. Functional Block Diagram (TPS2041B and TPS2051B)

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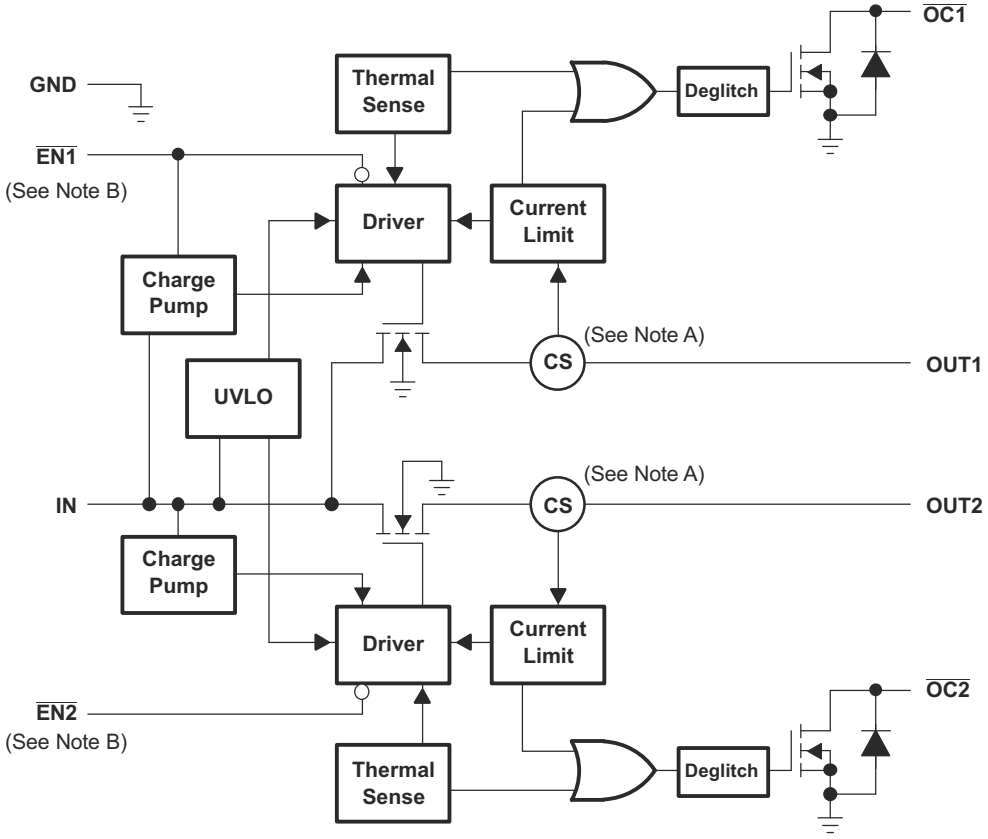
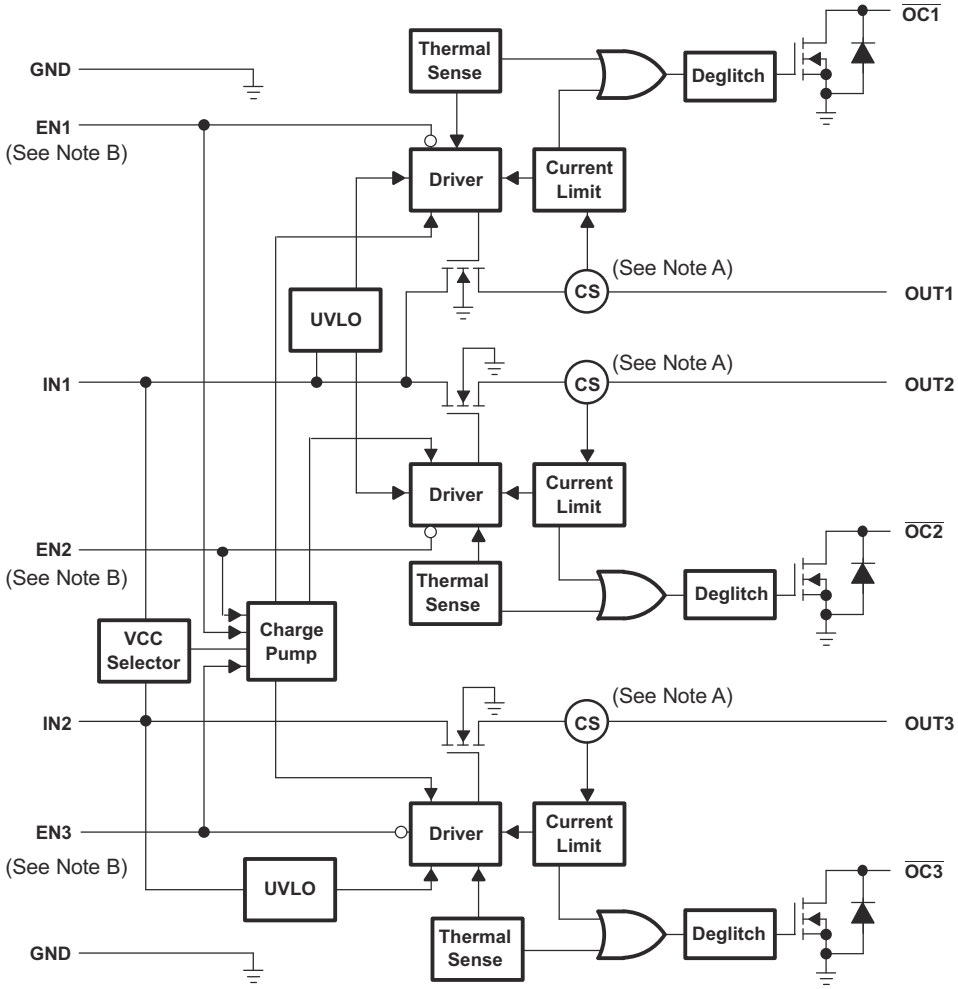


Note A: Current sense

Note B: Active low ($\overline{\text{ENx}}$) for TPS2042B; Active high (ENx) for TPS2052B

图 8-2. Functional Block Diagram (TPS2042B and TPS2052B)



Note A: Current sense

Note B: Active low ($\overline{ENx}$) for TPS2043B; Active high (ENx) for TPS2053B

图 8-3. Functional Block Diagram (TPS2043B and TPS2053B)

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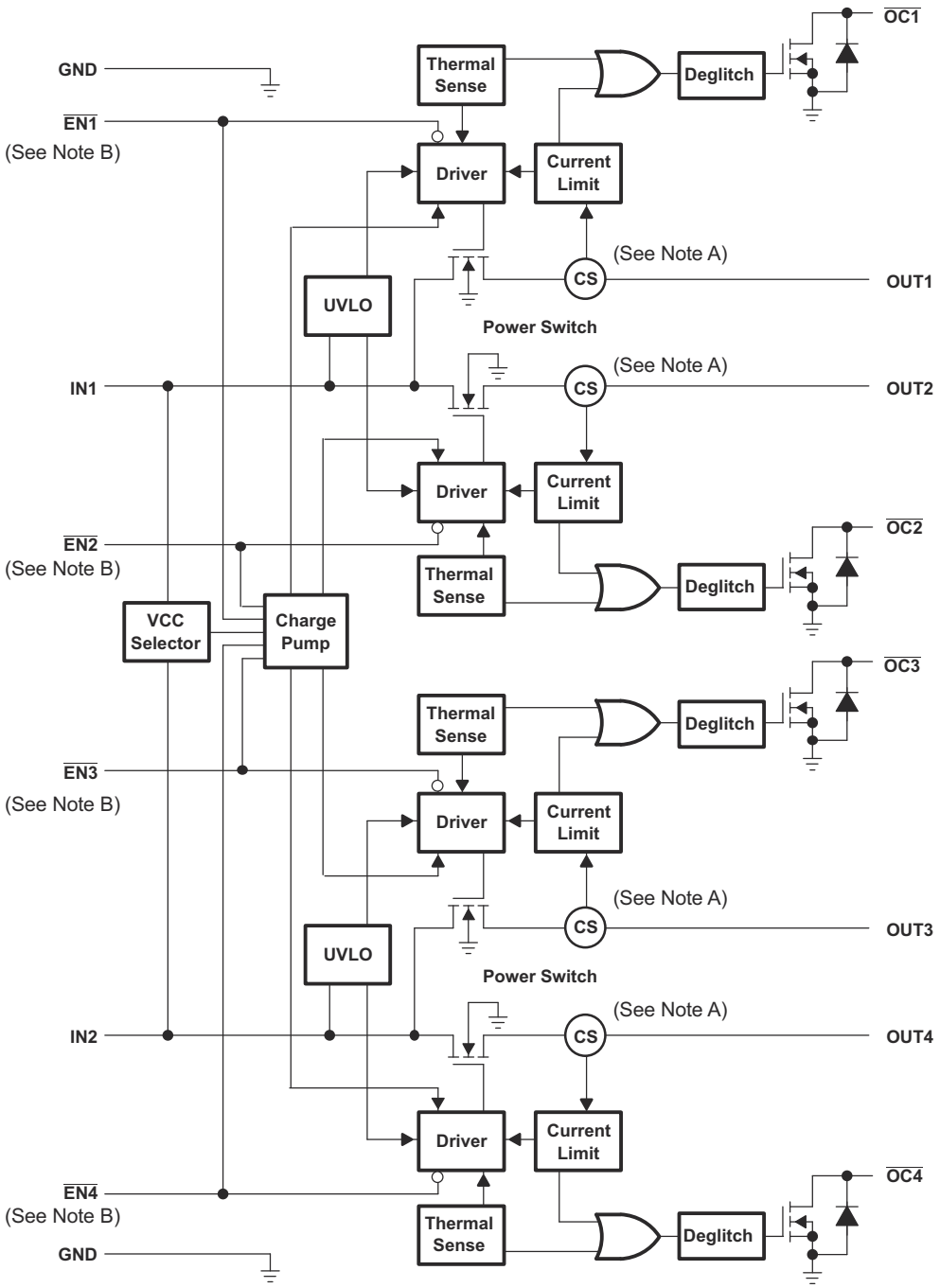

Note A: Current sense

Note B: Active low ($\overline{ENx}$) for TPS2044B; Active high (ENx) for TPS2054B

图 8-4. Functional Block Diagram (TPS2044B and TPS2054B)

8.3 Feature Description

8.3.1 Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

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8.3.2 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

8.3.3 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

8.3.4 Enable ($\overline{ENx}$)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

8.3.5 Enable (ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic low is present on ENx. A logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

8.3.6 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

8.3.7 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

There are two kinds of current limit profiles for the TPS20xxB family of devices.

The TPS20x3BD, TPS20x4BD, and TPS20x2BDRB devices have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in 图 8-5. This type of limiting can be characterized by two parameters, the overcurrent trip threshold (I_{OC}), and the short-circuit output current threshold (I_{OS}).

The TPS20x1B and TPS20x2B devices in the D, DGN, and DBV packages have an output I vs V characteristic similar to the plot labeled **Flat Current Limit** in 图 8-5. This type of limiting can be characterized by one parameters, the short circuit current (I_{OS}).

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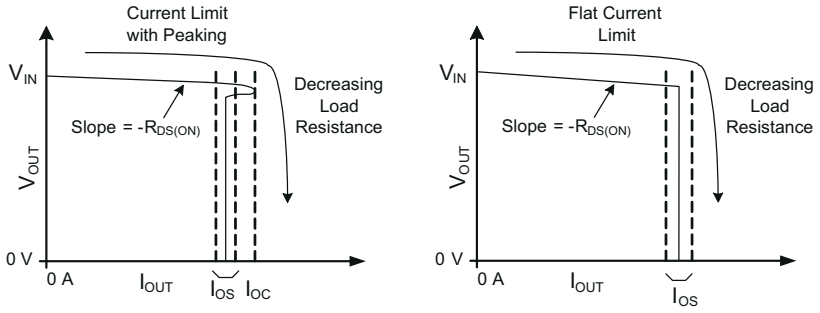

图 8-5. Current Limit Profiles

8.3.7.1 Overcurrent Conditions (TPS20x3BD, TPS20x4BD, and TPS20x2BDRB)

Three possible overload conditions can occur for TPS20x3BD, TPS20x4BD, and TPS20x2BDRB devices. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see 图 6-21 through 图 6-24). The TPS20xxB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold (I_{OC})), the device switches into constant-current mode and current is limited at the short-circuit output current threshold (I_{OS}).

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the overcurrent trip threshold (I_{OC}) is reached or until the thermal limit of the device is exceeded. The TPS20x3BD, TPS20x4BD, and TPS20x2BDRB are capable of delivering current up to the current-limit threshold without damaging the device. Once the overcurrent trip threshold (I_{OC}) has been reached, the device switches into its constant-current mode current is limited at the short-circuit output current threshold (I_{OS}).

8.3.7.2 Overcurrent Conditions (TPS20x1B & TPS20x2B in D, DGN, and DBV packages)

Three possible overload conditions can occur for the TPS20x1B and TPS20x2B devices in the D, DGN, and DBV packages. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see 图 6-42 through 图 6-45). The TPS20xxB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

8.3.8 Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

8.3.9 Thermal Sense

The TPS20xxB implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until

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the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

8.3.10 Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

8.4 Device Functional Modes

There are no other functional modes for TPS20xxB devices.

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts and self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS20xxB can provide power-distribution solutions to many of these classes of devices.

9.2 Typical Application

9.2.1 Typical Application (TPS2042B)

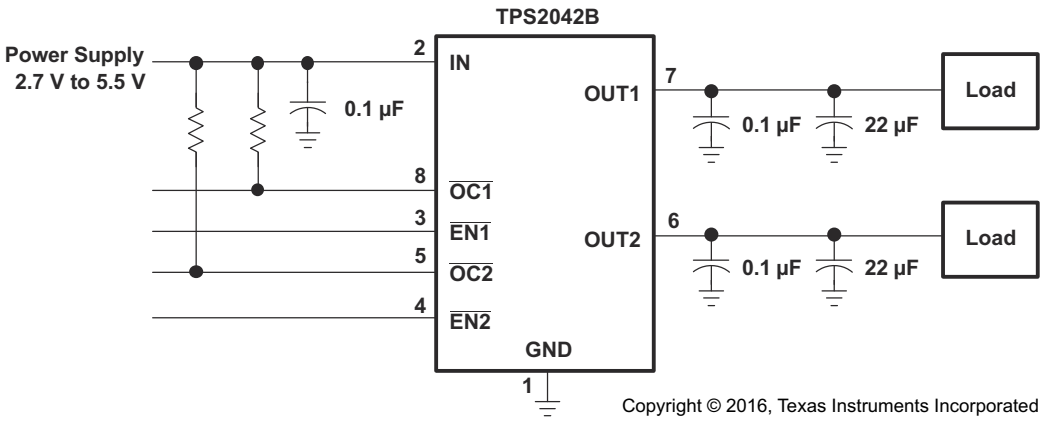

图 9-1. Typical Application (Example, TPS2042B)

9.2.1.1 Design Requirements

表 9-1 shows the design parameters for this application.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	5 V

表 9-1. Design Parameters（续）

DESIGN PARAMETER	VALUE
Output1 voltage	5 V
Output2 voltage	5 V
Output1 current	0.5 A
Output2 current	0.5 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Power-Supply Considerations

TI recommends placing a 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device. When the output load is heavy, TI recommends placing a high-value electrolytic capacitor on the necessary output pins. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

9.2.1.2.2 $\overline{OC}$ Response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS20xxB is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

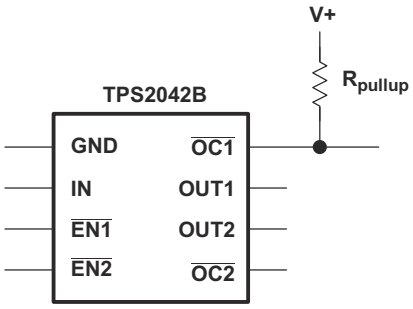

图 9-2. Typical Circuit for the $\overline{OC}$ Pin (Example, TPS2042B)

9.2.1.3 Application Curves

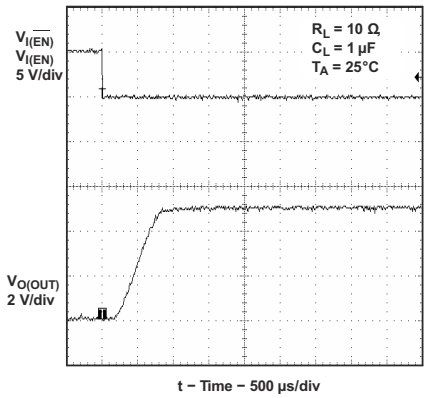

图 9-3. Turnon Delay and Rise Time With 1-µF Load

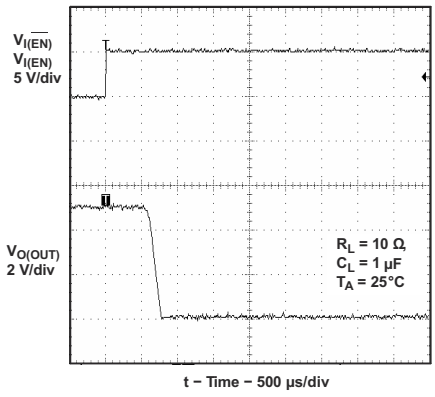

图 9-4. Turnoff Delay and Fall Time With 1-µF Load

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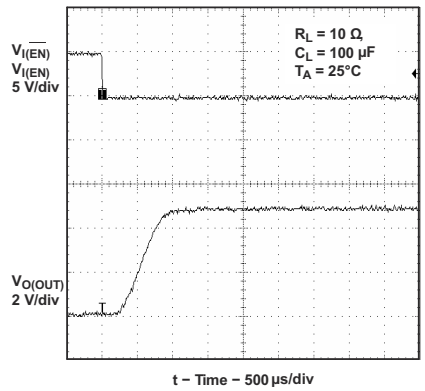

图 9-5. Turnon Delay and Rise Time With 100-µF Load

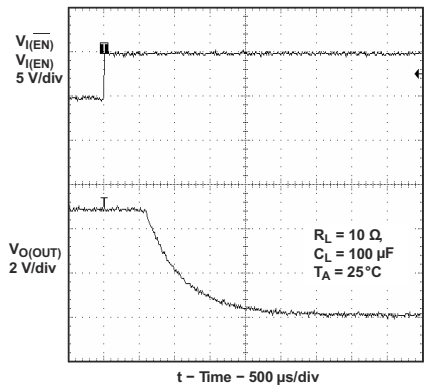

图 9-6. Turnoff Delay and Fall Time With 100-µF Load

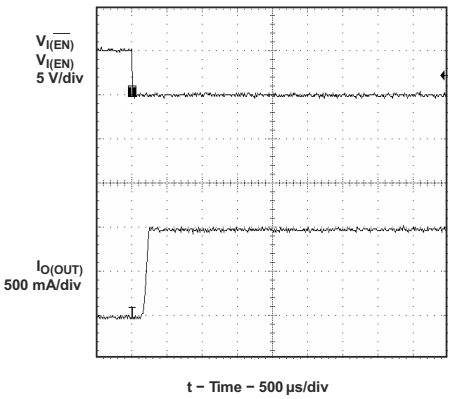

图 9-7. Short-Circuit Current, Device Enabled Into Short

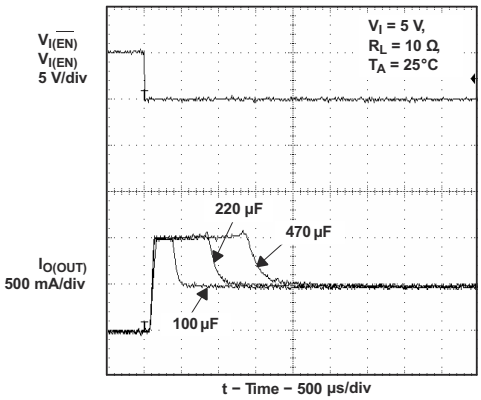

图 9-8. Inrush Current With Different Load Capacitance

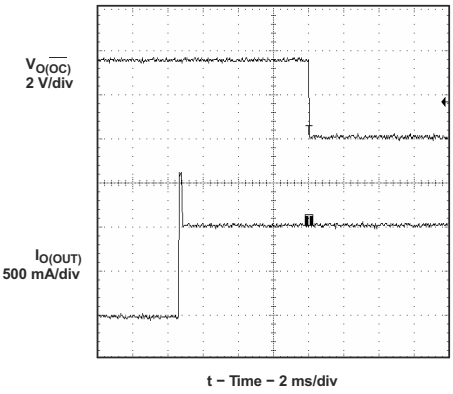

图 9-9. 3-Ω Load Connected to Enabled Device

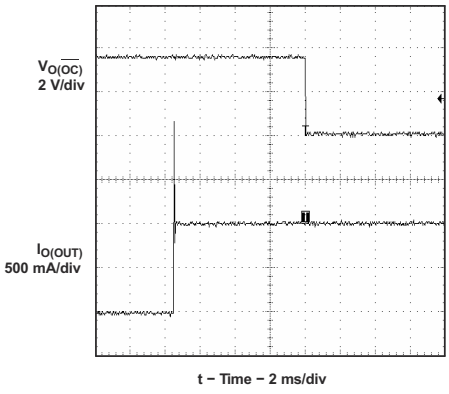

图 9-10. 2-Ω Load Connected to Enabled Device

9.2.2 Host and Self-Powered and Bus-Powered Hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see 图 9-11 and 图 9-12). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

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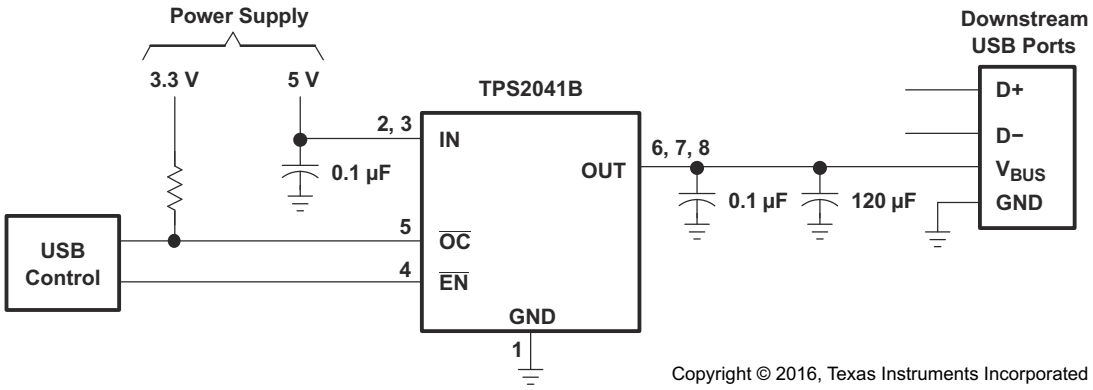

图 9-11. Typical One-Port USB Host and Self-Powered Hub

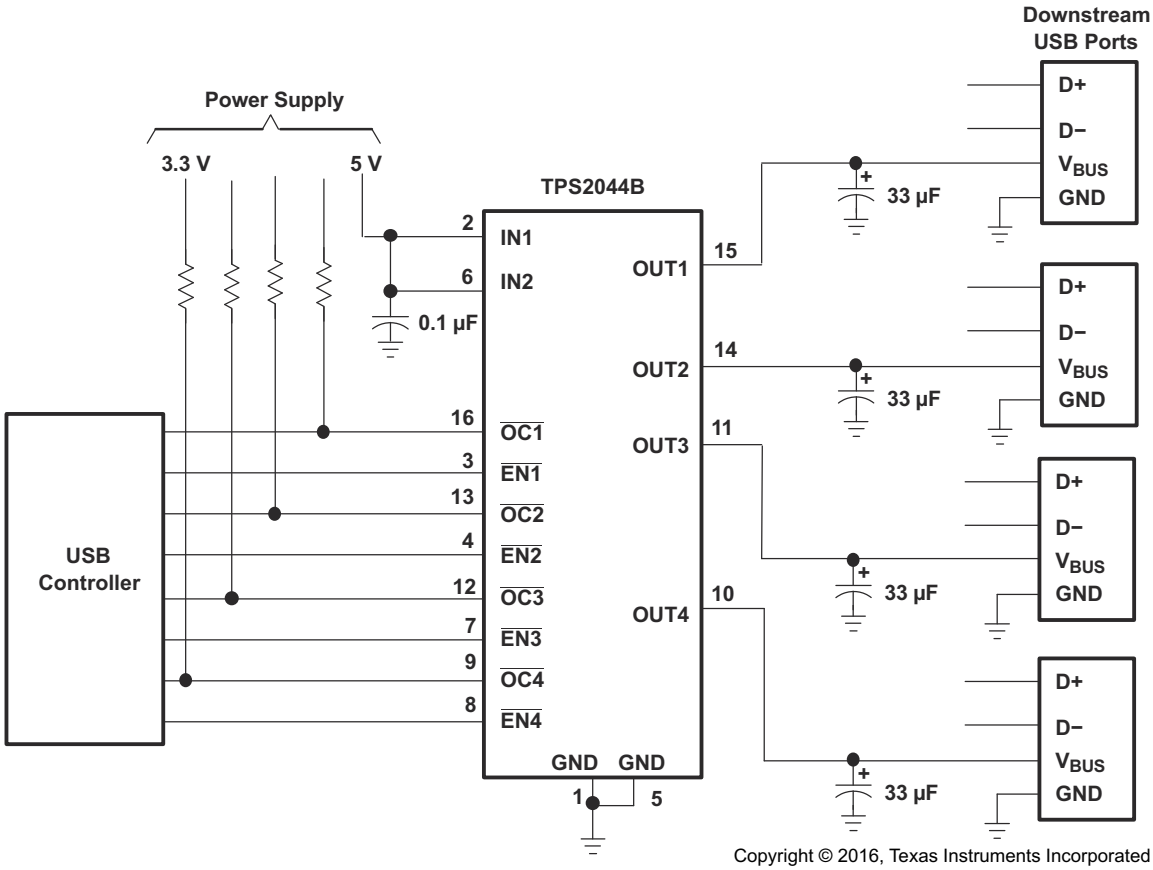

图 9-12. Typical Four-Port USB Host and Self-Powered Hub

9.2.2.1 Design Requirements

9.2.2.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts and self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports

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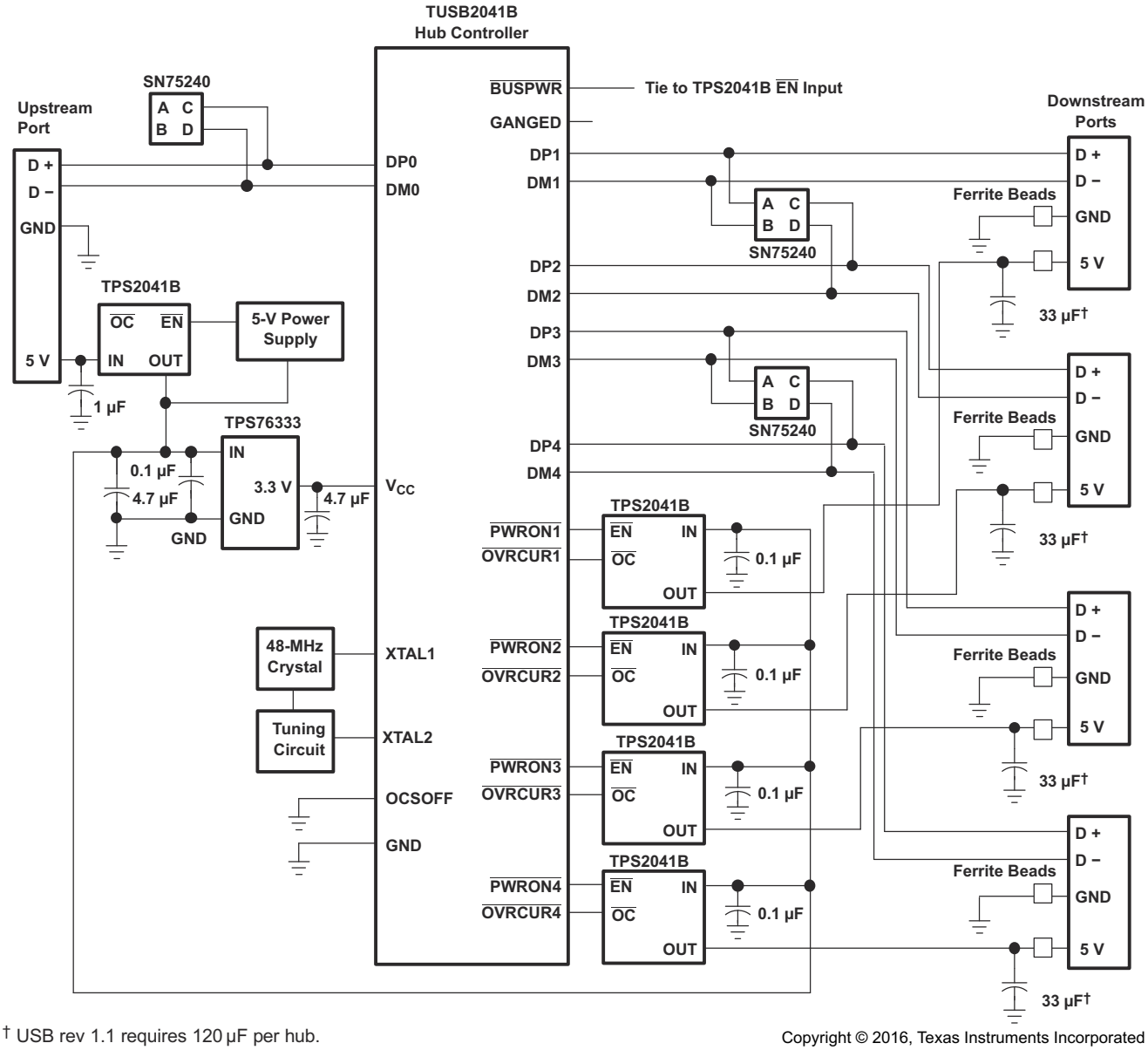
- Power up at <100 mA
- Limit inrush current (<44 Ω and 10 µF)

- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS20xxB allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see 图 9-13 through 图 9-16).



† USB rev 1.1 requires 120 µF per hub.

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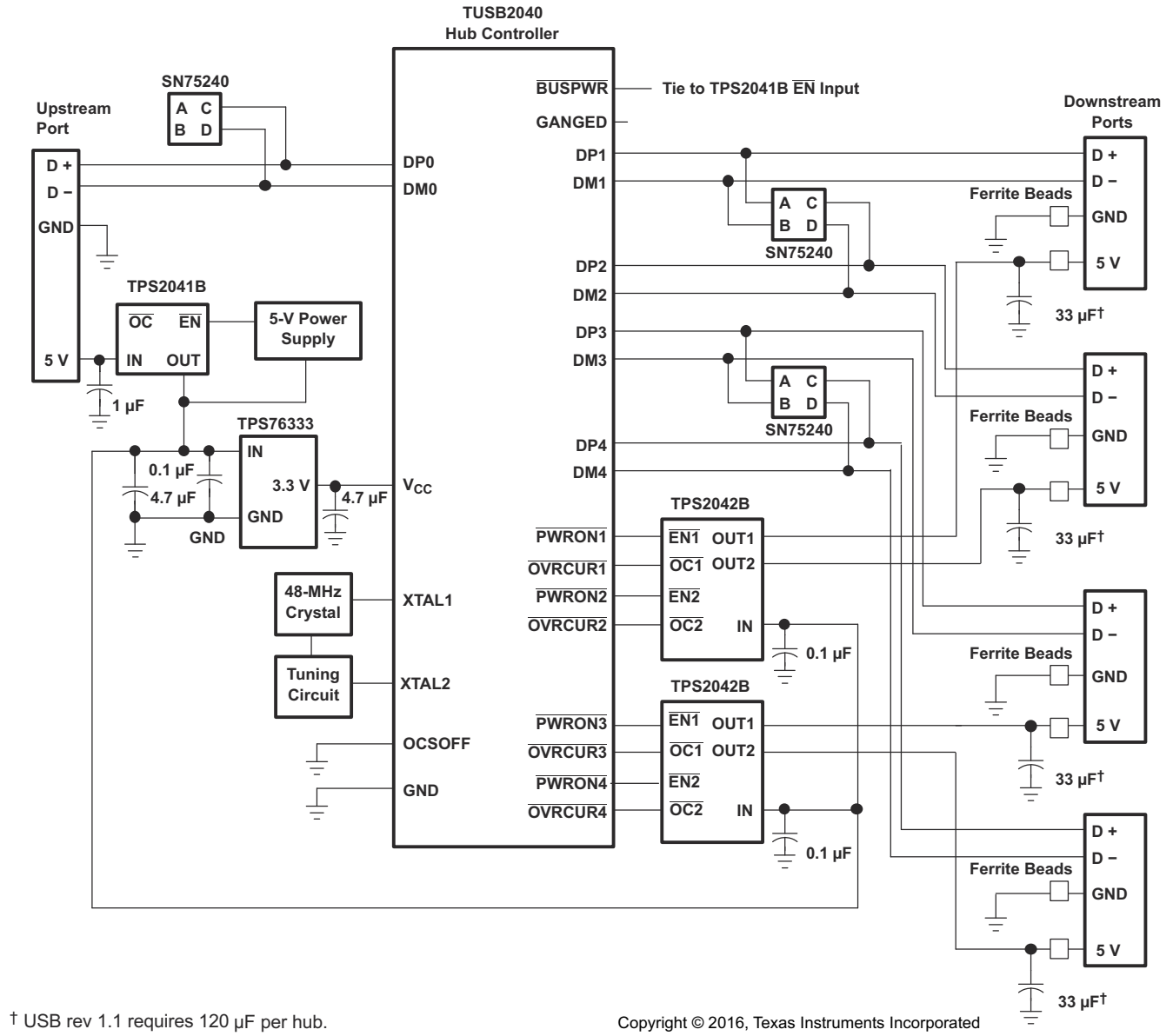
图 9-13. Hybrid Self and Bus-Powered Hub Implementation, TPS2041B and TPS2051B



† USB rev 1.1 requires 120 µF per hub.

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图 9-14. Hybrid Self and Bus-Powered Hub Implementation, TPS2042B and TPS2052B

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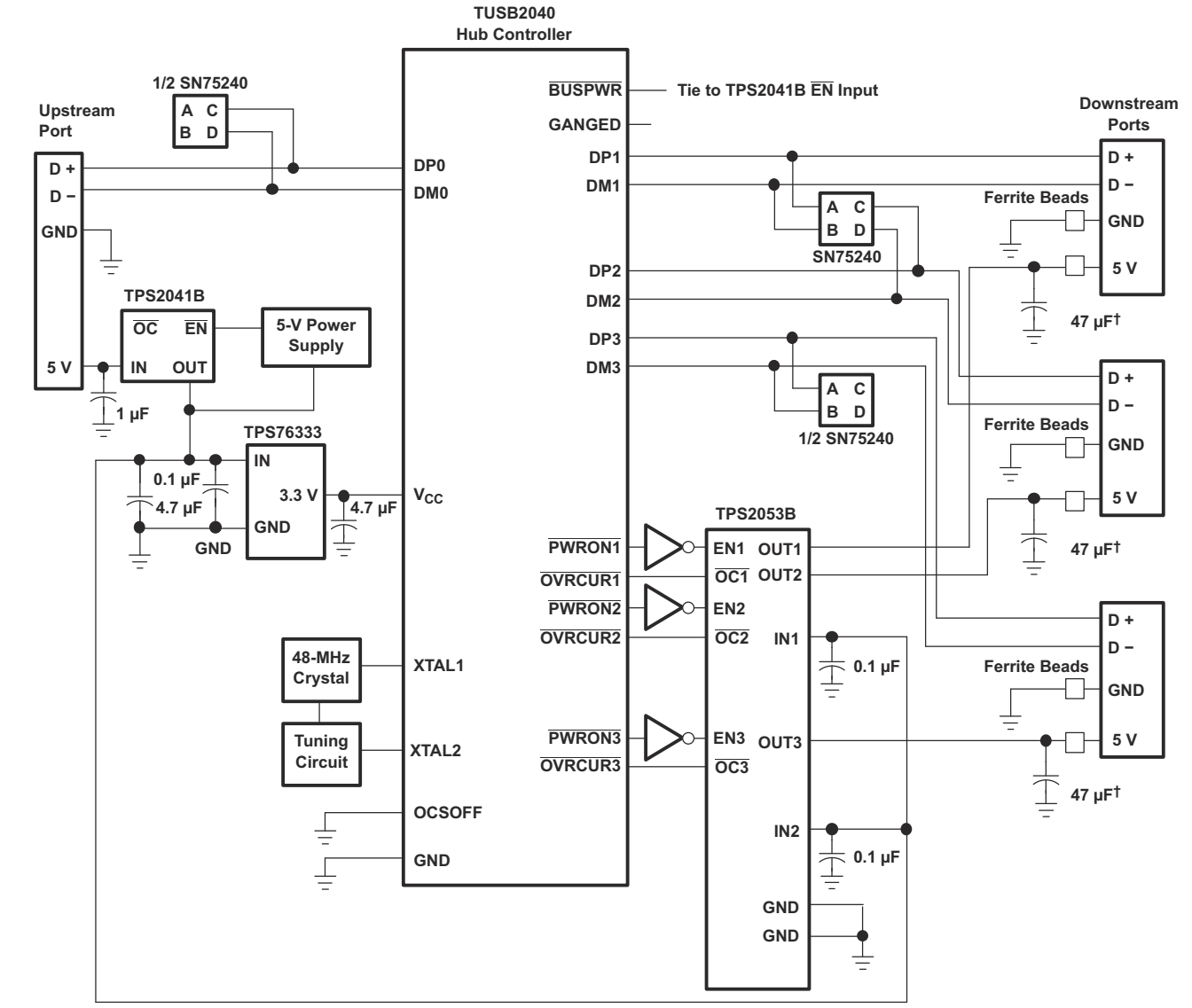

† USB rev 1.1 requires 120 µF per hub.

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图 9-15. Hybrid Self and Bus-Powered Hub Implementation, TPS2043B and TPS2053B

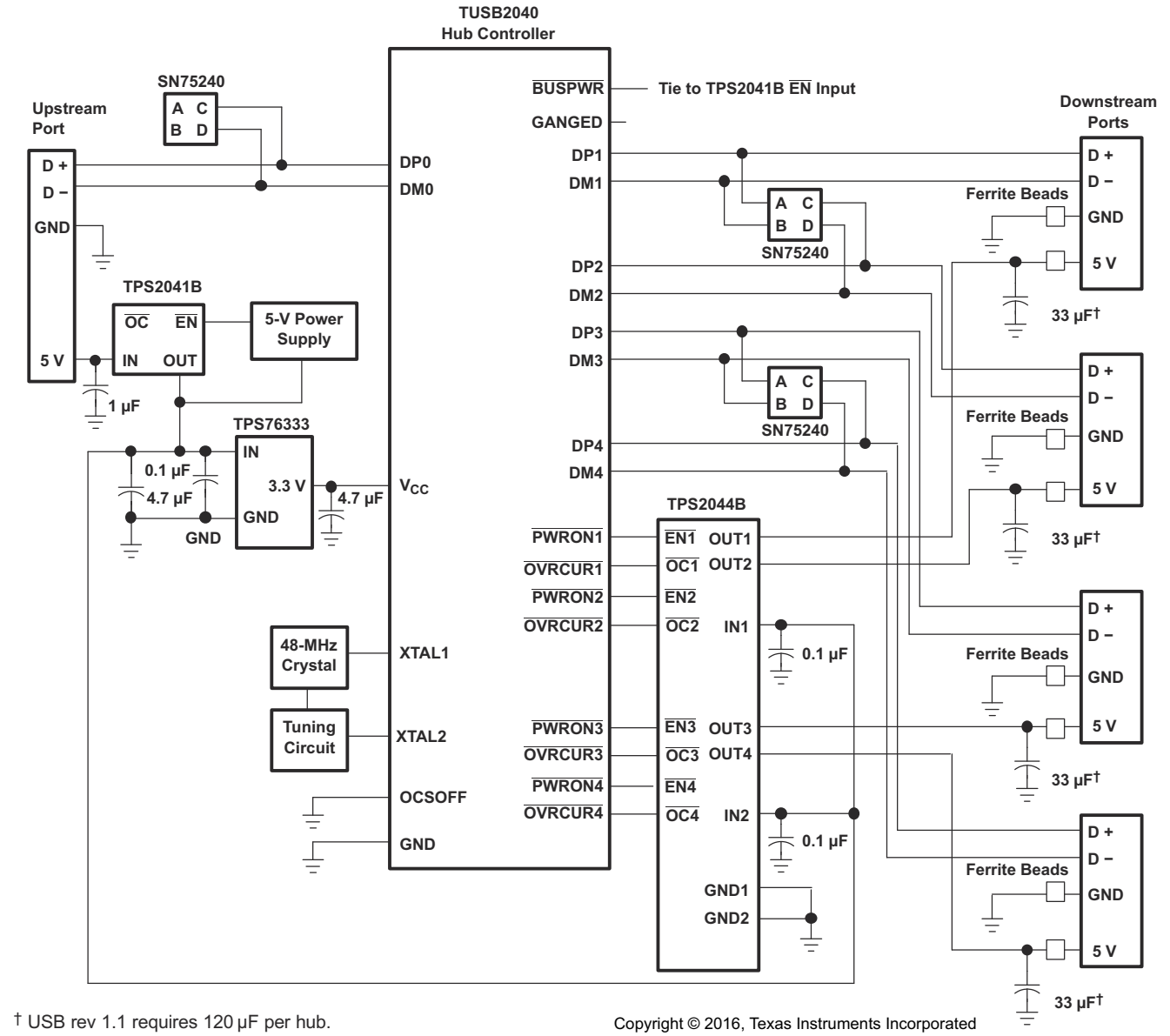

图 9-16. Hybrid Self and Bus-Powered Hub Implementation, TPS2044B and TPS2054B

9.2.2.2 Detailed Design Procedure

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

9.2.2.2.1 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can

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draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see 图 9-17).

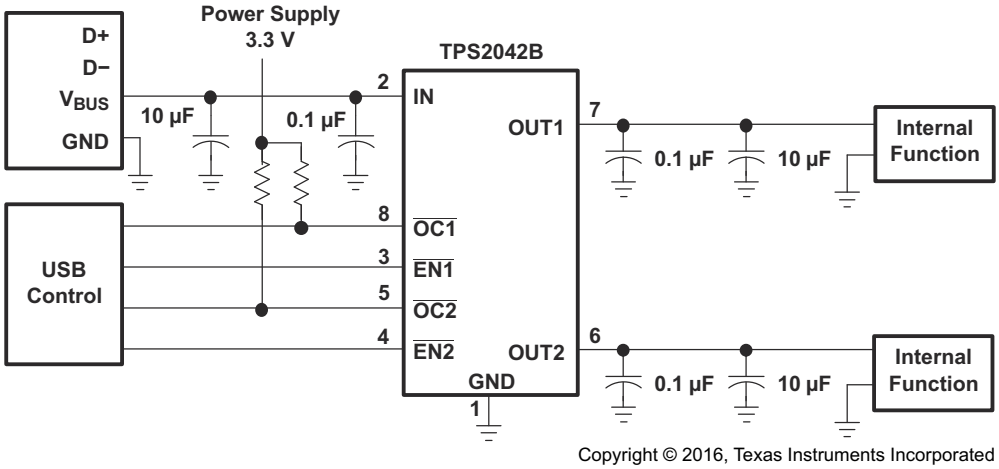

图 9-17. High-Power Bus-Powered Function (Example, TPS2042B)

9.2.2.3 Application Curves

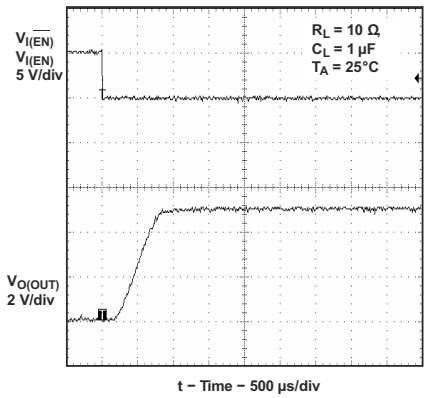

图 9-18. Turnon Delay and Rise Time With 1-µF Load

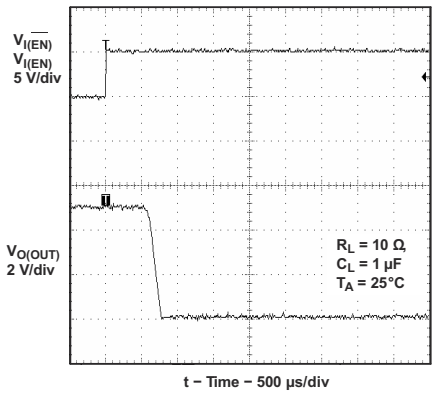

图 9-19. Turnoff Delay and Fall Time with 1- μ F Load

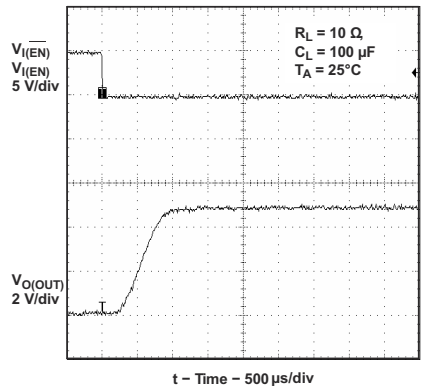

图 9-20. Turnon Delay and Rise Time With 100-µF Load

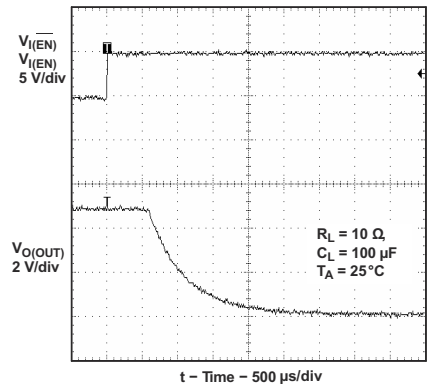

图 9-21. Turnoff Delay and Fall Time With 100-µF Load

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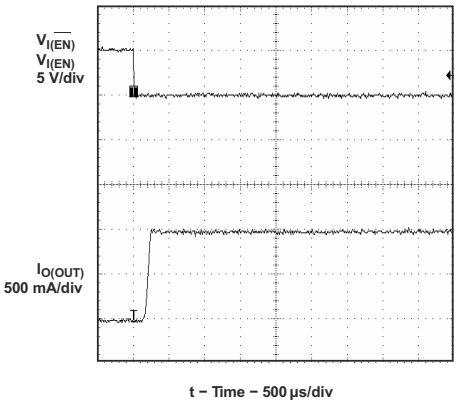

图 9-22. Short-Circuit Current, Device Enabled Into Short

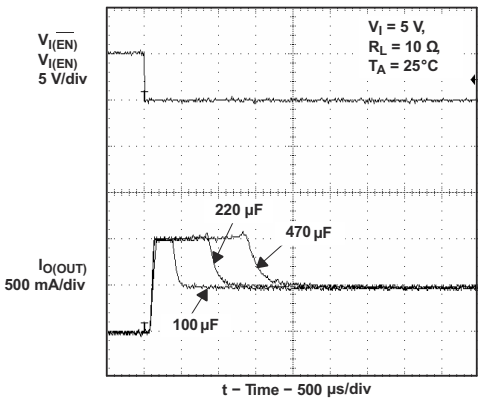

图 9-23. Inrush Current With Different Load Capacitance

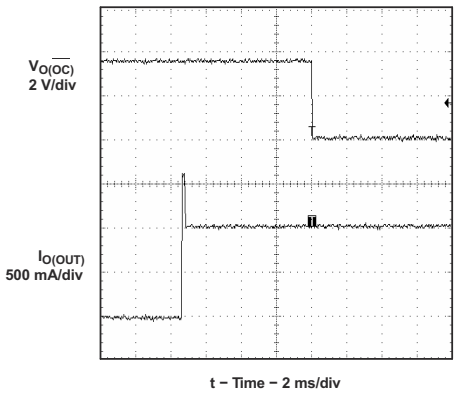

图 9-24. 3-Ω Load Connected to Enabled Device

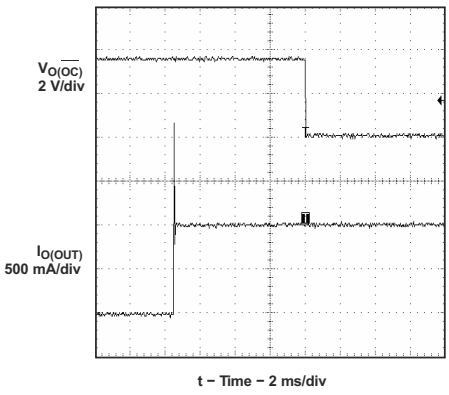

图 9-25. 2-Ω Load Connected to Enabled Device

9.2.3 Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS20xxB, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS20xxB also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

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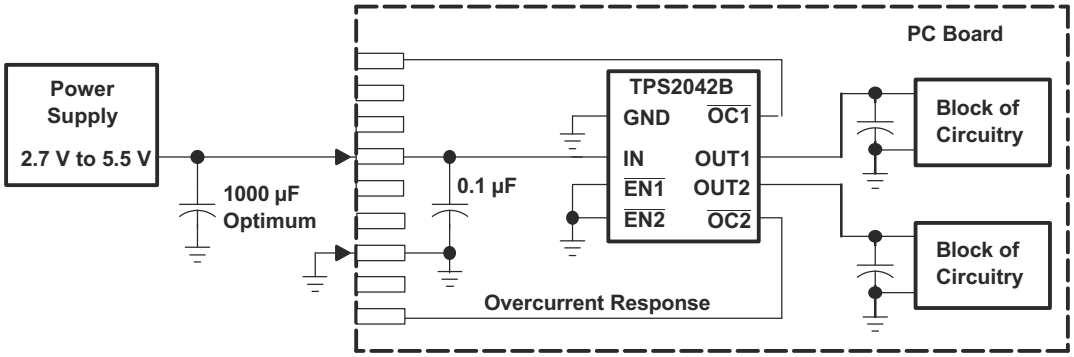

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图 9-26. Typical Hot-Plug Implementation (Example, TPS2042B)

By placing the TPS20xxB between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

9.2.3.1 Design Requirements

表 9-2 shows the design parameters for this application.

表 9-2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	5 V
Output1 voltage	5 V
Output2 voltage	5 V
Output1 current	0.5 A
Output2 current	0.5 A

9.2.3.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Current Limit

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2042 device or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. Preventing voltage undershoots and overshoots is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply. Output capacitance is not required, but TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output to reduce the undershoot, which is caused by the inductance of the output power bus just after a short has occurred and the TPS2042 device has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges.

9.2.3.3 Application Curves

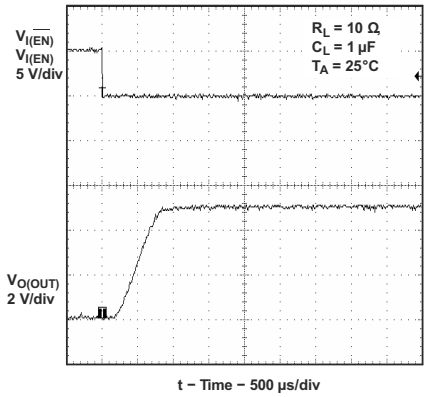

图 9-27. Turnon Delay and Rise Time With 1-µF Load

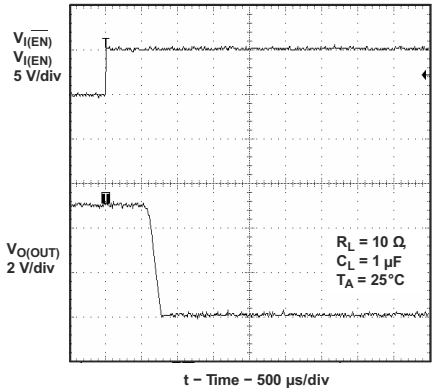

图 9-28. Turnoff Delay and Fall Time With 1-µF Load

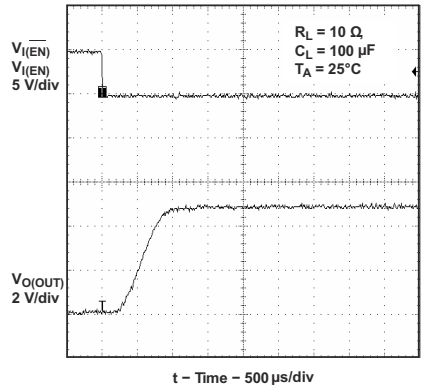

图 9-29. Turnon Delay and Rise Time With 100-µF Load

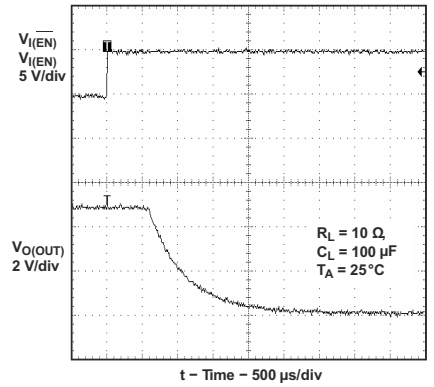

图 9-30. Turnoff Delay and Fall Time With 100-µF Load

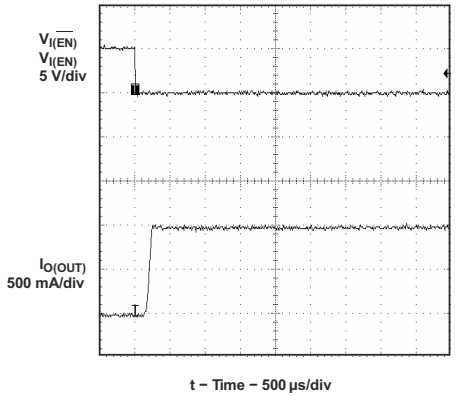

图 9-31. Short-Circuit Current, Device Enabled Into Short

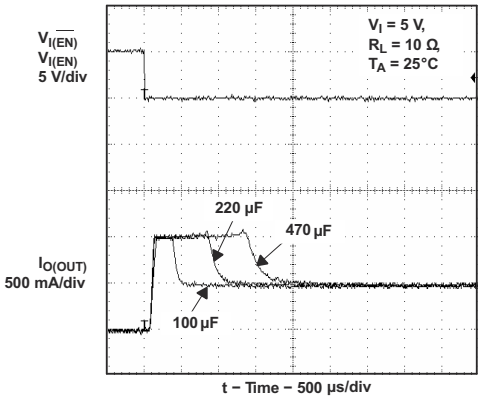

图 9-32. Inrush Current With Different Load Capacitance

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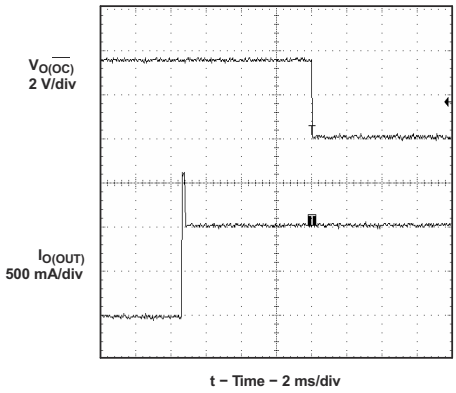

图 9-33. 3-Ω Load Connected to Enabled Device

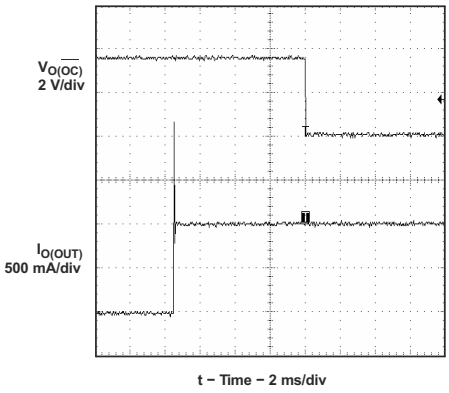

图 9-34. 2-Ω Load Connected to Enabled Device

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10 Power Supply Recommendations

10.1 Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. The UVLO facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

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11 Layout

11.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- Placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

11.2 Layout Example

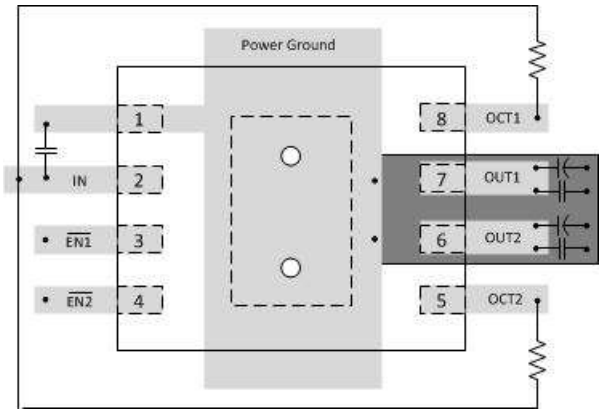

图 11-1. Layout Recommendation

11.3 Power Dissipation

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from 图 6-11. Using this value, the power dissipation per switch can be calculated by 方程式:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature with 方程式:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- T_A= Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

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11.4 Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS20xxB implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

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12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision O (June 2024) to Revision P (August 2024)	Page
• Removed revision history comment about adding TPS2051BDB to this section	22

Changes from Revision N (July 2023) to Revision O (June 2024)	Page
• 将始发日期从 2010 年 6 月更新为 2004 年 4 月，以便与数据表的初始发行日期保持一致	1
• 删除了“功耗额定值”表	1
• Deleted "TPS2042xx and TPS2053xx" in table title	6
• Updated max UVLO and Supply current, high-level output values for the TPS2041BDR, TPS2041BDGNR, TPS2042BDR, TPS2042BDGNR, TPS2051BDR, TPS2051BDGNR, TPS2052BDGNR, and TPS2041BDBVR	7
• Updated Overcurrent trip threshold to apply only to TPS2042B and TPS2052B (DRB packages only)	7
• Updated 节 8.3.7to show that the TPS20x1B and TPS20x2B devices in the D, DGN, and DBV packages do not have overcurrent trip thresholds	22
• Updated 节 8.3.7.1	23
• Updated 节 8.3.7.2	23

Changes from Revision M (June 2016) to Revision N (July 2023)	Page
• 通篇更新了表格、图和交叉参考的编号格式	1

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- Update TPS2051BDBV and TPS2052BD electrical characteristics, including overcurrent trip threshold, high-level output supply current and undervoltage lockout..... 7

Changes from Revision L (June 2011) to Revision M (June 2016) **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 6

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2041BDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PLII
TPS2041BDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PLII
TPS2041BDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PLII
TPS2041BDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2041B
TPS2041BDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2041B
TPS2041BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2041B
TPS2041BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2041B
TPS2041BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2041B
TPS2042BDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2042BDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2042BDGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2042BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2042BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2042BDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRBTG4.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042
TPS2042BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B
TPS2043BD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2043B
TPS2043BD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2043B
TPS2043BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2043B
TPS2043BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2043B
TPS2043BDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2043B
TPS2044BD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B
TPS2044BD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B
TPS2044BDG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B
TPS2044BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2044BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B
TPS2044BDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2044B
TPS2051BDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PLJI
TPS2051BDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLJI
TPS2051BDBVR1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	PLJI
TPS2051BDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	PLJI
TPS2051BDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2051BDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2051BDGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2051BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2051BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2051BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051B
TPS2052BDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052B
TPS2052BDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052B
TPS2052BDGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052B
TPS2052BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052B
TPS2052BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052B
TPS2052BDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052
TPS2052BDRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052
TPS2052BDRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052
TPS2052BDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2052
TPS2052BDRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2052
TPS2052BDRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2052
TPS2052BDRBTG4	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052
TPS2052BDRBTG4.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2052
TPS2053BD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2053B
TPS2053BD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2053B
TPS2053BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2053B
TPS2053BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2053B
TPS2054BD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B
TPS2054BD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2054BDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B
TPS2054BDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B
TPS2054BDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B
TPS2054BDRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2054B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2041B, TPS2042B, TPS2051B :

- Automotive : TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1

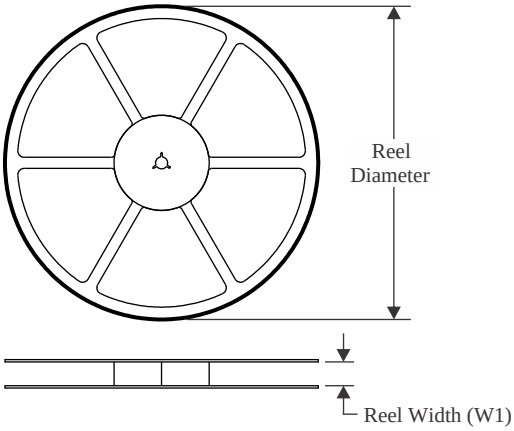
- Enhanced Product : TPS2041B-EP

NOTE: Qualified Version Definitions:

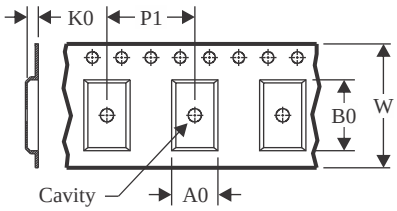
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

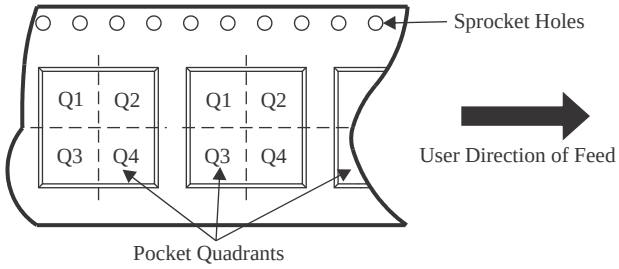


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

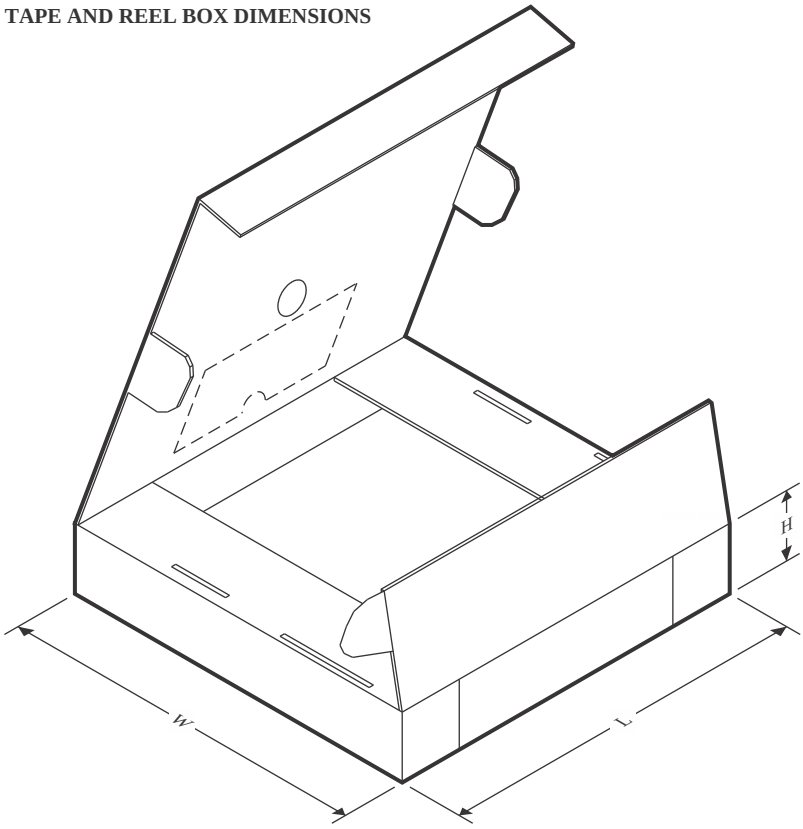


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2041BDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2041BDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041BDGNR	HVSSOP	DGN	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2041BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2041BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2042BDGNR	HVSSOP	DGN	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2042BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2042BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2042BDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2042BDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2042BDRBTG4	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2043BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2044BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2051BDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051BDGNR	HVSSOP	DGN	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2051BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2051BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2052BDGNR	HVSSOP	DGN	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2052BDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2052BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2052BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2052BDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2052BDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2052BDRBTG4	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS2053BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2054BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2054BDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

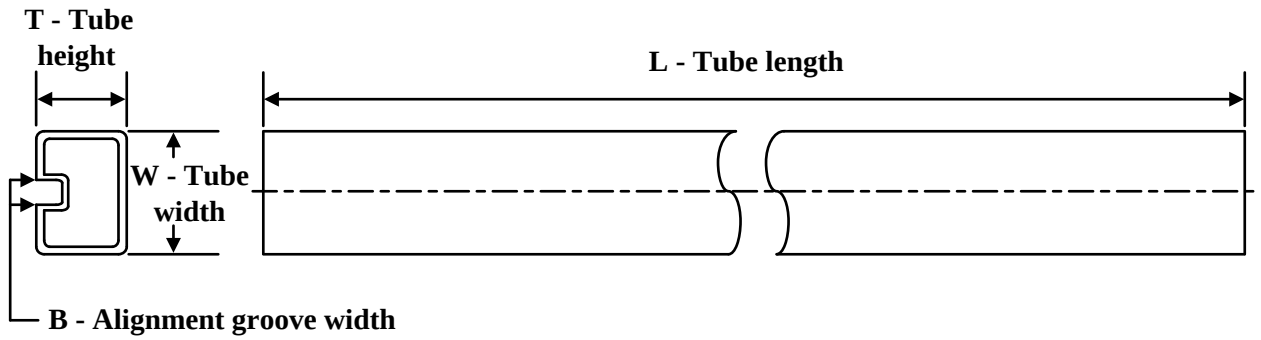


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2041BDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2041BDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2041BDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS2041BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2041BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2042BDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS2042BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2042BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2042BDRBR	SON	DRB	8	3000	346.0	346.0	35.0
TPS2042BDRBT	SON	DRB	8	250	200.0	183.0	25.0
TPS2042BDRBTG4	SON	DRB	8	250	200.0	183.0	25.0
TPS2043BDR	SOIC	D	16	2500	353.0	353.0	32.0
TPS2044BDR	SOIC	D	16	2500	353.0	353.0	32.0
TPS2051BDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051BDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS2051BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2051BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2052BDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2052BDGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2052BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2052BDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS2052BDRBR	SON	DRB	8	3000	346.0	346.0	35.0
TPS2052BDRBT	SON	DRB	8	250	200.0	183.0	25.0
TPS2052BDRBTG4	SON	DRB	8	250	200.0	183.0	25.0
TPS2053BDR	SOIC	D	16	2500	340.5	336.1	32.0
TPS2054BDR	SOIC	D	16	2500	353.0	353.0	32.0
TPS2054BDRG4	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2043BD	D	SOIC	16	40	507	8	3940	4.32
TPS2043BD.A	D	SOIC	16	40	507	8	3940	4.32
TPS2044BD	D	SOIC	16	40	507	8	3940	4.32
TPS2044BD.A	D	SOIC	16	40	507	8	3940	4.32
TPS2044BDG4	D	SOIC	16	40	507	8	3940	4.32
TPS2053BD	D	SOIC	16	40	507	8	3940	4.32
TPS2053BD.A	D	SOIC	16	40	507	8	3940	4.32
TPS2054BD	D	SOIC	16	40	507	8	3940	4.32
TPS2054BD.A	D	SOIC	16	40	507	8	3940	4.32

GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

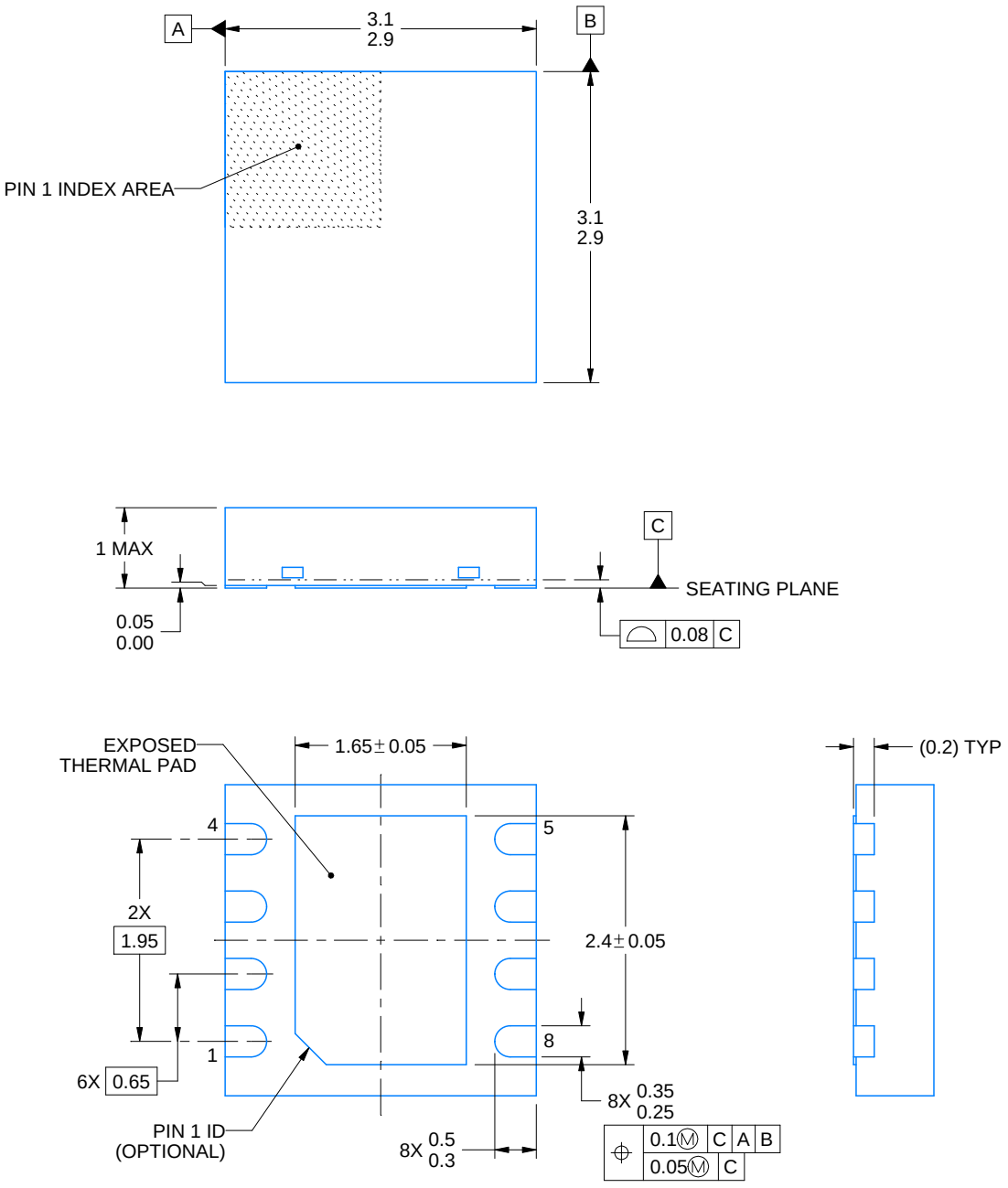
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRB0008B

PACKAGE OUTLINE

VSON - 1 mm max height

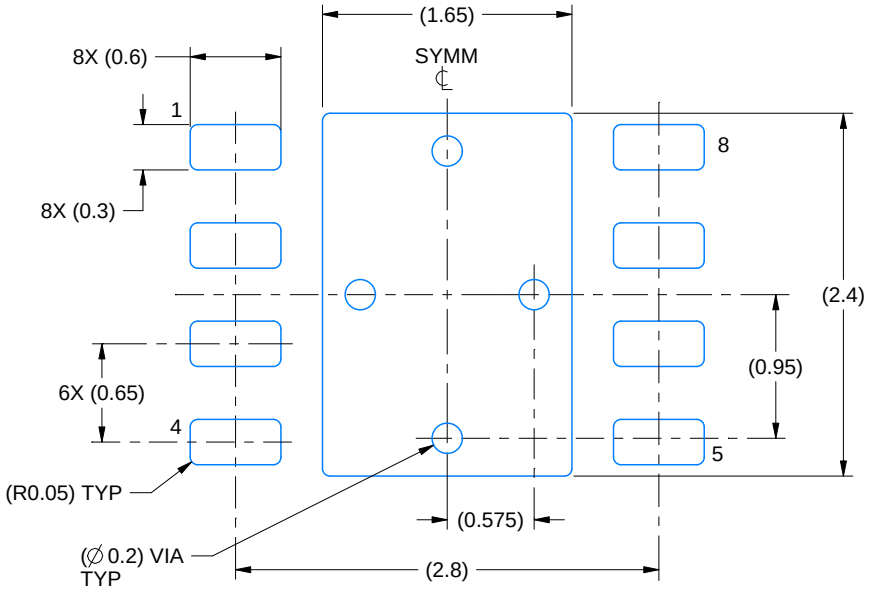
PLASTIC SMALL OUTLINE - NO LEAD



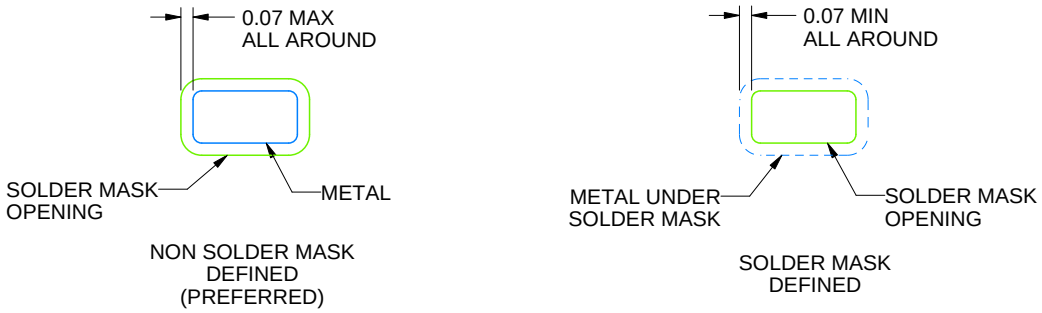
4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

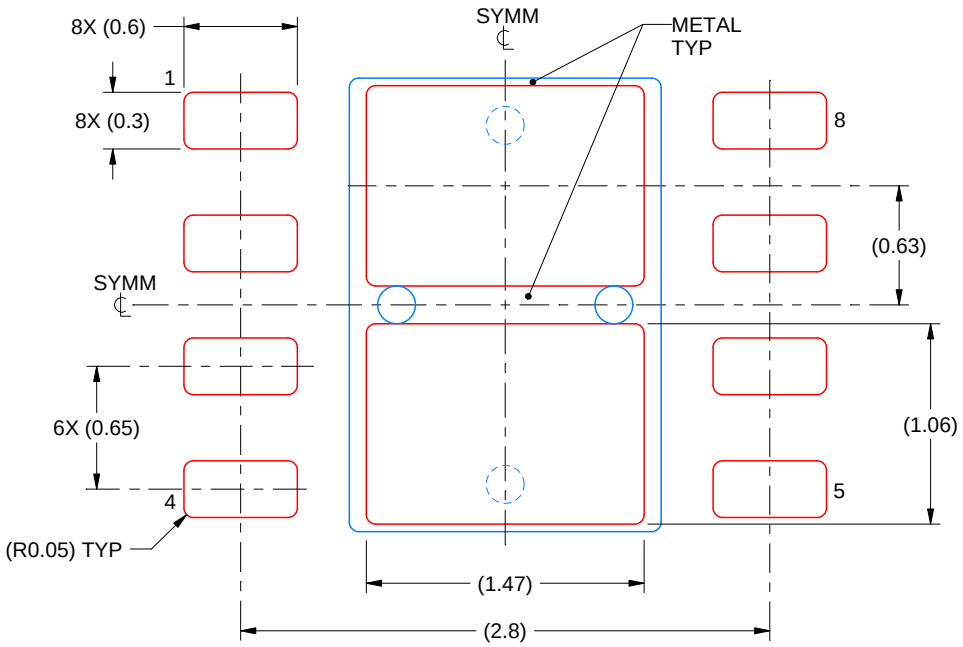
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

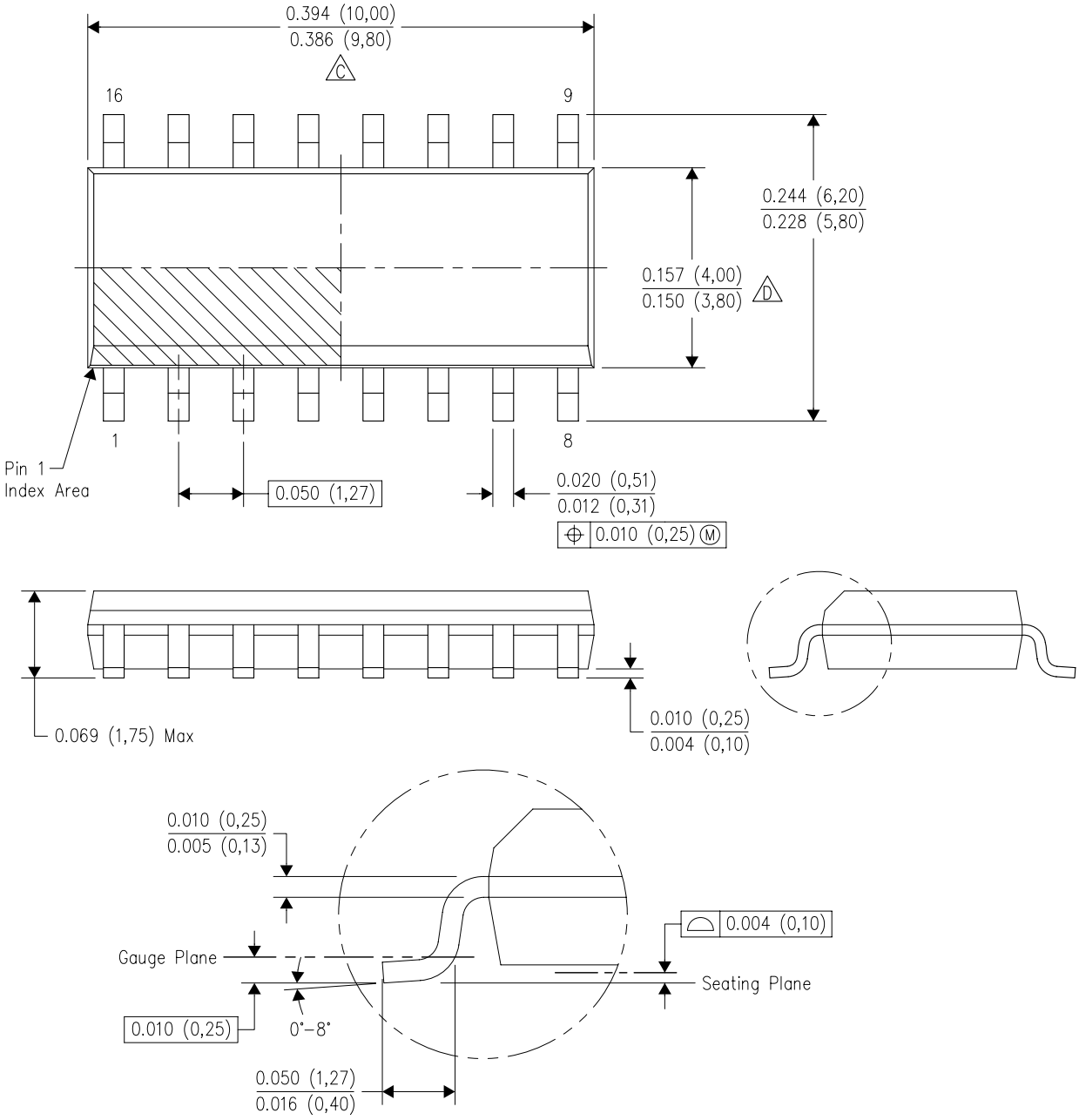
EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

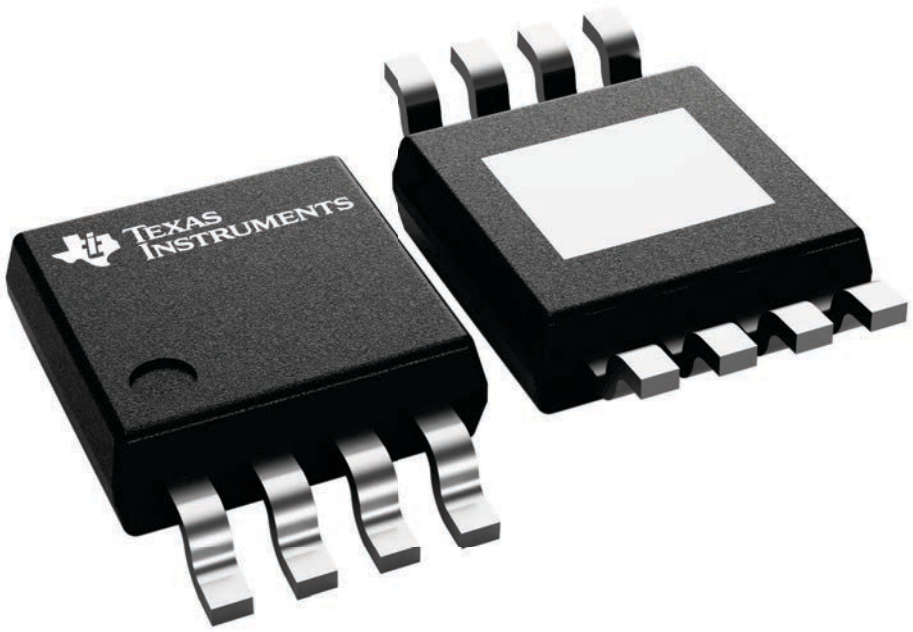
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

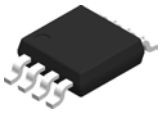
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



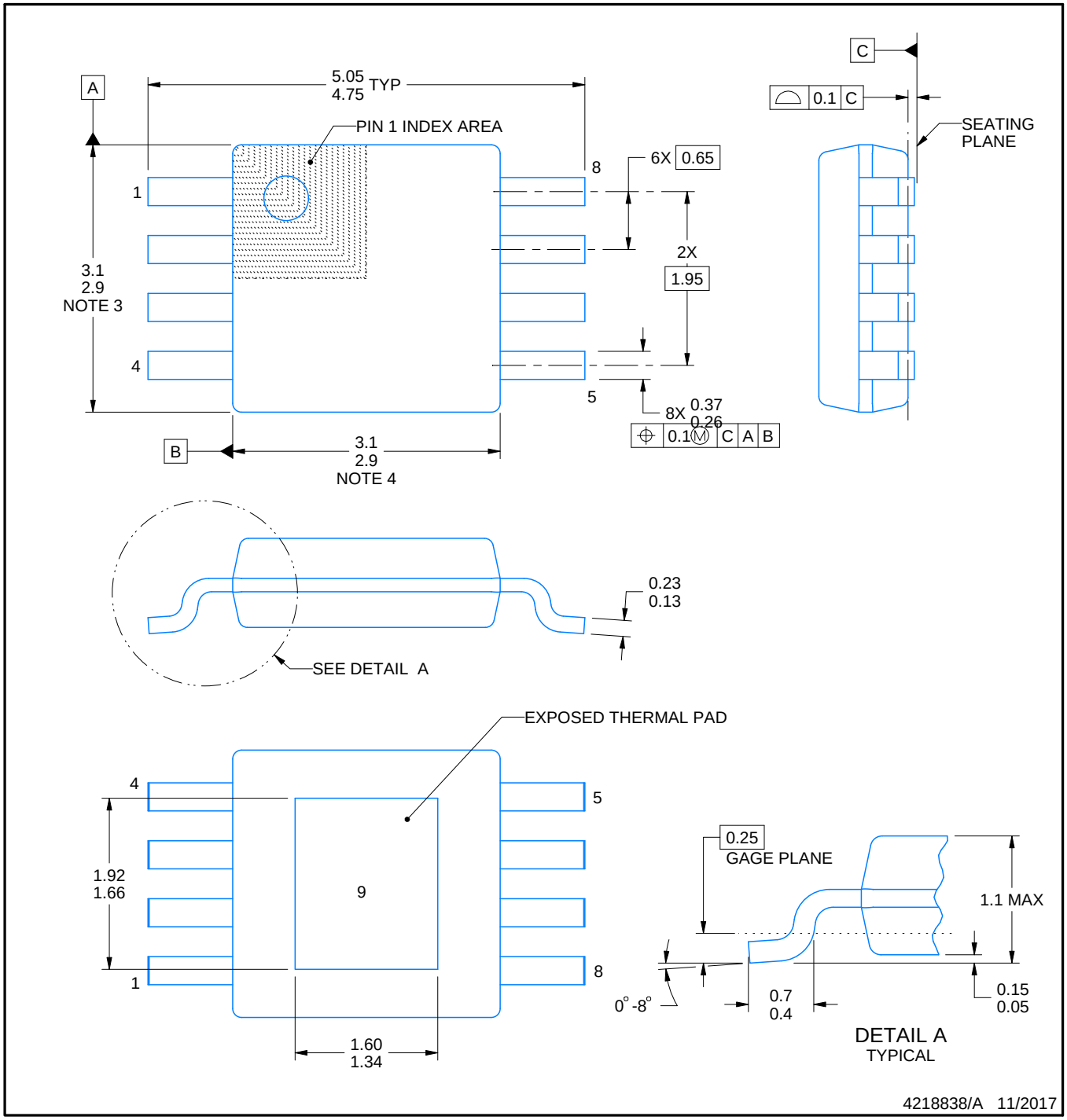
PACKAGE OUTLINE

DGN0008C



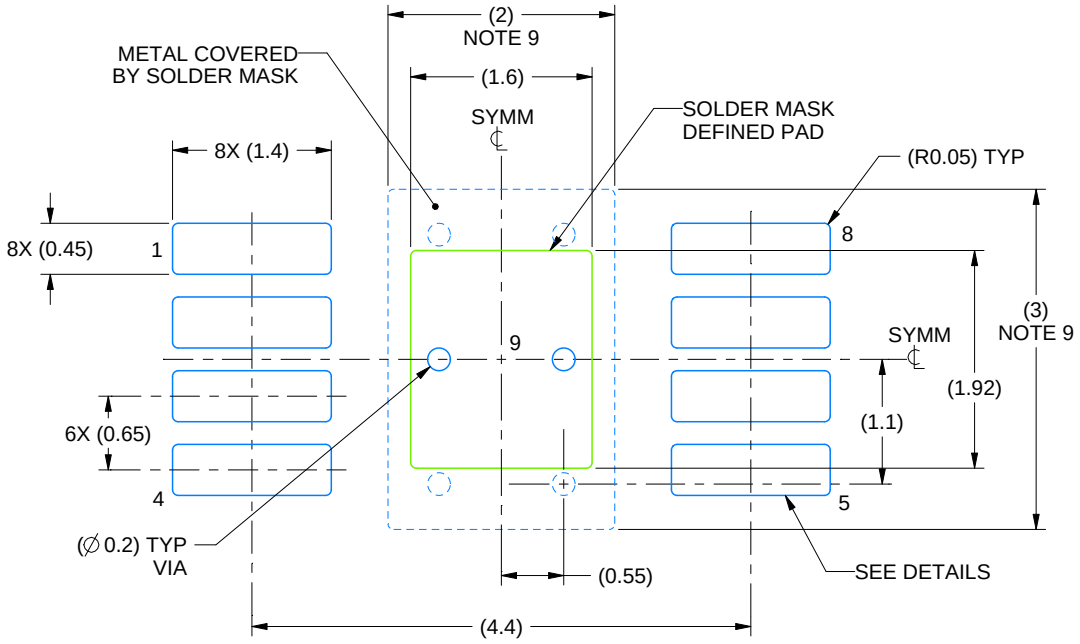
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

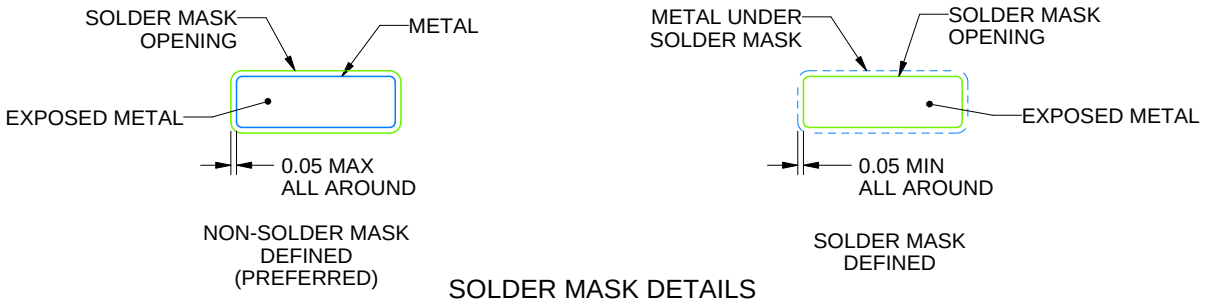


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

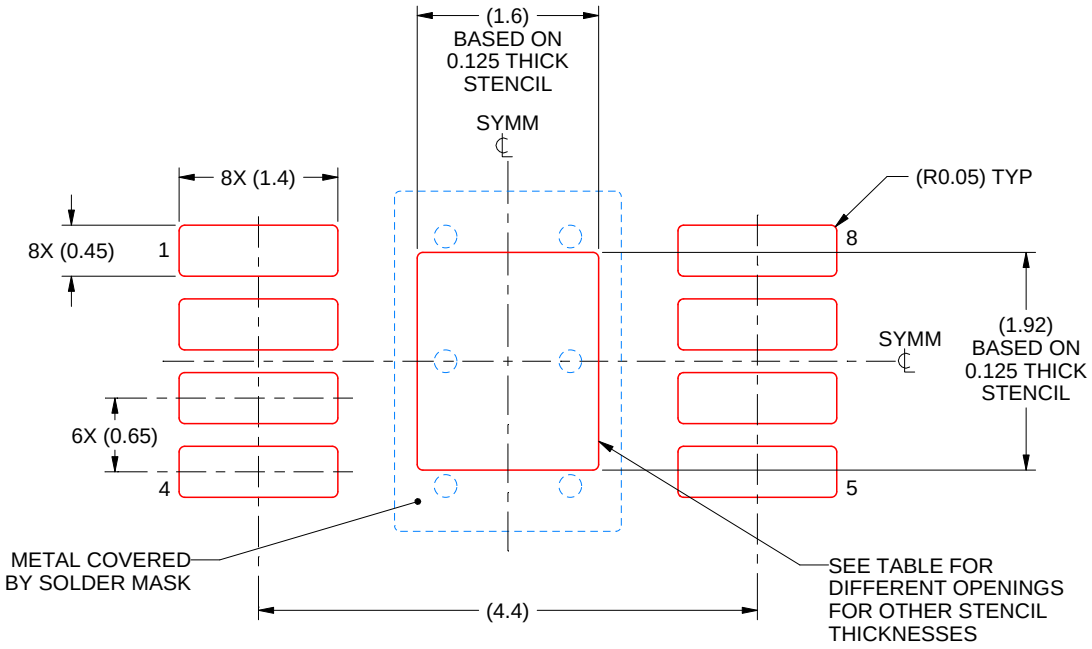


SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

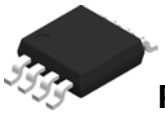
4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

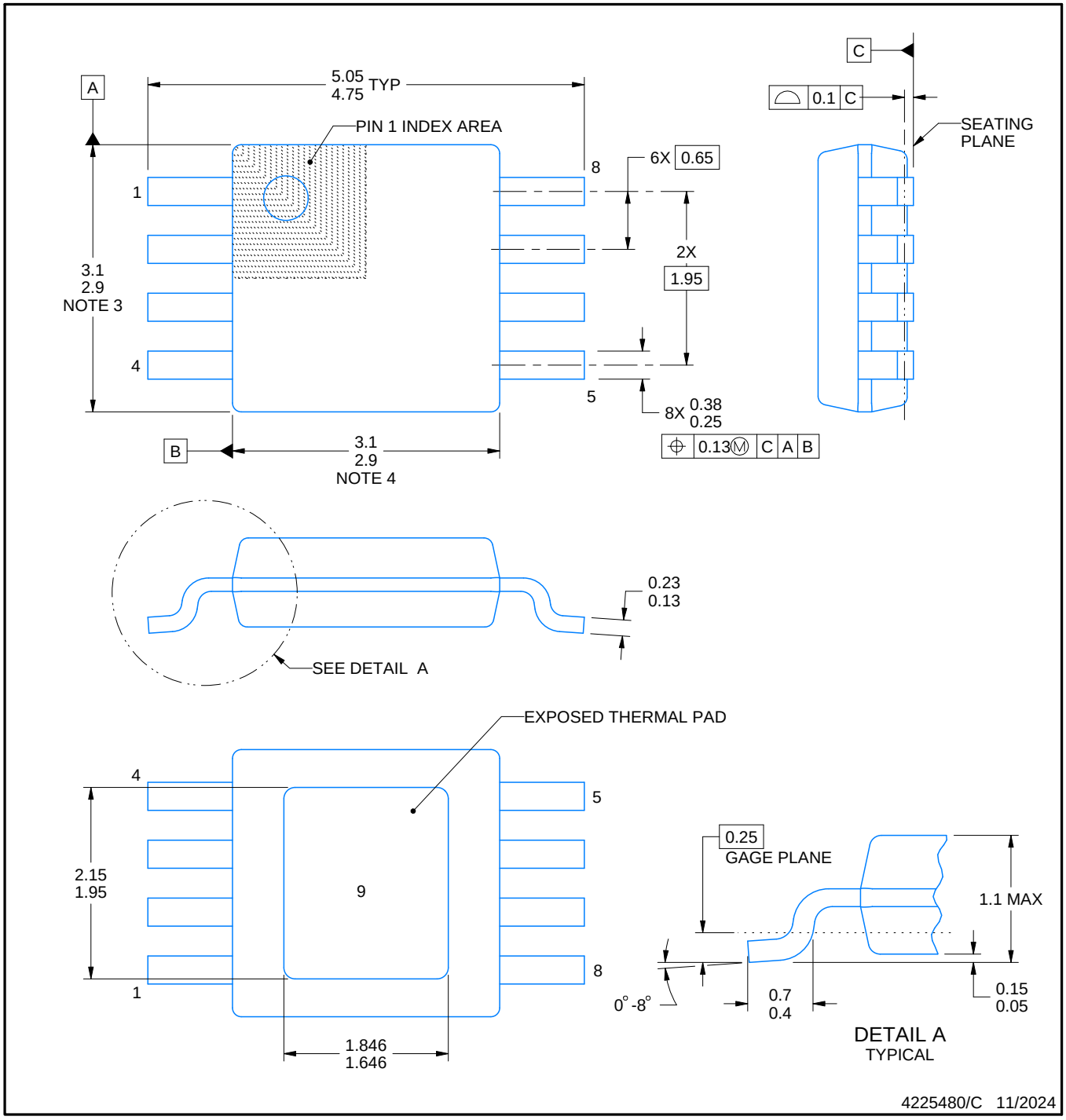
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

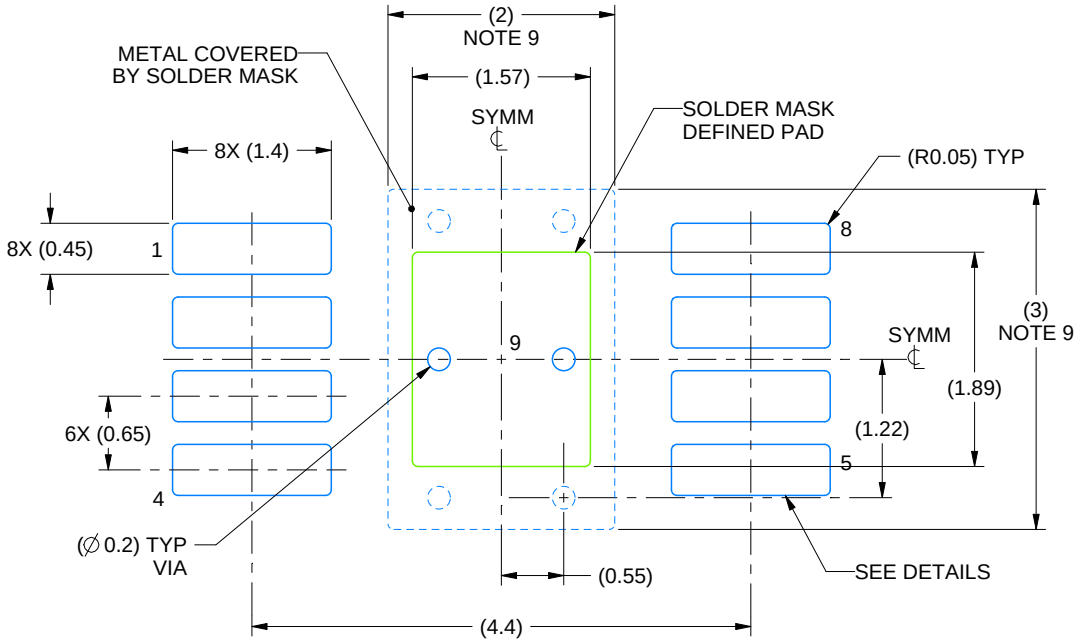
SMALL OUTLINE PACKAGE



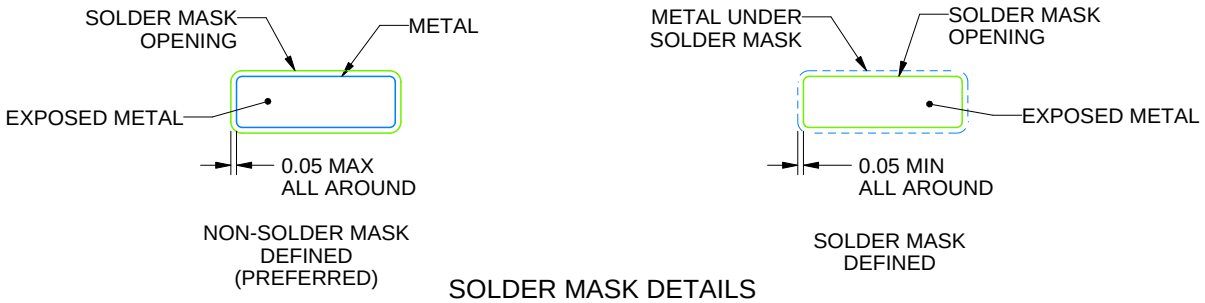
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

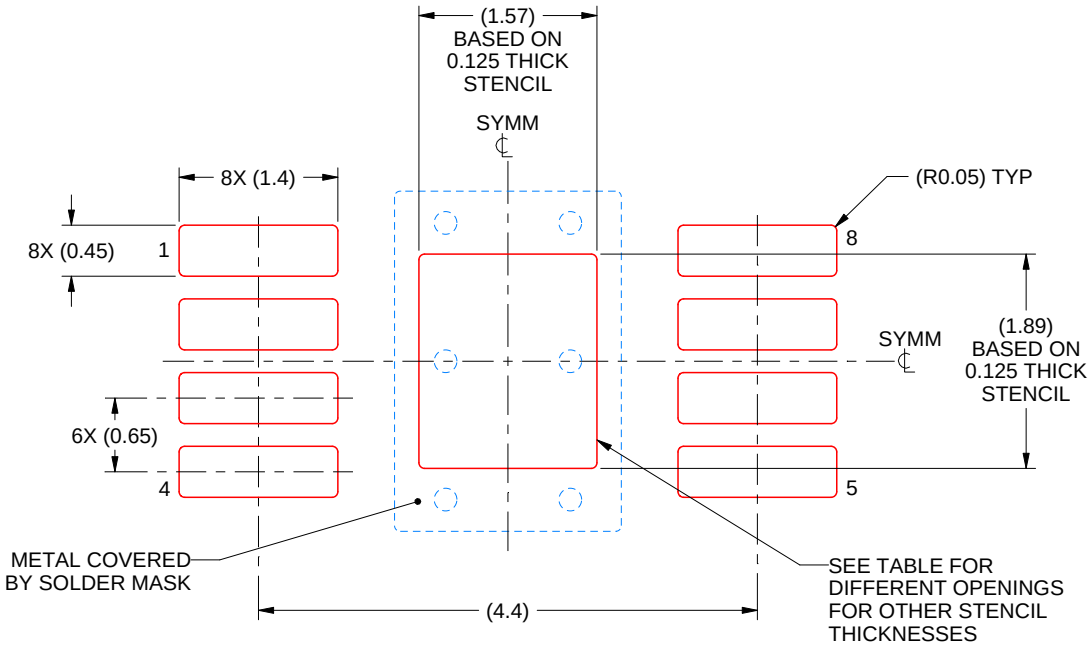


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

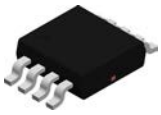
4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

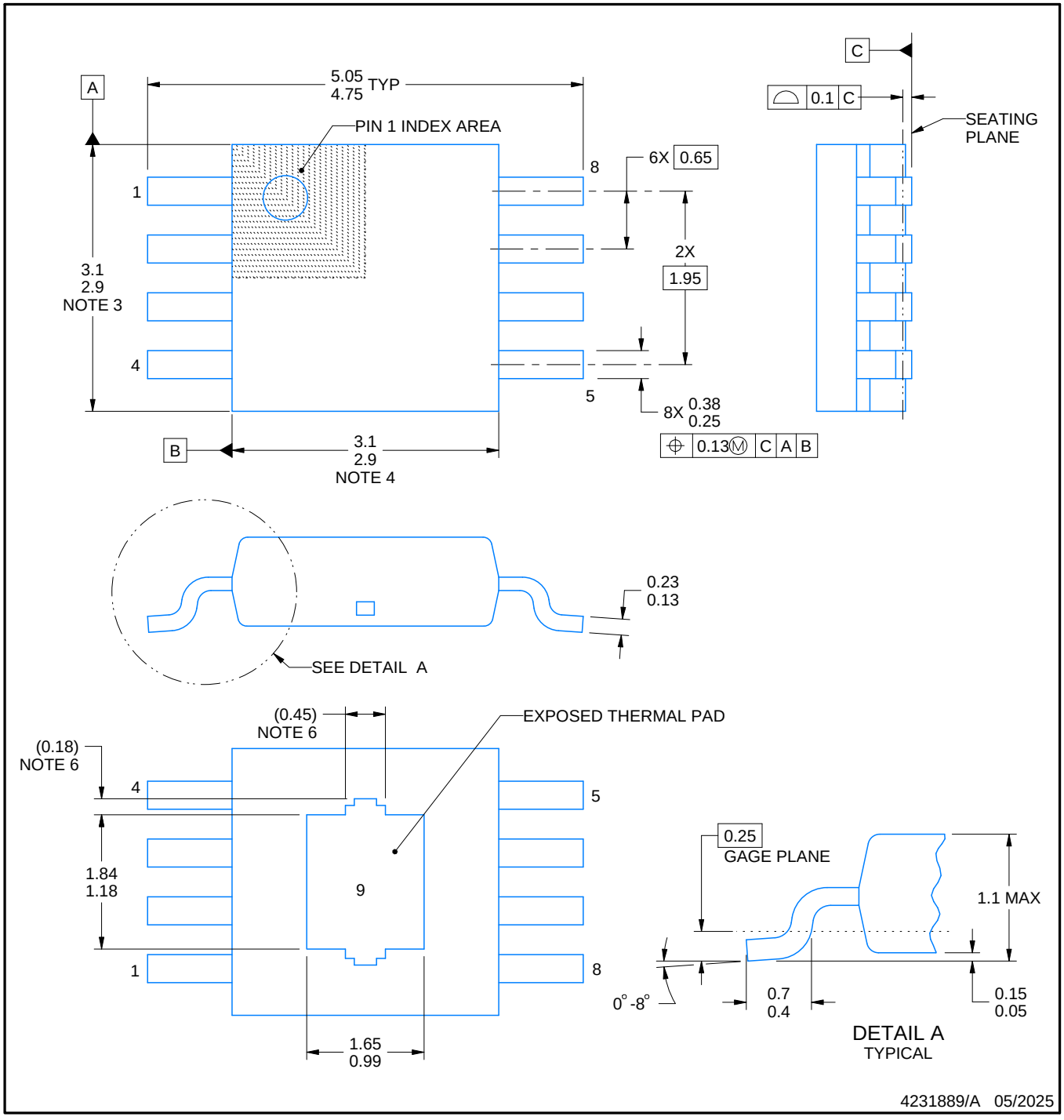
PACKAGE OUTLINE

DGN0008K



PowerPAD™ VSSOP - 1.1 mm max height

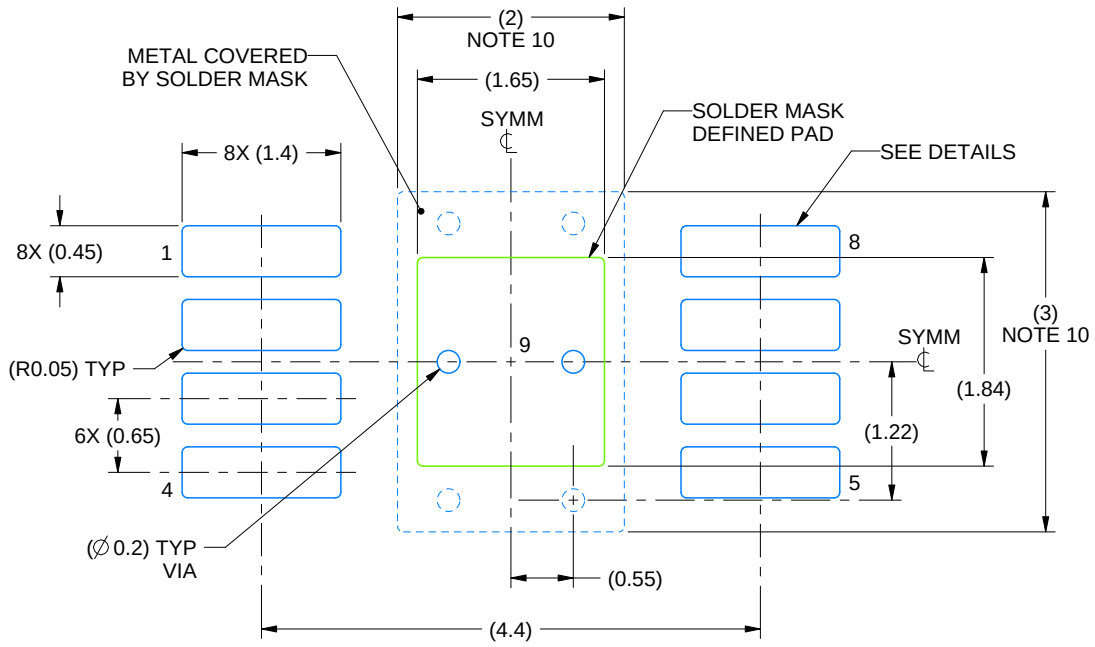
SMALL OUTLINE PACKAGE



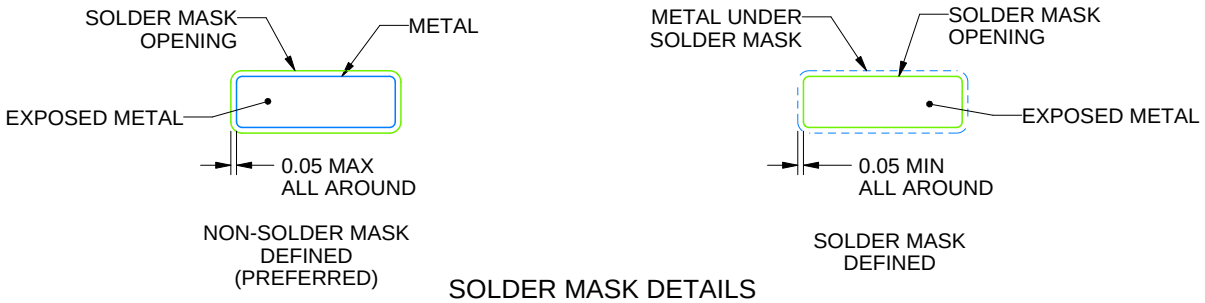
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

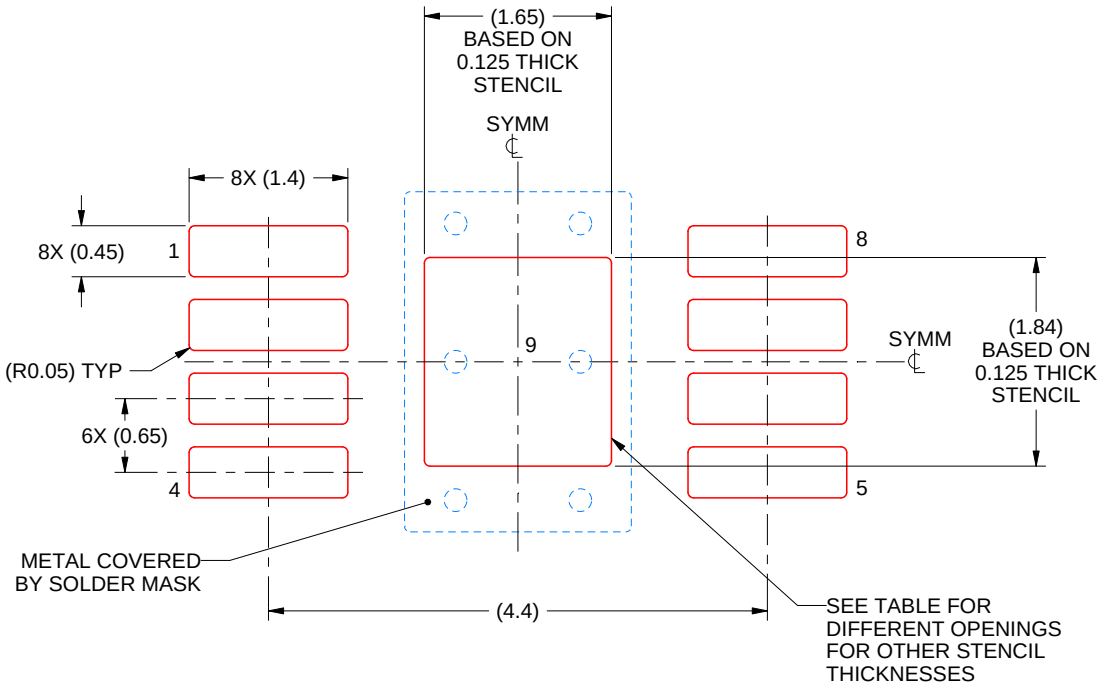


SOLDER MASK DETAILS

4231889/A 05/2025

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



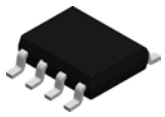
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 2.06
0.125	1.65 X 1.84 (SHOWN)
0.15	1.51 X 1.68
0.175	1.39 X 1.56

4231889/A 05/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

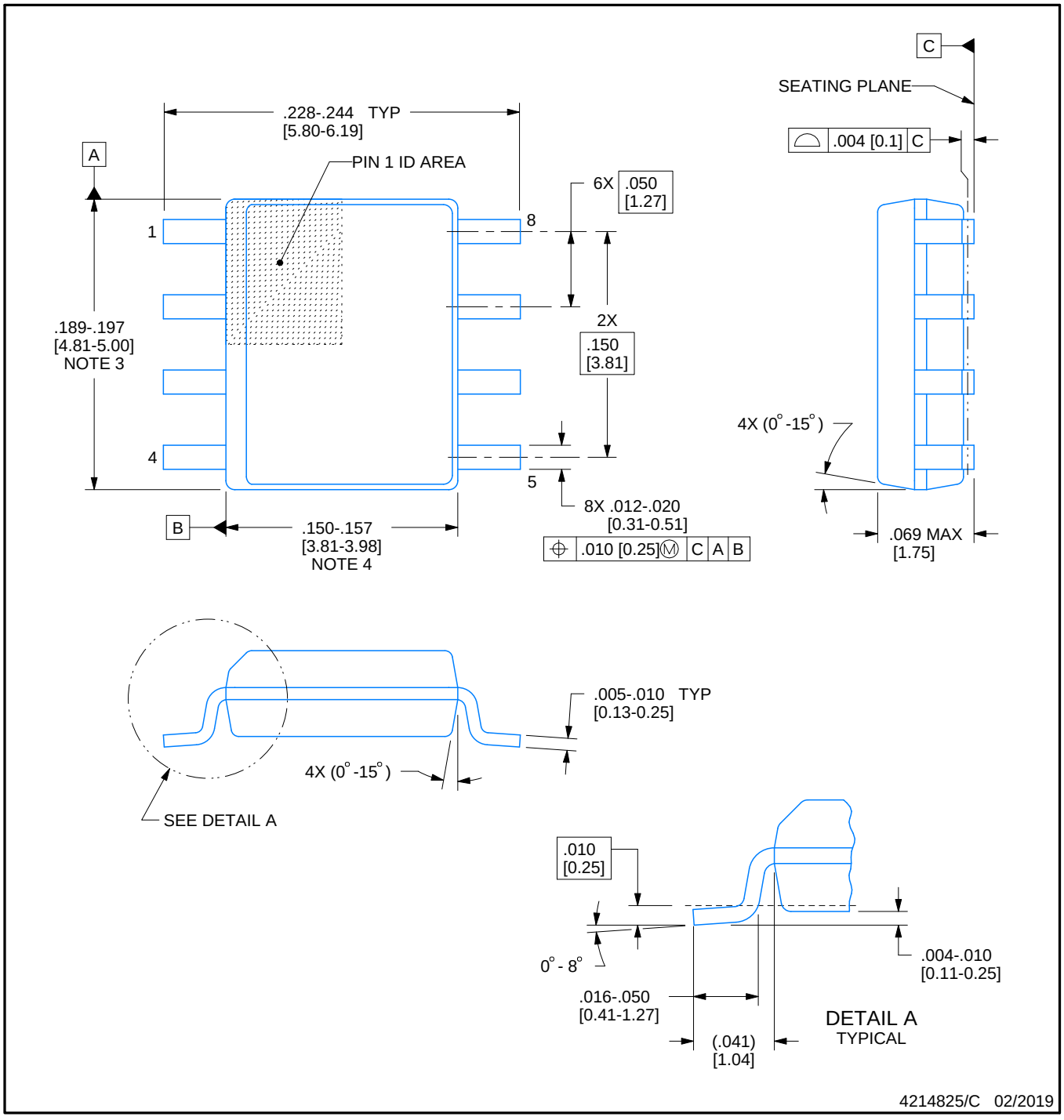


PACKAGE OUTLINE

D0008A

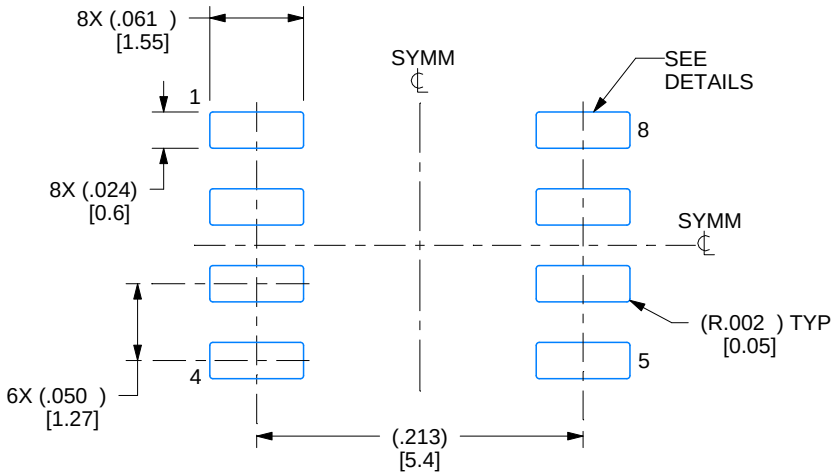
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

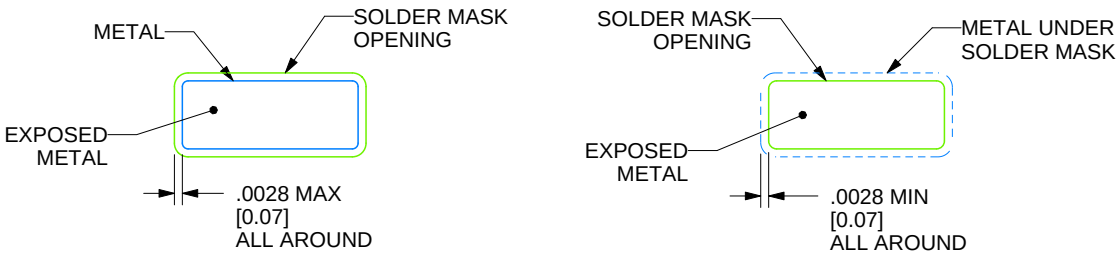


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

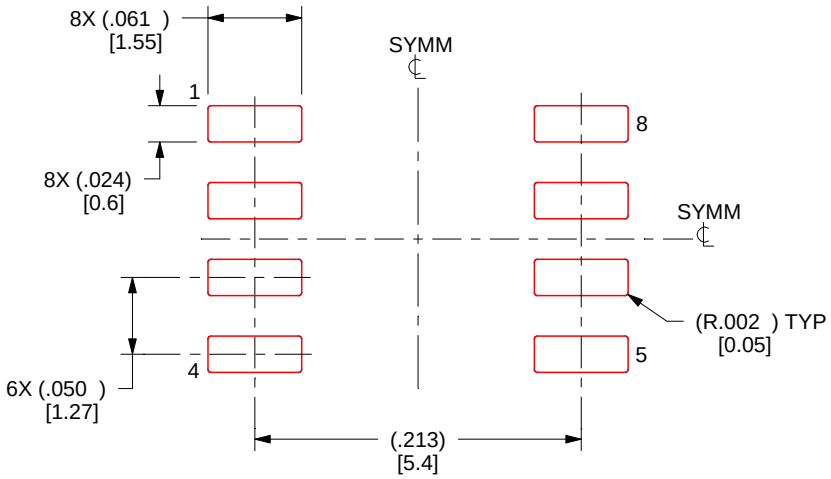
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

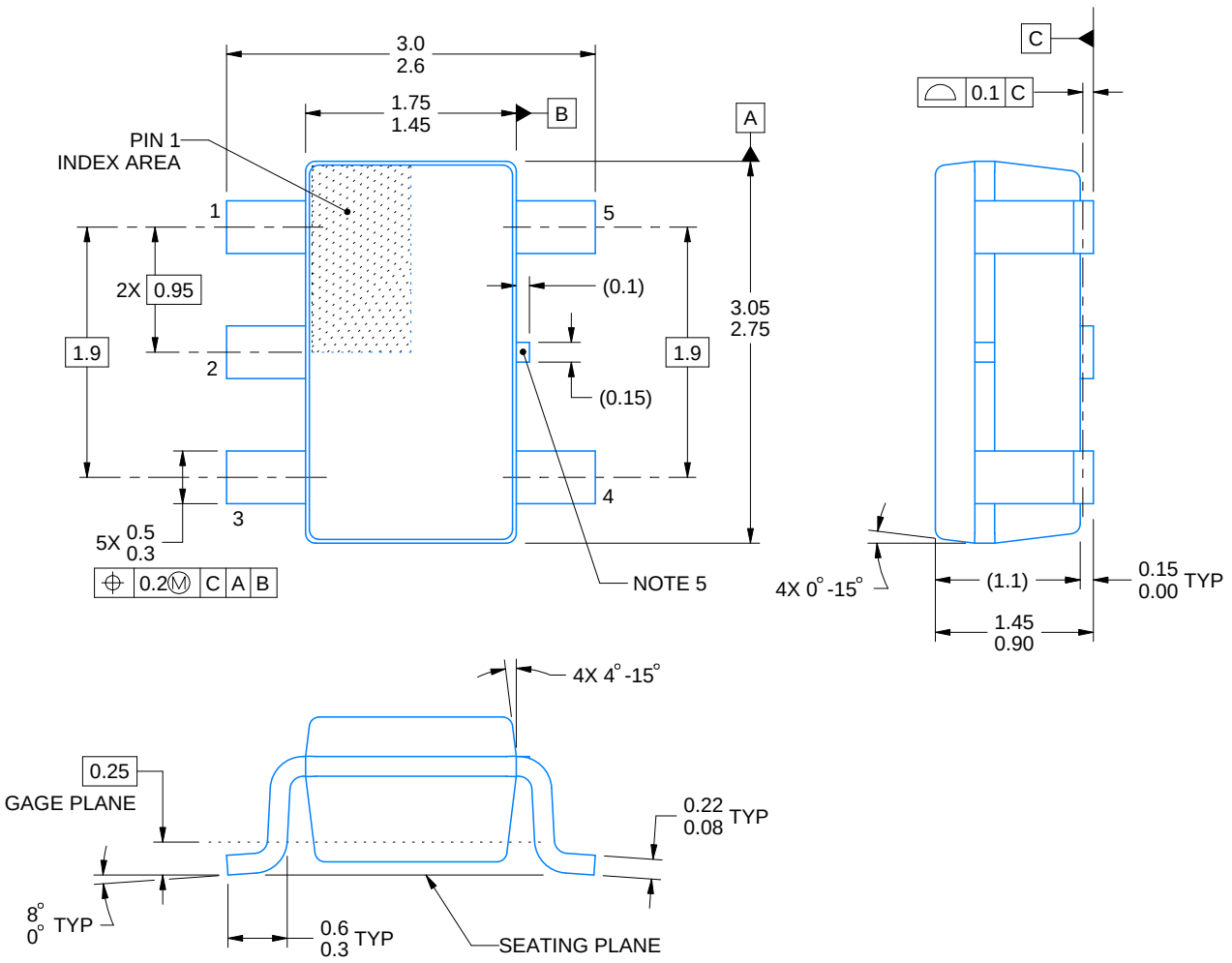
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

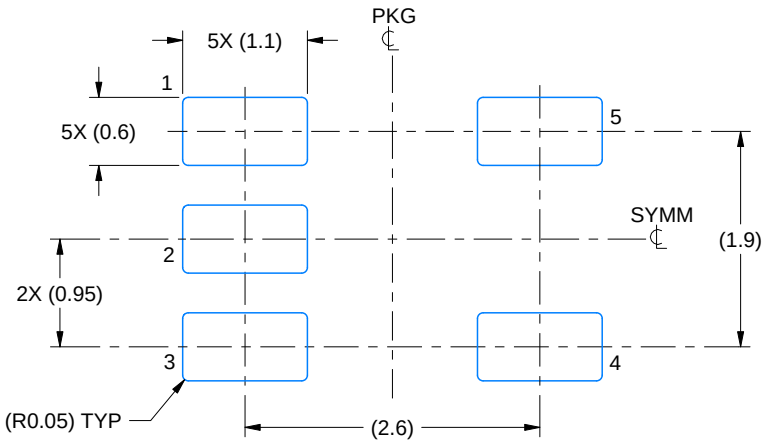
SMALL OUTLINE TRANSISTOR



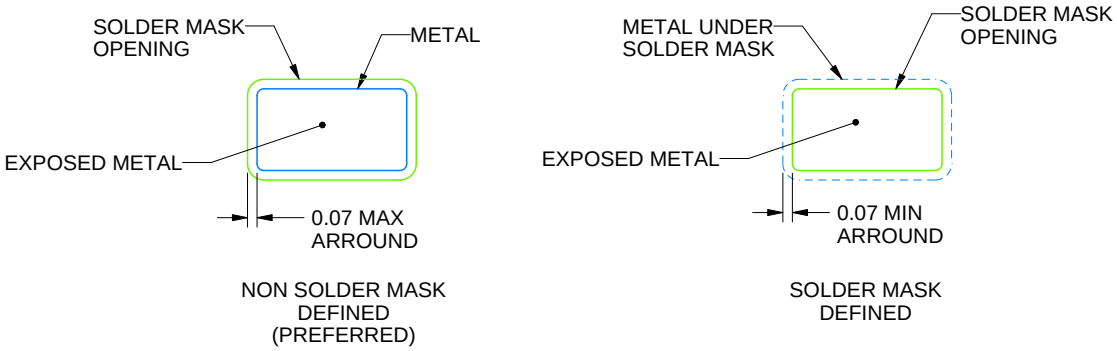
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

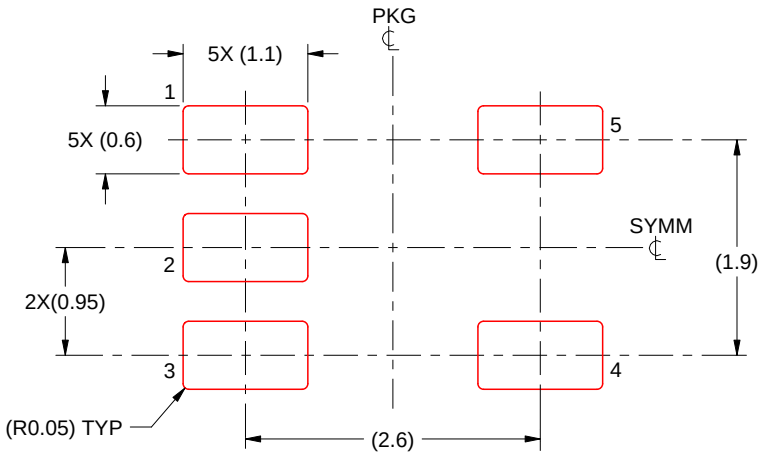


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月