TPIC2010 具有双通道 DC-DC 转换器、由串行接口控制的 9 通道电机驱动器

1 特性

- 串行外设接口
  - 最大读写频率 35MHz
  - 3.3V 数字 I/O
- 执行器和电机驱动器
  - 具有 H 桥输出的脉冲宽度调制 (PWM) 控制
  - 具有 12 位数模转换器 (DAC) 控制的聚焦/跟踪/倾斜执行器驱动器
  - 具有电流模式、10 位 DAC 控制的滑动电机驱动器
  - 具有 12 位 DAC 控制的负载驱动器
  - 具有 8 位 PWM 控制的步进电机驱动器
  - 无需位置传感器即可检测准直透镜和滑动结束位置
- 主轴电机驱动器
  - 无传感器反电动势 (BEMF) 位置反馈
  - 12 位主轴 DAC
  - 独立的感应位置感测和启动
  - 通过自动控制制动实现急停：主动制动和短制动
  - 最大持续电流为 0.7A，不存在散热问题
  - LS 模式：25% 速度
- 片上温度计（15°C 至 172.5°C）
- 开关
  - 两个可由软件控制的开关电路
  - 发光二极管 (LED)：具有 0.1A 过流保护 (OCP) 的 LED 驱动器开关
  - CSW：具有 0.1A OCP 的低 $R_{DS(ON)}$ 电流开关
- DC-DC 转换器
  - V1Px：可通过引脚选择的转换电压 1.0V/1.2V/1.5V；0.9A 输出能力，1.85A 过流保护
  - V3P3：固定 3.3V DC-DC 转换器；0.5A 输出能力，1.15A 过流保护
  - 2.5MHz 开关频率
  - 通过*断续稳压模式*在低电流下提高效率
- 保护
  - LED/CSW、开关、DCDC 转换器、SPM 和执行器上均配有独立的热保护电路
  - 两个警报级别：热保护中的*预检测*和*检测*
  - ACTTEMP：监视由过去累积的 DAC 值计算得出的执行器温度
  - 欠压锁定 (UVLO) 和过压保护 (OVP)

2 应用

- 蓝光碟™播放器
- DVD 播放器
- CD 播放器
- 光盘驱动器

3 说明

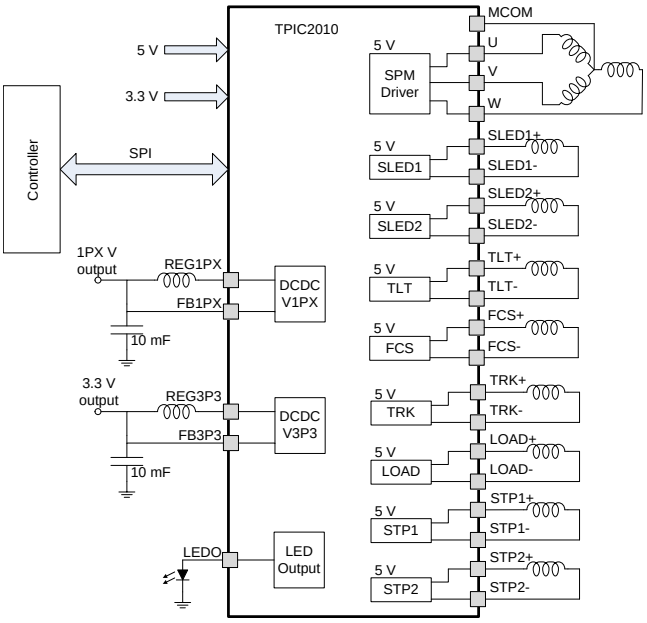
TPIC2010 是一款适用于薄型或超薄 ODD 的超低噪声电机驱动器集成电路 (IC)。该驱动器 IC 有 9 条通道且由串行接口控制，非常适用于驱动主轴电机、滑动电机（适用的步进电机）、负载电机以及针对准直透镜的聚焦/跟踪/倾斜执行器和步进电机。该驱动器 IC 具有 1 个双通道同步 DC-DC 转换器。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPIC2010DFD	带散热片薄型小外形尺寸封装 (HTSSOP) (56)	14.00mm x 6.10mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化框图



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4 修订历史记录

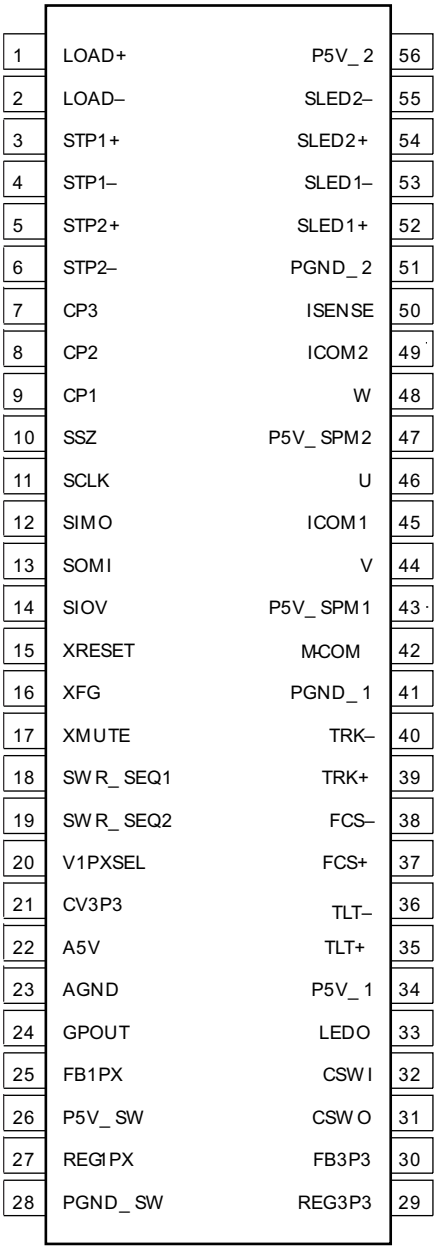
日期	修订版本	注释
2015 年 12 月	*	最初发布。

5 说明（续）

DC-DC 转换器的断续稳压模式能够以较低功耗显著提升效率。主轴电机驱动器利用 BEMF 反馈来进行启动、控制和低噪声操作，无需外部传感器。此外，TPIC2010 还具有诸多保护特性，包括主轴输出电流限制、热关断、滑动和准直透镜结束检测、执行器保护以及电源复位电路。TPIC2010 还内置有温度计，以便于测量 IC 温度。

6 Pin Configuration and Functions

DFD Package
56-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
A5V	22	PS	Power supply terminal for internal logic 5 V
AGND	23	PS	Ground terminal for internal logic
CP1	9	MISC	Capacitance connection for charge pump
CP2	8	MISC	Capacitance connection for charge pump
CP3	7	MISC	Capacitance connection for charge pump
CSWI	32	PS	Power supply terminal for 5-V OEIC power switch
CSWO	31	O	Power switch output for 5-V OEIC in OPU
CV3P3	21	MISC	Capacitance terminal for internal 3.3-V core
FB1PX	25	I	Feedback input terminal for 1PX converter
FB3P3	30	I	Feedback input terminal for 3.3-V DC-DC converter
FCS–	38	O	Focus negative output terminal
FCS+	37	O	Focus positive output terminal
GPOUT	24	O	General-purpose output (test monitor)
ICOM1	45	MISC	Current sense resister terminal for spindle driver
ICOM2	49	MISC	Current sense resister terminal for spindle driver
ISENS	50	I	Current sense input terminal for spindle drivers
LEDO	33	O	LED output terminal
LOAD–	2	O	Load negative output terminal
LOAD+	1	O	Load positive output terminal
M-COM	42	I	Motor center tap connection
P5V_1	34	PS	Power supply terminal for TI/F/T drivers
P5V_2	56	PS	Power supply terminal for SLED channel drivers
P5V_SPM1	43	PS	Power supply terminal for spindle driver
P5V_SPM2	47	PS	Power supply input for spindle driver
P5V_SW	26	PS	Power supply terminal for DCDC converters
PGND_1	41	PS	GND terminal for Ti/F/T channel drivers
PGND_2	51	PS	GND terminal for SLED channel drivers
PGND_SW	28	PS	GND terminal for DCDC converters
REG1PX	27	O	REG1PX DCDC converter switching output (GPOUT1(2))
REG3P3	29	O	REG3P3 DCDC converter switching output terminal (GPOUT2)
SCLK	11	I	SIO serial clock input terminal
SIMO	12	I	SIO slave input master output terminal
SIOV	14	PS	Power supply terminal for serial port 3.3-V typical
SLED1–	53	O	Sled1 negative output terminal
SLED1+	52	O	Sled1 positive output terminal
SLED2–	55	O	Sled2 negative output terminal
SLED2+	54	O	Sled2 positive output terminal
SOMI	13	O	SIO slave output master input terminal
SSZ	10	I	SIO slave select low active input terminal
STP1–	4	O	STP1 negative output terminal for collimator
STP1+	3	O	STP1 positive output terminal for collimator
STP2–	6	O	STP2 negative output terminal for collimator
STP2+	5	O	STP2 positive output terminal for collimator
SWR_SEQ1	18	I	Internal DC/DC converter startup sequence setting
SWR_SEQ2	19	I	Internal DC/DC converter startup sequence setting

(1) I: Input; O: Output; PS: Power; MISC: Miscellaneous
(2) To use as a GPOUT output pin, disable both DC-DC converters' output.

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
TLT–	36	O	Tilt negative output terminal
TLT+	35	O	Tilt positive output terminal
TRK–	40	O	Tracking negative output terminal
TRK+	39	O	Tracking positive output terminal
U	46	O	U phase output terminal for spindle motor
V	44	O	V phase output terminal for spindle motor
V1PXSEL	20	I	V1Px output voltage setting
W	48	O	W phase output terminal for spindle motor
XFG	16	O	Motor speed signal output, internally pulled up to SIOV
XMUTE	17	I	XMUTE input terminal to reset the driver IC (optional)
XRESET	15	O	Power-on reset output Internally pulled up to SIOV

7 Specifications

7.1 Absolute Maximum Ratings

see (1)(2)

		MIN	MAX	UNIT
	5-V supply voltage A5V, P5V		6	V
	Spindle output peak voltage(3)		7	V
	Input/output voltage	–0.3	V_{CC} + 0.3 V	V
	Spindle output current		1.0	A
	Spindle output peak current (PW ≦ 2 ms, Duty ≦ 30%)		2.5	A
	Sled output peak current		0.8	A
	Focus/tilt/tracking driver output peak current		1.5	A
	Load driver output peak current		0.8	A
	Power dissipation(4)		1344	mW
	Operating temperature	–20	75	°C
T_{stg}	Storage temperature	–50	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND.
(3) The output voltage generated with regeneration current at the time of output is off states.
(4) A lower $R_{\theta JC}$ is attainable if the exposed pad is connected to a large copper ground plane. $R_{\theta JC}$ and $R_{\theta JA}$ are values for 56-pin TSSOP without a exposed heat slug (HSL) on bottom. Actual thermal resistance would be better than the above values.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
A5V	Operating supply voltage (apply for A5V)	4.5	5.0	5.5	V
P5V	Driver 5V supply voltage (apply for P5V)	A5V – 0.2	A5V	A5V + 0.2	V
CSWIV	CSWI input voltage (apply for P5V)	A5V – 0.2	A5V	A5V + 0.2	V
V_{SIOV}	SIOV voltage	3.0	3.3	3.6	V
V_{SIFH}	SIMO, SSZ, SCLK pin “H” level input voltage range	2.2		SIOV + 0.2	V
V_{SIFL}	SIMO, SSZ, SCLK pin “L” level input voltage range	–0.2		0.8	V
V_{IHB}	XMUTE, SWR_SEQ1, SWR_SEQ2, V1pXSEL pin “H” level input voltage	2.2		A5V + 0.1	V
V_{ILB}	XMUTE, SWR_SEQ1, SWR_SEQ2, V1pXSEL pin “L” level input voltage range	–0.1		0.8	V
I_{SPMOA}	Spindle output average current (U, V, W total)			700	mA
I_{SPMO}	Spindle output current			700	mA
I_{SLDOA}	Sled output average current			400	mA
I_{Ld1Px}	1pXV switching regulator load current			900	mA
I_{Ld3P3}	3p3V switching regulator load current			500	mA
I_{ACTOA}	Focus / tracking / tilt / loading output average current			400	mA
I_{CSWOA}	CSWO output average current			200	mA
I_{STPOA}	STP output average current			200	mA
F_{ck}	SCLK frequency	30	33.8688	35	MHz
T_O	Operating temperature range	–20	25	75	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPIC2010 DFD (HTSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics – Serial Port Voltage Levels

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOMI	High-level output voltage, V_{OH}	I_{OH} = 1 mA	80% SPIOV			V
SOMI	Low-level output voltage, V_{OL}	I_{OL} = 1 mA			20% SPIOV	V
SIMO	High-level input voltage, V_{IH}		70% SPIOV			V
SIMO	Low level input voltage, V_{IL}				20% SPIOV	V
SIMO	Input rise/fall time	10% → 90% PIOV			3.5	ns
SIMO	Output rise/fall time(1)	Cload = 30 pF,10% → 90% SPIOV			10	ns
SCLK	Internal pulldown resistance			200		kΩ
SSZ	Internal pullup resistance			200		kΩ

(1) Specified by design

7.6 Electrical Characteristics – Common Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISTBY	Stand by Supply current	SWR_SEQ1 = SWR_SEQ2 = V1PxSEL = A5V			1	mA
VCV3	CV3P3 Output voltage	Iload = 25 mA	3.135	3.3	3.465	V
RXM	XMUTE pulldown resistor		100	200	300	kΩ
RSW1	SWR_SEQ1 pulldown resistor		100	200	300	kΩ
RSW2	SWR_SEQ2 pulldown resistor		100	200	300	kΩ
RSELS1	V1PxSEL pulldown resistor		100	200	300	kΩ
RXRST	XRESET pullup resistor		16.5	33	49.5	kΩ
VXRST	XRESET low level output voltage	SIOV = 3.3 V, I_{OL} = –100 µA			0.3	V
TPOR	Power-On Reset delay		15	20	25	ms
RXFG	XFG output resistor		100	200	300	Ω
VXFGH	XFG high level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OH} = 100 µA	2.7			V
VXFGL	XFG low level output voltage	SIOV = 3.3 V, XSLEEP = 1, I_{OL} = –100 µA			0.3	V
RGPO	GPOUT output resistor		100	200	300	Ω
VGPOH	GPOUT high level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1, GPOUT_HL = 1, I_{OH} = 100 µA	2.7			V
VGPOL	GPOUT low level output voltage	SIOV = 3.3 V, XSLEEP = 1, GPOUT_ENA = 1,GPOUT_HL = 0, I_{OH} = 100 µA			0.3	V
tTSD	Thermal protect on temperature	Design ensured value	130	145	165	ºC
hytTSD	Thermal protect hys temperature		5	15	25	ºC
Vonvcc	A5V Reset on voltage		3.6	3.7	3.8	V
Voffvcc	A5V Reset off voltage		3.8	3.9	4	V
VonCV3	CV3P3 reset on voltage		2.6	2.7	2.8	V
VoffCV3	CV3P3 reset off voltage		2.68	2.8	2.88	V
HysCV3	CV3P3 reset voltage Hys		35	85	135	mV
VovpspmOn	OVP detection voltage (Spindle)(1)		6	6.2	6.4	V
VovpspmOff	OVP release voltage (Spindle)(1)		5.8	6	6.2	V
VovpSpmHys	OVP voltage Hys (Spindle)(1)		140	240	340	mV
VovpOn	OVP detection voltage (except Spindle)(1)		6.3	6.5	6.7	V
VovpOff	OVP release voltage (except Spindle)(1)		6.1	6.3	6.5	V
VovpHys	OVP voltage Hys (except Spindle)(1)		140	240	340	mV

(1) Those are value as protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

7.7 Electrical Characteristics – Charge Pump

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FCHGP	Frequency	XSLEEP=1	132.6	156	179.4	kHz
VCHGP	Output Voltage	Ccp1 = Ccp3 = 0.1 µF Io = –1 mA	7.76	9.7	11.64	V

7.8 Electrical Characteristics – V1pXV DC-DC Converter

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rds1pxH	High-side FET RDSON	FB1PXV = 0 V REG1PXV + 100 mA, +300 mA		0.42	0.62	Ω
Rds1pxL	Low-side FET RDSON	FB1PXV = 1.2 V REG1PXV –100 mA , –300 mA		0.2	0.4	Ω
VO1p0	Output voltage (1p0V)	[V1PxSEL,SWR_SEQ1,SWR_SEQ2] = 011	0.95	1	1.05	V
VO1p2	Output voltage (1p2V)	[V1PxSEL,SWR_SEQ1,SWR_SEQ2] = 000	1.14	1.2	1.26	V
VO1p5	Output voltage (1p5V)	[V1PxSEL,SWR_SEQ1,SWR_SEQ2] = 100	1.425	1.5	1.575	V
Tdly1px	Soft start time	[SWR_SEQ1,SWR_SEQ2] = 00 From A5V reset off to target 90%	0.656	0.82	0.984	ms
RdsO1px	Output pulldown transistor Rdson	At Reset On (TSD, A5V_Reset)	616	880	1144	Ω
Fsw1px	Switching frequency		2.125	2.5	2.875	MHz
Vrston1px	Reset on voltage threshold level		75%	80%	85%	
Vrstoff1px	Reset off voltage threshold level		85%	90%	95%	
VrstHys	Reset off voltage threshold Hys		5%	10%	15%	
PSRR1px	PSRR ratio	P5V_SW = 5 V + 200 mVpp, Io = 200 mA, F ≈ 100 kHz	26			dB
Iovc1px	Overcurrent protective level(1)		1.3	1.85	2.4	A
TMskovc1px	Mask time of overcurrent protection(1)		0.72	1	1.32	ms

(1) Those are value as protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

7.9 Electrical Characteristics – 3.3-V DC-DC Converter

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rds3p3H	High-side FET RDSON	FB3P3V = 0 V REG3P3V + 100 mA + 300 mA		0.45	0.65	Ω
Rds3p3L	Low-side FET RDSON	FB3P3V = 3.3 V REG3P3V –100 mA – 300 mA		0.42	0.62	Ω
VO3p3	Output voltage		3.2	3.3	3.4	V
Tdly3p3	Soft start time	[SWR_SEQ1,SWR_SEQ2] = 00 From A5V reset off to target 90%	0.656	0.82	0.984	ms
Rds3p3	Output pull down transistor Rdson	At reset on (TSD, A5V_Reset)	616	880	1144	Ω
Fsw3p3	Switching frequency		2.125	2.5	2.875	MHz
Vrston3p3	Reset on voltage threshold level		75%	80%	85%	
Vrstoff3p3	Reset off voltage threshold level		85%	90%	95%	
Vrst3p3Hys	Reset off voltage threshold Hys		5%	10%	15%	
PSRR3p3	PSRR ratio	P5V_SW = 5 V + 200 mVpp, Io = 200 mA, F ≈ 100 kHz	26			dB
Iovc3p3	Overcurrent protective level(1)		0.65	1.15	1.65	A
Tmskovc3p3	Mask time of overcurrent protection(1)		0.72	1	1.32	ms

(1) Data are value as protection functions only, and stress beyond those listed under “Recommended Operating Condition” may cause permanent damage to the device.

7.10 Electrical Characteristics – Spindle Motor Driver Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlSPM	Total output resistance High side + low side	I_{OUT} = 0.1 A		0.25	0.5	Ω
VIsns	ISENSE detected voltage	ISENSE voltage	181	196	211	mV
ResSPM	Resolution			12		bit
VoutSPM	Spindle voltage	VSPM(REG8h) = 400h	2.6	3	3.4	V
		VSPM(REG8h) = C00h	–1.55	–1.25	–0.95	V
WidDZSPM	Spindle dead band	Forward	+12h	+52h	+92h	
		Reverse	–92h	–52h	–12h	
WidDZSPMLS	Spindle dead band (LS mode)		–40h	0h	40h	

7.11 Electrical Characteristics – Sled Motor Driver Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlSLD	Total output resistance High side + low side	I_O = 0.1 A		0.7	1.1	Ω
ResSLD	Resolution			10		bit
WidDZSLD	Input dead band	Forward	+4h	+51h	+90h	
		Reverse	–90h	–51h	–4h	
GnSLD	Sled current gain	A5V = 5 V, 5 V = 5 V R_L = 10 Ω, 2.2 mH VSLED = 7FFh	380	440	500	mA
VthEdetSLD	END_DET BEMF threshold voltage	ENDDET_SLCT = 0, SLEDENDTH<1:0> = 00, SLED Enable	26	46	66	mV

7.12 Electrical Characteristics – Focus/Tilt/Tracking/Driver Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlAct	Total output resistance High side + low side	I_O = 0.1 A		0.7	1.1	Ω
ResACT	Resolution			12		bit
VOfstACT	Each channel output offset voltage	DAC_code = 000h	–30	0	30	mV
VOfstDACT	Output offset voltage Focus and Tilt	DIFF_TLT = 1	–50	0	50	mV
GnDAct	Difference gain Focus and Tilt	DIFF_TLT = 1	–1	0	1	db
GnAct	Voltage gain	DAC_code = 400h	2.6	3	3.4	V
		DAC_code = C00h	–3.4	–3	–2.6	

7.13 Electrical Characteristics – Load Driver Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlLOD	Total output resistance High side + low side	I_O = 0.1 A		0.7	1.1	Ω
ResLOD	Resolution			12		bit
GnLOD	Voltage gain	VLOAD = 400h	2.6	3	3.4	V
		VLOAD = C00h	–3.4	–3	–2.6	
WidDZLOD	Dead band	Forward	2h	20h	40h	
		Reverse	–41h	–21h	–3h	
TocpLOD	Output 100% limit time	LOAD_05CH = 0	0.64	0.8	0.96	s
IocpLOD	Overcurrent protective level	LOAD_05CH = 1	125	250	375	mA
DlyocpLOD	Overcurrent protection delay time	LOAD_05CH = 1	0.64	0.8	0.96	s

7.14 Electrical Characteristics – Stepping Motor Driver Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RttlSTP	Total output resistance High Side + Low Side	I_O = 0.1 A		1.0	1.5	Ω
ResSTP	Resolution			8		bit
IocpSTP	Overcurrent protection level(1)		595	850	1105	mA
DlyocpSTP	OCP Monitor delay time(1)		0.7	1	1.3	us
ThlocpSTP	OCP hold time(1)		18.2	26	33.8	ms
VthEdetSTP	END_DET threshold level	ENDDET_SLCT = 1, STPDENDTH<1:0> = 00, STP Enable	19	39	59	mV

(1) The data are value as protection functions only, and stress beyond those listed under *Recommended Operating Conditions* may cause permanent damage to the device.

7.15 Electrical Characteristics – Current Switch Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RdsCSW	Rds(on)	I_O = 0.1 A		200	500	mΩ
IlmtCSW	Current limit threshold level		0.77	1.1	1.43	A
ThlCSW	Protection hold time		1.47	1.6	2.0	ms

7.16 Electrical Characteristics – LED Switch Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RdsLED	Rds(on)	I_O = 10 mA		4.4	10	Ω
IlmtLED	Current limit threshold level		0.07	0.1	0.13	A
ThlLED	Protection hold time		0.37	0.4	0.66	ms

7.17 Electrical Characteristics – Thermometer Part

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ResTEMP	Resolution			6		bit
TEMPrng	Temperature range	CHIPTEMP[5:0] = 00	8	15	22	°C
		CHIPTEMP[5:0] = 3Fh	155	165	175	
FTEMP	Update cycle		8	10	12	kHz

7.18 Electrical Characteristics – Actuator Protection

over recommended operating free-air temperature range (A5V ≈ 4.5 to 5.5 V, P5V_1, P5V_2, P5V_STP, P5V_SPM1, P5V_SPM2 = A5V, VREF = 1.65 V, T_A ≈ –20°C to 75°C; unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TintACTTEMP	Update cycle		21	26	31	ms

7.19 Serial Port I/F Write Timing Requirements

			MIN	NOM	MAX	UNIT
F_{ck}	SCLK clock frequency	PIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns

7.20 Serial Port I/F Read Timing Requirements

			MIN	NOM	MAX	UNIT
F_{ck}	SCLK clock frequency	PIOV = 3.3 V			35	MHz
t_{ckl}	SCLK low time		11			ns
t_{ckh}	SCLK high time		11			ns
t_{sens}	SSZ setup time		7			ns
t_{senh}	SSZ hold time		7			ns
t_{sl}	SSZ disable high time		11			ns
t_{ds}	SIMO setup time (Write)		7			ns
t_{dh}	SIMO hold time (Write)		7			ns
t_{rdly}	SOMI delay time (Read)	CLOAD = 10 pF, PIOV = 3.3 V	2		9	ns
t_{sendl}	SOMI hold time (Read)	CLOAD = 10 pF, PIOV = 3.3 V	2		9	ns
t_{rls}	SOMI release time (Read)	CLOAD = 10 pF, PIOV = 3.3 V From SSZ rise to SOMI HIZ	0		9	ns

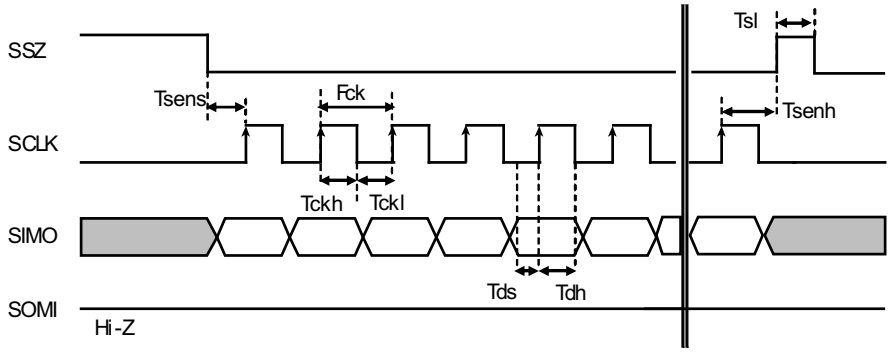


Figure 1. Serial Port Write Timing

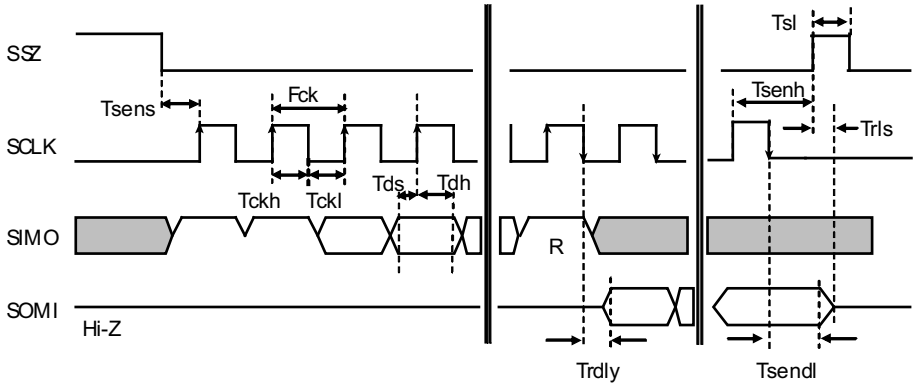


Figure 2. Serial Port Read Timings

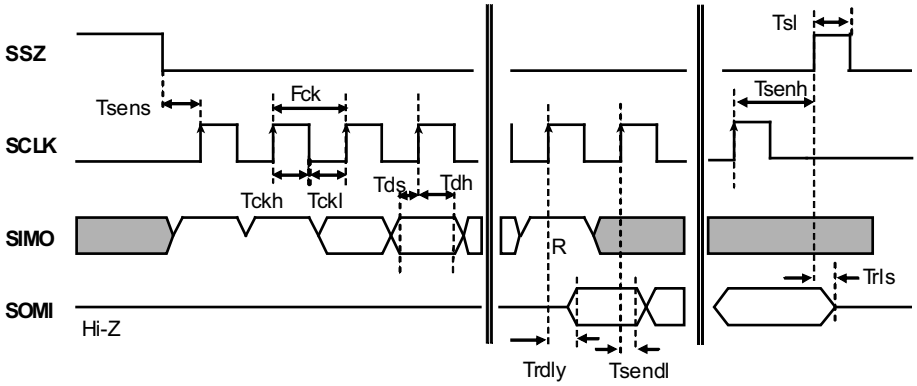


Figure 3. Serial Port Read Timings (ADVANCE_RD Mode)

7.21 Typical Characteristics

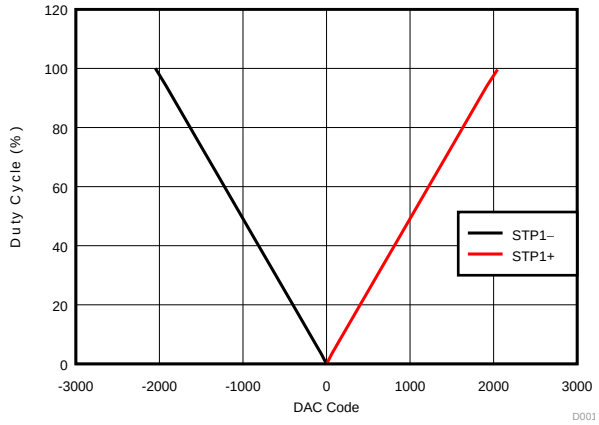


Figure 4. DAC Code vs Duty Cycle for STP1 Outputs

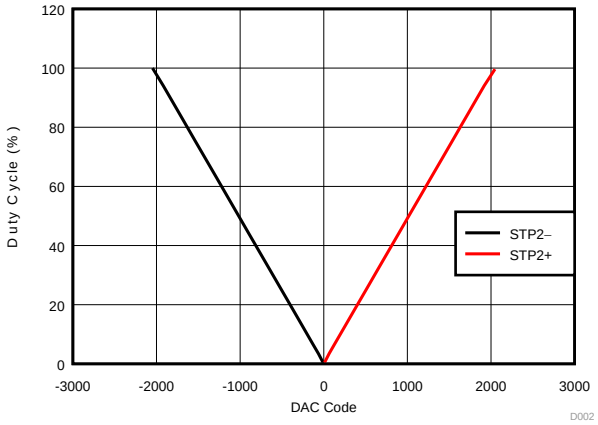


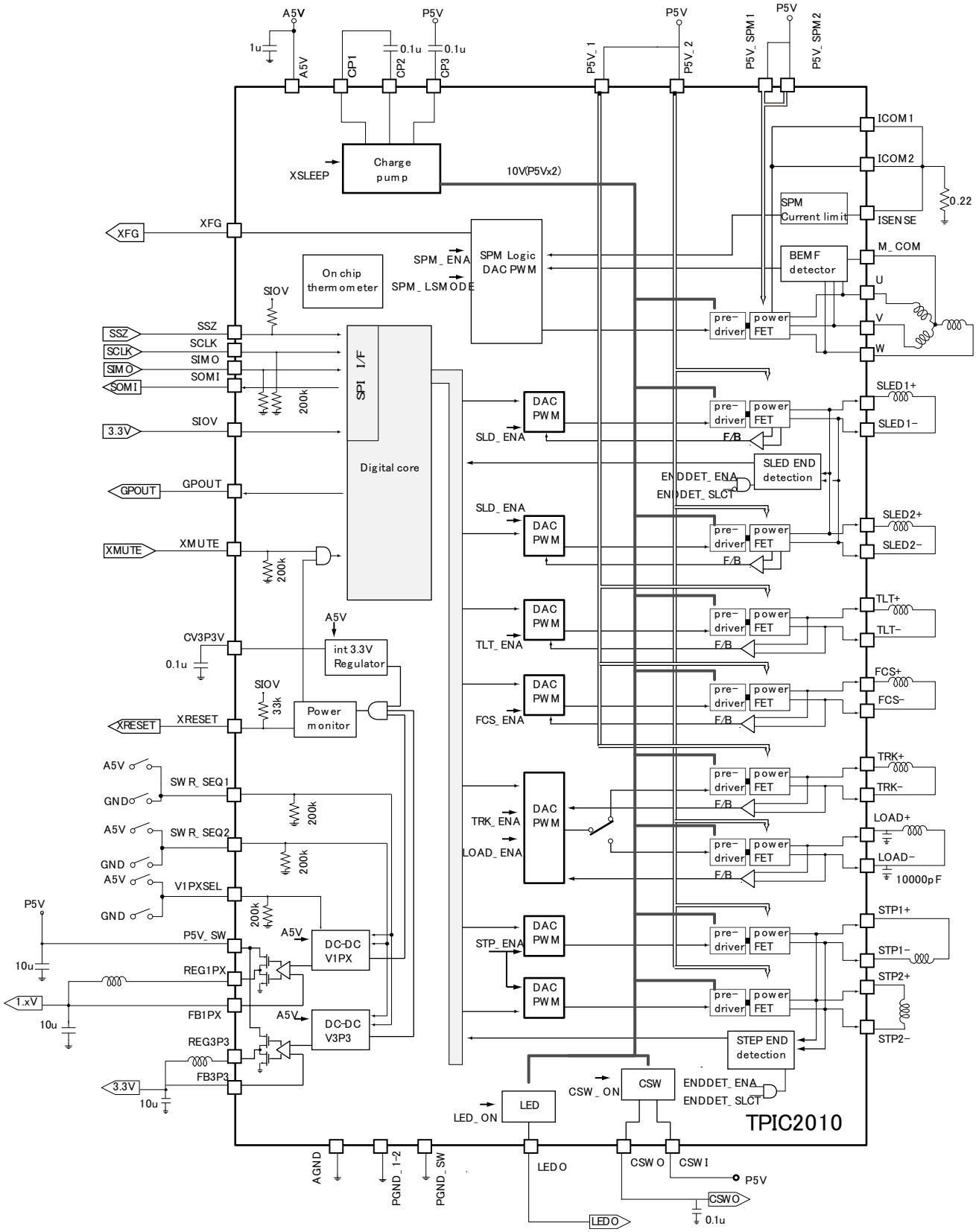
Figure 5. DAC Code vs Duty Cycle for STP2 Outputs

8 Detailed Description

8.1 Overview

TPIC2010 is low noise type motor driver IC suitable for 5V optical disk drives. The 9-channel driver IC controlled by SPI is optimum for driving a spindle motor, a sled motor (stepping motor applicable), a load motor, and Focus / Tracking / Tilt actuators and stepping motor for collimator lens. This IC requires an external current sense resistance to measure SPM current. The spindle motor driver part uses integrated sensorless logic to attain low-noise operation during startup and runtime. By using BEMF feedback, external sensors, such as a Hall device, are not needed to carry out self-starting by the starting circuit or perform position detection. By using the efficient PWM drivers, low-power operation can be achieved by controlling the PWM outputs. Dead zone less control is possible for a Focus / Tracking / Tilt actuator driver. In addition, the spindle part output current limiting circuit, the thermal shut down circuit, the sled end detection circuit, collimator lens end detection circuits offer protection for all actuators and motors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Protection Functions

TPIC2010 has five protection features: undervoltage lockout, overvoltage protection (OVP), over currentprotection (OCP), thermal protection (TSD), and actuator temperature protection (ACTTIMER) in order to protect target equipment. A protect behavior differ by generated events.

8.3.1.1 Undervoltage Lockout (UVLO)

Power Faults are reported in the UVLOMon register. Each UVLOMon bit will be initialized to zero upon a cold power up. After a fault is detected the appropriate fault bit will be latched high. Writing to the RST_ERRFLG (REG77) will clear all UVLOMon bits. The power device faults and actions are summarized in Table 1.

Table 1. Power Fault Monitor

FAULT TYPE	LATCHED REGISTER	XRESET	CRITERIA	SPM	ACTUATOR	DC-DC
A5V under voltage	UVLO_A5V	Yes	<3.7 V	Hi-Z	Hi-Z	Hi-Z Feedback pin to GND
internal 3.3V under voltage	UVLO_INT3P3	Yes	<2.7 V	Hi-Z	Hi-Z	Hi-Z
3.3V DC-DC output under voltage	UVLO_SWR3P3	Yes	<80%	Hi-Z	Hi-Z	
1.xV DC-DC output under-voltage	UVLO_SWR1PX	Yes	<80%	Hi-Z	Hi-Z	
P5V over-voltage	OVP_P5V		>6.2 V	Brake	—	—
			>6.5 V	Hi-Z	Hi-Z	Hi-Z

8.3.1.2 Overvoltage Protection (OVP)

Over voltage protect function is aimed to protect the unit from the supplying hi-voltage.

When the supply voltage exceeds 6.5 V, all driver and DC-DC converter output goes Hi-Z. When the supply voltage falls below typical 6.2 V, (6.0 V for SPM) all output start to operate again. The OVP and POR (XRESET) function is not interlocking. However, DC-DC converter output falls by Hi-Z operations, output voltage falls to 80% then XRESET signal goes low.

Moreover, when power supply exceeds 6.2 V, especially SPM enter short brake mode. This operation is offered supposing a voltage rising by motor BEMF of the high velocity revolution.

This function is for insurance, so it can not assure that the device is safety in the condition. Because the absolute maximum ratings range of the supply voltage is 6 V. When this function works, the feed back terminals are not shorted to GND.

Figure 6 shows the behavior of OVP.

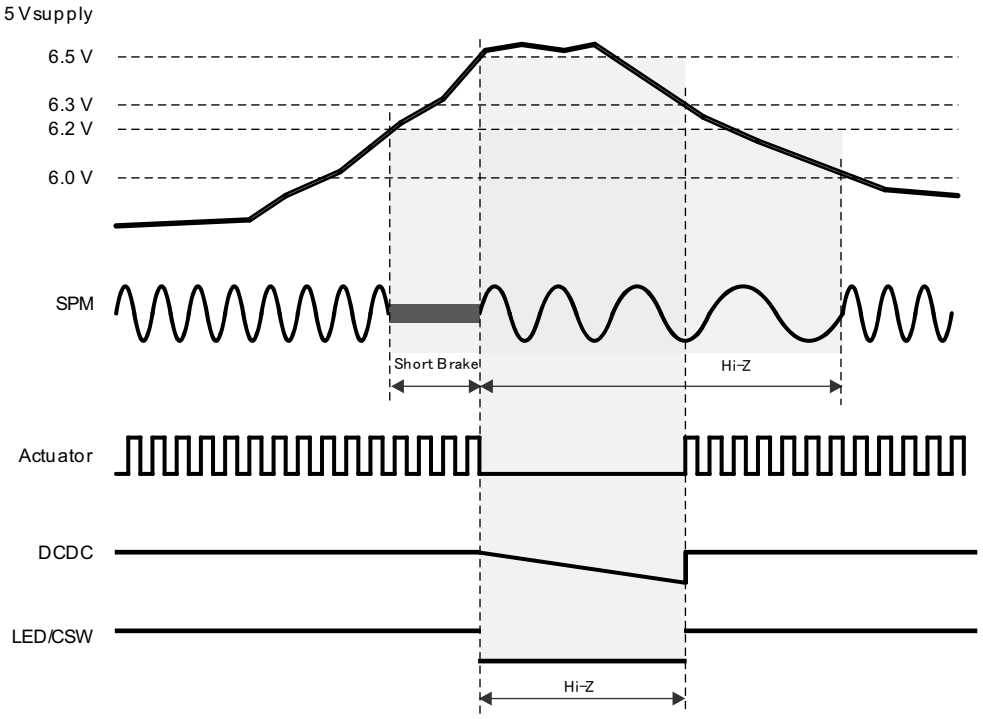


Figure 6. Overvoltage Protection

8.3.1.3 Overcurrent Protection (OCP)

The OCP function serve to protect the device from break down by large current. The OCP is provided for five circuit blocks, and each threshold are in Table 2.

Table 2. OCP Threshold

BLOCK	DETECTION CURRENT	MONITOR TIME	HI-Z HOLD TIME
DC-DC conv V1PX V3P3	1850 mA	1 ms	POR
	1150 mA	1 ms	POR
LOAD driver 1 ch 0.5 ch	100%	800 ms	Forever
	260 mA	800 ms	Forever
STEP driver	850 mA	1 µs	25 ms
LED driver	100 mA	20 µs	0.4 ms
CSW driver	1000 mA	20 µs	1.6 ms

When the large current is detected on each block, device put the output FET to Hi-Z.

The amounts of currents and time have specified the detection threshold for every circuit block.

When OCP occurs, it returns automatically after expiring set Hi-Z period. However, it restricts, the POR is performed at OCP for DC-DC converter. It keeps XRESET=L and does not return forever. It's necessary power ON/OFF actuation in order to make it release.

OCPERR (REG7F) and OCP flag (REG7B) are set at OCP detection.

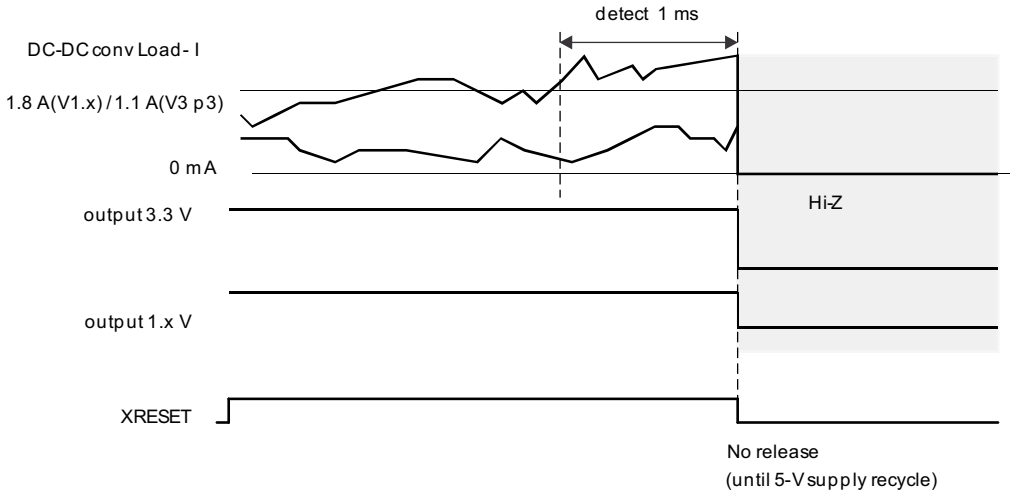


Figure 7. OCP DC-DC Converter

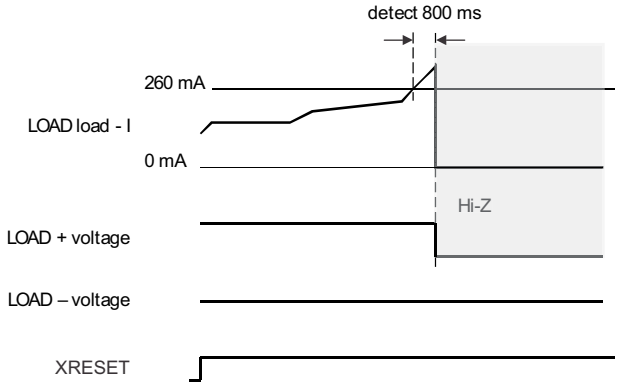


Figure 8. OCP Load 1-Channel

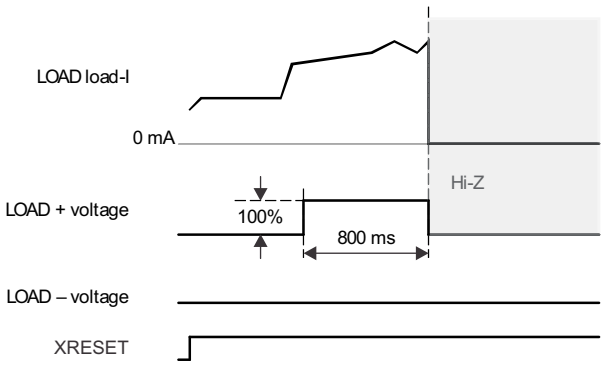
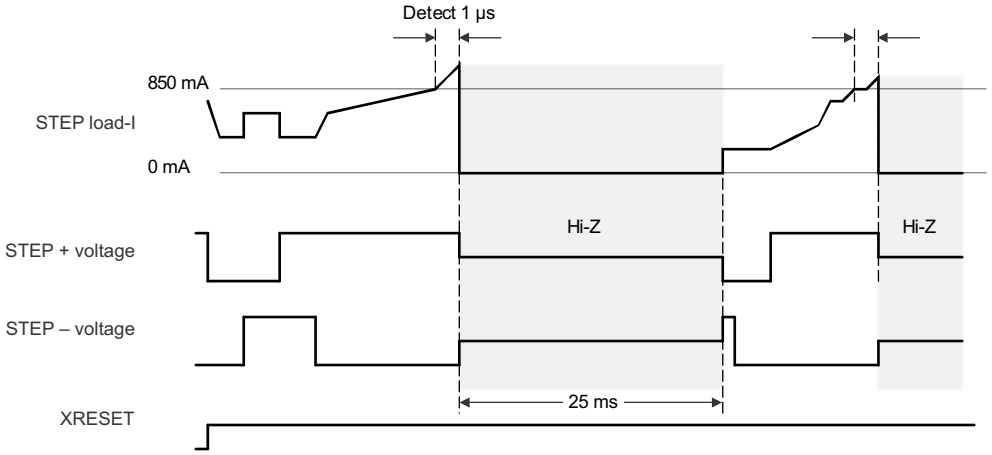


Figure 9. OCP Load 0.5-Channel



STP1 and STP2 channel has current trip function. The output of STEP channel will be changed Hi-Z if current exceed current limit threshold (850-mA typ). When the trip period 25ms is expired, trip state is automatically released.

Figure 10. OCP Step

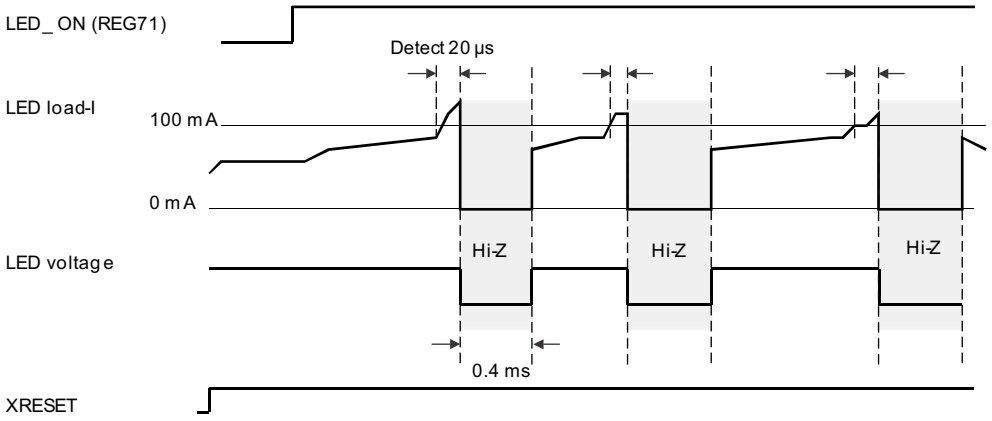


Figure 11. OCP LED Driver

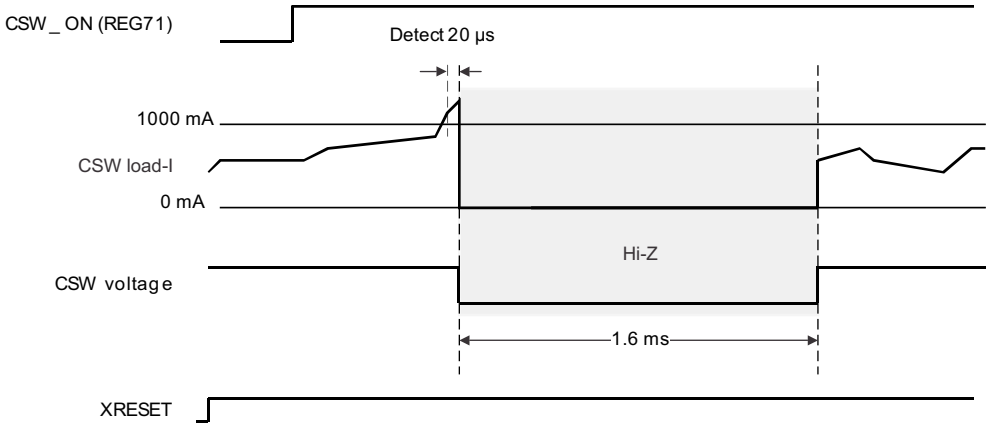


Figure 12. OCP Current Switch

8.3.1.4 Thermal Protection (TSD)

The thermal protection (TSD) is a protect function which intercepts an output and suspends an operation when the IC temperature exceed a maximum permissible on a safety. TSD makes an output Hi-Z when the temperature rises up and a threshold value is exceeded. There're two levels for threshold "Alert" and "Trip". Alarm is given by status register "TSD_FAULT_" on "Alert" level with 135°C. It continues rising up temperature, the register "TSD_" is set at 150°C and the driver output changes HI-Z. If temperature falls and is reached 135°C, it will output again. TPIC2010 has total 12 temperature sensors in each circuit block. Particular sensor is assigned to appropriate status flag in List 10 OCP threshold.

Table 3. Thermal Sensor Assignment

CIRCUIT	ALERT (°C)	TRIP (°C)	RELEASE (°C)	ALERT FLAG	TRIP FLAG
U	130	145	130	TSD_FAULT_SPM	TSD_SPM
V	130	145	130	TSD_FAULT_SPM	TSD_SPM
W	130	145	130	TSD_FAULT_SPM	TSD_SPM
TLT	130	145	130	TSD_FAULT_ACT	TSD_ACT
FCS	130	145	130	TSD_FAULT_ACT	TSD_ACT
TRC	130	145	130	TSD_FAULT_ACT	TSD_ACT
SLED1	130	145	130	TSD_FAULT_ACT	TSD_ACT
SLED2	130	145	130	TSD_FAULT_ACT	TSD_ACT
STP	130	145	130	TSD_FAULT_ACT	TSD_ACT
LOAD	130	145	130	TSD_FAULT_ACT	TSD_ACT
LED/CSW	130	145	130	TSD_FAULT_LEDCSW	TSD_ LEDCSW
2ch DCDC	130	145	130	TSD_FAULT_SWR	TSD_SWR

8.3.1.5 Actuator Temperature Protection (ACTTIMER)

TPIC2010 has Actuator protect function named ACTTIMER. This function enables to avoid from being broken by setting actuator channel output to HIZ when actuator coil current exceeds the specific value. Up to now, be used a simple actuator protect function such like exceeding max current with continuous time. However these types were not accurate. This new protection enables to calculate heat accumulation and judge correctly. When this function operates, load channel output will be Hi-Z, too. And spindle channel will be forced "Auto short brake" and disc motor will stop.

It's able to know the protection has occurred by checking Fault register ACTTIMER_FAULT (REG7F) and ACT_TIMER_PROT (REG78). ACTTIMER_FAULT has a character of advance notice, is set before detecting ACT_TIMER_PROT. Once an ACT_TIMER_PROT is set, even if temperature falls, it will not release protection automatically. It's necessary to clear the flag by setting RST_ERR_FLAG (REG77) or setting 0 to ACTTEMPTH (REG72). ACTTIMER function is able to disable by setting H to ACTPROT_OFF (REG72) or setting 0 to ACTTEMPTH (REG72).

In order to acquire the optimal value for ACTTEMPTH, you should set device into the condition of the detection level, and reading the value of ACTTEMP. Because of the present value can be read from ACTTEMP (REG78). (1)

(1) The ACTTEMP data is updated on Register in ACTPROT_OFF = 0 and ACTTEMPTH > 0.

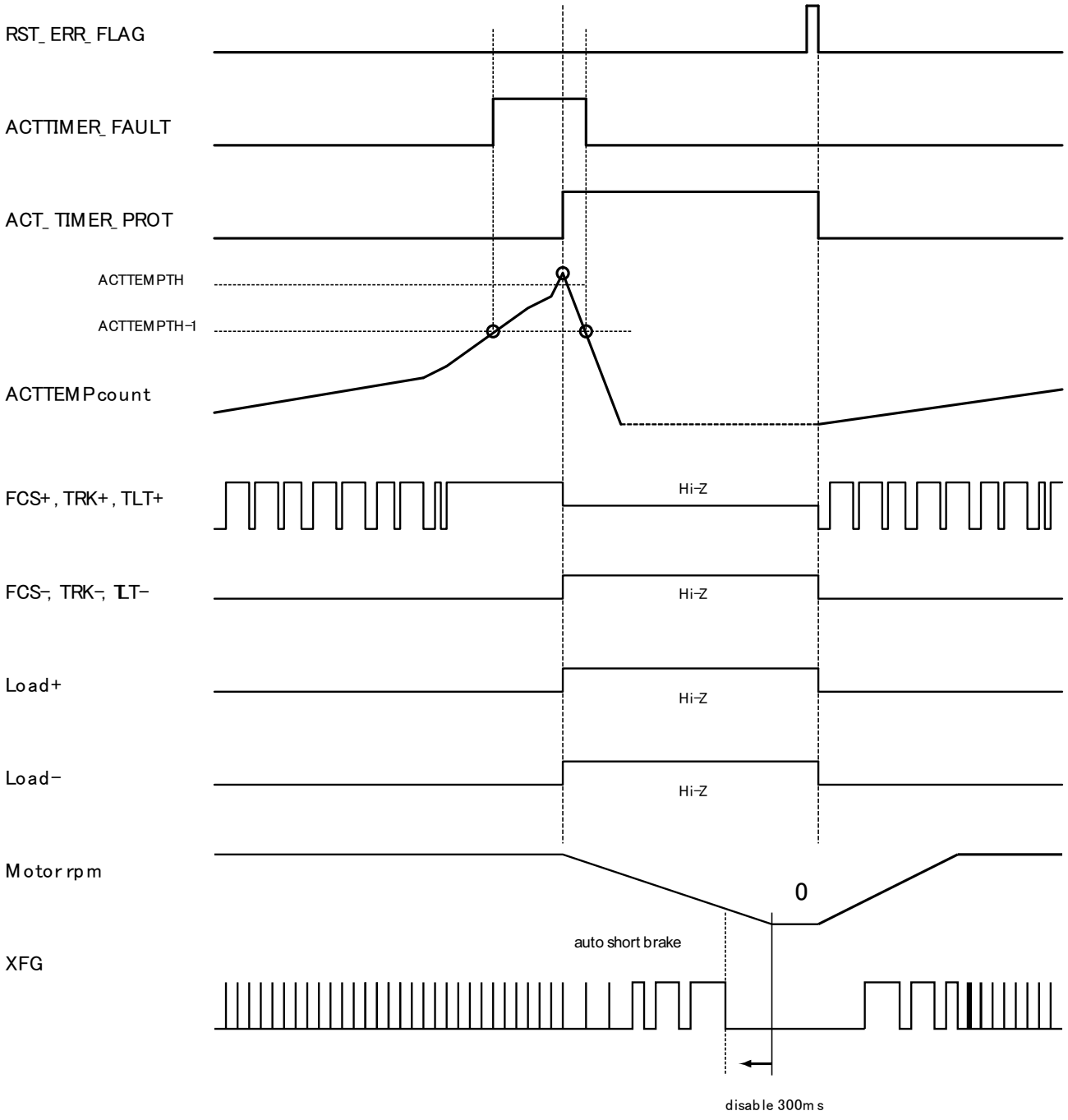


Figure 13. Actuator Temperature Protections

8.4 Device Functional Modes

8.4.1 Power-On Reset (POR)

8.4.1.1 Power-Up Sequences

The power up sequence is described in Table 4.

In TPIC2010, the normal sequence is to wait for 5-V supply to come up to 3.9 V. After 5 V establish, the internal 3.3 V will stabilize. Now the voltage monitors start to work and begin to look for the DC-DC V1Px and V3P3. Start up sequence for internal DC-DC converter is selected by external pin, SWR_SEQ1 and SWR_SEQ2. All DC-DC converters stabilize the power up sequence finishes and the part starts to function. Once the part finishes all of its power up tasks, it takes XRESET high to indicate that the part is no longer in reset and ready to communicate to the outside world. All the DC-DC converter have soft-start features to avoid rush current and voltage over shoot. Each soft-start sequence takes about 0.8 ms.

Table 4. DC-DC Start-Up Sequence and Output

V1PXSEL	SWR_SEQ2	SWR_SEQ1	REG1PX(V)	REG3P3(V)	SEQUENCE	
					REG1PX	REG3P3
0	0	0	1.2	3.3	Same	
0	0	1	1.2	3.3	2nd	1st
0	1	0	1.2	3.3	1st	2nd
0	1	1	1.0	3.3	Same	
1	0	0	1.5	3.3	Same	
1	0	1	1.5	3.3	2nd	1st
1	1	0	1.5	3.3	1st	2nd
1	1	1	Disable(1)			

(1) This setting is able to use REG1PX, REG3P3 pin as GPOUT pin.

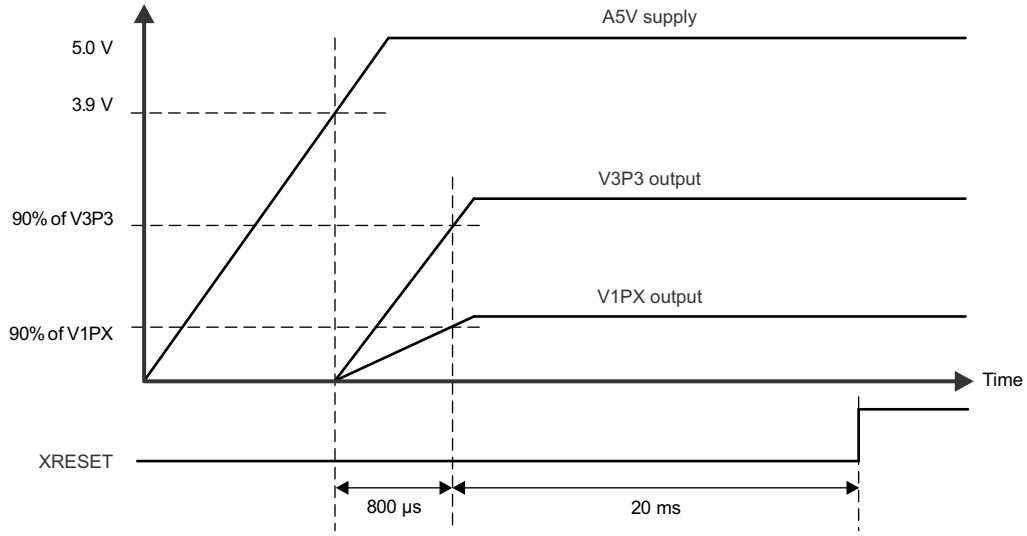


Figure 14. Simultaneously Start Up (SWR_SEQ[1:0] = 00)

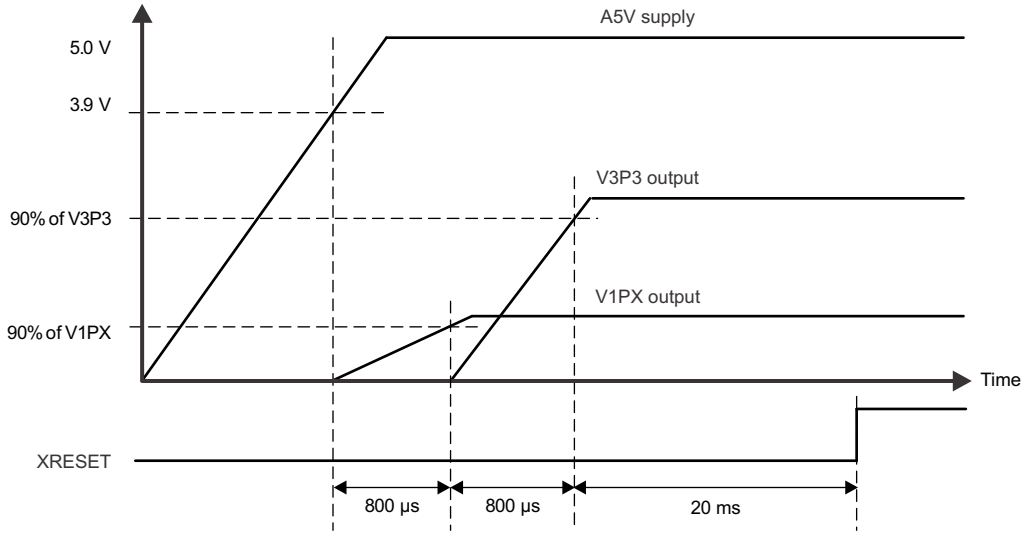


Figure 15. V1Px Start First (SWR_SEQ[1:0] = 10)

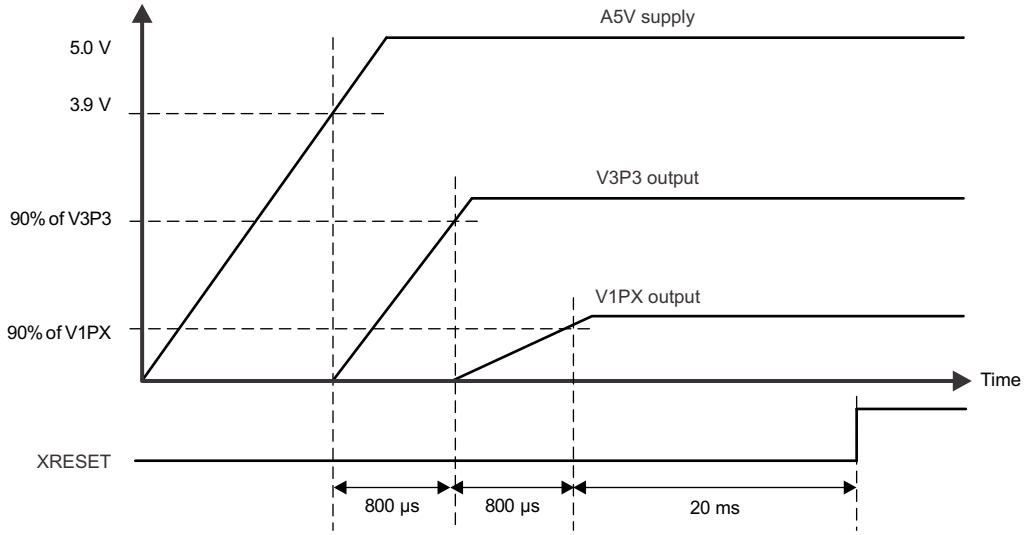


Figure 16. V3P3 Start First (SWR_SEQ[1:0] = 01)

8.4.1.2 XRESET

TPIC2010 is preparing XRESET pin in order to notify an own status to DSP. TPIC2010 set XRESET to L when the event which has a serious effect on DSP occurs such like the power failure, the over temperature and the drop of DC-DC converter output. If all the exception is removed, it will tell that XRESET pin would be set to H and it would be in the ready state. The POR (power on reset) condition is shown in Figure 17. All the behavior of XRESET is shown in Figure 21.

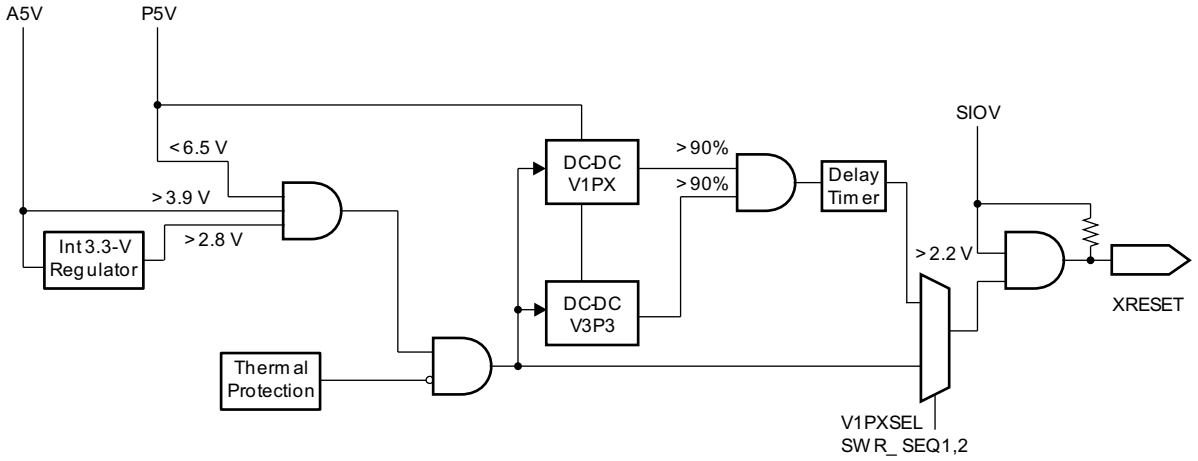


Figure 17. POR Block Diagram

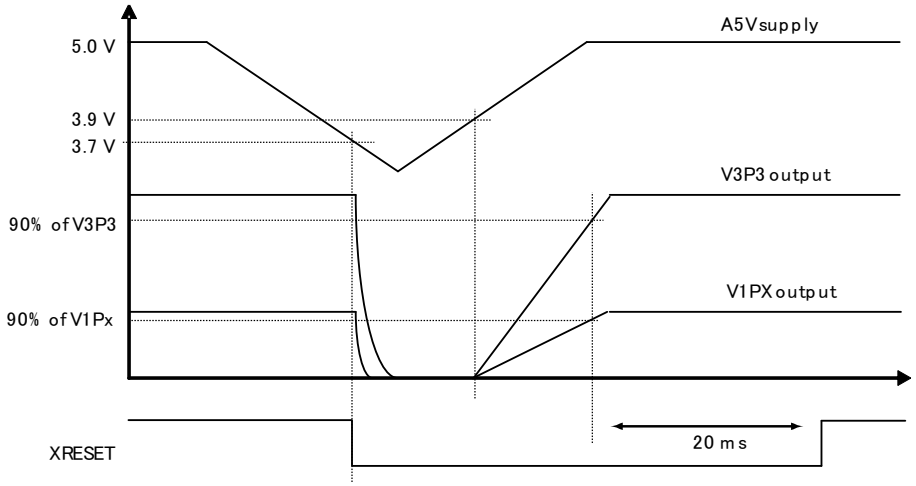


Figure 18. 5-V Supply Voltage Drop

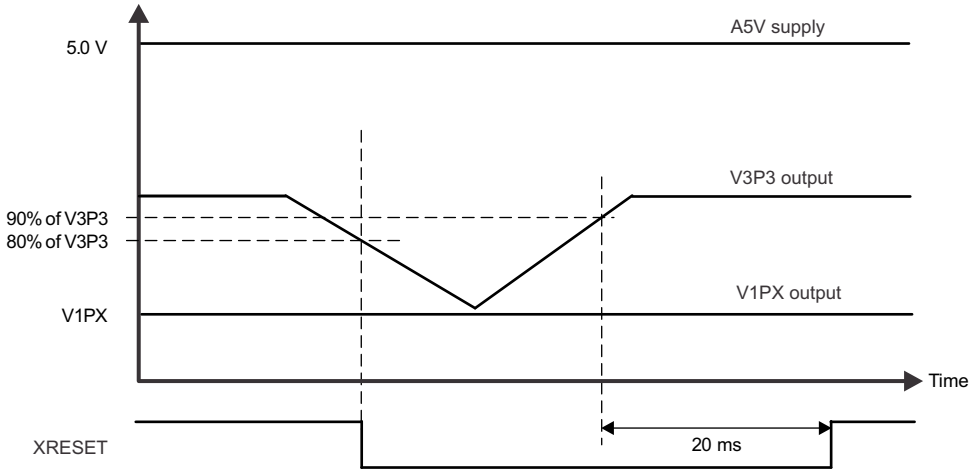


Figure 19. 3.3-V Output Voltage Drops (SWR_SEQ = 00, 11)

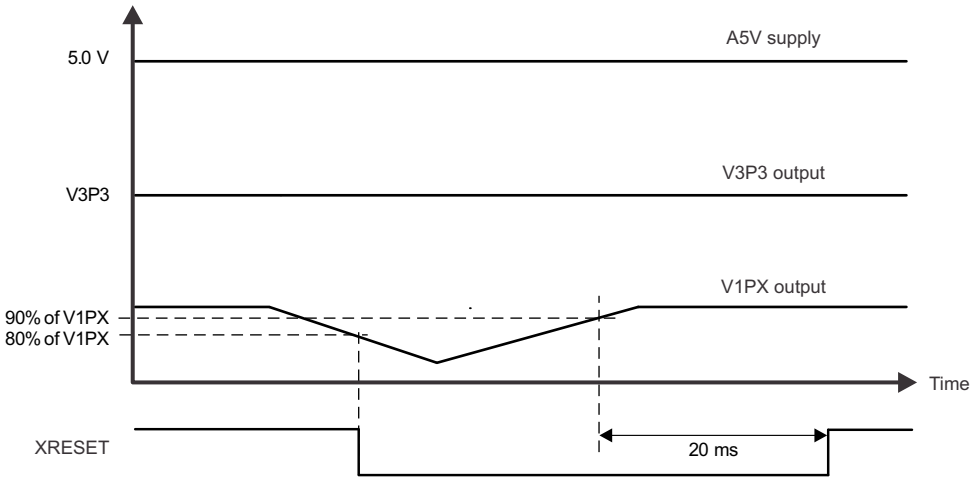
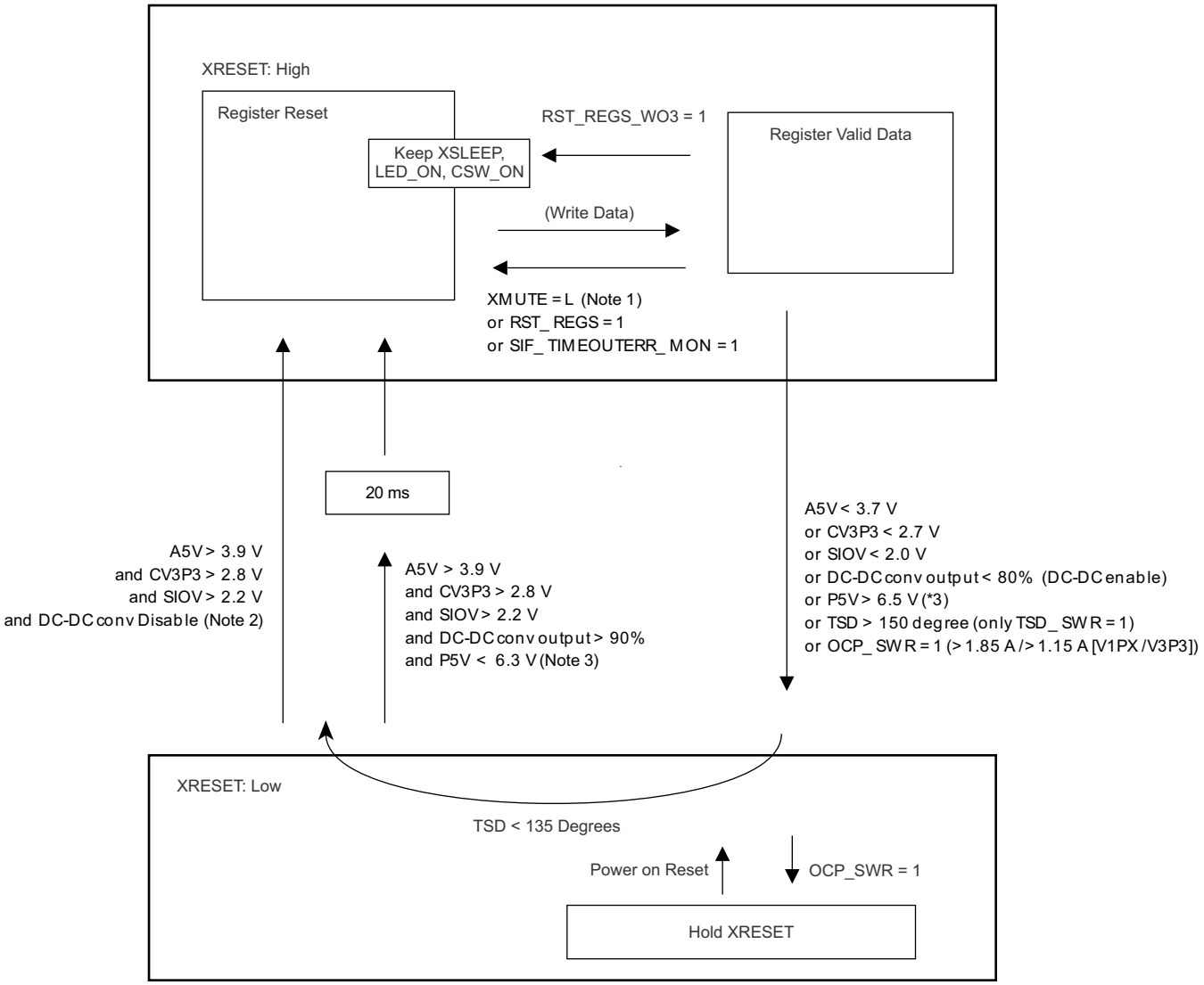


Figure 20. 1.x V Output Voltage Drops (SWR_SEQ = 00, 11)



(1) The period of XMUTE = L cannot be communicated with device.

(2) DC-DC converter disable is V1PXSEL = H, SWR_SEQ1 = H, SWR_SEQ2 = H

(3) When exceed 6.5 V, DC-DC converter output changed Hi-Z and output falling < 80%. Consequently force RESET event. (Released > 90%)

Figure 21. XRESET Behavior

8.5 Programming

8.5.1 Function and Operation

8.5.1.1 Serial Port Functional Description

The serial communication of TPIC2010 is based on a SPI communications protocol. TPIC2010 is put on the slave side. All 16-bit transmission data is effective in SSZ = L period.

The bit stream sent through SIMO from a master (DSP) is latched to an internal shift register by the rising edge of SCLK. All the data is transmitted in a total of 16-bit format of a command and data. A format has two types of data, 8 bits and 12 bits length. In order to access specific registers, an address and R/W flag are specified as a command part. In addition, 12 bit data do not have R/W flag in the packet because DAC register (= 12-bit data form) are Write only. A transfer packet, command and data, is transmitted sequentially from MSB to LSB. A packet is distinguished in MSB 2 bits of command. In the case of 11, it handles a packet for control register access, and the other processed as a packet for a DAC data setting.

There are the following four kinds of serial-data communication packets.

1. Write 12 bits DAC data (MSB two bit ≠ 11)
2. Write 8 bits control register (MSB two bit = 11)
3. Read 8 bits control register (MSB two bit = 11)
4. Write 12 bits Focus DAC data + Read 8 bits status register at the same time (MSB two bit ≠ 11)

8.5.1.2 Write Operation

For write operation, DSP transmits 16 bit (command + address + data) data a bit every in an order from MSB. Only the 16-bit data which means 16 SCLK sent from the master during SSZ = L becomes effective. If more than 17 or less than 15 SCLK pulses are received during the time that SSZ is low, the whole packet will be ignored. For all valid write operations, the data of the shift register is latched into its designated internal register at rising edge of 16th SCLK. All internal register bits, except indicated otherwise, are reset to their default states upon power-on-reset.

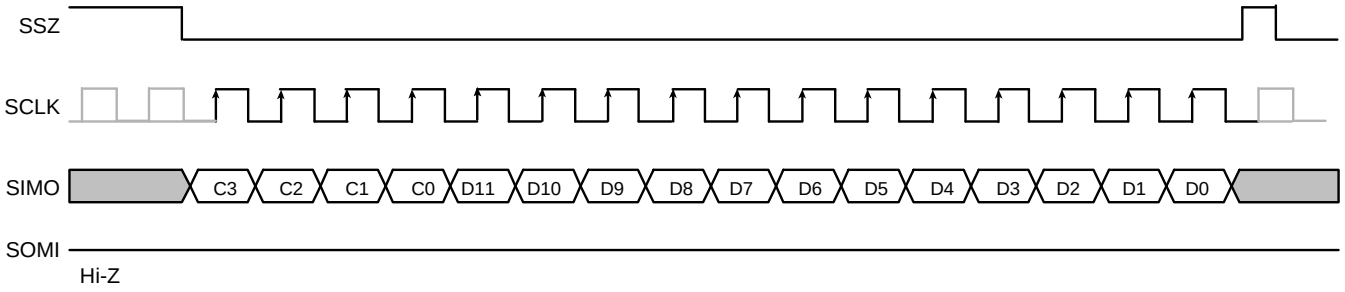


Figure 22. Write 12 Bits DAC Data

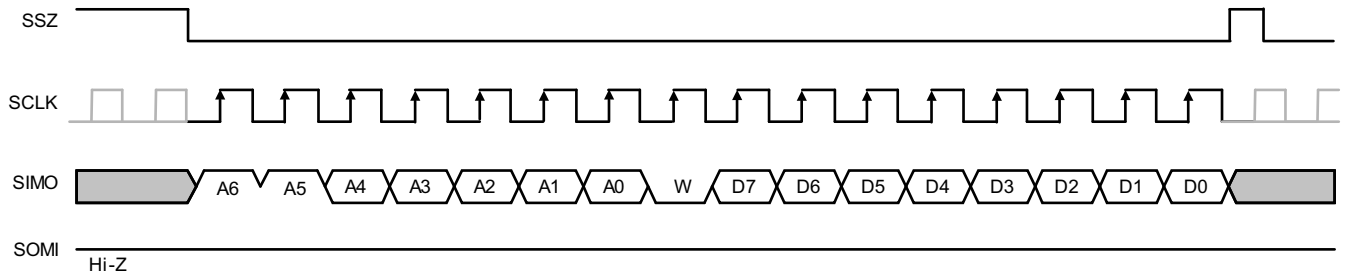


Figure 23. Write 8 Bits Control Register

Programming (continued)

8.5.1.3 Read Operation

DSP sends 8-bit header through SIMO, in order to perform Read operation. TPIC2010 will start to drive the SOMI line upon the eighth falling edge of SCLK and shift out eight data bits. The master DSP inputs 8bits data from SOMI after the ninth rising edge of SCLK. There's optional read mode that SOMI data is advanced a half clock cycle of SCLK. This mode becomes effective by setting "ADVANCE_RD" (REG74) = H.

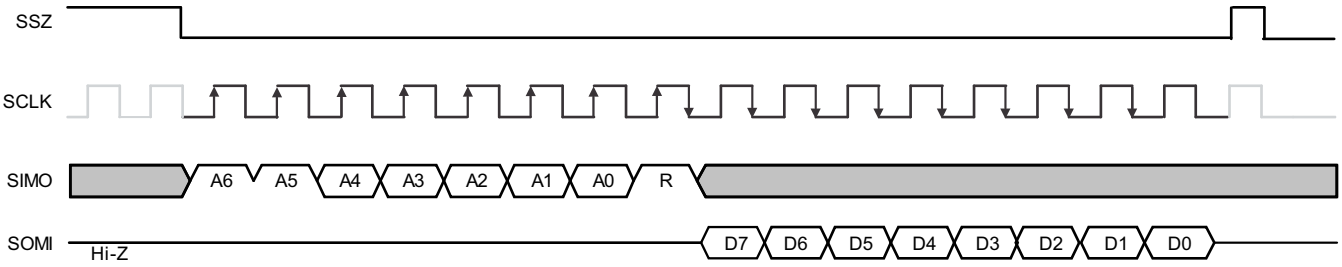


Figure 24. Read 8 Bits Control Register

8.5.1.4 Write and Read Operation

Optionally, the master DSP can read Status register during writing 12 bits DAC (Focus DAC) packet. It's enabled by setting bit "RDSTAT_ON_VFCS" (REG74) = H.

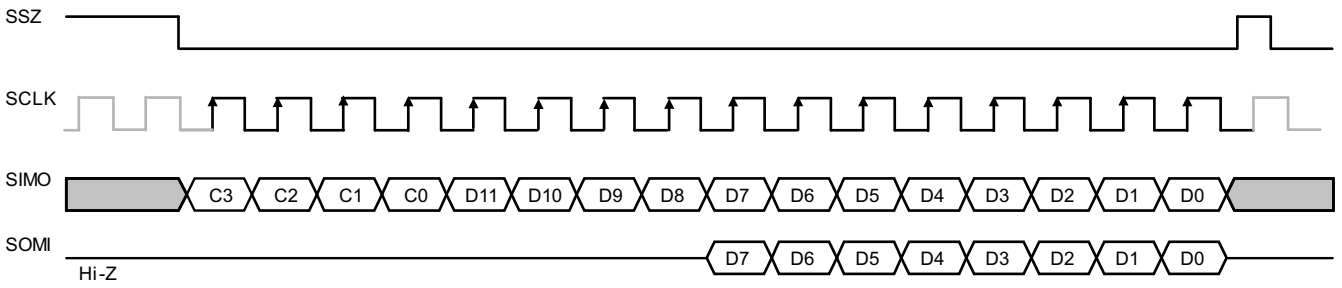
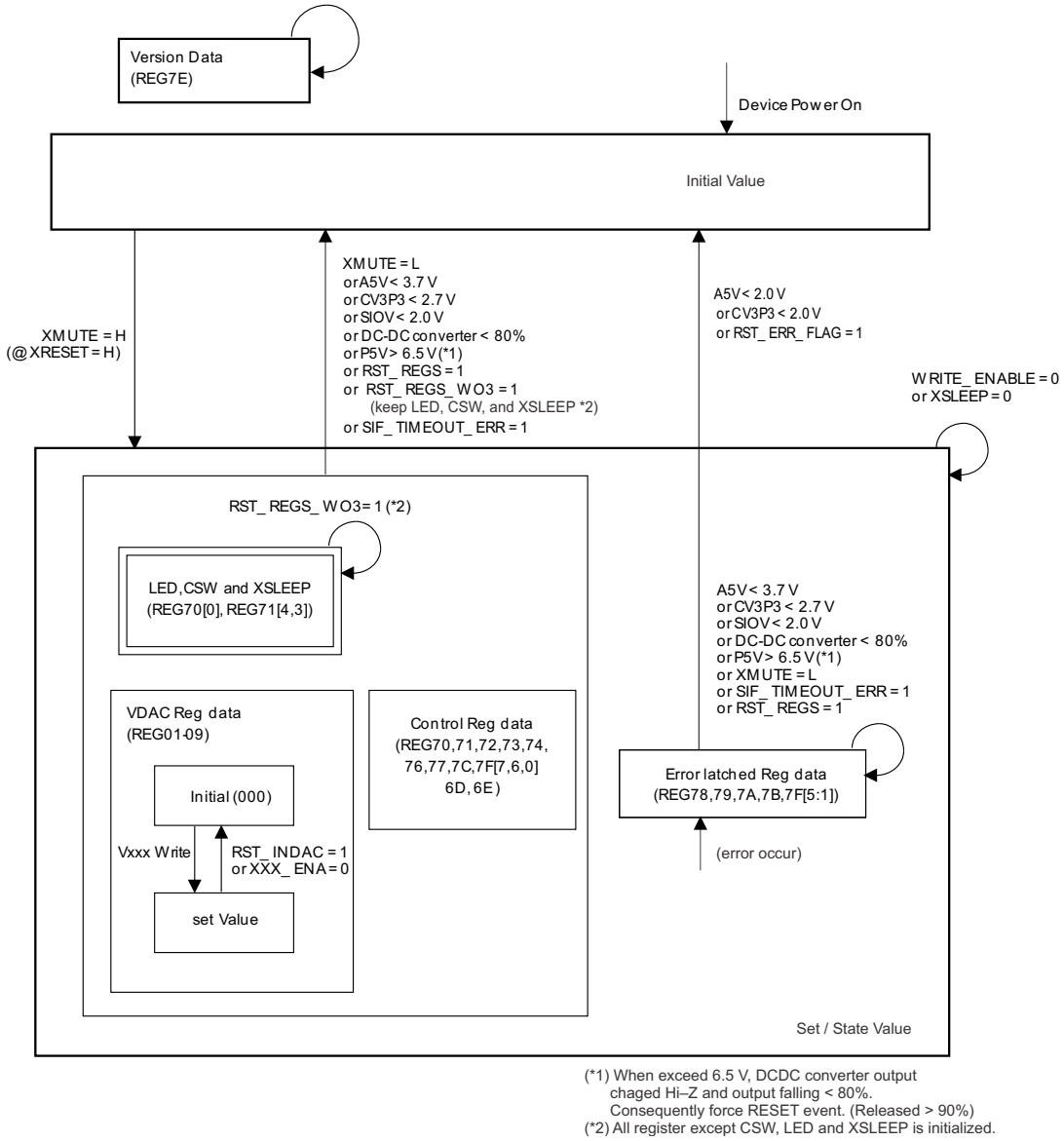


Figure 25. Write 12 Bits Focus DAC Data + Read 8 Bits Status Data

8.6 Register Maps

All registers are in WRITE-protect mode after XRESET release. “WRITE_ENA” bit (REG76) = H is required before writing data in register.

8.6.1 Register State Transition



(1) When exceed 6.5 V, DC-DC converter output changed Hi-Z and output falling <80%.

(2) All register except CSW, LED, and XSLEEP is initialized.

Figure 26. Register State Transition Chart

8.6.2 DAC Register (12-Bit Write Only)

Two difference forms are prepared in 12-bit DAC register, and the forms can be selected by setting VDAC_MAPSW (REG74h).

Table 5. DAC Register (VDAC_MAPSW = 0)

REG	NAME	F	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	W	N/A				N/A				N/A			
01h	VTLT	W	VTLT[11]	VTLT[10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
02h	VFCS	W	VFCS[11]	VFCS[10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTRK	W	VTRK[11]	VTRK[10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
04h	VSLD1	W	VSLD1[11]	VSLD1[10]	VSLD1[9]	VSLD1[8]	VSLD1[7]	VSLD1[6]	VSLD1[5]	VSLD1[4]	VSLD1[3]	VSLD1[2]	VSLD1[1](1)	VSLD1[0](1)
05h	VSLD2	W	VSLD2[11]	VSLD2[10]	VSLD2[9]	VSLD2[8]	VSLD2[7]	VSLD2[6]	VSLD2[5]	VSLD2[4]	VSLD2[3]	VSLD2[2]	VSLD2[1](1)	VSLD2[0](1)
06h	VSTP1	W	VSTP1[11]	VSTP1[10]	VSTP1[9]	VSTP1[8]	VSTP1[7]	VSTP1[6]	VSTP1[5]	VSTP1[4]	VSTP1[3](1)	VSTP1[2](1)	VSTP1[1](1)	VSTP1[0](1)
07h	VSTP2	W	VSTP2[11]	VSTP2[10]	VSTP2[9]	VSTP2[8]	VSTP2[7]	VSTP2[6]	VSTP2[5]	VSTP2[4]	VSTP2[3](1)	VSTP2[2](1)	VSTP2[1](1)	VSTP2[0](1)
08h	VSPM	W	VSPM[11]	VSPM[10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
09h	VLOAD	W	VLOAD[11]	VLOAD[10]	VLOAD[9]	VLOAD[8]	VLOAD[7]	VLOAD[6]	VLOAD[5]	VLOAD[4]	VLOAD[3]	VLOAD[2]	VLOAD[1]	VLOAD[0]
0Ah	N/A	W	N/A				N/A				N/A			
0Bh	N/A	W	N/A				N/A				N/A			

(1) TPIC2010 process as 0 even if set as 1.

Table 6. DAC Register (VDAC_MAPSW = 1)

REG	NAME	F	11	10	9	8	7	6	5	4	3	2	1	0
00h	N/A	W	N/A				N/A				N/A			
01h	VTLT	W	VTRK[11]	VTRK[10]	VTRK[9]	VTRK[8]	VTRK[7]	VTRK[6]	VTRK[5]	VTRK[4]	VTRK[3]	VTRK[2]	VTRK[1]	VTRK[0]
02h	VFCS	W	VFCS[11]	VFCS[10]	VFCS[9]	VFCS[8]	VFCS[7]	VFCS[6]	VFCS[5]	VFCS[4]	VFCS[3]	VFCS[2]	VFCS[1]	VFCS[0]
03h	VTRK	W	VTLT[11]	VTLT[10]	VTLT[9]	VTLT[8]	VTLT[7]	VTLT[6]	VTLT[5]	VTLT[4]	VTLT[3]	VTLT[2]	VTLT[1]	VTLT[0]
04h	VSLD1	W	VSLD1[11]	VSLD1[10]	VSLD1[9]	VSLD1[8]	VSLD1[7]	VSLD1[6]	VSLD1[5]	VSLD1[4]	VSLD1[3]	VSLD1[2]	VSLD1[1](1)	VSLD1[0](1)
05h	VSLD2	W	VSLD2[11]	VSLD2[10]	VSLD2[9]	VSLD2[8]	VSLD2[7]	VSLD2[6]	VSLD2[5]	VSLD2[4]	VSLD2[3]	VSLD2[2]	VSLD2[1](1)	VSLD2[0](1)
06h	VSTP1	W	VSPM[11]	VSPM[10]	VSPM[9]	VSPM[8]	VSPM[7]	VSPM[6]	VSPM[5]	VSPM[4]	VSPM[3]	VSPM[2]	VSPM[1]	VSPM[0]
07h	VSTP2	W	N/A				N/A				N/A			
08h	VSPM	W	N/A				N/A				N/A			
09h	VLOAD	W	N/A				VLOAD[11]	VLOAD[10]	VLOAD[9]	VLOAD[8]	VLOAD[7]	VLOAD[6]	VLOAD[5]	VLOAD[4]
0Ah	N/A	W	N/A				VSTP1[11]	VSTP1[10]	VSTP1[9]	VSTP1[8]	VSTP1[7]	VSTP1[6]	VSTP1[5]	VSTP1[4]
0Bh	N/A	W	N/A				VSTP2[11]	VSTP2[10]	VSTP2[9]	VSTP2[8]	VSTP2[7]	VSTP2[6]	VSTP2[5]	VSTP2[4]

(1) TPIC2010 process as 0 even if set 1.

8.6.3 Control Register (8-Bit Read/Write)

Table 7. Control Register(1)

REG	NAME	F	7	6	5	4	3	2	1	0
70h	DriverEna	R/W	TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
71h	FuncEna	R/W	SPM_LSMODE	ENDDET_ENA	ENDDET_SLCT	LED_ON	CSW_ON	TEMPMON_ENA	TI reserved	
72h	ACTCfg	R/W	LOAD_O5CH_HIGH	LOADPROT_OFF	ACTPROT_OFF	ACTTEMPTH				
73h	Parm0	R/W	SIF_TIMEOUT_TH		SLDEND_HZTIME	SLDENDTH		STPEND_HZTIME	STPENDTH	
74h	SIFCfg	R/W	DIFF_TLT	LOAD05_CH	RDSTAT_ON_VFCS	VSLD2_POL	VSTP2_POL	ADVANCE_RD	SOMI_HIZ	VDAC_MAPSW
75h	Protect	R/W	TI reserved							
76h	WriteEna	R/W	WRITE_ENABLE	TI reserved						REG6X_WR
77h	ClrReg	W	RST_INDAC	RST_REGS	RST_ERR_FLAG	RST_REGS_WO3	TI reserved			
78h	ActTemp	R	TI reserved		ACT_TIMER_PROT	ACTTEMP				
79h	UVLOMon	R	TI reserved			UVLO_A5V	UVLO_INT3P3	UVLO_SWR3P3	UVLO_SWR1PX	OVP_P5V
7Ah	ThPMon	R	TSD_FAULT_SWR	TSD_FAULT_SPM	TSD_FAULT_ACT	TSD_FAULT_LEDCSW	TSD_SWR	TSD_SPM	TSD_ACT	TSD_ LEDCSW
7Bh	OCPMon	R	TI reserved			OCP_SWR	OCP_STP	OCP_LOAD	OCP_LED	OCP_CSW
7Ch	TempMon	R	TI reserved	CHIPTEMP_STATUS	CHIPTEMP					
7Dh	Protect	R	TI reserved							
7Eh	Version	R	Version							
7Fh	Status	R	ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPERR	TSDFAULT	FG
60h	Protect	R/W	TI reserved							
61h	Protect	R/W	TI reserved							
62h	Protect	R/W	TI reserved							
63h	SpinAdj	R/W	TI reserved						Mask_Plus	TI reserved
64h	Protect	R/W	TI reserved							
65h	Protect	R/W	TI reserved							
66h	Protect	R/W	TI reserved							
6Ch	EdetCfg	R/W	TI reserved						STP_WIND_HIZ	STP_WIND_H
6Dh	DCCfg	R/W	SWR1_MD_BURST	SWR2_MD_BURST	SWR1_VOUTUP		TI reserved	SWR1_BST_HEFF	TI reserved	
6Eh	UtilCfg	R/W	GPOUT_HL	GPOUT_ENA	SWROCP_SELCLK		TI reserved		SWR1_GPIO_CNTL	SWR2_GPIO_CNTL
6Fh	MonitorSet	R/W	ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPERR_MON	TSDFAULT_MON	TI reserved

(1) VTRK and VLOAD is exclusive, using same DAC block

8.6.4 Detailed Description of Register

8.6.4.1 REG01 12-Bit DAC for Tilt

Figure 27. Tilt (REG01) 12-Bit DAC for Tilt (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VTLT			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTLT							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Tilt (REG01) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VTLT	w-0		Digital input code for Tilt. 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by "differential Tilt mode (REG74[7])" TLT_OUT = VTLT × (6.0 / 2048) (DIFF_TLT = 0) TLT_OUT = (VFCS-VTLT) × (6.0 / 2048) (DIFF_TLT = 1) TLT_OUT should be changed after writing VFCS. In DIFF_TLT mode (DIFF_TLT = 1), TLT_OUT should be changed after writing VFCS.

8.6.4.2 REG02 12-Bit DAC for Focus

Figure 28. Focus (REG02) 12-Bit DAC for Focus (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VFCS			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VFCS							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Focus (REG02) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VFCS	w-0		Digital input code for Focus 2's complement format 0x800(-2048) to 0x7ff(+2047) Output is changed by "differential Tilt mode (REG74[7])" FCS_OUT = VFCS × (6.0 / 2048) (DIFF_TLT = 0) FCS_OUT = (VFCS – VTLT) × (6.0 / 2048) (DIFF_TLT = 1)

8.6.4.3 REG03 12-Bit DAC for Tracking

Figure 29. Tracking (REG03) 12-Bit DAC for Tracking (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VTRK			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VTRK							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Tracking (REG03) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VTRK	w-0		Digital input code for Tracking. 2's complement format 0x800(-2048) to 0x7ff(+2047) TRK_OUT = VTRK × (6.0 / 2048)

8.6.4.4 REG04 12-Bit DAC for Sled1

Figure 30. Sled1 (REG04) 10bit DAC for Sled1 (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VSLD1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Sled1 (REG04) Field Descriptions

Bit	Field	Type	Default	Description
11-2	VSLD1	w-0		Digital input code for Sled1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD1[1:0], will be handled with zero. SLD1_OUT = VSLD1 × (440mA/2048)

8.6.4.5 REG05 12-Bit DAC for Sled2

Figure 31. Sled2 (REG05) 10bit DAC for Sled2 (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VSLD2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSLD2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Sled2 (REG05) Field Descriptions

Bit	Field	Type	Default	Description
11-2	VSLD2	w-0		Digital input code for Sled2. 2's complement format 0x800(-2048) to 0x7ff(+2047) Two bits on LSB, VSLD2[1:0], will be handled with zero. SLD2_OUT = VSLD2 × (440mA/2048)

8.6.4.6 REG06 12-Bit DAC for Stepping1

Figure 32. Stepping1 (REG06) 8bit DAC for Stepping1 (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VSTP1			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP1							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Stepping1 (REG06) Field Descriptions

Bit	Field	Type	Default	Description
11-4	VSTP1	w-0		Digital input code for Stepping1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Four bits on LSB, VSTP1[3:0], will be handled with zero. VSTP1_OUT = VSTP1 × (5.0/2048) @P5V=5.0V

8.6.4.7 REG07 12-Bit DAC for Stepping2

Figure 33. Stepping2 (REG07) 8bit DAC for Stepping2 (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VSTP2			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSTP2							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Stepping2 (REG07) Field Descriptions

Bit	Field	Type	Default	Description
11-4	VSTP2	w-0		Digital input code for Stepping1. 2's complement format 0x800(-2048) to 0x7ff(+2047) Four bits on LSB, VSTP2[3:0], will be handled with zero. VSTP2_OUT = VSTP2 × (5.0/2048) @P5V=5.0V

8.6.4.8 REG08 12-Bit DAC for Spindle

Figure 34. Spindle (REG08) 12-Bit DAC for Spindle (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VSPM			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VSPM							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Spindle (REG08) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VSPM	w-0		Digital input code for Spindle. 2's complement format 0x800(-2048) to 0x7ff(+2047) SPM_OUT = VSPM × (6.0 / 2048)

8.6.4.9 REG09 12-Bit DAC for Load

Figure 35. Load (REG09) 12-Bit DAC for Load (VDAC_MAPSW = 0)

15	14	13	12	11	10	9	8
				VLOAD			
				w-0	w-0	w-0	w-0
7	6	5	4	3	2	1	0
VLOAD							
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Load (REG09) Field Descriptions

Bit	Field	Type	Default	Description
11-0	VLOAD	w-0		Digital input code for Load. 2's complement format 0x800(-2048) to 0x7ff(+2047) LOAD_OUT = VLOAD × (6.0 / 2048)

8.6.4.10 REG63 8-Bit Control Register for SpinAdj

Figure 36. SpinAdj (REG63)

7	6	5	4	3	2	1	0
TI reserved						Mask_Plus	TI reserved
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. SpinAdj (REG63) Field Descriptions

Bit	Field	Type	Default	Description
7-2	TI reserved	r-0		
1	Mask_Plus	r-0	0	Mask Plus bit enables fly back robustness by optimizing masking time. 0: Default masking time 1: Extended masking time for large inductance motor
0	TI reserved	r-0		

8.6.4.11 REG6C 8-Bit Control Register for EDetCfg

Figure 37. EDetCfg (REG6C)

7	6	5	4	3	2	1	0
TI reserved						STP_WIND_HIZ	STP_WIND_H
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. EDetCfg (REG6C) Field Descriptions

Bit	Field	Type	Default	Description
7-2	TI reserved	r-0		
1	STP_WIND_HIZ	r-0	0	0: normal end detection 1: when detecting BEMF, set STP1 and STP2 FET HIZ to reduce mutual noise.
0	STP_WIND_H	r-0	0	0: normal end detection 1: when detecting BEMF, set driving phase to Hi (Detecting phase put Hi-Z) to reduce mutual noise.

8.6.4.12 REG6D 8-Bit Control Register for DCCfg

Figure 38. DCCfg (REG6D)

7	6	5	4	3	2	1	0
SWR1_MD_BURST	SWR2_MD_BURST	SWR1_VOUTUP		TI reserved	SWR1_BST_HEFF	TI reserved	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. DCCfg (REG6D) Field Descriptions

Bit	Field	Type	Default	Description
7	SWR1_MD_BURST	rw-0	0	0: V1Px normal regulation 1: V1Px discontinuous mode
6	SWR2_MD_BURST	rw-0	0	0: V3P3 normal regulation 1: V3P3 discontinuous mode
5-4	SWR1_VOUTUP	rw-0	0	V1Px DC-DC converter voltage up **For 1.2 V or 1.5 V:** 00: 0% 01: 2% 10: 3.6% 11: 5.5% **For 1.0 V:** 00: 0% 01: 1.3% 10: 2.4% 11: 3.3%
3	TI reserved	rw-0		
2	SWR1_BST_HEFF	rw-0	0	1: V1Px High efficiency mode on discontinuous mode This bit will be enabled in SWR1_MD_BURST=1
1-0	TI reserved	rw-0		

8.6.4.13 REG6E 8-Bit Control Register for UtilCfg

Figure 39. UtilCfg (REG6E)

7	6	5	4	3	2	1	0
GPOUT_HL	GPOUT_ENA	SWROCP_SELCLK		TI reserved		SWR1_GPIO_CNTL	SWR2_GPIO_CNTL
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. UtilCfg (REG6E) Field Descriptions

Bit	Field	Type	Default	Description
7	GPOUT_HL	rw-0	0	GPOUT (general-purpose output) pin output selection 0: low output 1: high output valid only REG6F = 00h
6	GPOUT_ENA	rw-0	0	Enable monitor signal output to GPOUT pin 0: No signal output, Hi-Z 1: output signal selected in REG6F with CMOS output Output is Logical OR when selected two more signals
5-4	SWROCP_SELCLK	rw-0	0	Over current protection monitoring frequency 5 counts by 00: 5 kHz (= exceed 1 ms) 01: 20 kHz 10: 50 kHz 11: 500 kHz
3-2	TI reserved	rw-0		
1	SWR1_GPIO_CNTL	rw-0	0	Set REG1PX pin as GPIO1 pin. 0: REG1PX pin as 1.xV DC-DC converter output 1: Open drain control for GPOUT1 pin (at V1Px DC-DC disable)
0	SWR2_GPIO_CNTL	rw-0	0	Set REG3P3 pin as GPIO2 pin. 0: REG3P3 pin as 3.3V DC-DC converter output 1: Open drain control for GPOUT1 pin (at V1Px DC-DC disable) Open drain control for GPOUT2 pin (at V3P3 DC-DC disable)

8.6.4.14 REG6F 8-Bit Control Register for MonitorSet

Figure 40. MonitorSet (REG6F)

7	6	5	4	3	2	1	0
ACTTIMER_FLT_MON	ENDDET_MON	SIF_TIMEOUTERR_MON	PWRERR_MON	TSDERR_MON	OCPERR_MON	TSDFAULT_MON	TI reserved
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. MonitorSet (REG6F) Field Descriptions

Bit	Field	Type	Default	Description
7	ACTTIMER_FLT_MON	rw-0	0	1: ACTTIMER fault output to GPOUT pin
6	ENDDET_MON	rw-0	0	1: ENDDET monitor output to GPOUT pin
5	SIF_TIMEOUTERR_MON	rw-0	0	1: SIF timeout monitor output to GPOUT pin
4	PWRERR_MON	rw-0	0	1: PWRERR monitor output to GPOUT pin
3	TSDERR_MON	rw-0	0	1: TSDERR fault output to GPOUT pin
2	OCPERR_MON	rw-0	0	1: OCPERR fault output to GPOUT pin
1	TSDFAULT_MON	rw-0	0	1: TSDFAULT fault output to GPOUT pin

8.6.4.15 REG70 8bit Control Register for DriverEna

Figure 41. REG70 8bit Control Register

7	6	5	4	3	2	1	0
TLT_ENA	FCS_ENA	TRK_ENA	SPM_ENA	SLD_ENA	STP_ENA	LOAD_ENA	XSLEEP
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. DriverEna (REG70) Field Descriptions

Bit	Field	Type	Default	Description
7	TLT_ENA	rw-0		1 : Tilt enable (with XSLEEP=1)
6	FCS_ENA	rw-0		1: Focus enable (with XSLEEP=1)
5	TRK_ENA	rw-0		1: Track enable (with XSLEEP=1)
4	SPM_ENA	rw-0		1: Spindle enable (with XSLEEP=1)
3	SLD_ENA	rw-0		1: Sled enable (with XSLEEP=1)
2	STP_ENA	rw-0		1: Step enable (with XSLEEP=1)
1	LOAD_ENA	rw-0		1 : LOAD enable (with XSLEEP=1) Track (bit5:TRK_ENA) will be disabled at LOAD_ENA=1 because of sharing the DAC PWM module. Load priority is higher than TRK_ENA.
0	XSLEEP	rw-0		1: Operation mode 0: Power save mode Charge pump enable bit. All driver enable bit (Bit[7:1]) change disabled and output change to Hi-Z (regardless of setting xxx_ENA bit is 1 when setting XSLEEP to 0. Therefore set 1 to XSLEEP before setting each enable bits.

8.6.4.16 REG71 8-Bit Control Register for FuncEna

Figure 42. REG71 8-Bit Control Register for FuncEna (REG71)

7	6	5	4	3	2	1	0
SPM_LSMODE	ENDDET_ENA	ENDDET_SLCT	LED_ON	CSW_ON	TEMPMON_ENA	TI reserved	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. FuncEna (REG71) Field Descriptions

Bit	Field	Type	Default	Description
7	SPM_LSMODE	rw-0		0 : Spindle Normal rotation mode 1 : Light Scribe mode (slow rotation mode)
6	ENDDET_ENA	rw-0		1 : use sled/step End detection enable (with STP_ENA=1 or SLD_ENA=1)
5	ENDDET_SLCT	rw-0		0 : Sled End detection monitor 1 : Step End detection monitor
4	LED_ON	rw-0		1 : LEDO enable (with XSLEEP=1)
3	CSW_ON	rw-0		1 : CSWO enable (with XSLEEP=1)
2	TEMPMON_ENA	rw-0		1: enable chip temperature monitoring (with XSLEEP=1)
1-0	TI reserved	rw-0		Reserved

8.6.4.17 REG72 8-Bit Control Register for ACTCfg

Figure 43. ACTCfg (REG72)

7	6	5	4	3	2	1	0
LOAD_O5CH_HIGH	LOADPROT_OFF	ACTPROT_OFF	ACTTEMPTH				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. ACTCfg (REG72) Field Descriptions

Bit	Field	Type	Default	Description
7	LOAD_05CH_HIGH	rw-0	0	LOAD output polarity at 0.5CH (REG74h[6]=1) 0: LOADP=Low 1: LOADP=High
6	LOADPROT_OFF	rw-0	0	1: Load Over Current Protection OFF
5	ACTPROT_OFF	rw-0	0	0 : Actuator protection ON 1 : Actuator Fault monitor disable (No protection for ACT channel)
4-0	ACTTEMPTH	rw-0	0	Actuator thermal protection (=ACT Timer) threshold level ACT Timer Protection enable except ACTTEMPTH[4:0] = 0x00 ACTTEMPTH = 0x00 equal to ACTPROT_OFF = 1 By writing value 0x00, ACTTIMER_PROT flag is cleared.

8.6.4.18 REG73 8-Bit Control Register for Parm0

Figure 44. Parm0 (REG73)

7	6	5	4	3	2	1	0
SIF_TIMEOUT_TH		SLEDEND_HZTIME	SLDENDTH		STPEND_HZTIME	STPENDTH	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Parm0 (REG73) Field Descriptions

Bit	Field	Type	Default	Description
7-6	SIF_TIMEOUT_TH	rw-0	0	Watch dog timer for Serial communication 0: disable 1: 1 ms 2: 100 µs 3: 10 µs Set SIF_TIMEOUTERR (REG7F) if communication is suspended for this time period. XRESET processing will be performed if a SIF_TIMEOUTERR occurs.
5	SLEDEND_HZTIME	rw-0	0	Time window for sled end detection. 0: 400 µs 1: 200 µs Caution) Need to recycle ENDDET_ENA = 0 → 1 after writing this bit.
4-3	SLDENDTH	rw-0	0	Sled end detection sensibility setting. Detection threshold for motor BEMF 00: 46 mV 01: 86 mV 10: 0 mV 11: 22 mV
2	STPEND_HZTIME	rw-0	0	Step High-Z detection period in End detection 0: 400 µs 1: 200 µs Caution) Need to recycle ENDDET_ENA = 0 → 1 after writing this bit.
1-0	STPENDTH	rw-0	0	Step end detection sensibility setting 00: 39 mV 01: 60 mV 10: 0 mV 11: 19 mV

8.6.4.19 REG74 8-Bit Control Register for SIFCfg

Figure 45. SIFCfg (REG74)

7	6	5	4	3	2	1	0
DIFF_TLT	LOAD_05CH	RDSTAT_ON_VFCS	VSLD2_POL	VSTP2_POL	ADVANCE_RD	SOMI_HIZ	VDAC_MAPSW
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. SIFCfg (REG74) Field Descriptions

Bit	Field	Type	Default	Description
7	DIFF_TLT	rw-0	0	1 : Differential Tilt mode enable (with TLT_ENA=FCS_ENA=1) Differential Tilt mode (DIFF_TLT=1), DAC value setting as follows FCS_OUT=(VFCS+VTLT) × 6/2048 TLT_OUT=(VFCS-VTLT) × 6/2048 In DIFF_TLT mode (DIFF_TLT=1), TLT_OUT should be changed after writing VFCS.
6	LOAD_05CH	rw-0	0	The setting of Load motor driving type. Load output changes as follow 0: 1ch mode (LOAD output is controlled by DAC code, VLOAD) Use for Slot-in model or 1ch tray model. 1: 0.5Ch mode (LOAD is only controlled by LOAD_05CH_HIGH) Use for Tray model
5	RDSTAT_ON_VFCS	rw-0	0	Set Read status data (REG7F) at VFCS write command (REG02) 1: enable Write and Read mode (Write 12bits Focus DAC data + Read 8bits status data)
4	VSLD2_POL	rw-0	0	change direction of SLED rotation
3	VSTP2_POL	rw-0	0	change direction of STEP rotation
2	ADVANCE_RD	rw-0	0	Advanced serial read timing 1: Read back timing changes half clock advance.
1	SOMI_HIZ	rw-0	0	0: SOMI line High-Z at bus idling time. 1: SOMI line Pull Down at bus idling time.
0	VDAC_MAPSW	rw-0	0	1: change channel assignments of DAC register (REG01~09)

8.6.4.20 REG76 8-Bit Control Register for WriteEna

Figure 46. WriteEna (REG76)

7	6	5	4	3	2	1	0
WRITE_ENABLE	TI reserved						REG6X_WR
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. WriteEna (REG76) Field Descriptions

Bit	Field	Type	Default	Description
7	WRITE_ENABLE	rw-0	0	0: Register Write disable except REG76 1: Write enable for registers REG01~0B, REG70~7F
6-1	TI reserved	rw-0		
0	REG6X_WR	rw-0	0	0: Register REG63 write disable 1: Register REG63 write enable

8.6.4.21 REG77 8-Bit Control Register for ClrReg

Figure 47. ClrReg (REG77)

7	6	5	4	3	2	1	0
RST_INDAC	RST_REGS	RST_ERR_FLAG	RST_REGS_WO3	TI reserved			
w-0	w-0	w-0	w-0	w-0	w-0	w-0	w-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. ClrReg (REG77) Field Descriptions

Bit	Field	Type	Default	Description
7	RST_INDAC	w-0	0	1 : Reset all 12bit input DAC register (REG01~0B) *Self clear bit
6	RST_REGS	w-0	0	1 : Reset all 8bit R/W Registers (REG70h~77h, 60h-6Fh) *Self clear bit
5	RST_ERR_FLAG	w-0	0	1 : Reset Fault Flag Latch (REG7F[5:1], REG79~REG7B) *Self clear bit
4	RST_REGS_WO3	w-0	0	1 : Reset all 8bit R/W Registers w/o XSLEEP, CSW_ON, LED_ON (REG70h~76h, REG60h~66h) *Self clear bit
3-0	TI reserved	w-0		

8.6.4.22 REG78 8-Bit Control Register for ActTemp

Figure 48. ActTemp (REG78)

7	6	5	4	3	2	1	0
TI reserved		ACT_TIMER_PROT	ACTTEMP				
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. ActTemp (REG78) Field Descriptions

Bit	Field	Type	Default	Description
7-6	TI reserved	r-0		
5	ACT_TIMER_PROT	r-0	0	ACT timer protection flag 1: ACT Timer Protection has detected and latched. (ACTTEMP > ACTTEMPTH) This bit holds data after temperature change to low since this is a latch bit. Also driver output keep Hi-Z until setting RST_ERR_FLAG or ACTTEMPTH = 0.
4-0	ACTTEMP	r-0	0	An integrated value of ACT_TIMER counters at present.

8.6.4.23 REG79 8-Bit Control Register for UVLOMon

Figure 49. UVLOMon (REG79)

7	6	5	4	3	2	1	0
TI reserved			UVLO_A5V	UVLO_INT3P3	UVLO_SWR3P3	UVLO_SWR1PX	OVP_P5V
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. UVLOMon (REG79) Field Descriptions

Bit	Field	Type	Default	Description
7-5	TI reserved	r-0		
4	UVLO_A5V	r-0	0	UVLO flag for detection Low A5V supply(1)
3	UVLO_INT3P3	r-0	0	UVLO flag for detection Low internal 3.3V regulator(1)
2	UVLO_SWR3P3	r-0	0	UVLO flag for detection Low DC-DC 3.3V (1)
1	UVLO_SWR1PX	r-0	0	UVLO flag for detection Low DC-DC 1.xV (1)
0	OVP_P5V	r-0	0	Over voltage protection flag for P5Vsply (1)

(1) Latched first reset event only. Cleared by “RST_ERR_FLG” (REG77)

8.6.4.24 REG7A 8-Bit Control Register for ThPMon

Figure 50. ThPMon (REG7A)

7	6	5	4	3	2	1	0
TSD_FAULT_SWR	TSD_FAULT_SPM	TSD_FAULT_ACT	TSD_FAULT_LEDCSW	TSD_SWR	TSD_SPM	TSD_ACT	TSD_ LEDCSW
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. ThPMon (REG7A) Field Descriptions

Bit	Field	Type	Default	Description
7	TSD_FAULT_SWR	r-0	0	Pre alert of thermal protection for DC-DC converter block*.
6	TSD_FAULT_SPM	r-0	0	Pre alert of thermal protection of Spindle block*
5	TSD_FAULT_ACT	r-0	0	Pre alert of thermal protection of Focus /Track /Tilt Sled1 /Sled2 /Step1 /Step2 /Load *
4	TSD_FAULT_LEDCSW	r-0	0	Pre alert of thermal protection of CSW/LED *
3	TSD_SWR	r-0	0	Thermal protection flag for DC-DC converter block * DC-DC converter output Hi-Z until temperature falls on release level 1: detect (latch)
2	TSD_SPM	r-0	0	Thermal protection flag for Spindle * SPM output Hi-Z until temperature falls on release level 1: detect (latch)
1	TSD_ACT	r-0	0	Thermal protection flag for Focus /Track /Tilt Sled1 /Sled2 /Step1 /Step2 /Load * Actuator output Hi-Z until temperature falls on release level 1: detect (latch)
0	TSD_ LEDCSW	r-0	0	Thermal protection flag for CSW/LED * LED/CSW output Hi-Z until temperature falls on release level 1: detect (latch)

8.6.4.25 REG7B 8-Bit Control Register for OCPMon

Figure 51. OCPMon (REG7B)

7	6	5	4	3	2	1	0
TI reserved			OCP_SWR	OCP_STP	OCP_LOAD	OCP_LED	OCP_CSW
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. OCPMon (REG7B) Field Descriptions

Bit	Field	Type	Default	Description
7-5	TI reserved	r-0		
4	OCP_SWR	r-0	0	Over current protection flag bit for DC-DC converter block. (1)
3	OCP_STP	r-0	0	Over current protection flag bit for step block. (1)
2	OCP_LOAD	r-0	0	Over current protection flag bit for Load block. (1)
1	OCP_LED	r-0	0	Over current protection flag bit for LED block. (1)
0	OCP_CSW	r-0	0	Over current protection flag bit for CSW block. (1)

(1) Cleared by “RST_ERR_FLAG” bit (REG77)

8.6.4.26 REG7C 8-Bit Control Register for TempMon

Figure 52. TempMon (REG7C)

7	6	5	4	3	2	1	0
TI reserved	CHIPTEMP_STATUS	CHIPTEMP					
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. TempMon (REG7C) Field Descriptions

Bit	Field	Type	Default	Description
7	TI reserved	r-0		
6	CHIPTEMP_STATUS	r-0	0	1: New data CHIPTEMP[5:0] is updated It will be cleared after reading.
5-0	CHIPTEMP	r-0	0	Chip temperature monitor (2.5deg/LSB) 15(0) to 172.5(63) degrees. For monitoring, TEMPMON_ENA=1 and XSLEEP=1 is required

8.6.4.27 REG7E 8-Bit Control Register for Version (REG7E)

Figure 53. Version (REG7E)

7	6	5	4	3	2	1	0
Version							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Version (REG7E) Field Descriptions

Bit	Field	Type	Default	Description
7-0	Version	r-0		Version[7:4] = revision number of TPIC2010 Version[3:0]=option

8.6.4.28 REG7F 8-Bit Control Register for Status (REG7F)

Figure 54. Status (REG7F)

7	6	5	4	3	2	1	0
ACTTIMER_FAULT	ENDDET	SIF_TIMEOUTERR	PWRERR	TSDERR	OCPERR	TSDFAULT	FG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Status (REG7F) Field Descriptions

Bit	Field	Type	Default	Description
7	ACTTIMER_FAULT	r-0	0	Status flag of ACTTIMER protection 1: Pre alert of ACTTIMER protection. It is close to the threshold level. You can get current ACTTIMER value in REG78. Both of this bit and ACT_TIMER_PROT (REG78) will be set when over the threshold.
6	ENDDET	r-0	0	status flag of END detection 1: end position detected (not latch bit)
5	SIF_TIMEOUTERR	r-0	0	error flag of serial I/F watch dog timer 1: SIF communication was interrupted, expired watch dog timer
4	PWRERR	r-0	0	error flag of Power 1 : Voltage problem occurred, details in REG79
3	TSDERR	r-0	0	error flag of any over thermal protections 1: Dispatched thermal protection, details in REG7A
2	OCPERR	r-0	0	error flag of any over current protection 1: Dispatched OCP, details in REG7Bh
1	TSDFAULT	r-0	0	warning of TSD of any thermal protection 1 : Detect pre thermal protection details in REG7A
0	FG	r-0	0	FG signal. Spindle rotation pulse for speed monitor

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

NOTE

- Operate every driver channel after 5 V power supplied and stable.
- To calculate spindle motor driver over current limit (I_{Limit}), use the following equation. I_{Limit} = Internal REF voltage / RCS = 196 mV / 0.22 Ω ≈ 890 mA
- Appropriate capacity of decoupling capacitor is required enough value of over 10 µF due to reduce influence of PWM switching noise. And the A5V pin needs to connect a filter of 1 µF. It is effective to put bypass capacitor (about 0.1 µF) near power pin (P5V_1, P5V_2, P5V_SW, P5V_SPM1, P5V_SPM2) for PWM switching noise reduction on power and GND line.
- Much current flow to driver circuits, to consider as below matters.
  - Pattern-layout and line-impedance. And noise influence from supply line.

9.1 Application Information

9.1.1 DAC Type

TPIC2010 has nine channels of Actuator. Each channel is assigned to the most suitable DAC engine with a different type respectively. ACT(F/T/Ti) has 12-bit DAC. Upper 8 (MSB sign bit) are converted at a time in 5MHz and LSB 4 bits are output in sequence with 1.25-MHz PWM. SPIN, SLED and Load DAC has same DAC types and sampling rate with 312kHz. All channel (except SLED and STP) have x6 gain. The DAC for STP is 8-bits resolution output with 40 kHz PWM, no Feed Back. The Gain for STP is 5x relative to P5V voltage. Table 36 shows configuration of each actuator.

Table 36. List 5 DAC Type

	FCS/TRK/TLT	SLED	SPIN	LOAD	STP
Resolution	12bit	10bit	12bit	12bit	8bit
Type	8-bit over sampling	8-bit over sampling	8-bit over sampling	8-bit over sampling	1 bit Direct Duty PWM
Sampling	1.25M / 10bit 312K / 12bit	1.25M / 10bit 312K / 12bit	312K	312K	40 kHz
PWM freq	312 kHz	78 kHz	156 kHz	312 kHz	40 kHz
Out range	±6 V	±440 mA	±6 V	±6 V	±(P5V*1)
Feed back	Voltage feedback	Current feedback	Power supply compensation	Voltage feedback shared with TRK	Direct PWM no feedback

9.1.2 Example Sampling Rate of 12-Bit DAC for FCS/TRK/TLT

The input data is separated in the upper 8 bits and the lower 4 bits. Upper 8 bits (MSB sign 1 bit) will be put into 8-bit current DAC in every 5 MHz. The lower 4 bits will be put into one bit current DAC in sequence from upper to lower bit. This one bit DAC output with PWM in 1.25 MHz. At any PWM duty, 100%, 75%, 50%, 25%, or 0%, will be summed in 8-bit current DAC in every 1.25 MHz. Thus it takes 3.2 µs for all lower 4 bits summing to PWM output. As a result, 12-bit data is sampled in every PWM cycle. Example of sampling rate for FCS/TRK/TLT is Figure 55.

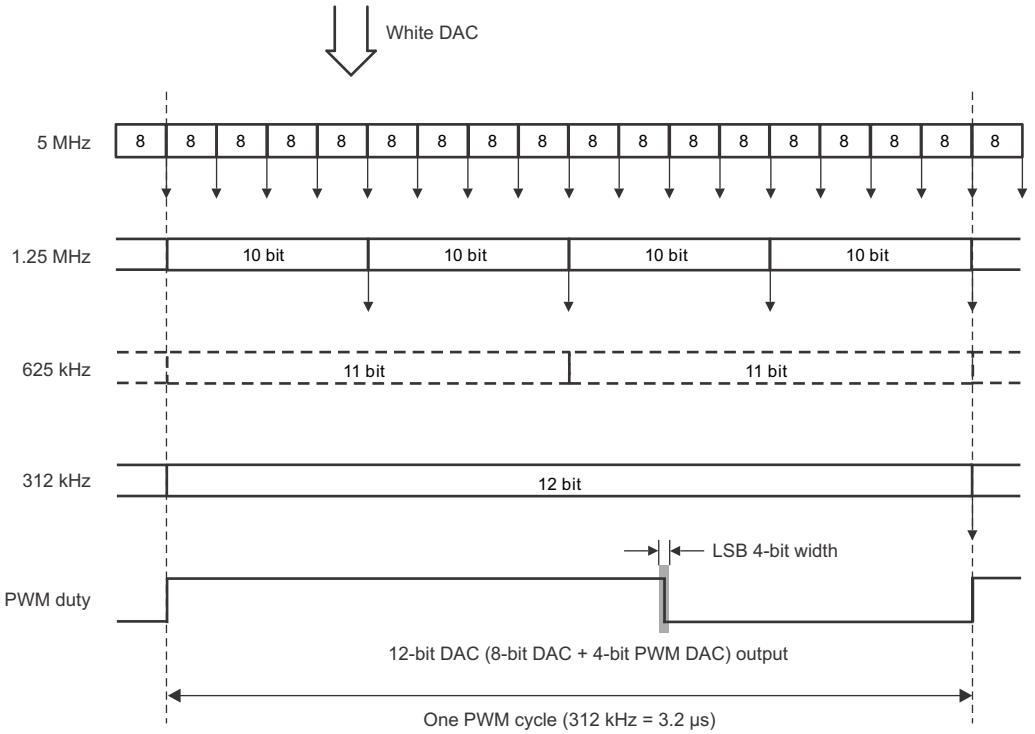


Figure 55. Example of 12-Bit DAC Conversion Time (FCS/TRK/TLT)

9.1.3 Digital Input Coding

The output voltage (current) is commanded via programming to the DAC. All of the DAC input format is 12bit in two's complement though some DAC has a low resolution. When 12 bits data is input 8 bits DAC, TPIC2010 recognizes four subordinate position bits (LSB) as 0. To arrange for 12bit DAC format, DSP should shift 8bit or 10 bit data to an appropriate bit position. The full scale is +/-1.0 V and driver gain is set 6. The output voltage (Vout) is given by the following equation:

$$Vout = DACcode \times \frac{6.0}{2048} \quad (1)$$

$$Vdac = 1.0 \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + \ldots + bit[0] \times 0.5^{11}\right)$$

$$Vdac = (-1.0) \times \left(bit[10] \times 0.5^{1} + bit[9] \times 0.5^{2} + bit[8] \times 0.5^{3} + \ldots + bit[0] \times 0.5^{11} + 0.5^{12}\right)$$

$$Vout = Vdac \times 6.0\ (V)$$

$$STPVout = Vdac \times (P5V)\ (V)$$

$$SLEDIout = Vdac \times 0.44\ (A)$$

where

- bit[11:0] is the digital input value, range 000000000000b to 111111111111b. (2)

Table 37. DAC Format

MSB DIGITAL INPUT (BIN) LSB	HEX	DEC	VDAC	ANALOG OUTPUT
1000_0000_0000	0x800	–2048	–0.9995	–5.997
1000_0000_0001	0x801	–2047	–0.9995	–5.997
1111_1111_1111	0xFFF	–1	–0.0005	–0.003
0000_0000_0000	0x000	0	0	0.000
0000_0000_0001	0x001	+1	+0.0005	+0.003
0111_1111_1110	0x7FE	+2046	+0.9990	+5.994

Table 37. DAC Format (continued)

MSB DIGITAL INPUT (BIN) LSB	HEX	DEC	VDAC	ANALOG OUTPUT
0111_1111_1111	0x7FF	+2047	+0.9995	+5.997

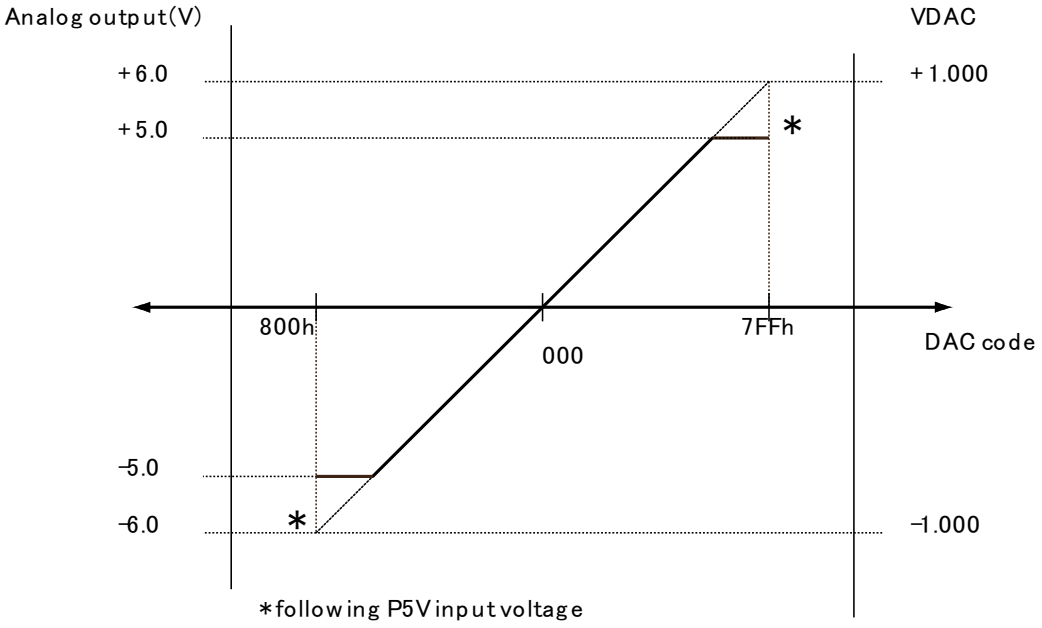


Figure 56. Output Voltage vs DAC Code

9.1.4 Example Timing of Target Control System

TPIC2010 is designed for that meets the requirements updating control data in 400 kHz. The example of control system parameter is Table 38. It takes 0.51 µs for transmit a 16-bit data packet to TPIC2010 with 35-MHz SCLK. Therefore, DSP can be sent four packets a 400-kHz interval. If SCLK is lower than 28.8 MHz, the system designer must reduce the packet quantity under three. For example, Focus/Truck command is updating in every 2.5 µs (400 kHz), and it is able to send another two kind of packet in this same slot. Figure 57 shows the example of the control timing when TPIC2010 is used.

Table 38. Example Timing of Target Control System

SIGNAL	BIT	UPDATE CYCLE (kHz)
Focus	12	400
Track	12	400
Tilt	12	100
Sled1	10	100
Sled2	10	100
Spindle	12	100
Load	12	—
Step1	8	40
Step2	8	40

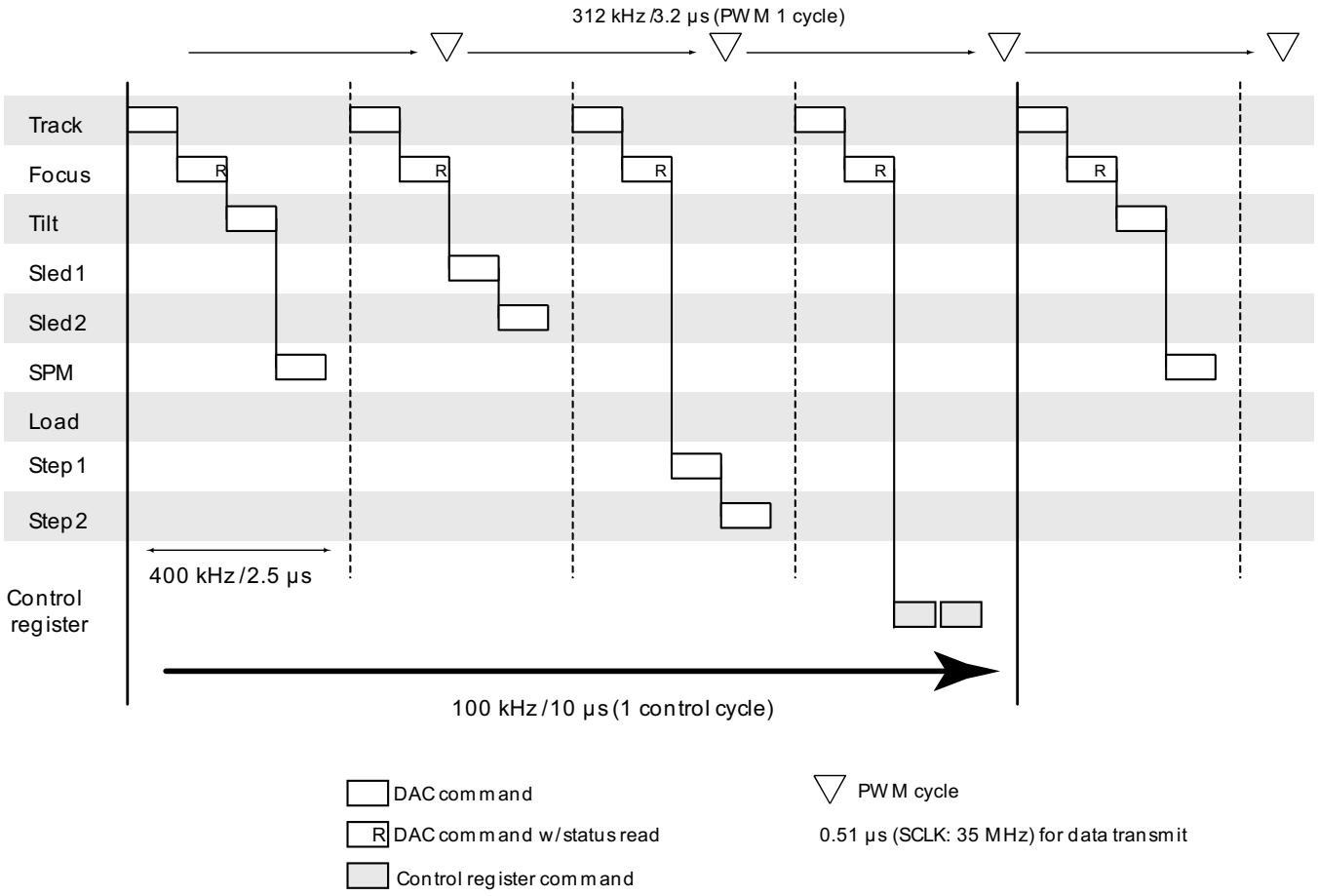


Figure 57. Example DAC Control

9.1.5 Spindle Motor Driver Part

When VSPM is set a positive DAC code then it'll be into acceleration mode. "IS" mode operates then the start-up circuit offers the special start-up pattern sequence to the driver in start-up, and then switch to spin-up mode by detecting the rotor position by BEMF signal from the spindle motor coil.

The spin-down and brake function also be controlled by DAC value VSPM. When it's set the brake command to VSPM, driver goes into active-brake mode, then switch to short-brake mode in slow revolution speed, and then stop automatically. The FG signal is composed from EXOR of three-phase signal, and is output from XFG pin shown below.

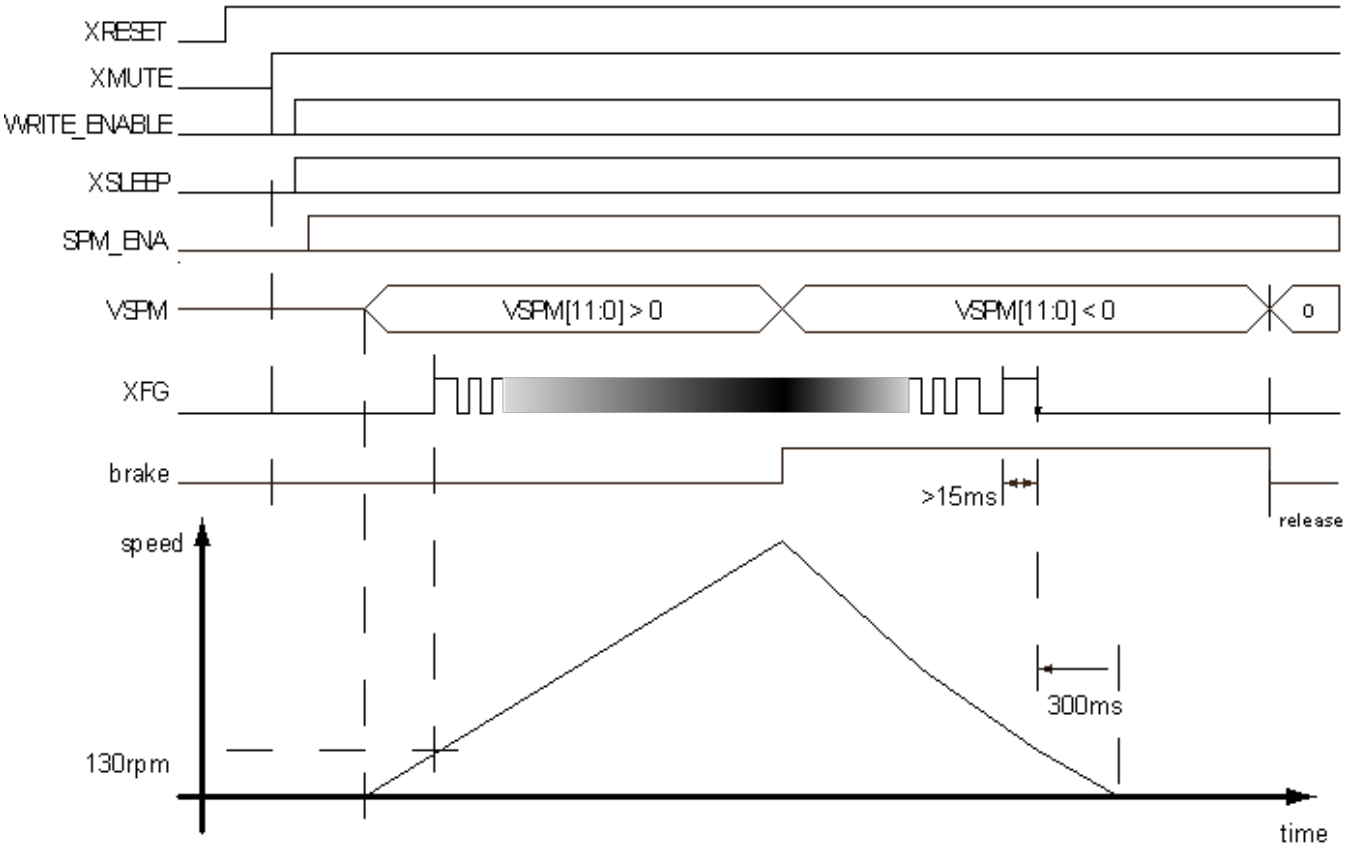


Figure 58. Spindle Operating Sequence

- It is recommended to use down-edge of FG signal for monitoring FG frequency. The FG terminal needs to be pull up to the appropriate supply voltage by external resistor.
- Short Brake mode is asserted after 300ms of FG signal stays L-level in deceleration.
- The FG Output is set to H-level in Sleep Mode in order to reduce sleep mode current.
- This value is the nominal number of using motor with 16-poles.
- First of all, power supply voltage of A5V/P5V must be supplied before any signals input.
- Internal circuit starts after 800 µs(TYP) since XMUTE changed to “H”. Recommended marginal delay value is 1ms for being ready.

9.1.5.1 Spindle PWM Control

The output PWM duty of Spindle is controlled by DAC code (VSPM). The gain in acceleration setting is always six times. However, the maximum output is restricted to P5V voltage. A dead band which output = 0 exists in the width of plus or minus 0x52 focusing on zero.

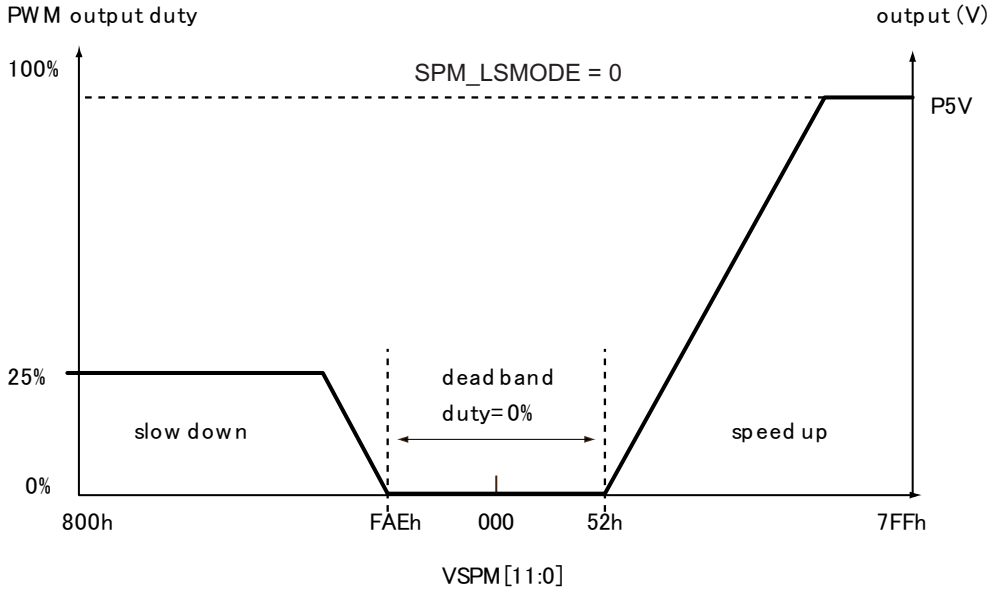


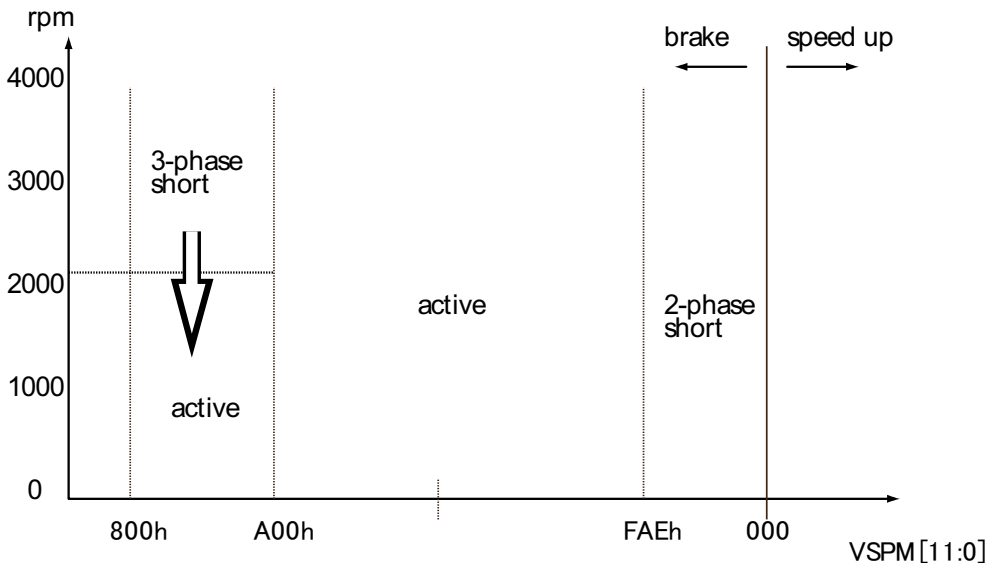
Figure 59. Spindle PWM Control

9.1.5.2 Auto Short Brake Function

TPIC2010 provides auto short brake function which is selecting brake mode automatically by motor speed. Auto Short Brake is the intelligent brake function that includes two modes: short brake and active brake. When VSPM value is controlled more than equivalent 75% duty brake, deceleration is done by short brake under the rotation speed is over 3000 rpm. After deceleration, driver goes into Active-brake mode automatically by internal logic circuit under rotation speed is lower 2000 rpm. This function enables low power consumption and silent during braking.

Table 39. Brake Mode

VSPM[11:0]	ROTATION SPEED (RPM)	
	≈ 0 TO 2000	≈ 3000
0x000 - 0xFAE	2-phase short brake	2-phase short brake
0xFAE - 0xA00	Active brake	Active brake
0xA00 - 0x800	Active brake	3-phase short brake



This value is the nominal number of using motor with 16-poles motor.

Figure 60. Brake Mode Selections

9.1.5.3 Spindle Low Speed Mode

LS mode is the low rotation mode which made the maximum 25% duty. When using SPM_LSMODE = 1, brake mode is always *short brake*. Figure 61 shows the output duty of LS mode.

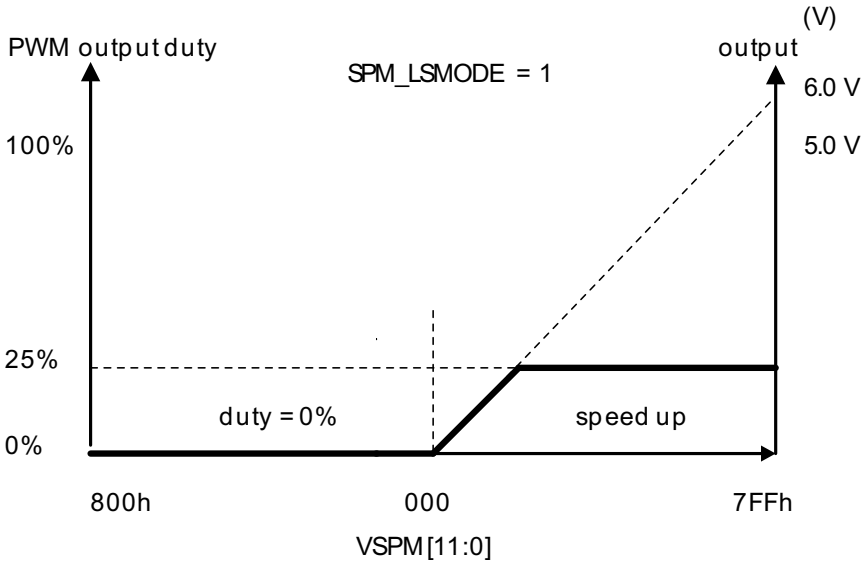


Figure 61. Spindle PWM Control (Low Speed Mode)

9.1.5.4 Spindle Driver Current Limiting Circuit

The current limit circuit monitors the RCS voltage at ICOM pin, and limits the output current by reducing PWM duty, when detecting overcurrent conditions.

9.1.6 Sled Driver Part

The Sled driver outputs the PWM pulse set as DAC code (VSLDx) with current feed back. The maximum output is restricted to 440 mA at 0x7FF and 0x800. A dead band which output = 0 exists in the width of plus or minus 0x33 focusing on zero.

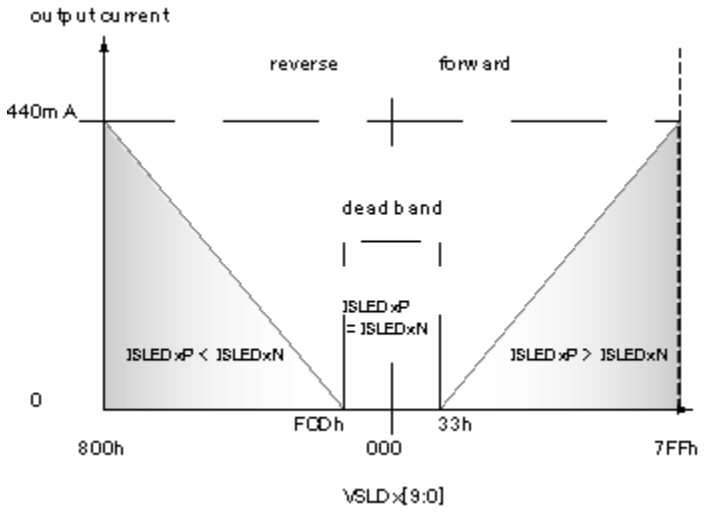


Figure 62. Sled Output Current

- Both outputs of SLED1/2 are “H” when input code is in dead band.

9.1.6.1 End Detect Function

This device has the function of end position detection for Sled and Collimator lens. This function aim to eliminate the position switch at PUH inner and collimator lens end position. This function is enabled by ENDDET_ENA = 1 with setting object actuator (ENDDET_SLCT = 0: for Sled ENDDET_SLCT = 1: for Step). When this function is enabled, internal logic will detect the sled out zero-cross point and at that time, internal BEMF detect circuit measures the BEMF level of stepping motor. There’re four threshold levels. If BEMF is lower than selected threshold, device recognizes motor at stop and ENDDET bit to 1. ENDDET bit will be cleared at the BEMF voltage exceed threshold again.

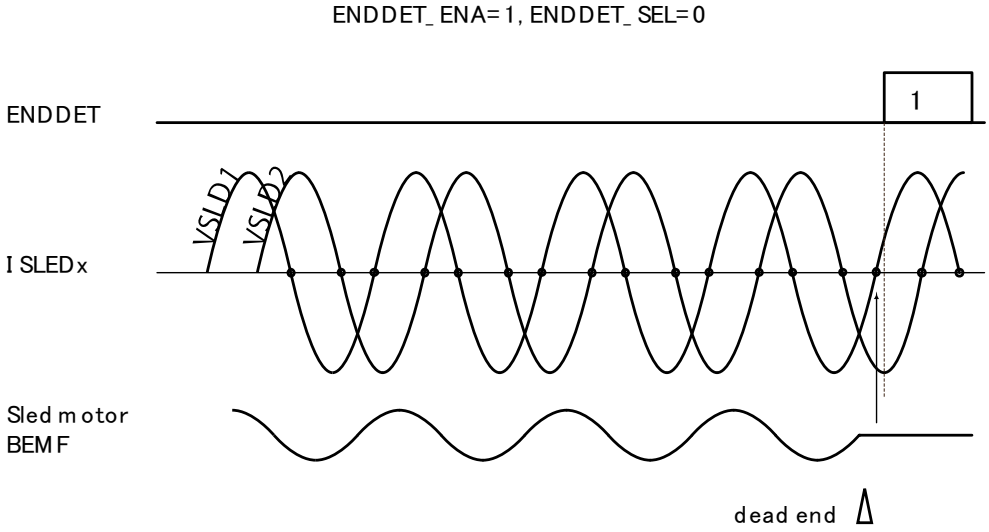


Figure 63. Timing of Sled End Detection

- For the purpose of getting correct stepping motor BEMF, we recommend to choose more than 110Hz (440pps) control frequency. However this control frequency depends on the stepping motor characteristic.
- BEMF detection level is selectable 22, 46, 86 mV.

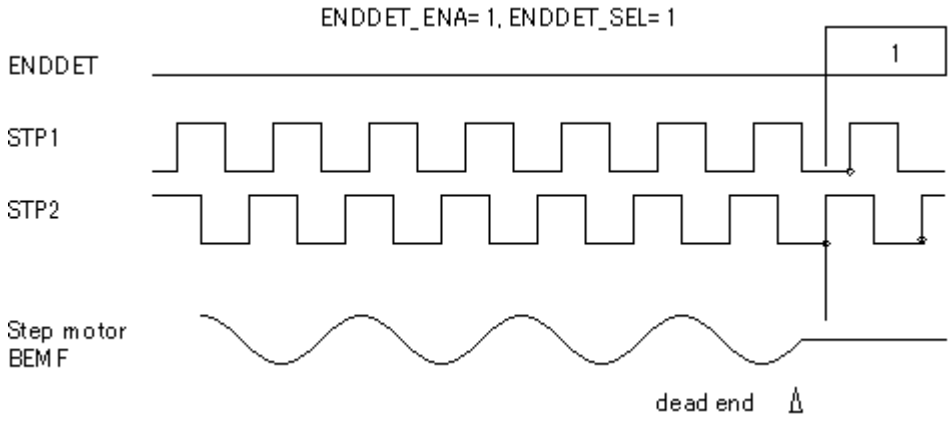


Figure 64. Timing of Step End Detection

- Recommended control speed is around 1200 pps for getting correct BEMF level. It depends on the stepping motor characteristic. Please evaluate on your condition adequately.
- BEMF detection level is selectable 19, 39, 60 mV.

9.1.7 Load Driver Part

Load driver outputs the voltage with voltage feed back corresponding to the input DAC value. This channel has power voltage compensation thus it is suit for Slot-in type load control. This channel becomes active exclusively to other actuator channels. Load driver is shared with the TRK driver.

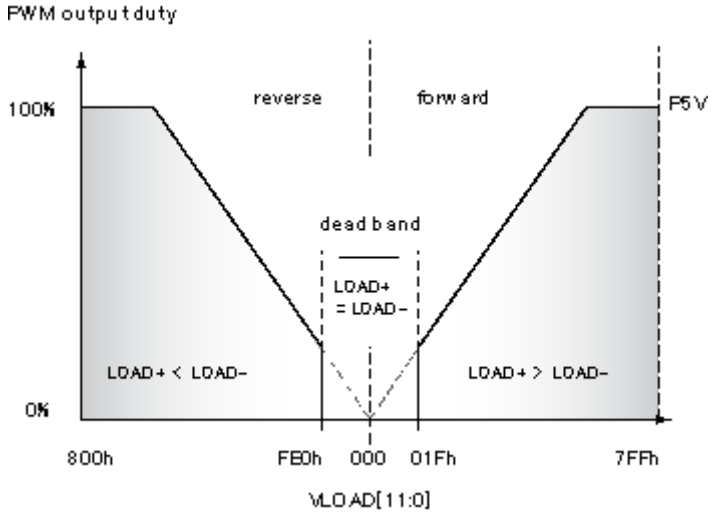


Figure 65. Load Output Duty

- Output voltage is controlled by PWM
- Both LOAD+ and LOAD- are connected to PGND through the internal clamp diode respectively.

9.1.8 Focus/Track/Tilt Driver Part

9.1.8.1 Input vs Output Duty

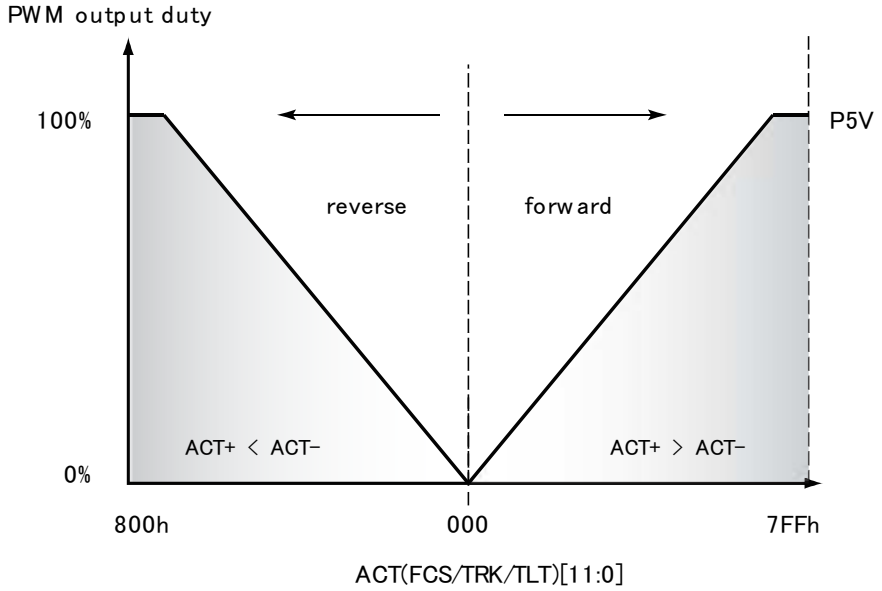


Figure 66. FCS/TRK/TLT Output Duty

9.1.8.2 Differential Tilt Mode

TPIC2010 support differential Tilt mode which output the value calculated from Focus and Tilt. Focus and Tilt can be set in differential mode by DIFF_TLT (REG74) = 1. Because Focus and Tilt are updated at the same time, the update interval of Tilt can be thinned out. Output data changes at after writing VFCS data. Therefore it's necessary to write VFCS data when set VTLT. In differential mode, the output value is calculated as follows.

$$FCS\_OUT = (VFCS + VTLT) \times 6 \quad (3)$$

$$TLT\_OUT = (VFCS - VTLT) \times 6 \quad (4)$$

9.1.9 2-Channel Synchronous DC-DC Converter

TPIC2010 has two channels synchronous step-down DC-DC converters. Two converters operate with a 120-degree turn-on phase shift of the PMOS (high side) transistors. It prevents the high side switches of both regulators to be turned on simultaneously, and therefore smooth the input current. This feature reduces the surge current drawn from the supply.

Switching frequency is 2.5 MHz. Because the ripple current in the coil can reduce, the smaller inductor value can be selected. And the inductor with lowest DC resistance can be selected for highest efficiency. And the regulators have fast transient response.

9.1.9.1 V1Px DC-DC Converter

The V1Px is a DC-DC converter producing an output 1.0, 1.2, 1.5 V. It only requires an external inductor and bypass capacitor(s). The gate drivers and compensations are all internal to the chip. The required input supply is 5 V for P5V_SW. It has a soft start approximately about 0.8ms to limit the in-rush current when the regulator comes alive. The soft-start circuit uses the internal clock to profile its ramp.

It is able to up 2%, 3.8% and 5.5% of the output voltage by setting SWR1_VOUTUP[2] (REG6D) for 1.2 V, 1.5 V. For 1.0 V, up to 1.3%, 2.4% and 3.3%.

9.1.9.2 V3P3 DC-DC Converter

V3P3 is a DC-DC converter producing an output of 3.3 V. It only requires an external inductor and bypass capacitor(s). The gate drivers and compensations are all internal to the chip. The required input supply is 5 V. It has a 0.8ms soft start to limit the in-rush current when the regulator comes alive. The soft-start circuit uses the internal clock to profile its ramp.

9.1.9.3 Setup When Not Using DC-DC Converter

When not using DC-DC converter, it recommends that each terminal makes the following connection.

Table 40. Not Using DC-DC Converter

PIN NAME	PIN NO.	CONNECTION
SWR_SEQ1	18	5V (H)
SWR_SEQ2	19	5V (H)
V1PXSEL	20	5V (H)
FB1PX	25	OPEN
P5V_SW	26	5V
REG1PX	27	OPEN
PGND_SW	28	GND
REG3P3	29	OPEN
FB3P3	30	OPEN

9.1.9.4 Discontinuous Regulation Mode

The regulation mode called discontinuous regulation mode improves the conversion efficiency at a low current loading by changing regulation timing. Discontinuous mode is able to set 1 to SWx_MD_BURST (REG6D) bit. Figure 67 shows the discontinuous regulation action. The current consumption has been reduced by shortening the energizing time of driving FET. On the other hand, DC voltage ripple grows.

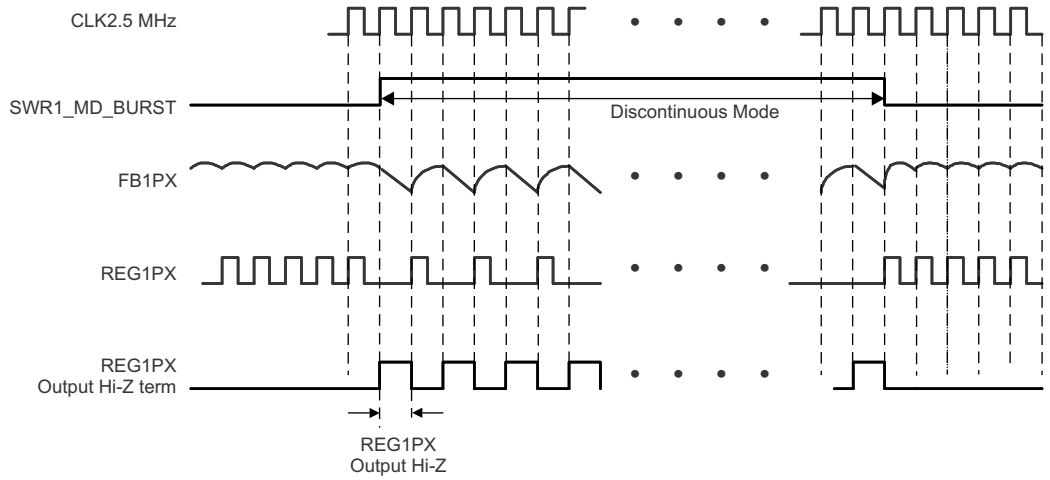


Figure 67. Discontinuous Regulation Mode

9.1.10 Monitor Signal on GPOUT

The device can output a specific signal to the GPOUT pin. To output a signal, choose a signal from REG6F by enabling first, then enable GPOUT_ENA. When two or more signals are set for GPOUT, the output is a logical sum

9.2 Typical Application

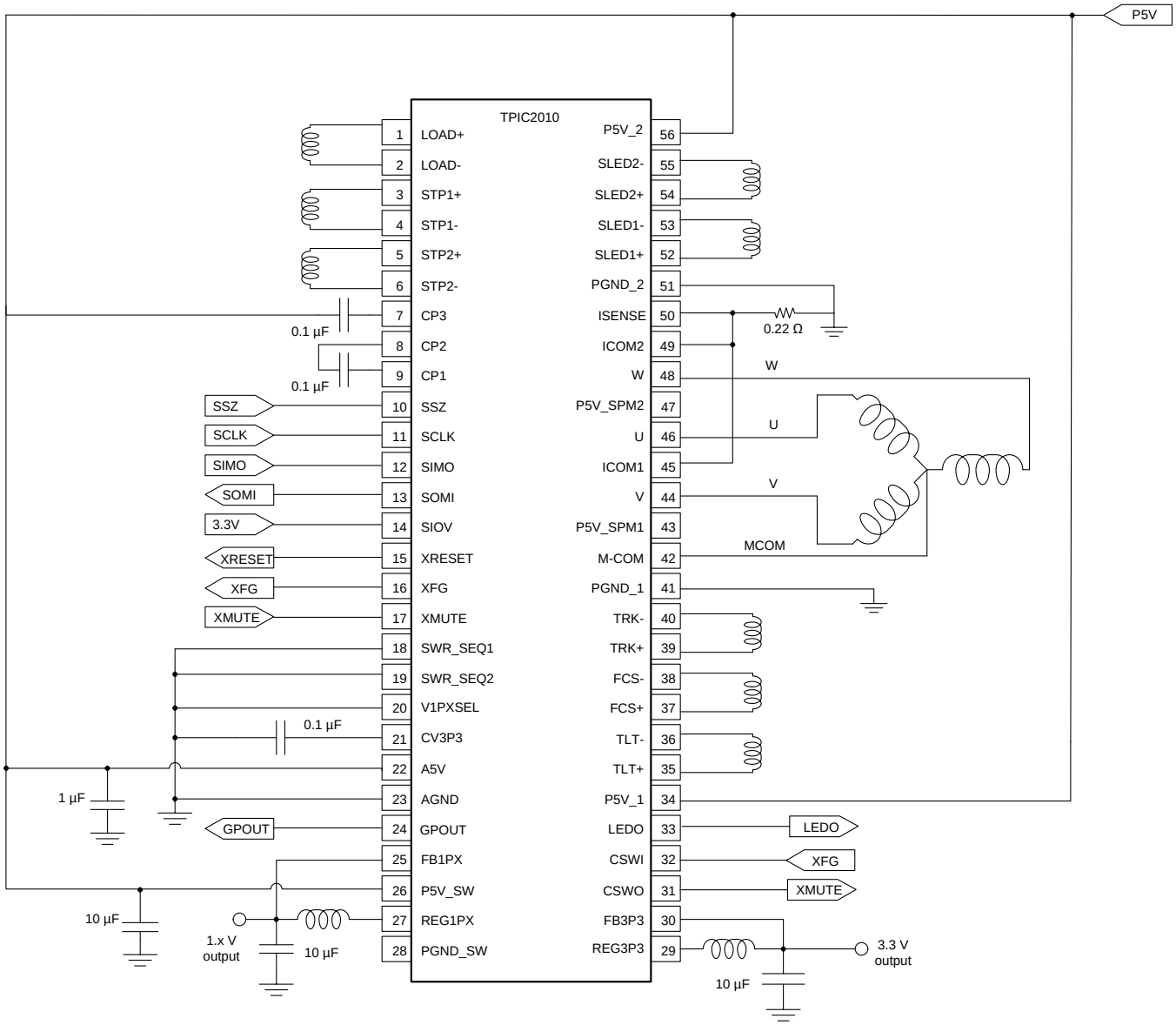


Figure 68. Typical Application Circuit

9.2.1 Design Requirements

To begin the design process, determine the following:

1. Motor configuration: The user can use all motor channels or some of them.
2. Power up devices with a 5-V supply.

9.2.2 Detailed Design Procedure

After power up on 5-V supply, the following values may be written to the following registers to enable motors.

1. Set WRITE_ENABLE = 1 on REG76 via SPI.
2. Set XSLEEP = 1 at REG70
3. Enable motor channel by ENA_XXX bits on REG70
4. Change the DAC settings for each motor in REG01-0B. Then, output channels will start driving load.

Typical Application (continued)

Table 41. Recommended External Components

PIN	TO	FUNCTION	VALUE (RATE)	UNIT
A5V	AGND	Noise decoupling	1.0 (10%16V)	μF
P5V1	PGND	Noise decoupling	10.0 (10%16V)	μF
P5V2	PGND	Noise decoupling	10.0 (10%16V)	μF
P5V_SW	PGND_SW	Noise decoupling	10.0 (10%16V)	μF
P5V_SPM	PGND	Noise decoupling	10.0 (10%16V)	μF
SIOV	AGND	Noise decoupling	1.0 (10%16V)	μF
REG1PX	FB1PX	Inductor (ESR = 0.1 Ω) for DC-DC converter	1.5 (20% 1.2A)	μH
FB1PX	PGND_SW	Capacitor (ESR = 0.025 Ω)	10.0 (10%10V)	μF
CV3P3	AGND	Noise decoupling for internal 3.3V	0.1 (10%10V)	μF
ISENSE	PGND	Spindle current sense resistor	0.22 (1% 1W)	Ω
LOAD+	PGND	Prevent surge current	10000(10% 16V)	pF
LOAD-	PGND	Prevent surge current	10000(10% 16V)	pF
REG3P3	FB3P3	Inductor (ESR = 0.1 Ω)	1.5 (20% 1.2A)	μH
FB3P3	PGND_SW	Capacitor (ESR = 0.025 Ω)	10.0 (10% 10V)	μF
CP1	CP2	Charge pump capacitor	0.1 (10% 25V)	μF
CP3	P5V	Charge pump capacitor (P5V only, prohibit other power supply)	0.1 (10% 25V)	μF

Table 42. Specific for DC-DC Converter Components

COMPONENTS	RECOMMENDED VALUE	RECOMMENDED SUPPLIER	PART NUMBER
Inductor	1.5 (μH)	TAIYO YUDEN	BRL2518T1R5M
Capacitor	10 (μF)	MURATA	GRM21BB31A106KE18L

Table 43. Restriction of Selection Parts

PIN	VALUE	GROUNDS
CSWO	Less than 4.7 μF	Since voltage will not rise within monitoring time if a big capacitance is connected on CSWO, the protected operation operates and repeat On / Off .

9.2.3 Application Curves

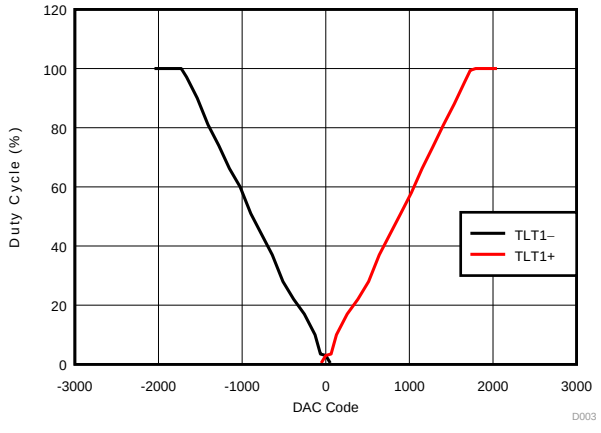


Figure 69. DAC Code vs Duty Cycle for TLT Outputs

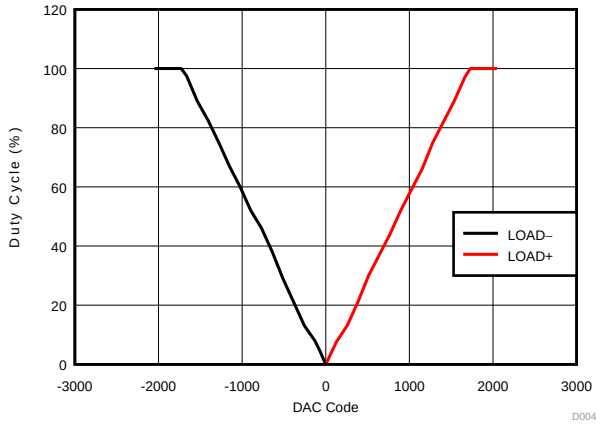


Figure 70. DAC Code vs Duty Cycle for LOAD Outputs

10 Power Supply Recommendations

All driver channels should be operated after the required power is supplied and stable.

The appropriate capacity of the decoupling capacitor requires a value over 10 µF to reduce the influence of PWM switching noise. The P5V1, P5V2,P5V_SW, and P5V_SPM pins must connect to 10-µF decoupling capacitors.

Current flow to the driver circuits takes both pattern-layout, line-impedance, and noise influence from the supply line into consideration.

11 Layout

11.1 Layout Guidelines

1. CV3P3V requires an external capacitor. Because this is a reference voltage for device, locate the capacitor as close to device as possible. Keep away from noise sources.
2. TI recommends SCLK ground shielding.
3. Place the inductors for the DC-DC converters as close to the chip as possible, and keep the feedback lines to the FB3P3 and FB1PX pins as short as possible.

11.2 Layout Example

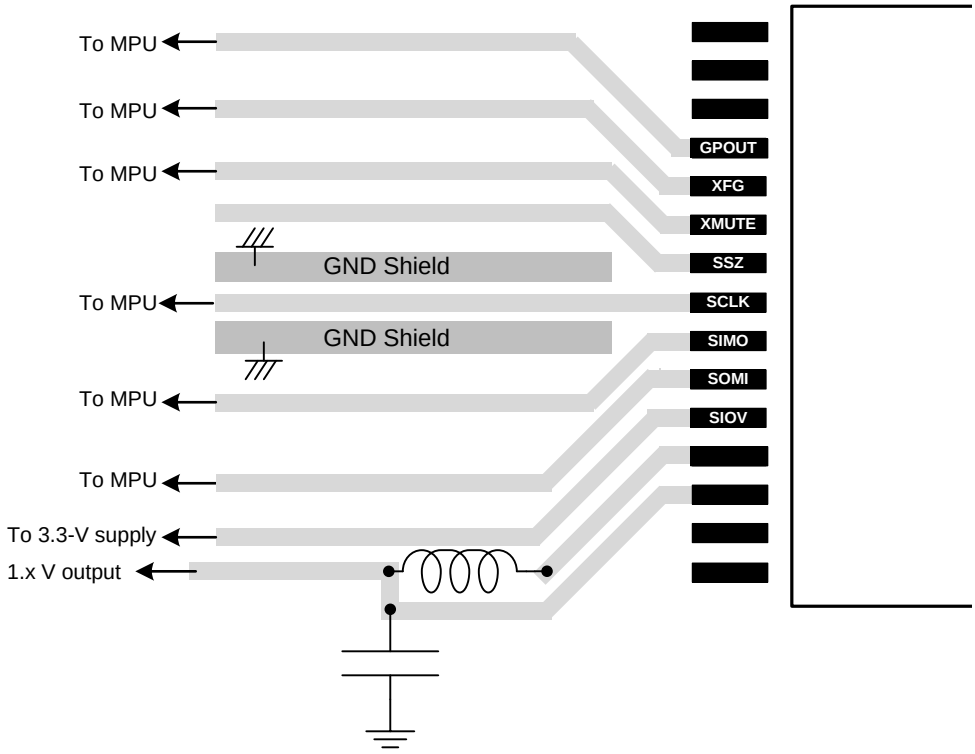


Figure 71. Layout Recommendation

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC2010RDFDRG4	ACTIVE	HTSSOP	DFD	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 75	2010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

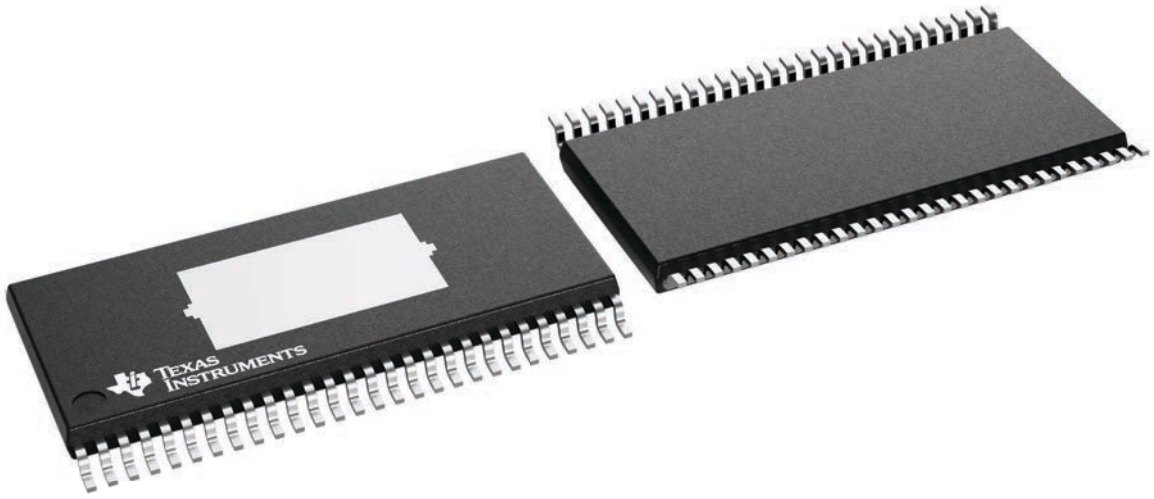
DFD 56

PowerPAD TSSOP - 1.2 mm max height

6.1 x 14, 0.5 mm pitch

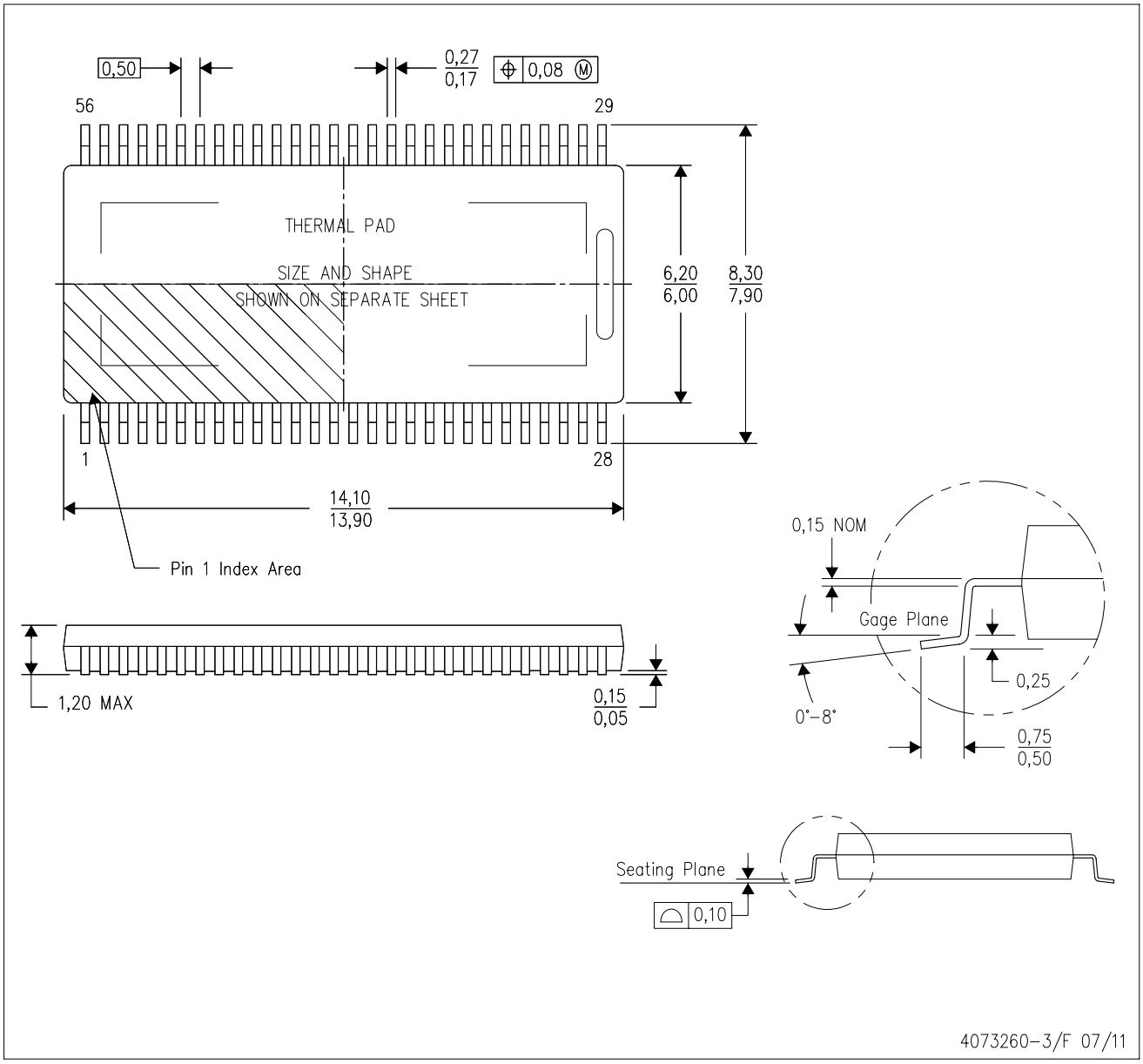
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230655/A

DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

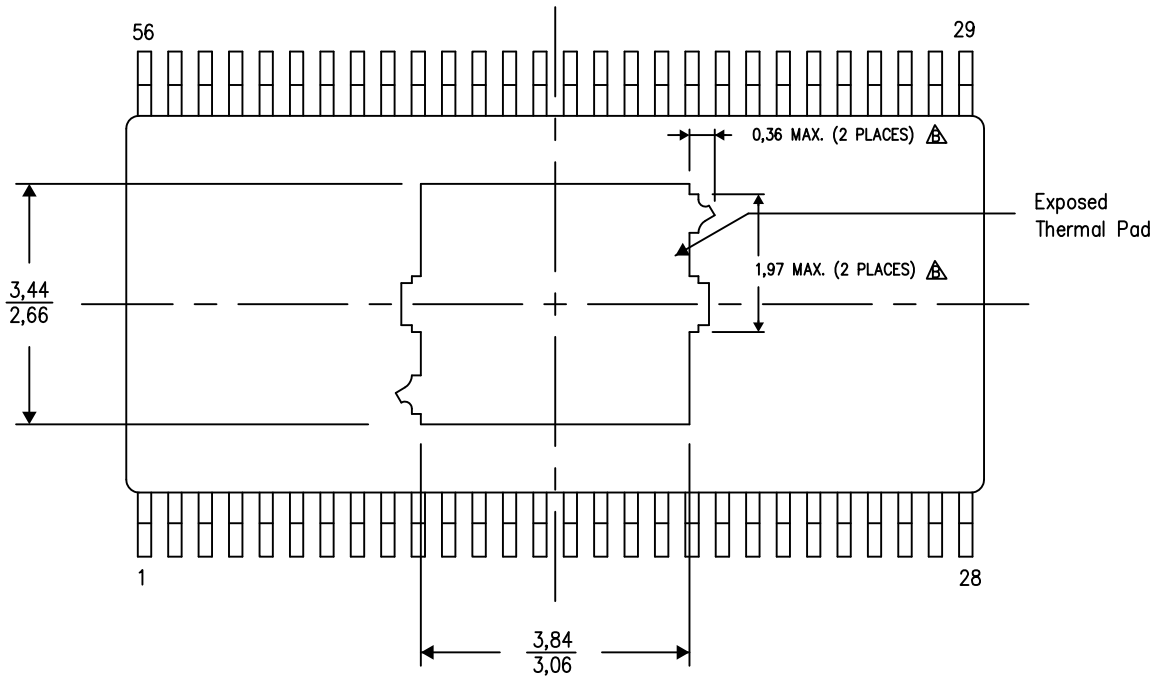
DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4210501–2/G 07/12

NOTES: A. All linear dimensions are in millimeters

B Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

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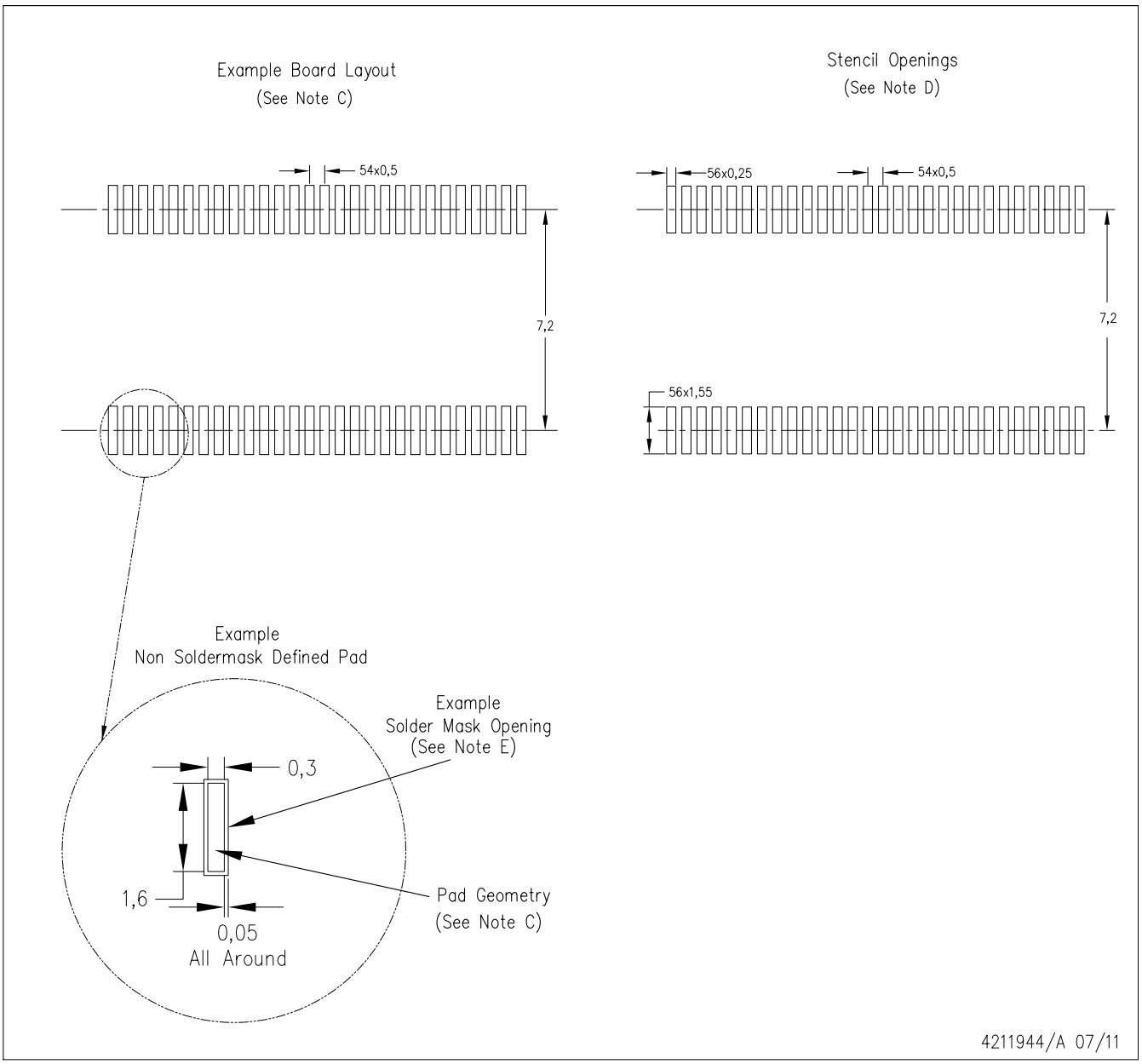
DFD (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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