TPD13S523 用于 HDMI 发送器端口的带有限流负载开关的 13 通道 ESD 保护解决方案

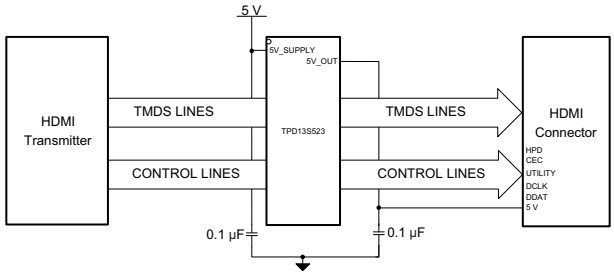
1 特性

- IEC 61000-4-2 4 级接触静态放电 (ESD) 保护
  - 外部线路上 ±12kV 接触放电
- 适用于 HDMI 1.4 和 HDMI 1.3 接口的单芯片 ESD 解决方案
- 具有电流限制和反向电流保护功能的片载 5V 负载开关
- 支持针对 HDMI 1.4 音频返回线路的实用 (UTILITY) 线路保护
- 最小化传输差分信号 (TMDS) 信号对之间 < 0.05pF 的差分电容
- 工业标准 16-TSSOP 和节省空间的 16-RSV 封装
- 支持超过 3.4Gbps 的数据速率
- R_{DYN} = 0.5Ω（典型值）
- 商业温度范围：–40°C 到 85°C

2 应用

- 终端设备
  - 机顶盒
  - 电子书
  - 平板电脑
  - 智能电话
  - 便携式摄像机
- 接口
  - HDMI

HDMI 发送器端口的原理图



3 说明

TPD13S523 器件是一款集成 IEC 61000-4-2 ESD 保护的单芯片解决方案（适用于 HDMI 1.4 或 HDMI 1.3 接口）。该器件提供 13 条 TVS 二极管通道，带有与 HDMI 连接器高速线路匹配的直通引脚映射。在提供 ESD 保护的同时，TPD13S523 不会增加高速差分信号的额外失真。单片集成电路技术确保不同线路间的双信号对出色匹配（TMDS 线路间的差分匹配 < 0.05pF）。这比离散 ESD 解决方案更具优势，因为两个不同 ESD 保护电路间的差异可能显著降低差分信号质量。

TPD13S523 采用了片上电流限制负载开关，符合 HDMI 5V 输出电气规范。5V_OUT 处的短路保护可确保器件不会损坏，防止接 GND 意外短路。负载开关也采用了反向电流阻断功能，可确保两个 HDMI 驱动器连接在一起时 HDMI 驱动器侧不会错误导通。

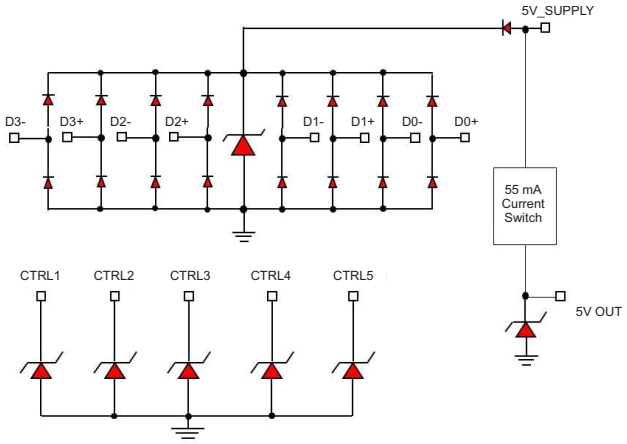
这些 器件 TPD13S523，包括机顶盒 (STB)、电子书、平板电脑、智能手机以及便携式摄像机。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD13S523	TSSOP (16)	5.00mm x 4.40mm
	UQFN (16)	2.60mm x 1.80mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

方框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (June 2015) to Revision D **Page**

- Added table note to *Absolute Maximum Ratings* ... 4
- Added test condition frequency to capacitance ... 5

Changes from Revision B (December 2012) to Revision C **Page**

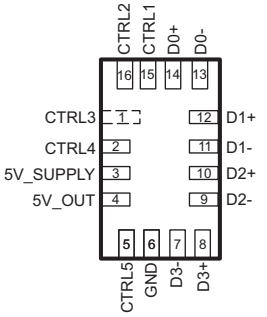
- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision A (May 2012) to Revision B **Page**

- 已添加 RSV 封装至订购信息表。 ... 1
- Removed PREVIEW status from RSV package. ... 3

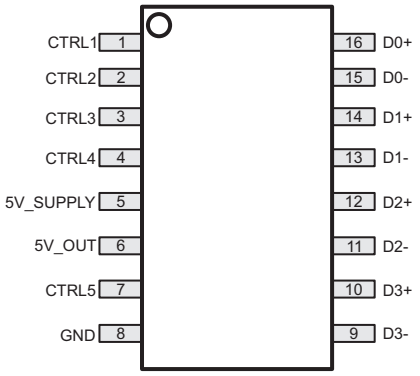
5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



All the CTRLx pins have the same ESD circuit and are interchangeable.

PW Package
16-Pin TSSOP
Top View



All the CTRLx pins have the same ESD circuit and are interchangeable.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	UQFN	TSSOP		
CTRL1	15	1	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL2	16	2	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL3	1	3	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL4	2	4	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
CTRL5	5	7	I/O	ESD Clamp for Control Lines: provides ESD protection to HDMI control lines: CEC, SCL, SDA, HPD, and UTILITY. All the control pins have the same ESD circuit and are interchangeable.(1)
5V_SUPPLY	3	5	I	**Supply Pin for HDMI 5V_OUT** 5 V, connects to internal VCC plane on the PCB board; connect a 0.1 to 1-µF capacitor shunt to ground.
5V_OUT	4	6	O	**Current Limited HDMI 5V_OUT:** connect to HDMI 5V_OUT; offers IEC61000-4-2 ESD protection; connect a 0.1 to 1-µF capacitor shunt to ground.
GND	6	8	G	Ground
D0+	14	16	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D0–	13	15	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D1+	12	14	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D1–	11	13	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D2+	10	12	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D2–	9	11	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D3+	8	10	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)
D3–	7	9	I/O	High-speed ESD Clamp: provides ESD protection for TMDS lines.(1)

(1) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

6 Specifications

6.1 Absolute Maximum Ratings

T_A = –40°C to 85°C (1)

		MIN	MAX	UNIT
V_{CC} voltage tolerance	5V_SUPPLY	–0.3	6	V
IO voltage tolerance	Connector pins(2)	–0.3	6	V
IEC 61000-4-5 peak current (8/20 µs)	Connector pins(2)		3	A
IEC 61000-4-5 peak power (8/20 µs)	Connector pins(2)		30	W
Storage temperature, T_{stg}		–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Connector pins are Dx+, Dx–, CTRLx, and 5V_OUT

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 Contact Discharge	±12000	
		IEC 61000-4-2 Air-gap Discharge	±14000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = –40°C to 85°C

		MIN	MAX	UNIT
VCC Voltage	5V_SUPPLY	4.5	5.5	V
IO voltage at external signal pins	Signal Pins(1)	–0.3	5.5	V
Operating free-air temperature		–40	85	°C

(1) External Signal pins are Dx+, Dx–, CTRLx, and 5V_OUT

6.4 Thermal Information

THERMAL METRIC(1)		TPD13S523		UNIT
		PW [TSSOP]	RSV [UQFN]	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9	153.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	70.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.0	74.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.7	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	n/a	74.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOAD SWITCH						
I_{CC}	Supply current at 5V_SUPPLY	5V_SUPPLY =5V, 5V OUT = Open	6.5	7	10	µA
I_{SC}	Short-circuit current at 5V_OUT	5V_SUPPLY =5V, 5V_OUT = GND	100	116	147	mA
$I_{BACKDRIVE}$	Reverse leakage current at 5VOUT	5V_SUPPLY =0V, 5V_OUT = 5 V		0.01	0.69	µA
V_{DROP}	5V_OUT output voltage drop	5V_SUPPLY =5V, I_{5V_OUT} = 55 mA		170	205	mV
CONNECTOR PINS						
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	Ipp = 1 A, 8/20 µs(1)			13	V
		Ipp = 3 A, 8/20 µs(1)			15	
I_{IO}	Leakage current through external signal pins(2)	5V_SUPPLY =5V, V_{IO} = 5 V	2	7	65	nA
I_{OFF}	Current from IO Port to supply pins when powered down through signal pins(3)	5V_SUPPLY = 0 V, V_{IO} = 2.5 V	1	5	44	nA
V_F	Diode forward voltage through external signal pins(2); lower clamp diode	I_D = 8 mA	0.7	0.85	0.95	V
R_{DYN}	Dynamic resistance of ESD clamps external pins(3)	Pin to ground(2)		0.5		Ω
C_{IO_TMDS}	IO capacitance Dx+, Dx– pins to GND	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		1		pF
ΔC_{IO_TMDS}	Differential capacitance for the Dx+, Dx– lines	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		0.05		pF
$C_{IO\_CONTROL}$	CTRLx pin capacitance	5V_SUPPLY = 5 V, V_{IO} = 2.5 V; f = 1 MHz		1		pF
V_{BR}	Break-down voltage through signal pins(3)	I_{IO} = 1 mA	6			V

(1) Non-repetitive current pulse of an 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I=1A AND I=10A.
(3) Signal pins are Dx+, Dx–, and CTRLx.

6.6 Typical Characteristics

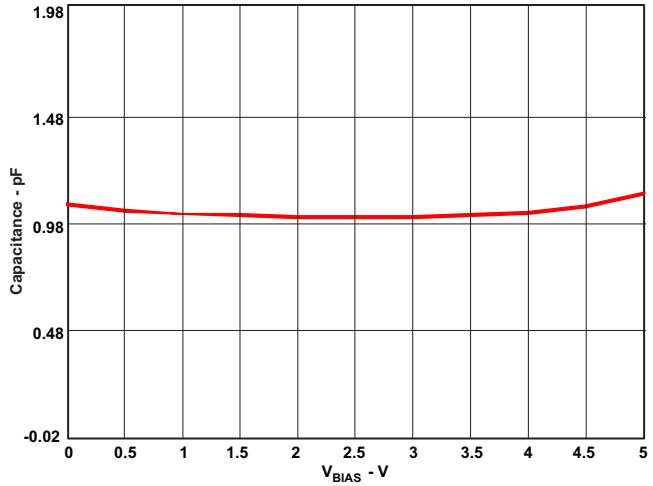


Figure 1. Pin Capacitance

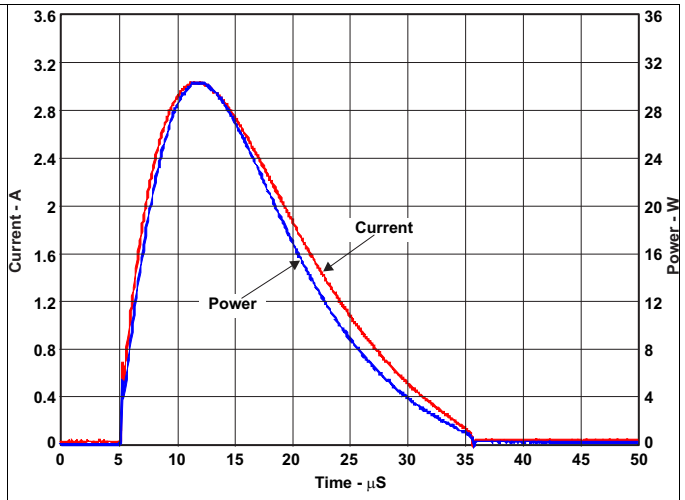


Figure 2. IEC 61000-4-5 (Surge) I_{PP} and P_{PP} Waveform

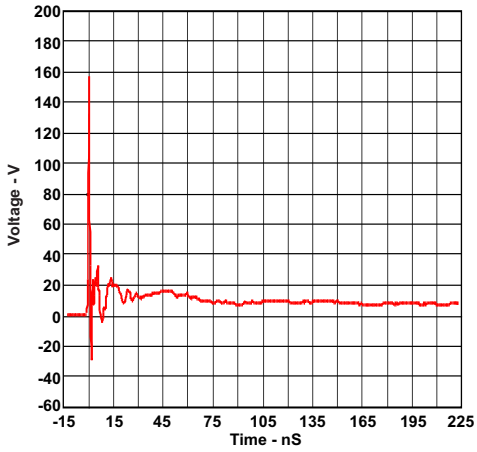


Figure 3. IEC Positive Clamping Waveform Using 8-kV Contact

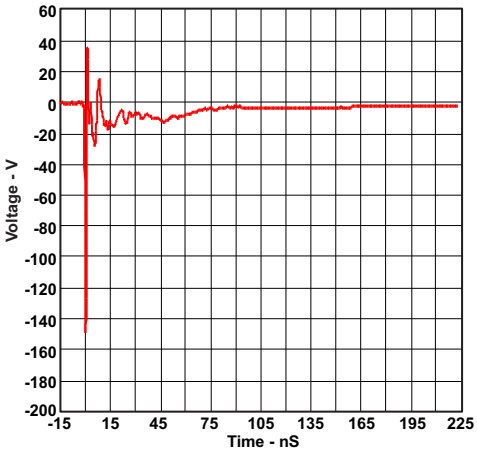


Figure 4. IEC Negative Clamping Waveform Using –8-kV Contact

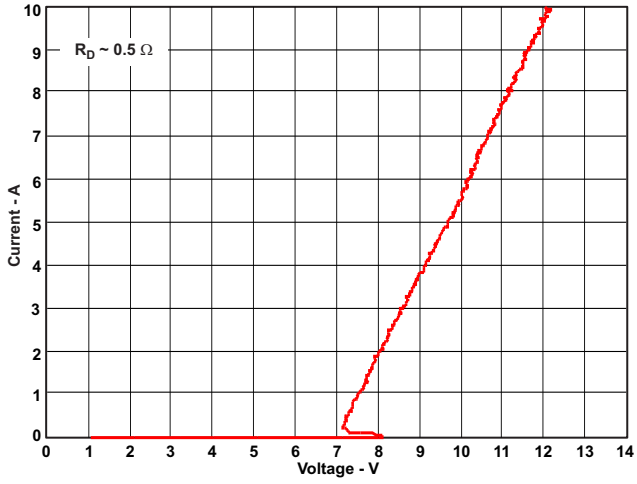


Figure 5. TLP Plot On Connector Pins

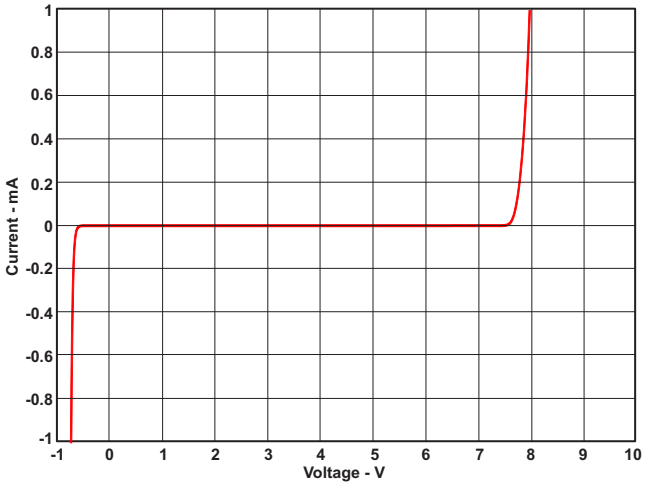
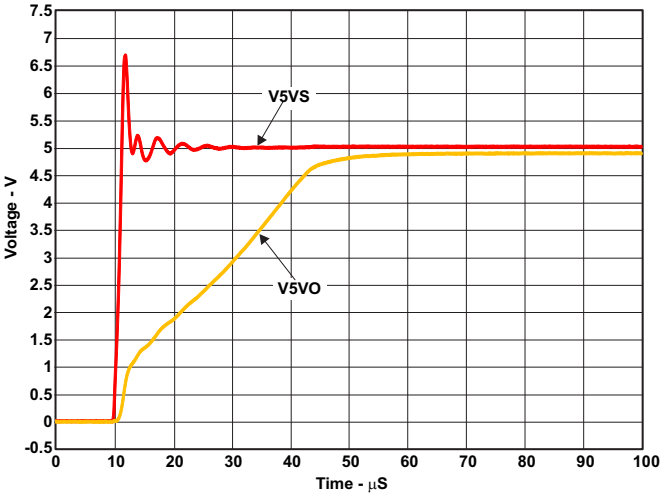


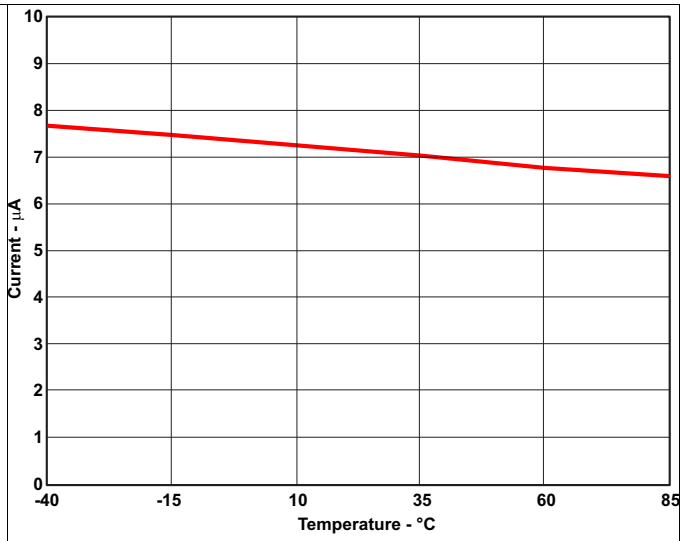
Figure 6. IV Curve On Signal Pins

Typical Characteristics (continued)



C_{IN} = 1 µF C_{OUT} = 1µF I_{SWITCH} = 55 mA
T_A = 25°C

Figure 7. Load Switch Start-Up Transient Waveform



5V_SUPPLY = 5 V 5V_OUT = Open

Figure 8. Load Switch Supply Current

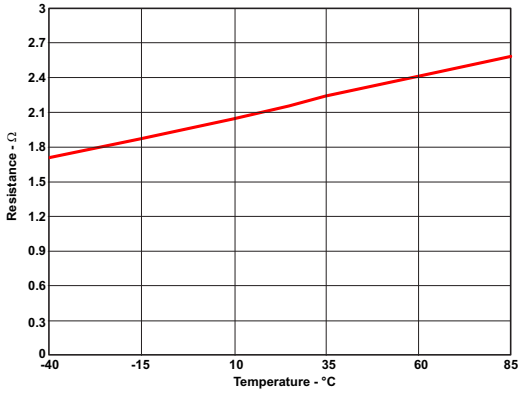


Figure 9. Load Switch Resistance vs Temperature

7 Detailed Description

7.1 Overview

The TPD13S523 device is a single-chip ESD solution for the HDMI transmitter port. By providing system-level ESD protection for a full HDMI port, the TPD13S523 can protect the core IC from ESD strikes and absorb the associated energy.

While providing the ESD protection, the TPD13S523 adds little-to-no signal distortion to the high-speed differential signals. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line.

The TPD13S523 also provides an on-chip regulator with current output ratings of 55 mA at pin 38. This current enables HDMI receiver detection even when the receiver device is powered off.

7.2 Functional Block Diagram

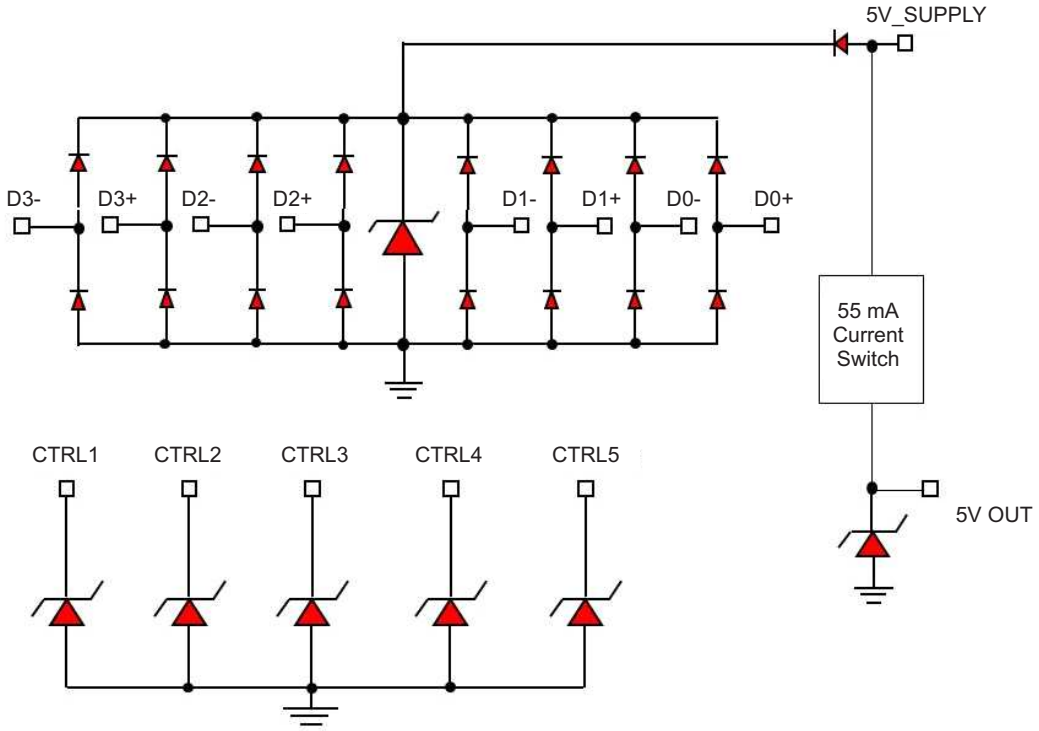


Figure 10. Electrical Equivalent Circuit Diagrams

7.3 Feature Description

7.3.1 IEC 61000-4-2 Protection

The connector-facing I/O pins can withstand ESD events up to ±12-kV contact and ±14-kV air. An ESD clamp diverts the current to ground.

7.3.2 Single-Chip ESD Solution

The TPD13S523 provides a complete ESD protection scheme for an HDMI 1.4 compliant port. No additional components are required for ESD protection and current-limiting besides this device.

Feature Description (continued)

7.3.3 On-Chip 5-V Load Switch

The TPD13S523 provides an on-chip regulator with a current output rating of 55-mA. This regulator also prevents reverse current flow from occurring, in compliance with the HDMI 5-V supply specification.

7.3.4 Supports UTILITY Line Protection

This device provides protection for all control lines in HDMI, including the UTILITY pin.

7.3.5 < 0.05-pF Differential Capacitance Between TMDS Pairs

The TPD13S523 has a very low capacitance variation (< 0.05 pF) between different TMDS ESD clamps. This provides excellent matching and does not degrade differential signal quality.

7.3.6 Industry Standard Package and Space-Saving Package

The TPD13S523 is offered in 2 different packages. A 16-pin industry standard TSSOP package is provided for ease of routing and easy layout. A 16-pin UQFN (RSV) is provided where small size is needed in the application.

7.3.7 Supports Data Rates in Excess of 3.4 Gbps

The TMDS ESD clamps have a very low capacitance that is capable of supporting HDMI data rates exceeding 3.4 Gbps.

7.3.8 R_{DYN} = 0.5 Ω

The TMDS ESD clamps have a very low R_{DYN} of 0.5Ω (typ) which provides excellent ESD protection clamping characteristics for the upstream core transmitter.

7.3.9 Commercial Temperature Range

The TPD13S523 is rated to operate from -40°C to 85°C.

7.4 Device Functional Modes

TPD13S523 is active with the conditions in the *Recommended Operating Conditions* met. Each connector side pin has an ESD clamp that triggers when voltages are greater than V_{BR} or less than the lower diode's V_f. During ESD events, voltages as high as ±12-kV contact ESD can be directed to ground through the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10's of nano-seconds), these pins revert to a nonconductive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD13S523 provides IEC 61000-4-2 Level 4 Contact ESD protection for an HDMI 1.4 transmitter port. An integrated current limit switch ensures compliance with the HDMI 5-V power supply requirements. This section presents a simplified discussion of the design process for this protection device.

8.2 Typical Application

A typical application schematic for an HDMI 1.4 transmitter port protected by the TPD13S523 is shown in Figure 11. The eight TMDS lines and five control lines are connected to their respective pins for ESD protection. The 5-V power path is connected through the 55-mA current limit switch.

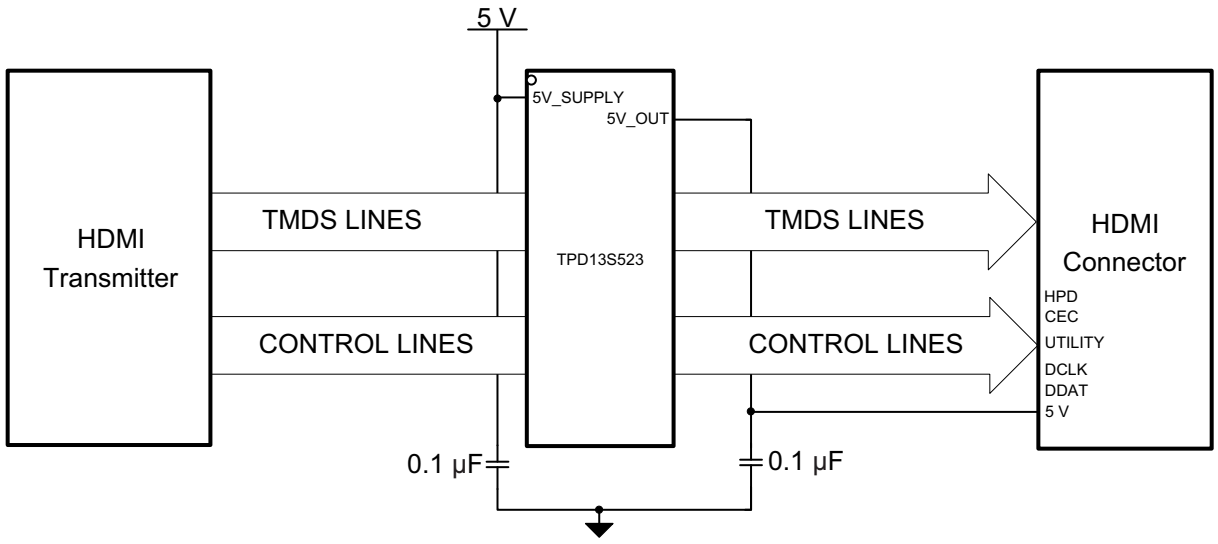


Figure 11. TPD13S523 Configured With an HDMI 1.4 Transmitter Port

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Voltage on 5V_SUPPLY	4.8 V - 5.3 V
HDMI Data Rate	3.4 Gbps

8.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following parameters:

- 5V_SUPPLY voltage range
- Maximum HDMI data rate

8.2.2.1 5V_SUPPLY Voltage Range

The TPD13S523 is capable of operating the 5V_SUPPLY up to 5.5 V, with recommended voltage from 4.5 V to 5.5 V. In this example, the supply range is 4.8 V to 5.3 V, which satisfies this requirement.

8.2.2.2 Maximum HDMI Data Rate

The TPD13S523 is capable of operating at HDMI data rates in excess of 3.4 Gbps, compliant to the HDMI 1.4 maximum data rate. In this example, the maximum HDMI 1.4 data rate of 3.4 Gbps has been chosen.

8.2.3 Application Curves

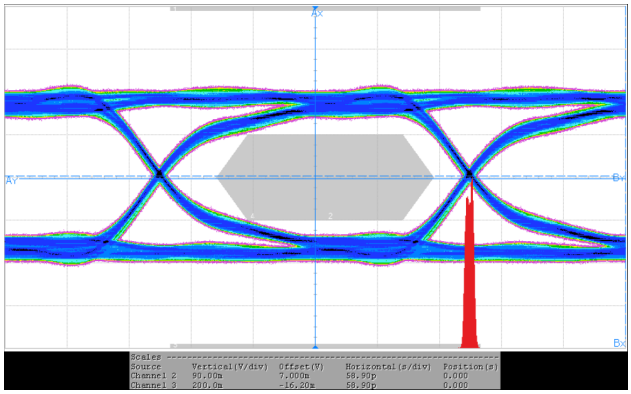


Figure 12. Eye Diagram Using EVM Without TPD13S523 for the TMDS Lines at 1080p, 340-MHz Pixel Clock, 3.4 Gbps

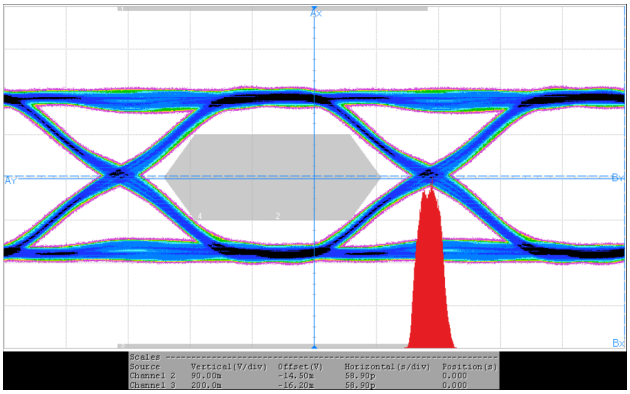


Figure 13. Eye Diagram Using EVM With TPD13S523 for the TMDS Lines at 1080p, 340-MHz Pixel Clock, 3.4 Gbps

9 Power Supply Recommendations

The designer must consider the requirement for the 5V_OUT voltage level. To ensure the voltage is within tolerance under load, set 5V_SUPPLY to at least 4.8 V + V_{DROP} (205 mV). Otherwise, TPD13S523 is a passive ESD protection device and there is no need to power it.

10 Layout

10.1 Layout Guidelines

The TPD13S523 device offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. In the event of an ESD stress, this device ensures that the core circuitry is protected and the system is functioning properly. For proper operation, the following layout and design guidelines should be followed:

1. Place the TPD13S523 as close to the connector as possible. This allows the TPD13S523 to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place two 0.1-μF capacitors very close to the 5V_SUPPLY and 5V_OUT pins. These capacitors will help limit the noise at the 5V_OUT power line, and also help with system level ESD protection.
3. Ensure that there is enough metallization for the GND pad. During normal operation, the TPD13S523 ESD pins consume ultra-low leakage current. During the ESD event, GND pin will see multiple amps of current. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. The critical routing paths for HDMI interface are the high-speed TMDS lines. With the PW package, all the TMDS lines (pin Dxx) can be routed in a single signal plane and still maintain the differential coupling and trace symmetry. This helps reduce the overall board manufacturing cost. The slow speed control lines can be routed in another signal layer through vias.
5. If the UTILITY or any other pin is not utilizied, tie the pin to a ground rather than leave floating. Use a 75-Ω resistor to protect against shorts to ground.

10.2 Layout Examples

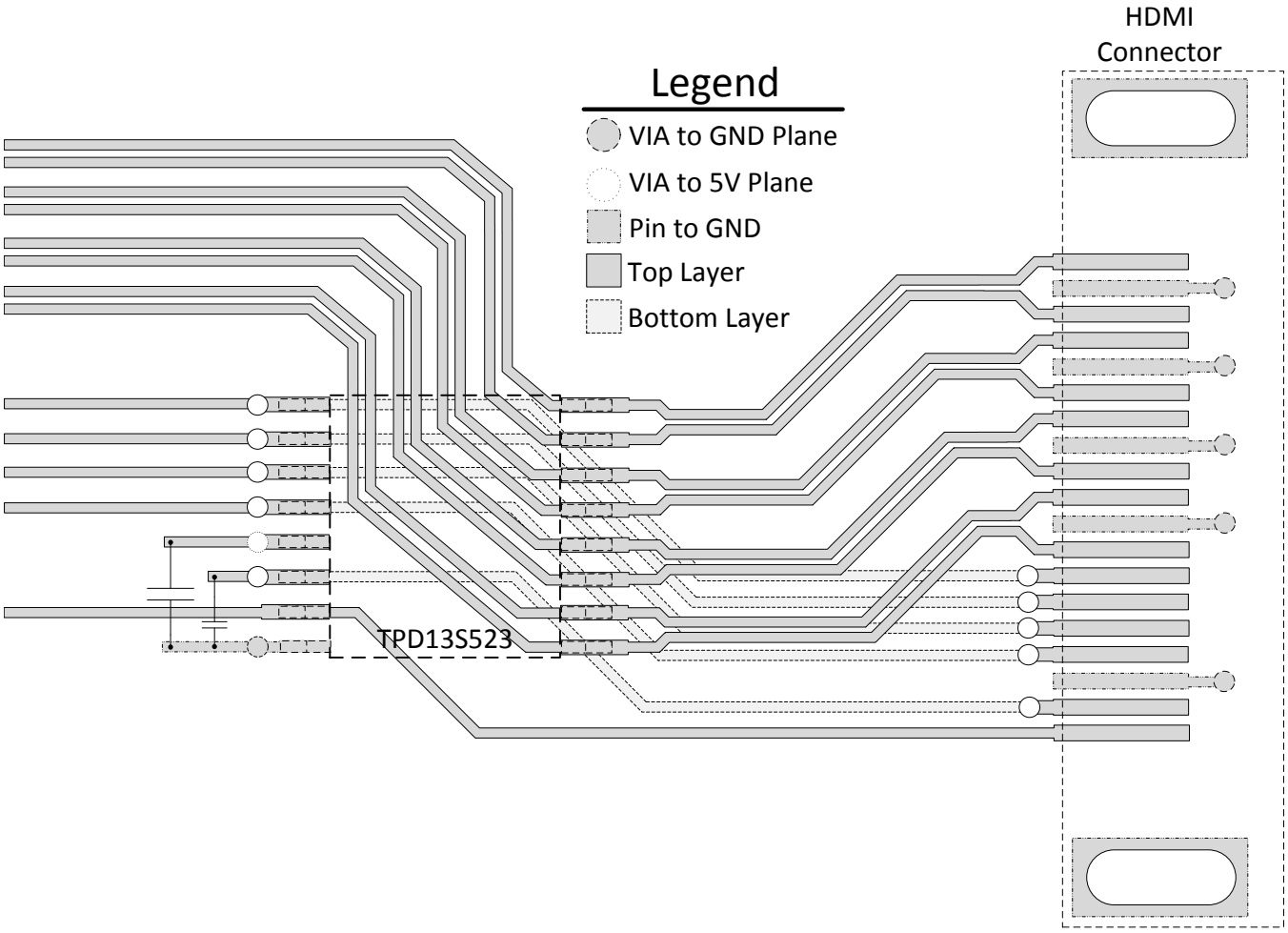


Figure 14. TPD13S523PWR Layout Example 13-Line HDMI Protection

Layout Examples (continued)

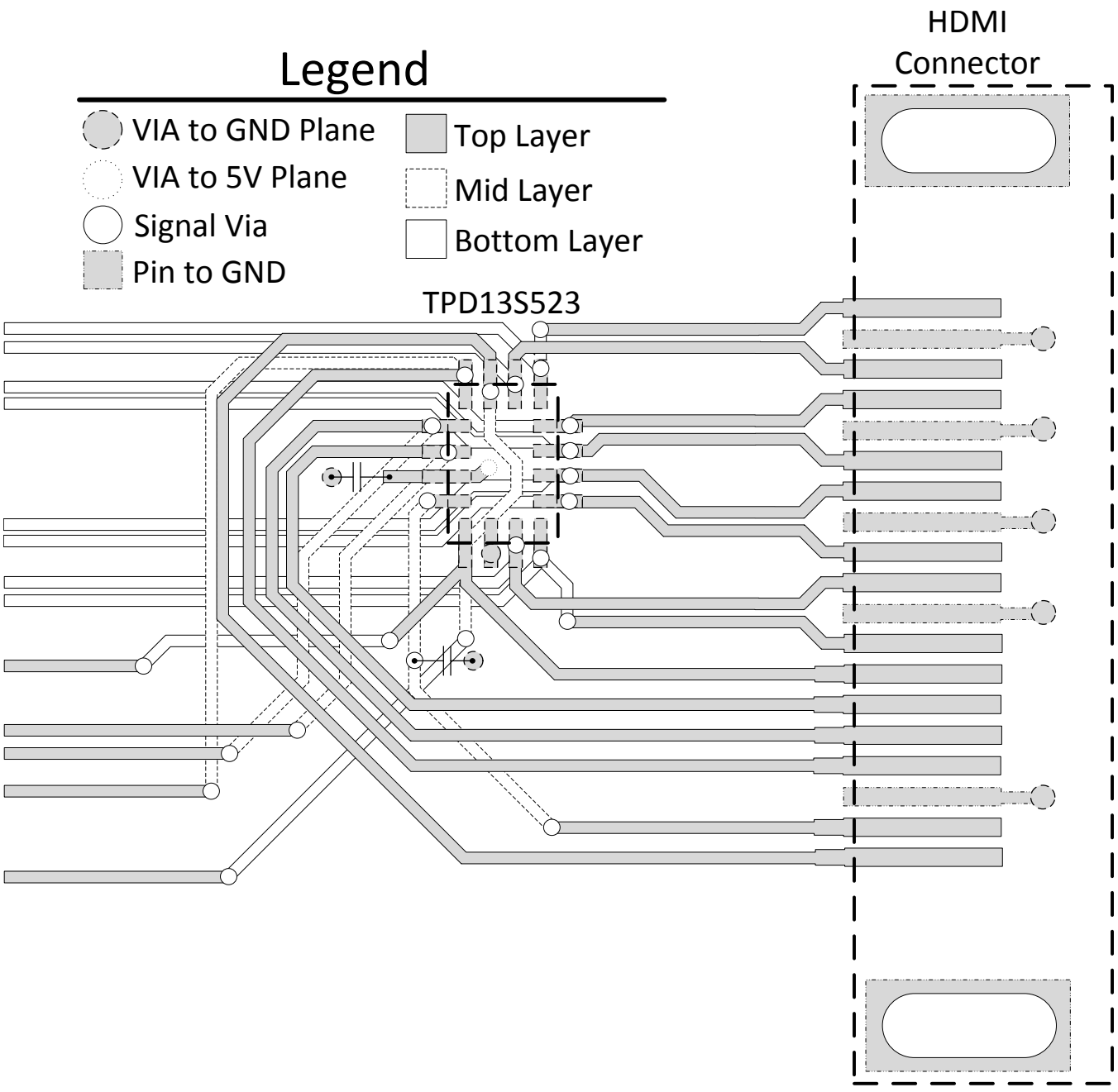


Figure 15. TPD13S523RSVR Layout Example 13-Line HDMI Protection

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD13S523PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RA523
TPD13S523RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

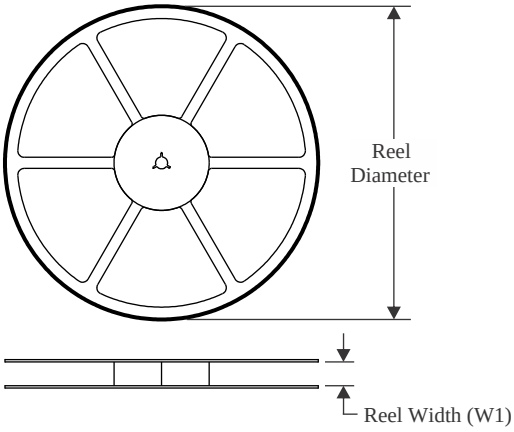
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

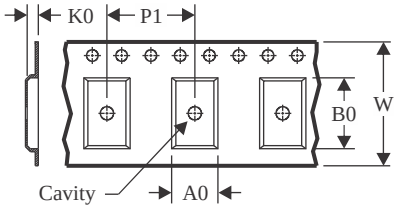
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

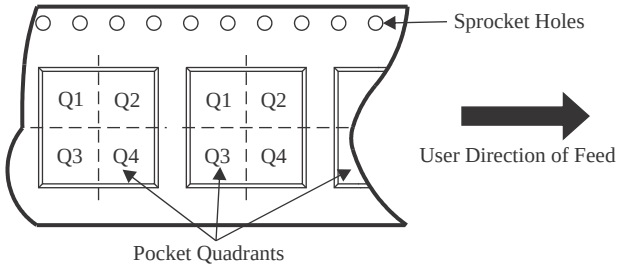


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

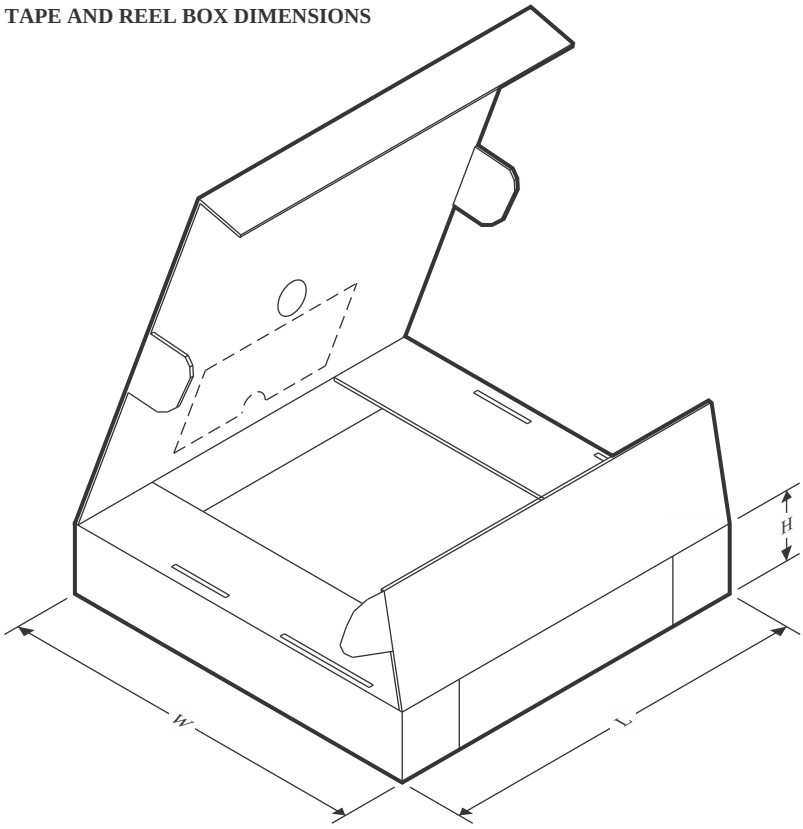
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD13S523PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPD13S523RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TPD13S523RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

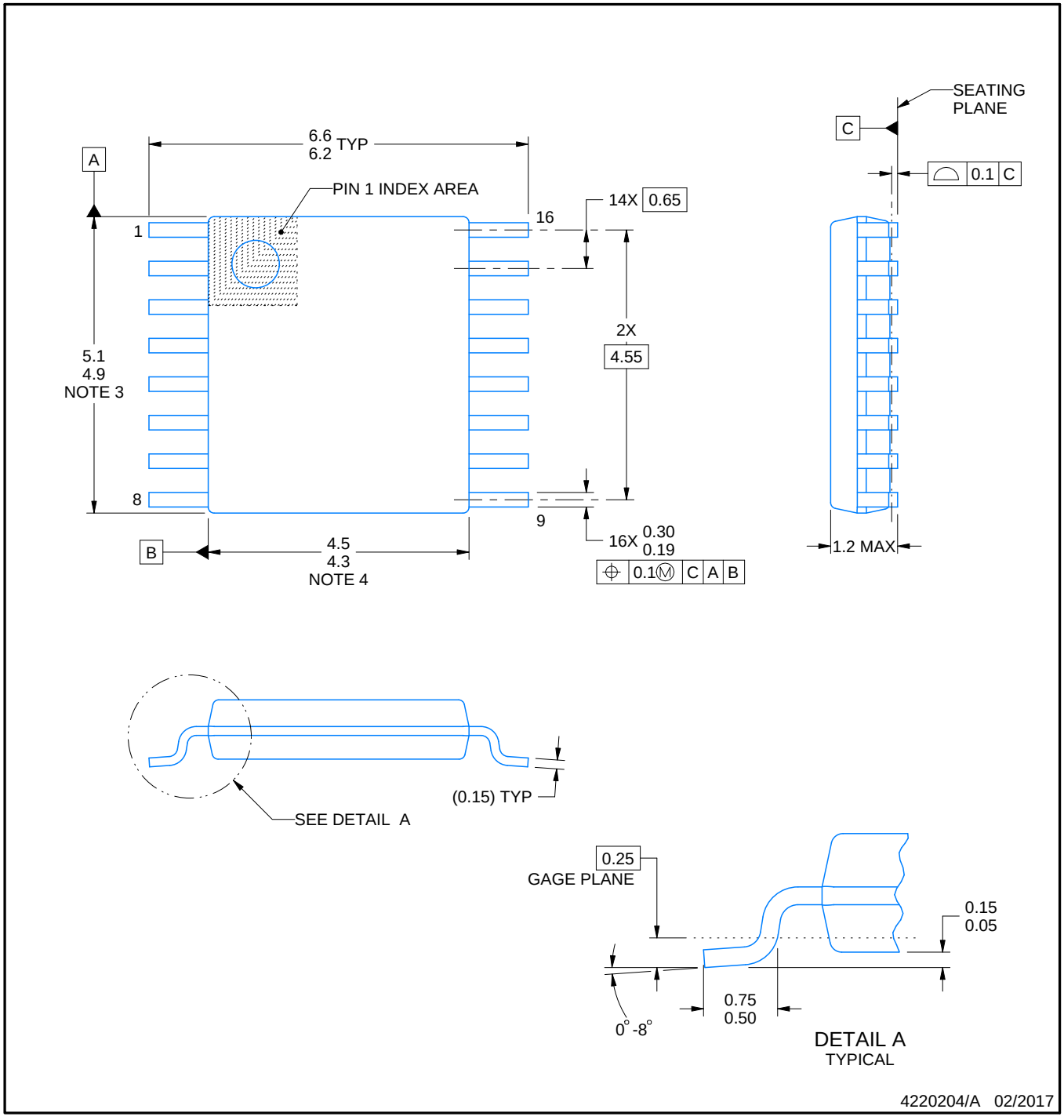
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD13S523PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TPD13S523RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TPD13S523RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0

PACKAGE OUTLINE

PW0016A

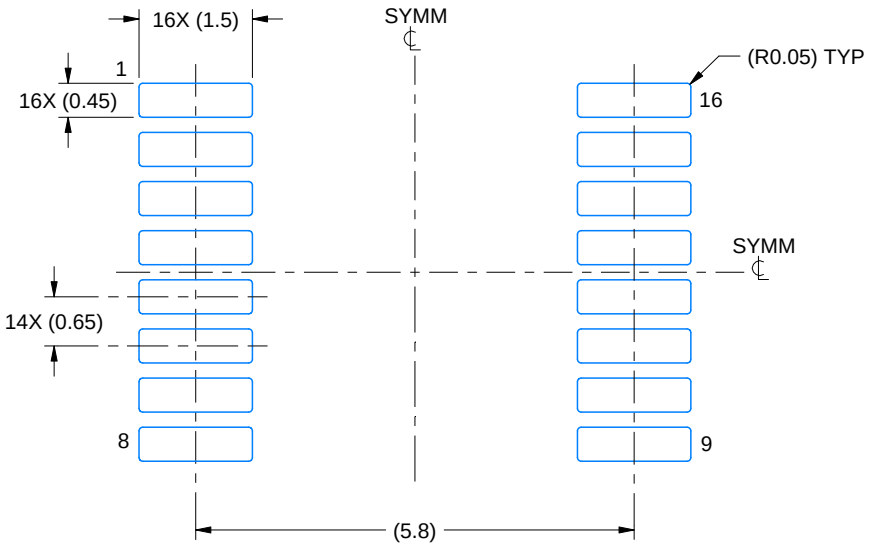
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

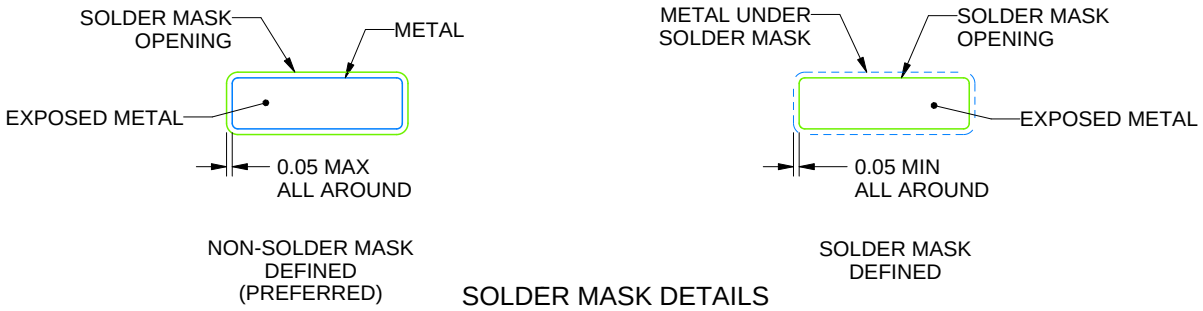


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

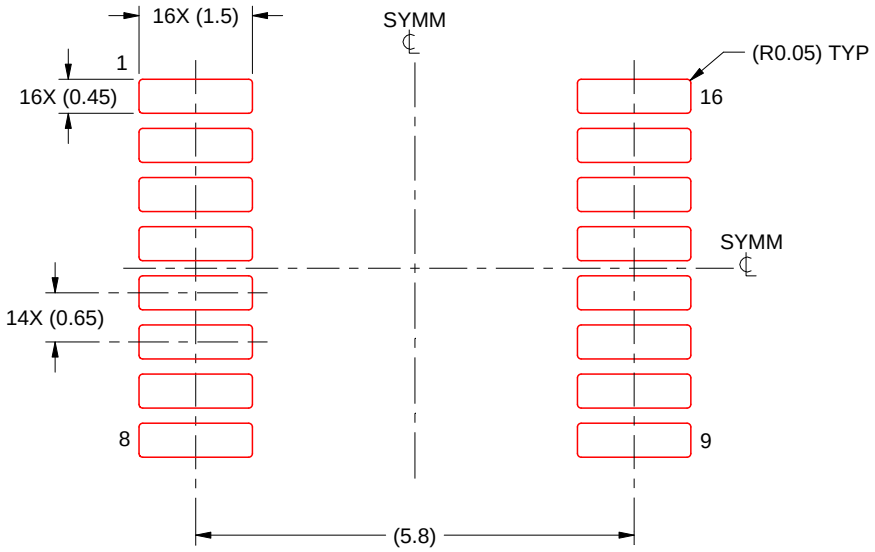


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

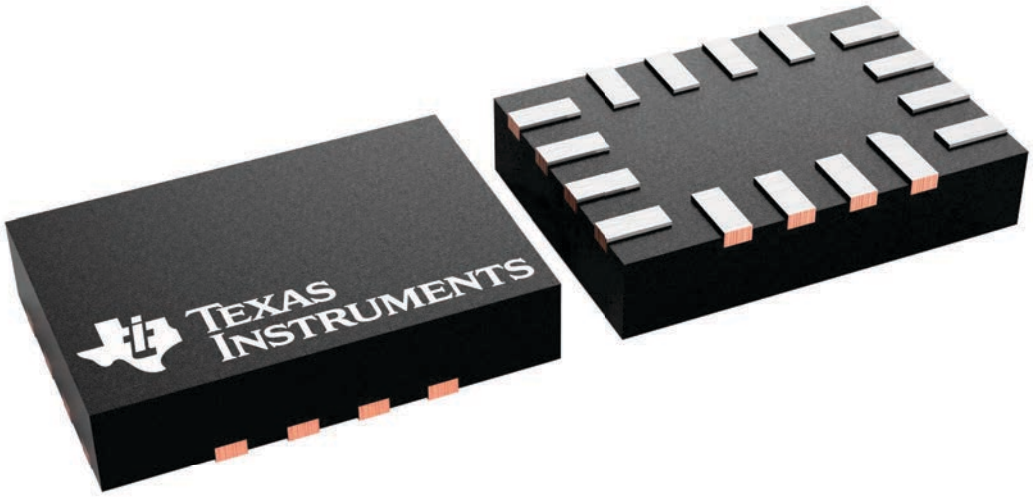
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



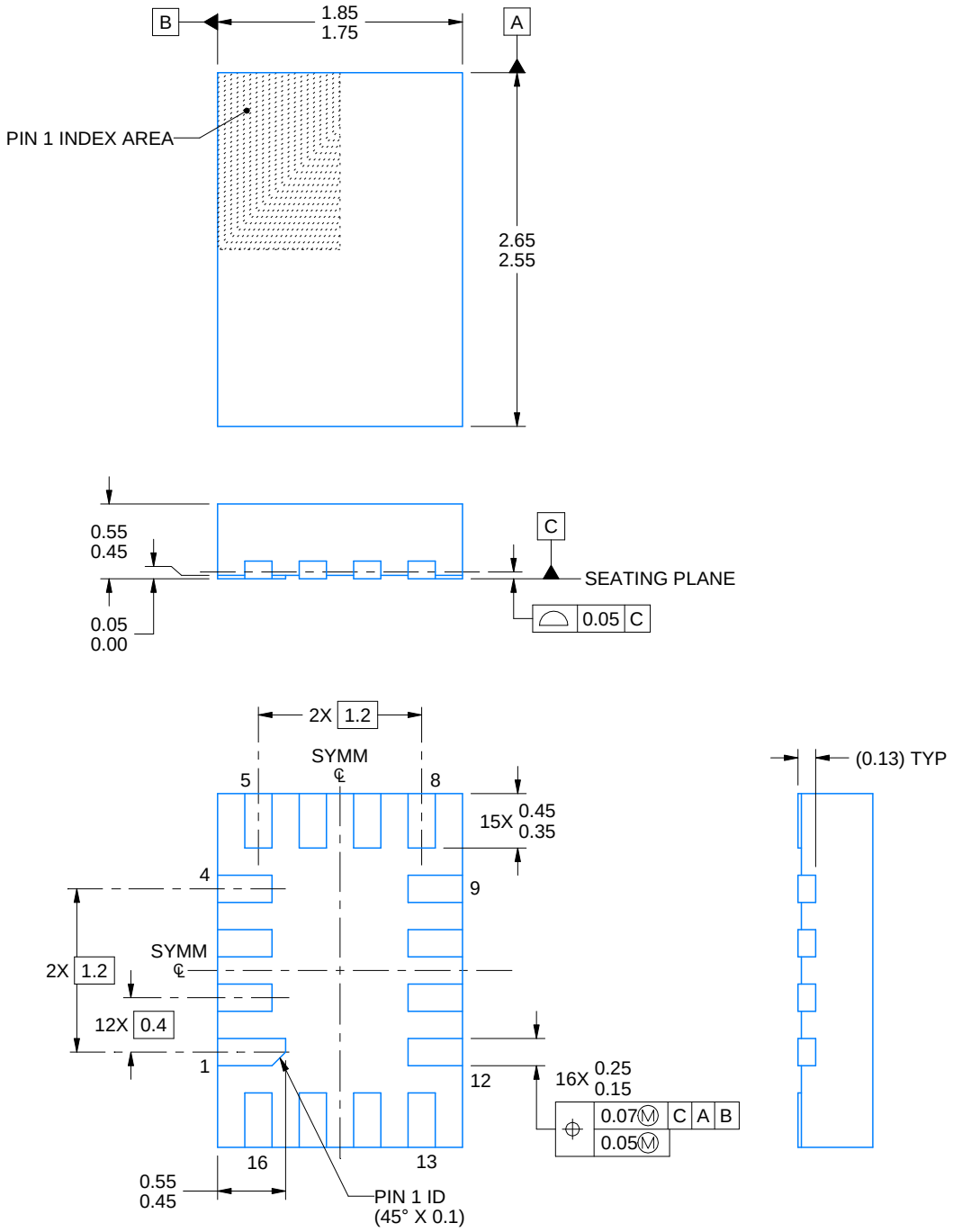
4231225/A

RSV0016A

PACKAGE OUTLINE

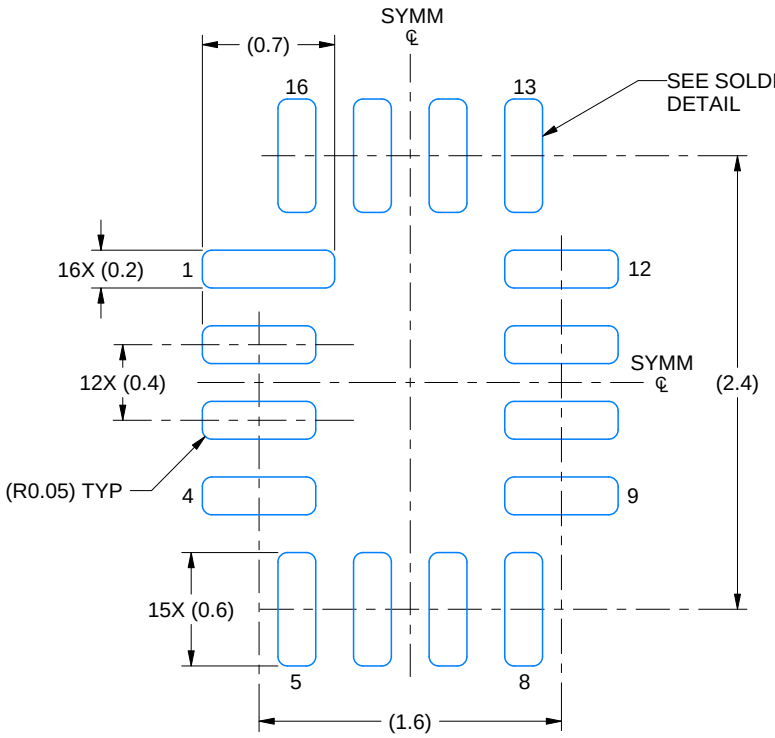
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

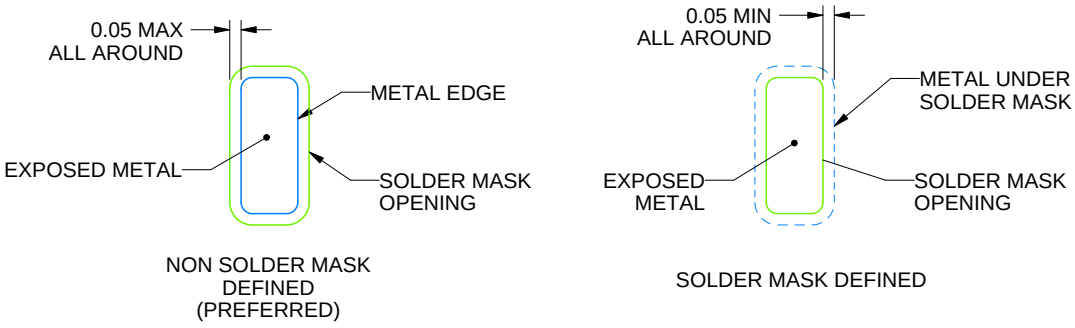


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

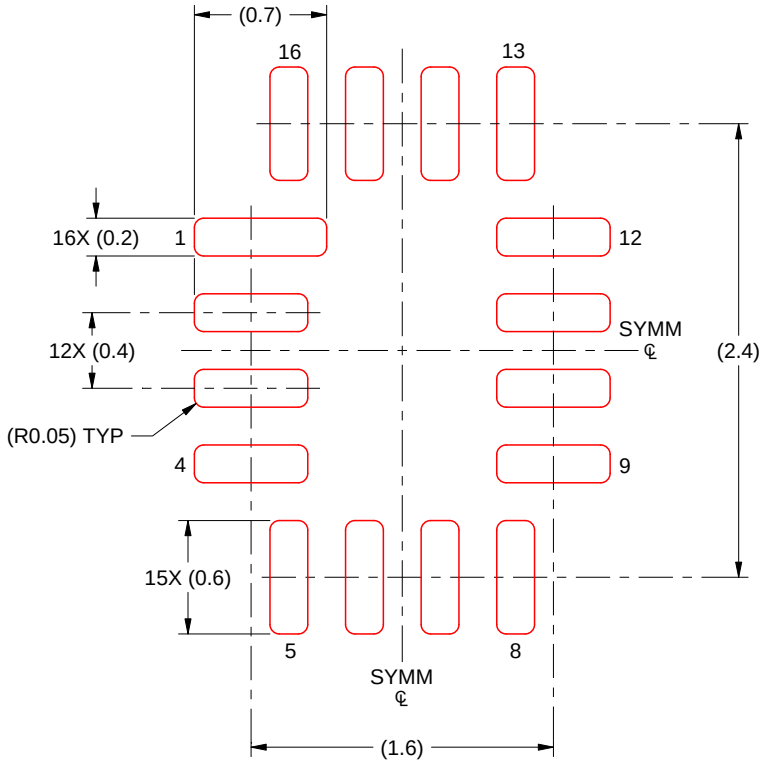


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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