TPA6204A1 1.7-W Mono Fully Differential Audio Power Amplifier

1 Features

- Designed for Wireless or Cellular Handsets and PDAs
- 1.7 W Into 8 Ω From a 5-V Supply at THD = 10% (Typical)
- Low Supply Current: 4 mA Typical at 5 V
- Shutdown Current: 0.01 µA Typical
- Fast Start-Up With Minimal Pop
- Only Three External Components
  - Improved PSRR (−80 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation
  - Fully Differential Design Reduces RF Rectification
  - −63-dB CMRR Eliminates Two Input Coupling Capacitors
- Pin-to-Pin Compatible With TPA2005D1 and TPA6211A1 in SON Package
- Available in 3 mm × 3 mm SON Package (DRB)

2 Applications

- Ideal for Wireless Handsets
- PDAs
- Notebook Computers

3 Description

The TPA6204A1 device (sometimes referred to as TPA6204) is a 1.7-W mono fully-differential amplifier designed to drive a speaker with at least 8-Ω impedance while consuming only 20 mm^2 total printed-circuit board (PCB) area in most applications. The device operates from 2.5 V to 5.5 V, drawing only 4 mA of quiescent supply current. The TPA6204A1 (TPA6204) is available in the space-saving 3 mm × 3 mm SON (DRB) package.

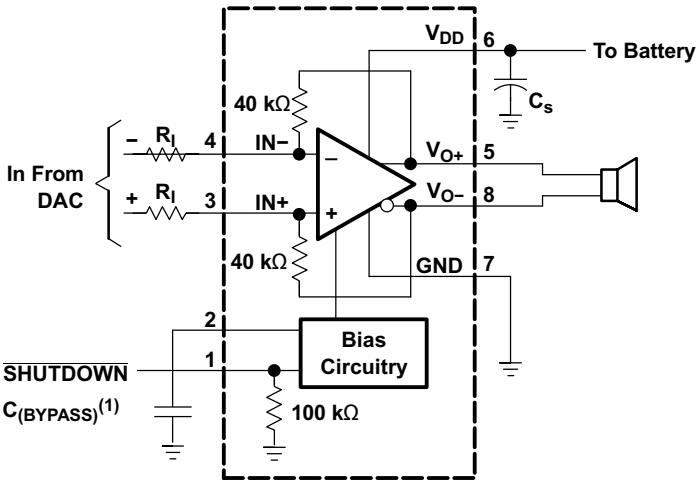
The TPA6204A1 (TPA6204) is ideal for PDA or smartphone applications due to features such as −80-dB supply voltage rejection from 20 Hz to 2 kHz, improved RF rectification immunity, small PCB area, and a fast start-up with minimal pop.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6204A1	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit



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(1) $C_{(BYPASS)}$ is optional.

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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 3
7.1 Absolute Maximum Ratings ... 3
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics: T_A = 25°C ... 4
7.6 Operating Characteristics: T_A = 25°C, Gain = 1 V/V 5
7.7 Dissipation Ratings ... 5
7.8 Typical Characteristics ... 6
8 Parameter Measurement Information ... 8
9 Detailed Description ... 9
9.1 Overview ... 9
9.2 Functional Block Diagram ... 9
9.3 Feature Description ... 9
9.4 Device Functional Modes ... 12
10 Application and Implementation ... 13
10.1 Application Information ... 13
10.2 Typical Application ... 13
10.3 System Examples ... 15
11 Power Supply Recommendations ... 16
11.1 Power Supply Decoupling Capacitor ... 17
12 Layout ... 17
12.1 Layout Guidelines ... 17
12.2 Layout Example ... 17
13 Device and Documentation Support ... 18
13.1 Community Resources ... 18
13.2 Trademarks ... 18
13.3 Electrostatic Discharge Caution ... 18
13.4 Glossary ... 18
14 Mechanical, Packaging, and Orderable Information ... 18

4 Revision History

Changes from Revision B (September 2009) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

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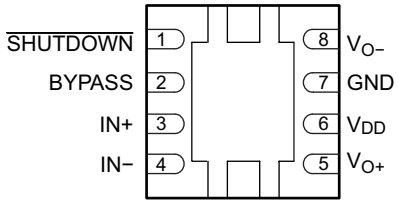
5 Device Comparison Table

DEVICE NUMBER	TPA6203A1	TPA6204A1	TPA6205A1 (1.8-V COMP SD)	TPA6211A1
Speaker Channels	Mono	Mono	Mono	Mono
Output Power (W)	1.25	1.7	1.25	3.1
PSRR (dB)	90	85	90	85
Pin/Package	8BGA, 8MSOP, 8SON	8SON	8BGA, 8MSOP, 8SON	8MSOP, 8SON

6 Pin Configuration and Functions

DRB Package
8-Pin SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BYPASS	2	—	Mid-supply voltage, adding a bypass capacitor improves PSRR
IN–	4	I	Negative differential input
IN+	3	I	Positive differential input
GND	7	I	High-current ground
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown terminal (active low logic)
Thermal Pad	—	—	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.
V_{DD}	6	I	Power supply
V_{O+}	5	O	Positive BTL output
$V_{O–}$	8	O	Negative BTL output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.3	6	V
Input voltage, V_I	–0.3	V_{DD} + 0.3	V
Continuous total power dissipation	See *Dissipation Ratings*		
Operating free-air temperature, T_A	–40	85	°C
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.5	5.5	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$	1.55		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$		0.5	V
Operating free-air temperature, T_A		–40	85	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPA6204A1 DRB (SON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Output offset voltage (measured differentially)	V_I = 0 V differential, Gain = 1 V/V, V_{DD} = 5.5 V		–9	0.3	9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			–85	–60	dB
V_{IC}	Common mode input range	V_{DD} = 2.5 V to 5.5 V		0.5		V_{DD} – 0.8	V
CMRR	Common mode rejection ratio	V_{DD} = 5.5 V, V_{IC} = 0.5 V to 4.7 V			–63	–40	dB
		V_{DD} = 2.5 V, V_{IC} = 0.5 V to 1.7 V			–63	–40	
	Low-output swing	R_L = 8 Ω, V_{IN+} = V_{DD}, Gain = 1 V/V, V_{IN-} = 0 V or V_{IN+} = 0 V, V_{IN-} = V_{DD}	V_{DD} = 5.5 V		0.45		V
			V_{DD} = 3.6 V		0.37		
			V_{DD} = 2.5 V		0.26	0.4	
	High-output swing	R_L = 8 Ω, V_{IN+} = V_{DD}, Gain = 1 V/V, = 0 V or V_{IN-} = V_{DD} VIN− V_{IN+} = 0 V	V_{DD} = 5.5 V		4.95		V
			V_{DD} = 3.6 V		3.18		
			V_{DD} = 2.5 V	2	2.13		
$\lvert I_{IH} \rvert$	High-level input current, SHUTDOWN	V_{DD} = 5.5 V, VI = 5.8 V			58	100	µA
$\lvert I_{IL} \rvert$	Low-level input current, SHUTDOWN	V_{DD} = 5.5 V, VI = −0.3 V			3	100	µA
I_Q	Quiescent current	V_{DD} = 2.5 V to 5.5 V, no load			4	6	mA
$I_{(SD)}$	Supply current	V($\overline{\text{SHUTDOWN}}$) ≤ 0.5 V, V_{DD} = 2.5 V to 5.5 V, R_L = 8 Ω			0.01	1	µA
	Gain	R_L = 8 Ω		38 kΩ / R_I	40 kΩ / R_I	42 kΩ / R_I	V/V
	Resistance from shutdown to GND				100		kΩ

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7.6 Operating Characteristics: T_A = 25°C, Gain = 1 V/V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5.5 V		1.36		W
			V_{DD} = 3.6 V		0.72		
			V_{DD} = 2.5 V		0.33		
		THD + N = 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5.5 V		1.7		W
			V_{DD} = 3.6 V		0.85		
			V_{DD} = 2.5 V		0.4		
THD+N	Total harmonic distortion + noise	V_{DD} = 5 V, PO = 1 W, R_L = 8 Ω, f = 1 kHz			0.02%		
		V_{DD} = 3.6 V, PO = 0.5 W, R_L = 8 Ω, f = 1 kHz			0.02%		
		V_{DD} = 2.5 V, PO = 200 mW, R_L = 8 Ω, f = 1 kHz			0.03%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs AC-grounded with C_i = 2 µF, $V_{(RIPPLE)}$ = 200 mV_{PP}	f = 217 Hz		–80		dB
			f = 20 Hz to 20 kHz		–70		
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω			105		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs AC-grounded with C_i = 2 µF	No weighting		15		μV_{RMS}
			A weighting		12		
CMRR	Common-mode rejection ratio	V_{DD} = 3.6 V V_{IC} = 1 V_{PP}	f = 217 Hz		–65		dB
R_F	Feedback resistance			38	40	44	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V, C_{BYPASS} = 0.1 µF			27		ms

7.7 Dissipation Ratings

PACKAGE	$T_A \leq$ 25°C POWER RATINGS	DERATING FACTOR	T_A = 70°C POWER RATINGS	T_A = 85°C POWER RATINGS
DRB	2.7 W	21.8 mW/°C	1.7 W	1.4 W

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7.8 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
P_O	Output power	vs Supply voltage	Figure 1
		vs Load resistance	Figure 2
P_D	Power dissipation	vs Output power	Figure 3
THD+N	Total harmonic distortion + noise	vs Output power	Figure 4
		vs Frequency	Figure 5
		vs Common-mode input voltage	Figure 6
K_{SVR}	Supply voltage rejection ratio	vs Frequency	Figure 7
	GSM Power supply rejection	vs Time	Figure 8
	GSM Power supply rejection	vs Frequency	Figure 9
	Closed-loop gain/phase	vs Frequency	Figure 10
	Open-loop gain/phase	vs Frequency	Figure 11
I_{DD}	Supply current	vs Supply voltage	Figure 12
		vs Shutdown voltage	Figure 13
	Start-up time	vs Bypass capacitor	Figure 14

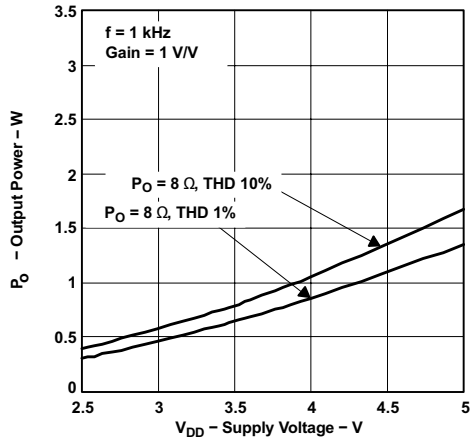

Figure 1. Output Power vs Supply Voltage

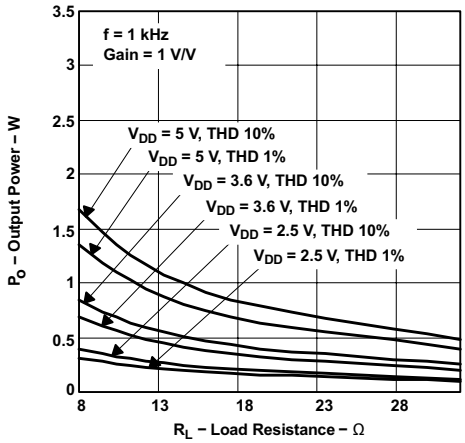

Figure 2. Output Power vs Load Resistance

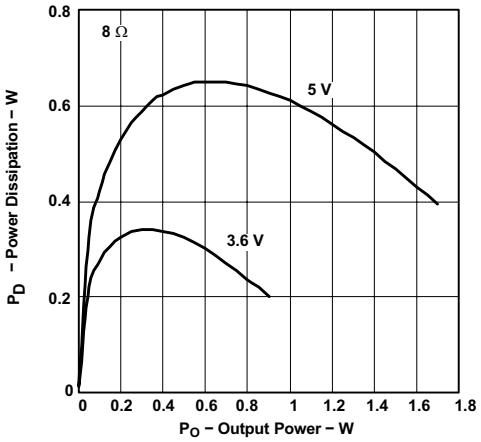

Figure 3. Power Dissipation vs Output Power

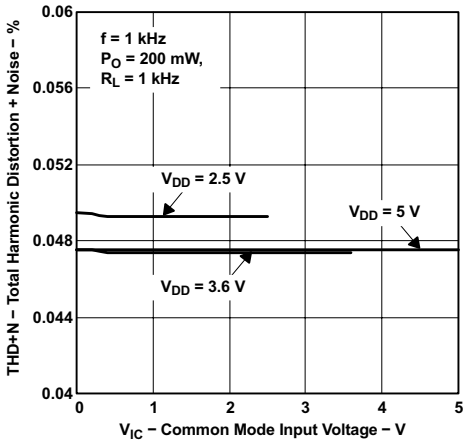

Figure 4. Total Harmonic Distortion + Noise vs Common-Mode Input Voltage

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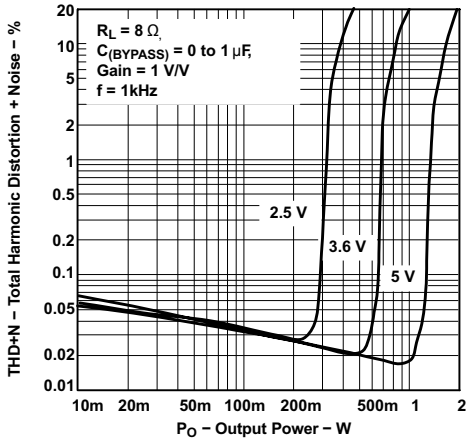

Figure 5. Total Harmonic Distortion + Noise vs Output Power

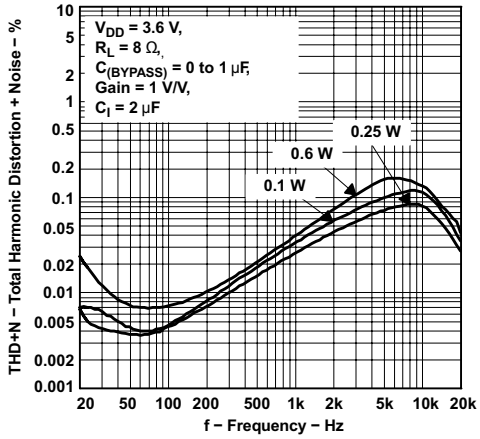

Figure 6. Total Harmonic Distortion + Noise vs Frequency

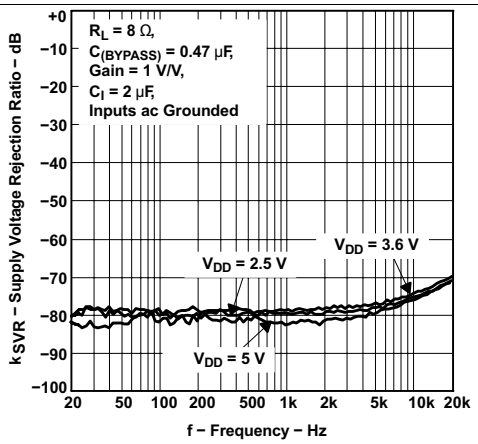

Figure 7. Supply Voltage Rejection Ratio vs Frequency

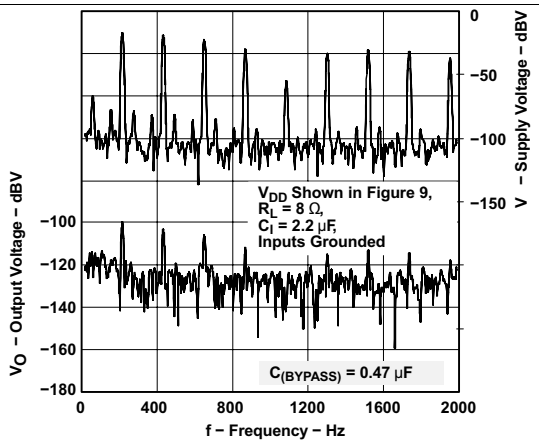

Figure 8. GSM Power Supply Rejection vs Frequency

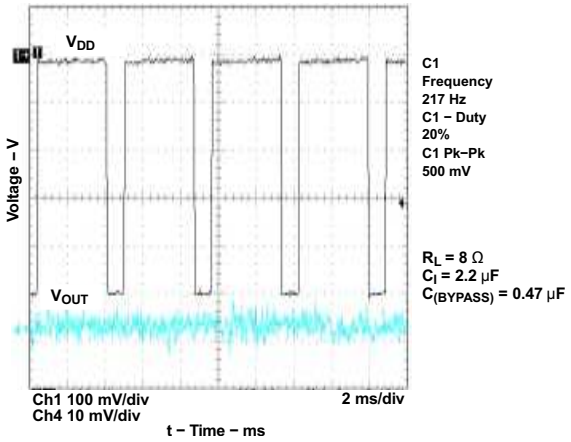

Figure 9. GSM Power Supply Rejection vs Time

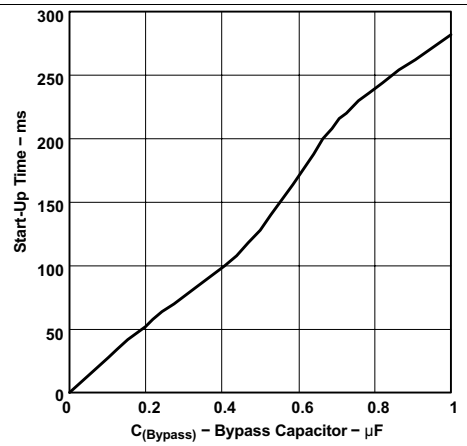

Figure 10. Start-Up Time vs Bypass Capacitor

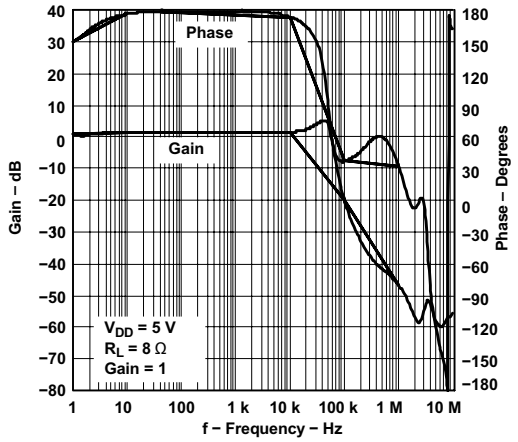

Figure 11. Closed-Loop Gain/Phase vs Frequency

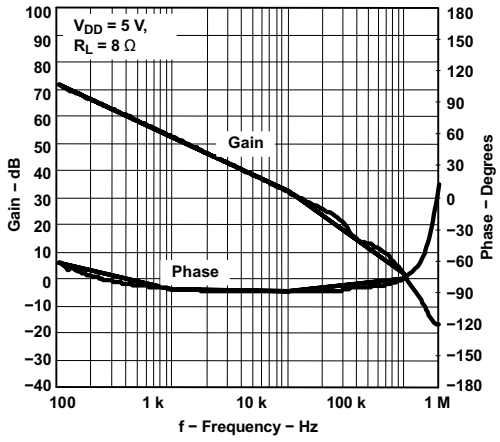

Figure 12. Open-Loop Gain/Phase vs Frequency

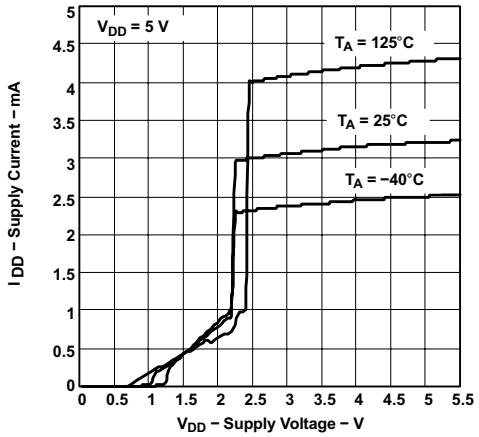

Figure 13. Supply Current vs Supply Voltage

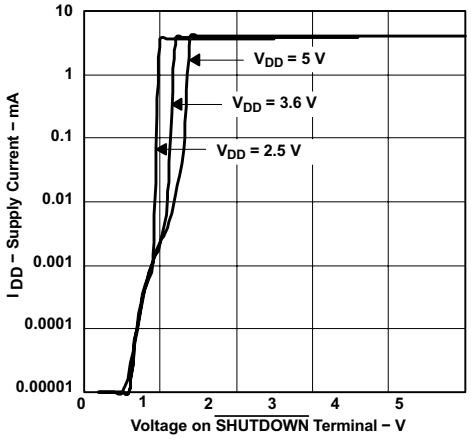

Figure 14. Supply Current vs Supply Voltage

8 Parameter Measurement Information

All parameters are measured according to the conditions described in *Specifications*.

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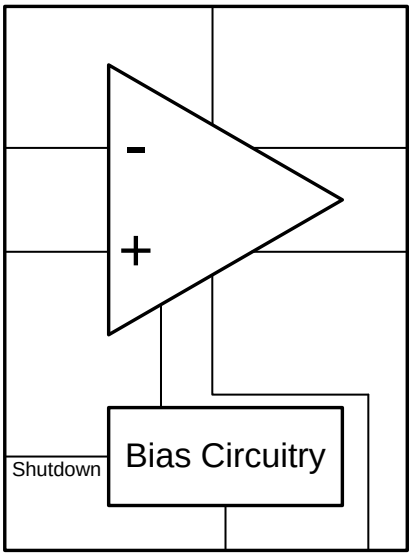
9 Detailed Description

9.1 Overview

The TPA6204A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around VDD/2 regardless of the common-mode voltage at the input.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Advantages of Fully Differential Amplifiers

- **Input coupling capacitors not required:** A fully differential amplifier with good CMRR, like the TPA6204A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has mid-supply lower than the mid-supply of the TPA6204A1, the common-mode feedback circuit adjusts for that, and the TPA6204A1 outputs are still biased at mid-supply of the TPA6204A1. The inputs of the TPA6204A1 can be biased from 0.5 V to VDD − 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.
- **Mid-supply bypass capacitor, C(BYPASS), not required:** The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output. It is important to remember that removing the bypass capacitor slightly worsens the kSVR. A slight decrease of kSVR, however, may be acceptable when an additional component can be eliminated.
- **Better RF-immunity:** GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

9.3.2 Fully Differential Amplifier Efficiency and Thermal Information

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or DC voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from VDD. The internal voltage drop multiplied by the average value of the supply current, IDD(avg), determines the internal power dissipation of the amplifier.

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Feature Description (continued)

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 15).

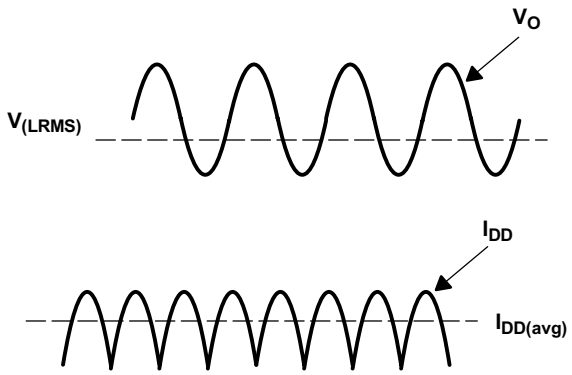

Figure 15. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Figure 13 and are the basis for calculating amplifier efficiency.

$$Efficiency\ of\ a\ BTL\ amplifier = \frac{P_L}{P_{SUP}}$$

where

$$P_L = \frac{V_L rms^2}{R_L},\ and\ V_{LRMS} = \frac{V_P}{\sqrt{2}},\ therefore,\ P_L = \frac{V_P{}^2}{2R_L}$$

where

- P_L = Power delivered to load
- V_{LRMS} = RMS voltage on BTL load
- R_L = Load resistance
- V_P = Peak voltage of BTL load

and

$$P_{SUP} = V_{DD} I_{DD}avg\ and\ I_{DD}avg = \frac{1}{\pi}\int_0^{\pi}\frac{V_P}{R_L}\sin(t)\,dt = -\frac{1}{\pi}\times\frac{V_P}{R_L}[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

where

- P_{SUP} = Power drawn from power supply
- R_L = Load resistance
- V_P = Peak voltage of BTL load
- I_{DD}avg = Average current drawn from the power supply
- V_{DD} = Power supply voltage

Therefore,

$$P_{SUP} = \frac{2V_{DD}V_P}{\pi R_L} \quad (2)$$

Substituting P_L and P_{SUP} in Equation 5,

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Feature Description (continued)

$$\textit{Efficiency if a BTL amplifer} = \frac{\frac{V_P{}^2}{2R_L}}{\frac{2V_{DD}V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}}$$

where

$$V_P = \sqrt{2P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\sqrt{2P_L R_L}}{4V_{DD}}$$

where

- η_{BTL} = Efficiency of a BTL amplifier (4)

Table 2 and Table 3 employ Equation 5 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 1.6 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible.

A simple formula for calculating the maximum power dissipated, PDmax, may be used for a differential output application:

$$P_{D\max} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (5)$$

The P_{Dmax} for a 5-V, 8-Ω system is 0.64 W.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 3 mm × 3 mm DRB package is shown in the dissipation rating table. Converting this to $R_{\theta JA}$:

$$R_{\theta JA} = \frac{1}{\textit{Derating Factor}} = \frac{1}{0.0218} = 45.9^{\circ}C/W \quad (6)$$

Given $R_{\theta JA}$, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA6204A1 is 150°C.

$$T_A Max = T_J Max - R_{\theta JA} P_{Dmax} \quad (7)$$

$$= 150 - 45.9(0.64) = 120.6^{\circ}C$$

Equation 7 shows that the maximum ambient temperature is 120.6°C (package limited to 85°C) at maximum power dissipation with a 5-V supply.

Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6204A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition, using speakers with an impedance higher than 8-Ω dramatically increases the thermal performance by reducing the output current.

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Feature Description (continued)

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power in 3.6-V 8-Ω BTL Systems(1)

OUTPUT POWER (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE(2) (°C)
0.1	27.6	0.262	0.36	85
0.2	39.0	0.312	0.51	85
0.5	61.7	0.310	0.81	85
0.6	67.6	0.288	0.89	85

(1) DRB package
(2) Package limited to 85°C ambient

Table 3. Efficiency and Maximum Ambient Temperature vs Output Power in 5-V 8-Ω Systems(1)

OUTPUT POWER (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE(2) (°C)
0.5	44.4	0.625	1.13	85
1	62.8	0.592	1.60	85
1.36	73.3	0.496	1.86	85
1.7	81.9	0.375	2.08	85

(1) DRB package
(2) Package limited to 85°C ambient

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The TPA6204A1 can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW level. While in shutdown mode, the device is turned off, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin.

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10 Application and Implementation

NOTE

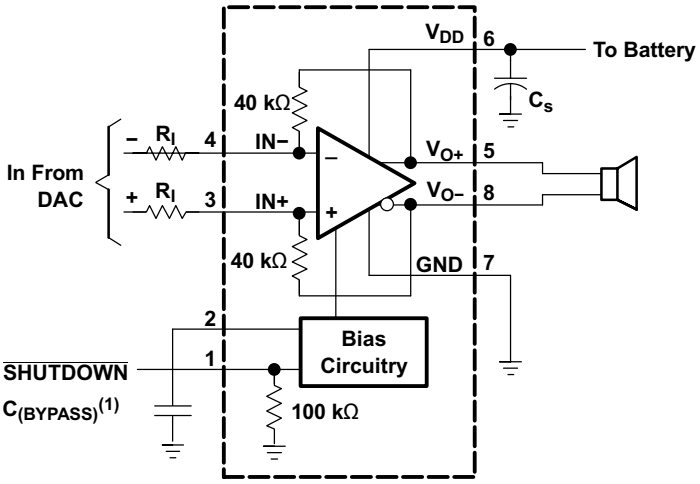
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA6204A1 device starts its operation by asserting the SHUTDOWN pin to logic 1. The device enters in shutdown mode when pulling the SHUTDOWN pin low. This typical connection diagram highlights the required external components and system level connections for proper operation of the device in popular use case. Any design variation can be supported by TI through schematic and layout reviews. Visit e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Application

Figure 16 shows a typical circuit for the TPA6204A1 with a speaker, input resistors and supporting power supply capacitors.



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(1) $C_{(BYPASS)}$ is optional.

Figure 16. Typical Differential Input Application Schematic

10.2.1 Design Requirements

Table 4 lists the design parameters for this example.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Power supply	2.5 V to 5 V
Current	1 A
Speaker	8 Ω

10.2.2 Detailed Design Procedure

10.2.2.1 Selecting Components for Resistors (R_I)

The input resistor (RI) can be selected to set the gain of the amplifier according to Equation 8.

$$\text{Gain} = R_F/R_I \quad (8)$$

The internal feedback resistors (RF) are trimmed to 40 kΩ. Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, TI recommends using 1% tolerance resistors or better to keep the performance optimized.

10.2.2.2 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

10.2.2.2.1 Bypass Capacitor ($C_{(BYPASS)}$) and Start-Up Time

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common-mode voltage to VDD/2. Adding a capacitor to this pin filters any noise into this pin and increases kSVR. $C_{(BYPASS)}$ also determines the rise time of VO+ and VO− when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Figure 10 shows the relationship of $C_{(BYPASS)}$ to start-up time.

10.2.2.2.2 Input Capacitor (C_I)

The TPA6204A1 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to VDD − 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors. In the single-ended input application an input capacitor, CI, is required to allow the amplifier to bias the input signal to the proper DC level. In this case, CI and RI form a high-pass filter with the corner frequency determined in Equation 9.

$$f_c = \frac{1}{2\pi R_I C_I} \tag{9}$$

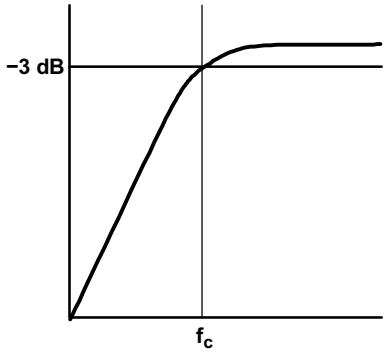

Figure 17. CI and RI High-Pass Filter Cutoff Frequency

The value of CI is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where RI is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 9 is reconfigured as Equation 10.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{10}$$

In this example, CI is 0.16 µF, so one would likely choose a value in the range of 0.22 µF to 0.47 µF. Ceramic capacitors should be used when possible, as they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor must face the amplifier input in most applications, as the DC level there is held at VDD/2, which is likely higher than the source DC level. It is important to confirm the capacitor polarity in the application.

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10.2.2.2.3 Decoupling Capacitor (C_S)

The TPA6204A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF, placed as close as possible to the device VDD lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

10.2.3 Application Curves

For application curves, see the figures listed in Table 5.

Table 5. Table of Graphs

			FIGURE
P_O	Output power	vs Supply voltage	Figure 1
		vs Load resistance	Figure 2
P_D	Power dissipation	vs Output power	Figure 3
THD+N	Total harmonic distortion + noise	vs Output power	Figure 4
		vs Frequency	Figure 5
		vs Common-mode input voltage	Figure 6
K_{SVR}	Supply voltage rejection ratio	vs Frequency	Figure 7
	GSM Power supply rejection	vs Time	Figure 8
	GSM Power supply rejection	vs Frequency	Figure 9
	Closed-loop gain/phase	vs Frequency	Figure 10

10.3 System Examples

Figure 18 through Figure 19 show application schematics for differential and single-ended inputs. Typical values are shown in Table 6.

Table 6. Typical Component Values

COMPONENT	VALUE
R_I	40 kΩ
$C_{(BYPASS)}$	0.22 µF
C_S	1 µF
C_I	0.22 µF

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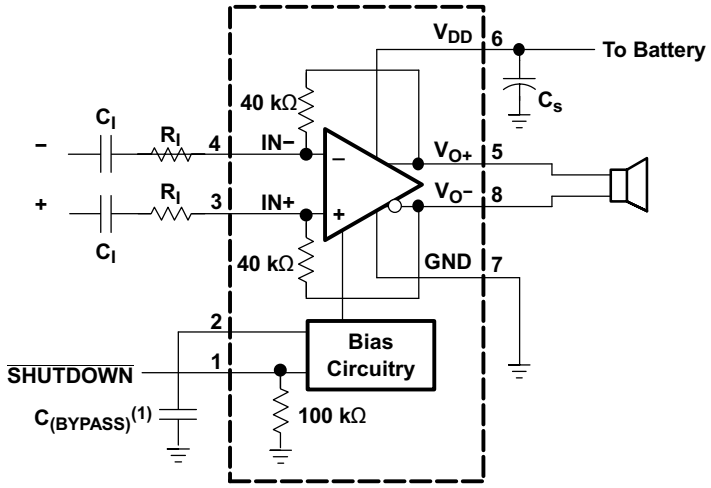
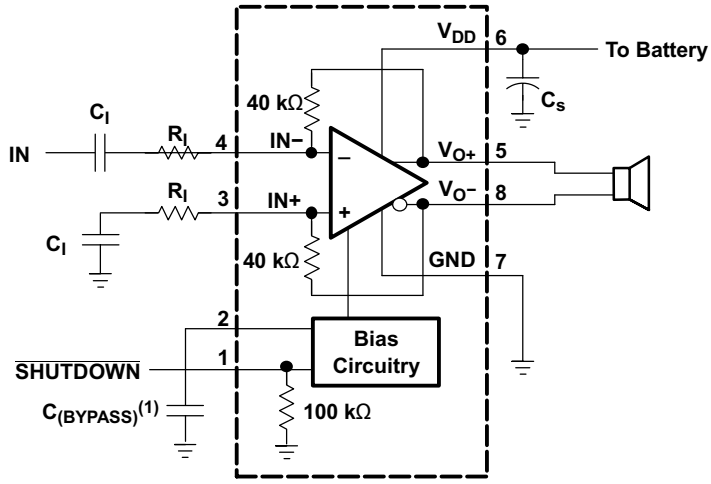


(1) $C_{(BYPASS)}$ is optional

Figure 18. Differential Input Application Schematic Optimized With Input Capacitors



(1) $C_{(BYPASS)}$ is optional
(2) Due to the fully differential design of this amplifier, the performance is severly degraded if you connect the unused input to **BYPASS** when using single-ended inputs.

(1) $C_{(BYPASS)}$ is optional

(2) Due to the fully differential design of this amplifier, the performance is severely degraded if you connect the unused input to BYPASS when using single-ended inputs.

Figure 19. Single-Ended Input Application Schematic

11 Power Supply Recommendations

The TPA6204A1 is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. Therefore, the output voltage range of power supply must be within this range and well regulated. The current capability of upper power must not exceed the maximum current limit of the power switch. TI recommends placing decoupling capacitors in every voltage source pin. Place these decoupling capacitors as close as possible to the TPA6204A1.

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11.1 Power Supply Decoupling Capacitor

The TPA6204A1 device requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent series resistance (ESR) ceramic capacitor, typically 0.1 µF, as close as possible of the VDD pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Also is recommended to place a 2.2-µF to 10-µF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

12 Layout

12.1 Layout Guidelines

It is important to keep the TPA6204A1 external components very close to the TPA6204A1 to limit noise pickup.

12.2 Layout Example

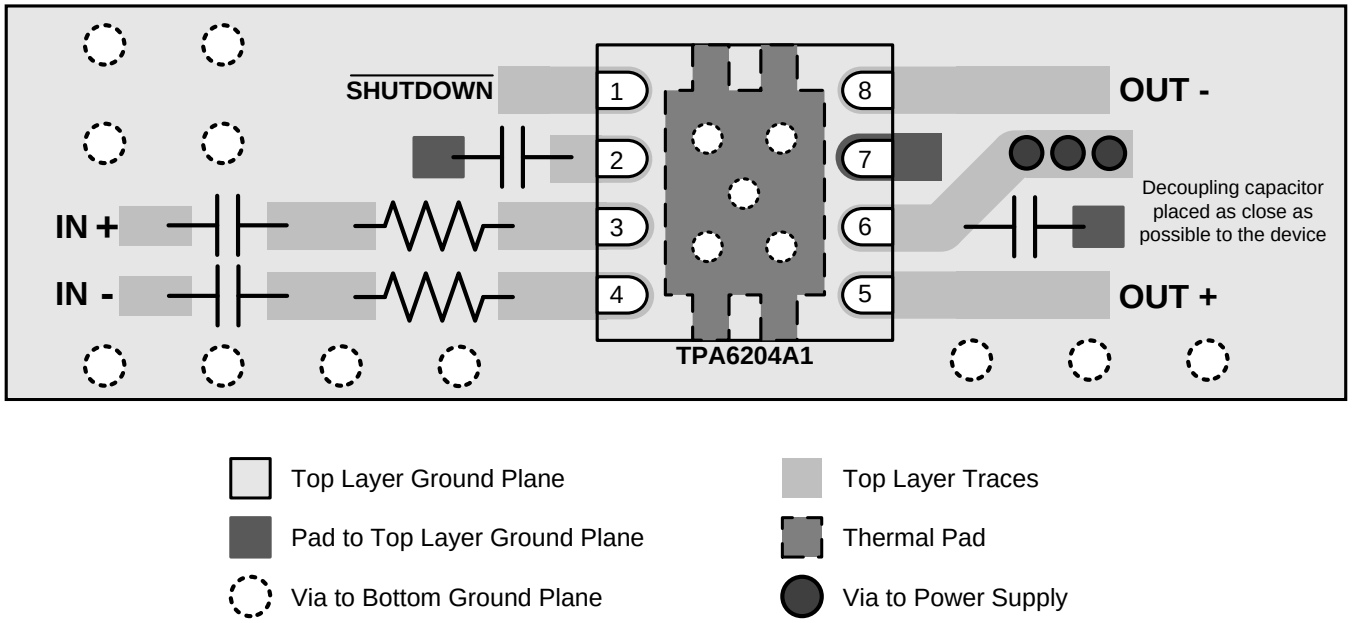

Figure 20. TPA6204A1 Layout Recommendation

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6204A1DRB	Active	Production	SON (DRB) | 8	121 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ
TPA6204A1DRB.B	Active	Production	SON (DRB) | 8	121 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ
TPA6204A1DRBG4	Active	Production	SON (DRB) | 8	121 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ
TPA6204A1DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ
TPA6204A1DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ
TPA6204A1DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AYJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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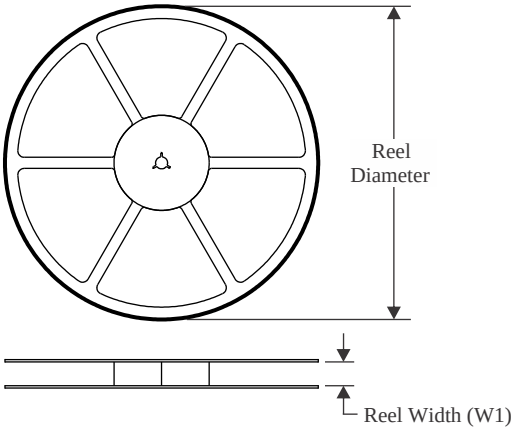
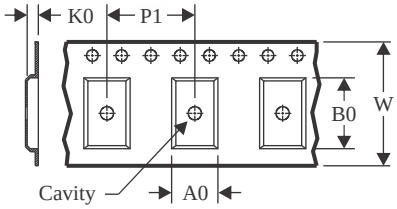
TAPE AND REEL INFORMATION

REEL DIMENSIONS

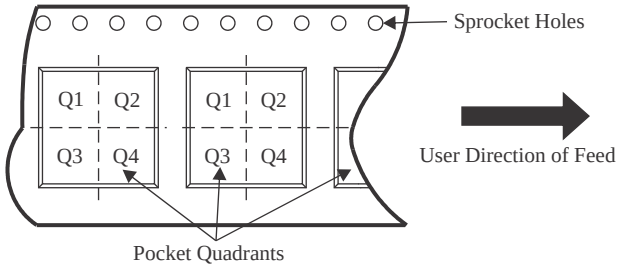


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

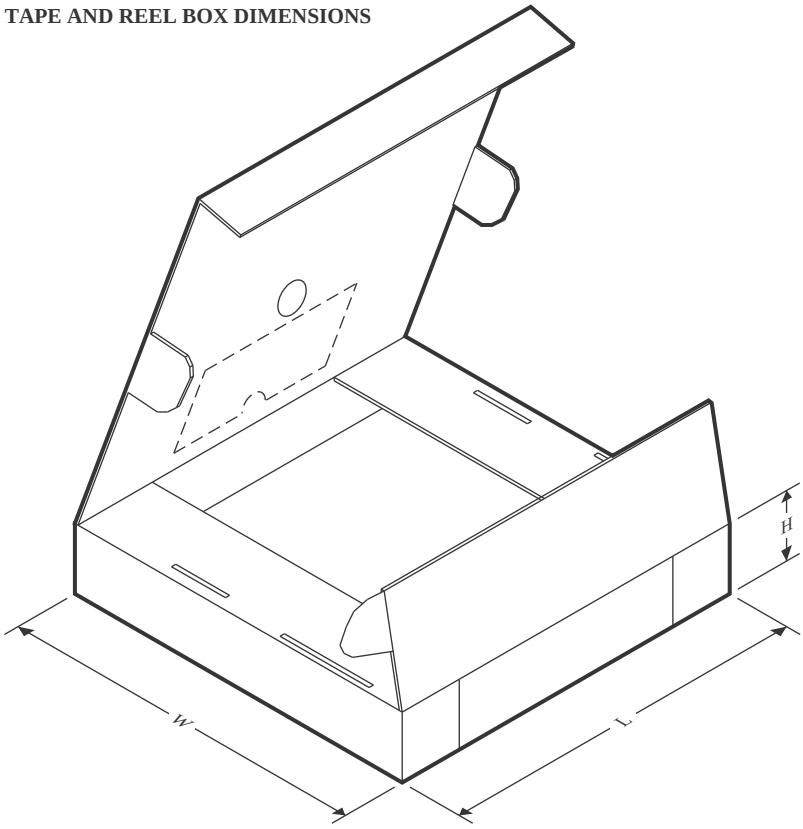
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6204A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6204A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

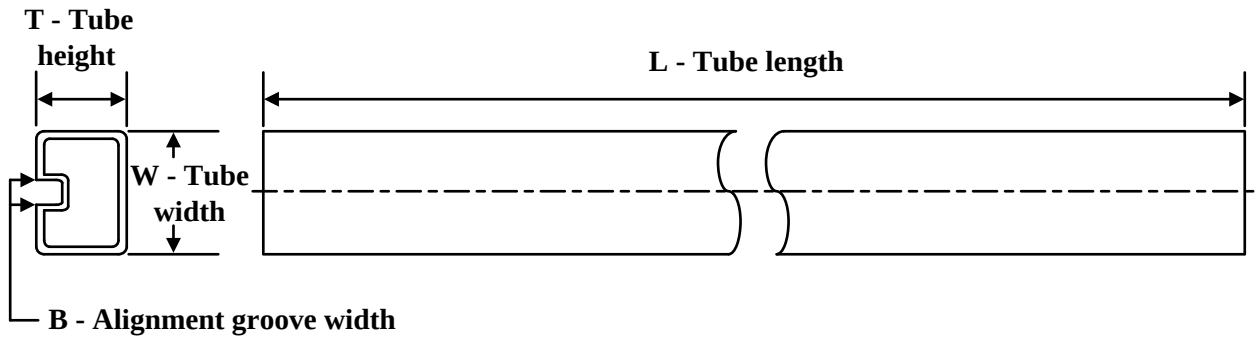
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6204A1DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPA6204A1DRBR	SON	DRB	8	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6204A1DRB	DRB	VSON	8	121	381	4.83	2286	0
TPA6204A1DRB	DRB	VSON	8	121	381	4.82	2286	NA
TPA6204A1DRB.B	DRB	VSON	8	121	381	4.83	2286	0
TPA6204A1DRB.B	DRB	VSON	8	121	381	4.82	2286	NA
TPA6204A1DRBG4	DRB	VSON	8	121	381	4.82	2286	NA
TPA6204A1DRBG4	DRB	VSON	8	121	381	4.83	2286	0

GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

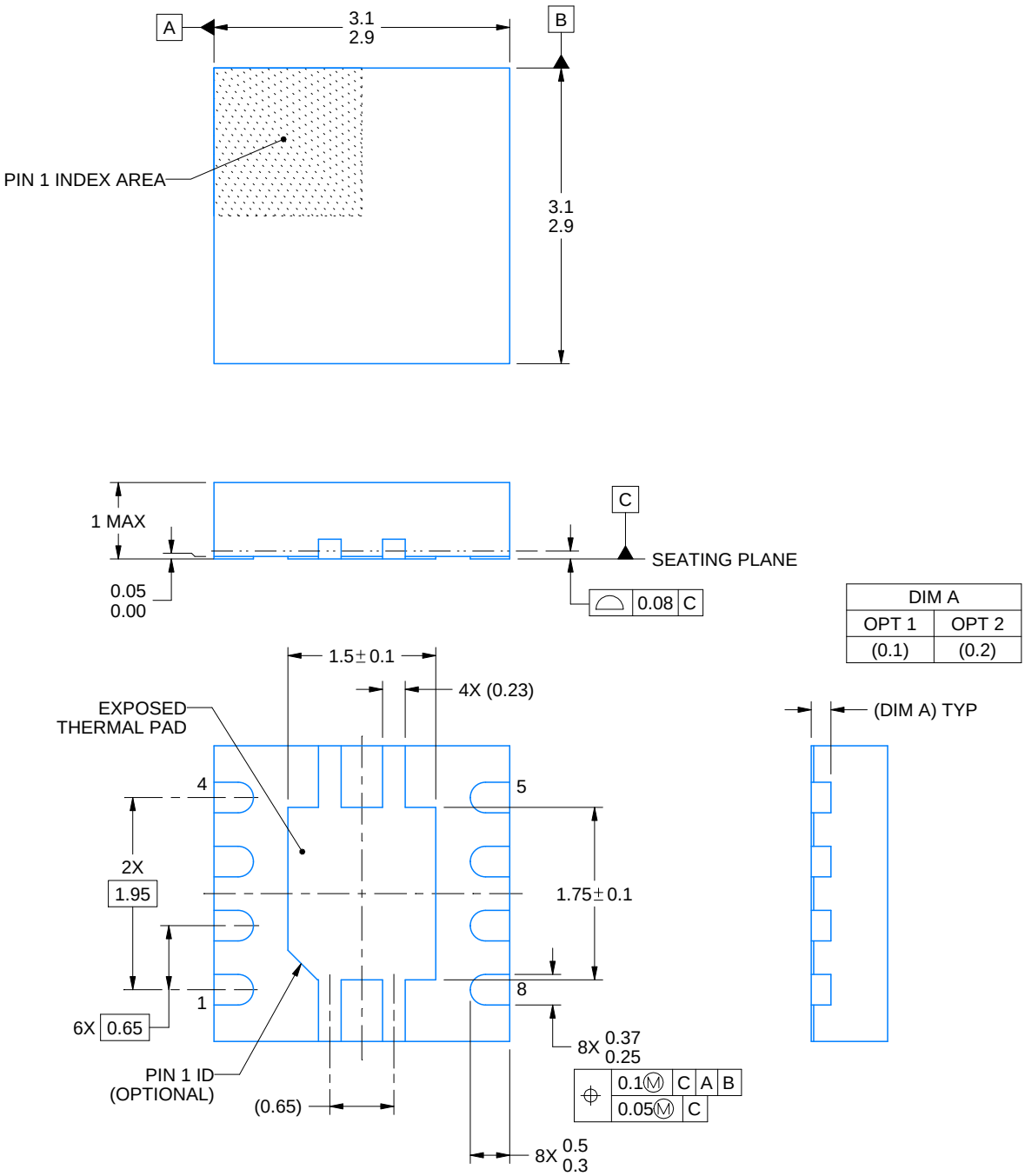
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRB0008A

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

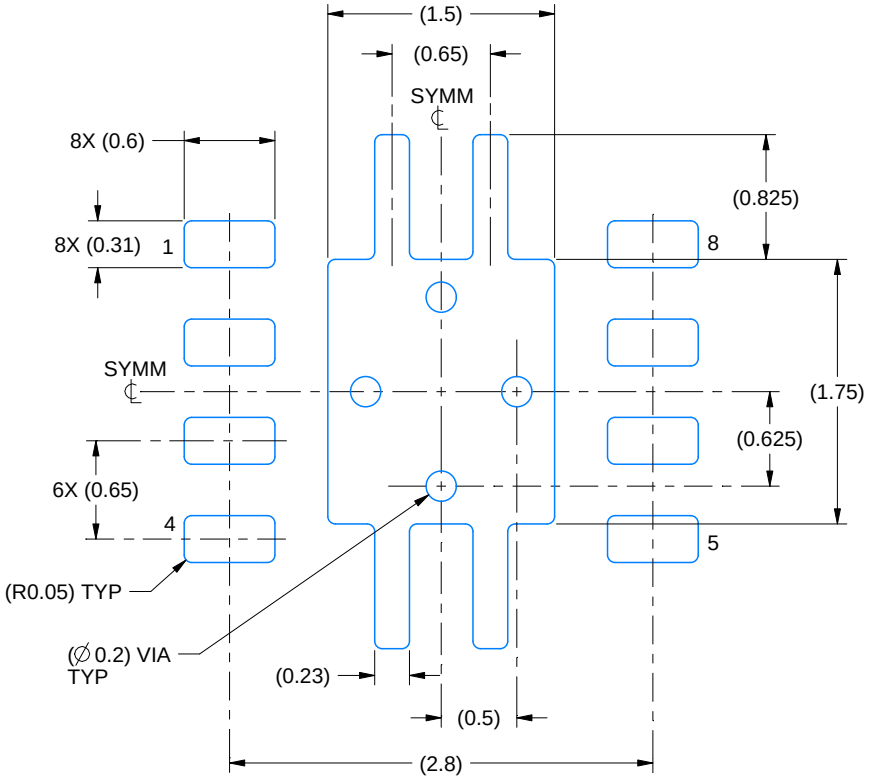
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

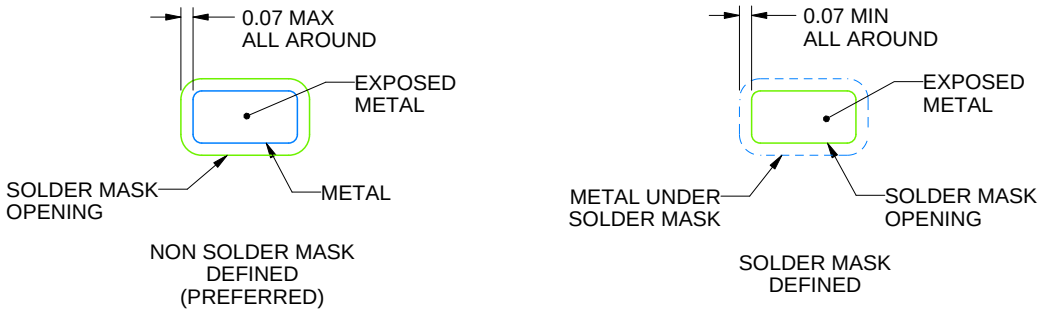
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

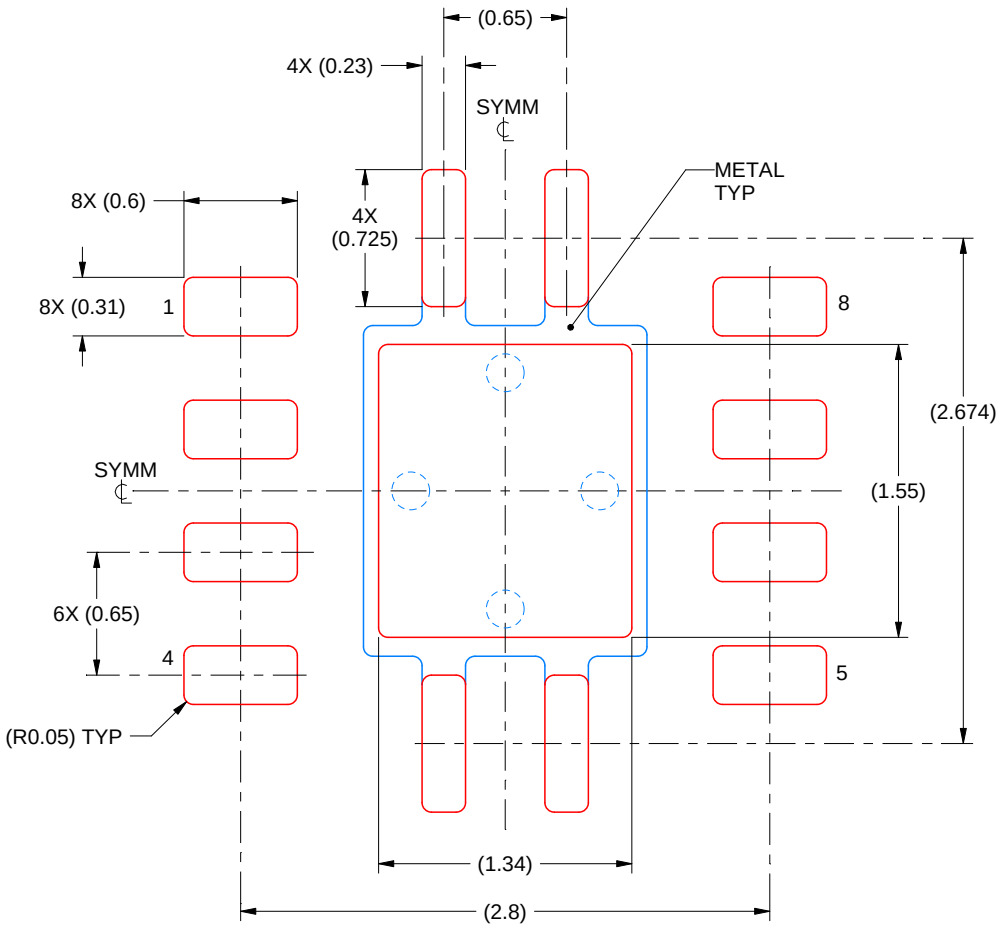


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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