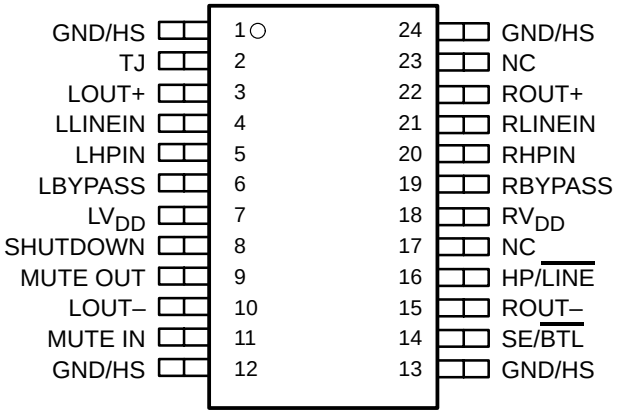
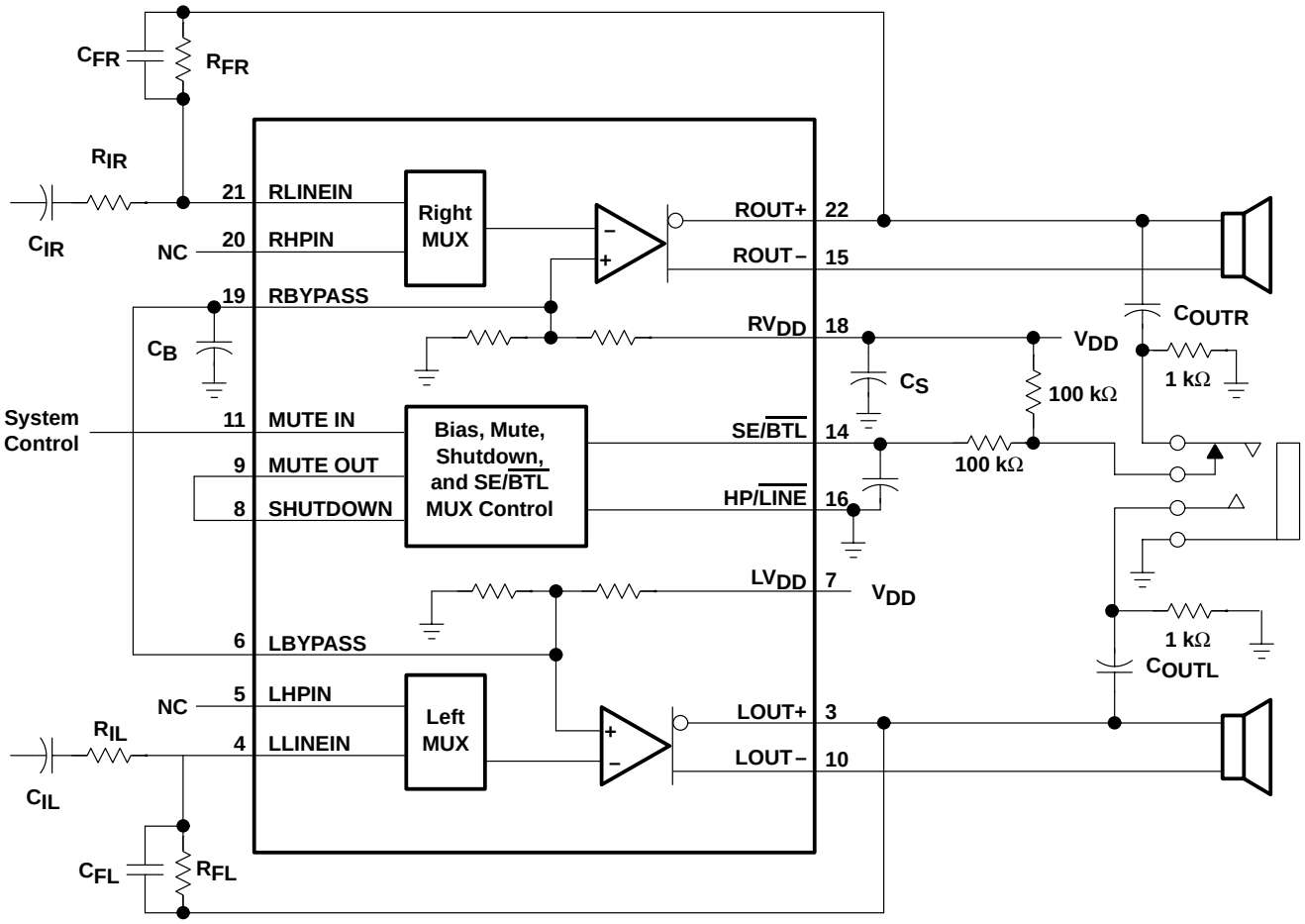
- **Integrated Depop Circuitry**
- **High Power with PC Power Supply**
  - **2 W/Ch at 5 V into a 3-Ω Load**
  - **800 mW/Ch at 3 V**
- **Fully Specified for Use With 3-Ω Loads**
- **Ultra-Low Distortion**
  - **0.05% THD+N at 2 W and 3-Ω Load**
- **Bridge-Tied Load (BTL) or Single-Ended (SE) Modes**
- **Stereo Input MUX**
- **Surface-Mount Power Package**
  24-Pin TSSOP PowerPAD™
- **Shutdown Control . . . I_{DD} = 5 μA**

PWP PACKAGE
(TOP VIEW)





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description

The TPA0202 is a stereo audio power amplifier in a 24-pin TSSOP thermal package capable of delivering greater than 2 W of continuous RMS power per channel into 3-Ω loads. The TPA0202 simplifies design and frees up board space for other features. Full power distortion levels of less than 0.1% THD+N from a 5-V supply are typical. Low-voltage applications are also well served by the TPA0202 providing 800-mW per channel into 3-Ω loads with a 3.3-V supply voltage.

The TPA0202 has integrated depop circuitry that virtually eliminates transients that cause noise in the speakers during power up and when using the mute and shutdown modes.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the TPA0202 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. Using the TPA0202 to drive line outputs up to 700 mW/channel into external 3-Ω loads is ideal for small non-powered external speakers in portable multimedia systems. The TPA0202 also features a shutdown function for power sensitive applications, holding the supply current at 5 μA.

The PowerPAD package† (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0202 to operate at full power into 3-Ω loads at ambient temperature of up to 85°C with 300 CFM of forced-air cooling. Into 8-Ω loads, the operating ambient temperature increases to 100°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP‡ (PWP)
–40°C to 85°C	TPA0202PWP

‡ The PWP packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA0202PWPR).

† See Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (Literature Number SLMA002) for more information on the PowerPAD package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND/HS	1, 12, 13, 24		Ground connection for circuitry, directly connected to thermal pad
HP/$\overline{\text{LINE}}$	16	I	Input MUX control input, hold high to select LHP IN or RHP IN (5, 20), hold low to select LLINE IN or RLINE IN (4, 21)
LBYPASS	6		Tap to voltage divider for left channel internal mid-supply bias
LHP IN	5	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
LLINE IN	4	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
LOUT+	3	O	Left channel + output in BTL mode, + output in SE mode
LOUT–	10	O	Left channel – output in BTL mode, high-impedance state in SE mode
LV_{DD}	7	I	Supply voltage input for left channel and for primary bias circuits
MUTE IN	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute
MUTE OUT	9	O	Follows MUTE IN terminal (11), provides buffered output
NC	17, 23		No internal connection
RBYPASS	19		Tap to voltage divider for right channel internal mid–supply bias
RHPIN	20	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
RLINEIN	21	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
ROUT+	22	O	Right channel + output in BTL mode, + output in SE mode
ROUT–	15	O	Right channel – output in BTL mode, high impedance state in SE mode
RV_{DD}	18	I	Supply voltage input for right channel
SE/$\overline{\text{BTL}}$	14	I	Hold low for BTL mode, hold high for SE mode
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, I_{DD} = 5 μA
TJ	2	O	Sources a current proportional to the junction temperature. This terminal should be left unconnected during normal operation. For more information, see the *junction temperature measurement* section of this document.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP‡	2.7 W	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}			3	5	5.5	V
Operating free-air temperature, T_A	V_{DD} = 5 V, 250 mW/ch average power,	4-Ω stereo BTL drive, with proper PCB design	–40		85	°C
	V_{DD} = 5 V, 2 W/ch average power,	3-Ω stereo BTL drive, with proper PCB design and 300 CFM forced-air cooling	–40		85	
Common mode input voltage, V_{ICM}	V_{DD} = 5 V		1.25		4.5	V
	V_{DD} = 3.3 V		1.25		2.7	

dc electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP†	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 5 V	Stereo BTL		19	30	mA
			Stereo SE		9	18	mA
			Mono BTL		9	18	mA
			Mono SE		3	10	mA
		V_{DD} = 3.3 V	Stereo BTL		13	20	mA
			Stereo SE		5	10	mA
			Mono BTL		5	10	mA
			Mono SE		3	6	mA
V_{OO}	Output offset voltage (measured differentially)	V_{DD} = 5 V,	Gain = 2,	See Note 1	5	25	mV
$I_{DD(MUTE)}$	Supply current in mute mode	V_{DD} = 5 V			1.5		mA
$I_{DD(SD)}$	I_{DD} in shutdown	V_{DD} = 5 V			5	20	μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 3 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%,	BTL,	See Figure 3	2		W
		THD = 1%,	BTL,	See Figure 3	2.2		
THD+N	Total harmonic distortion plus noise	P_o = 2W,	f = 20 – 20 kHz,	See Figure 5	200		m%
		V_I = 1 V,	R_L = 10 kΩ,	A_V = 1 V/V	100		m%
B_{OM}	Maximum output power bandwidth	A_V = 10 V/V	THD < 1 %,	See Figure 5	>20		kHz
	Phase margin	R_L = 4 Ω,	Open Loop,	See Figure 43	85°		
	Supply ripple rejection ratio	f = 1 kHz,	See Figure 37		80		dB
		f = 20 – 20 kHz,	See Figure 37		60		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz,	See Figure 39		85		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_o = 500 mW,	BTL		95		dB
V_n	Output noise voltage	See Figure 35			21		μV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 3 Ω

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%,	BTL,	See Figure 10	800		mW
		THD = 1%,	BTL,	See Figure 10	900		
THD+N	Total harmonic distortion plus noise	P_o = 800 mW,	f = 20 – 20 kHz,	See Figure 11	350		m%
		V_I = 1 V,	R_L = 10 kΩ,	A_V = 1 V/V	200		m%
B_{OM}	Maximum output power bandwidth	A_V = 10 V/V	THD < 1 %,	See Figure 11	>20		kHz
	Phase margin	R_L = 4 Ω,	Open Loop,	See Figure 44	85°		
	Supply ripple rejection ratio	f = 1 kHz,	See Figure 37		70		dB
		f = 20 – 20 kHz,	See Figure 37		55		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz,	See Figure 40		85		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_o = 500 mW,	BTL		95		dB
V_n	Output noise voltage	See Figure 37			21		μV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

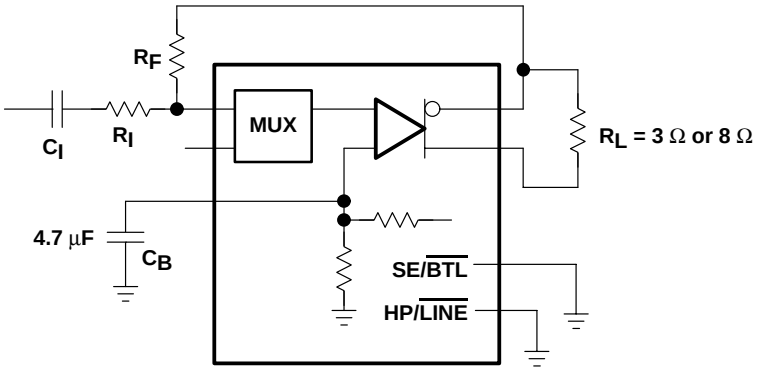


Figure 1. BTL Test Circuit

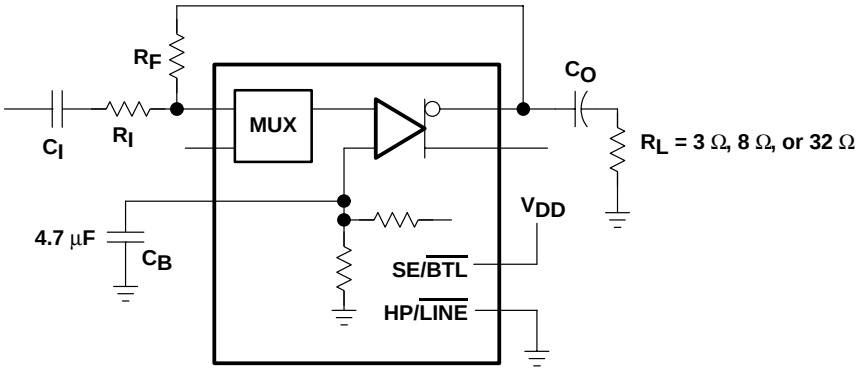


Figure 2. SE Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Frequency	4, 5, 7, 8, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24, 26, 27, 29, 30 32, 33
		vs Output power	3, 6, 9, 10, 13, 16, 19, 22, 25, 28, 31, 34
V_n	Output noise voltage	vs Frequency	35,36
	Supply ripple rejection ratio	vs Frequency	37,38
	Crosstalk	vs Frequency	39 – 42
	Open loop response	vs Frequency	43,44
	Closed loop response	vs Frequency	45, 48
I_{DD}	Supply current	vs Supply voltage	49
P_O	Output power	vs Supply voltage vs Load resistance	50, 51 52, 53
P_D	Power dissipation	vs Output power	54 – 57

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

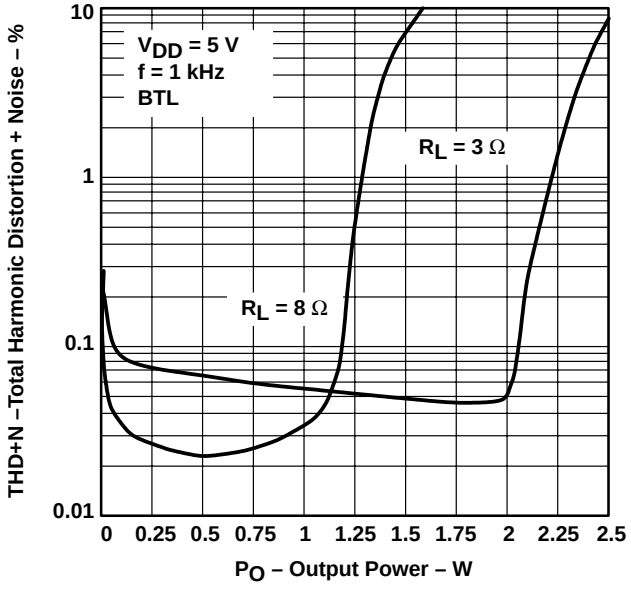


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

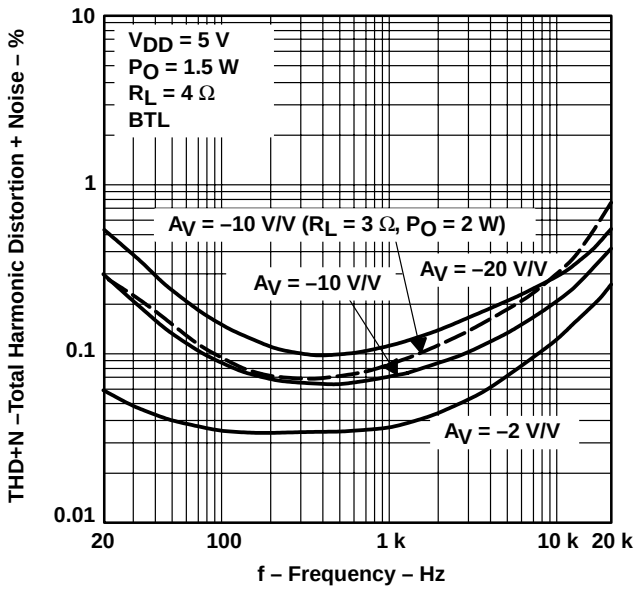


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

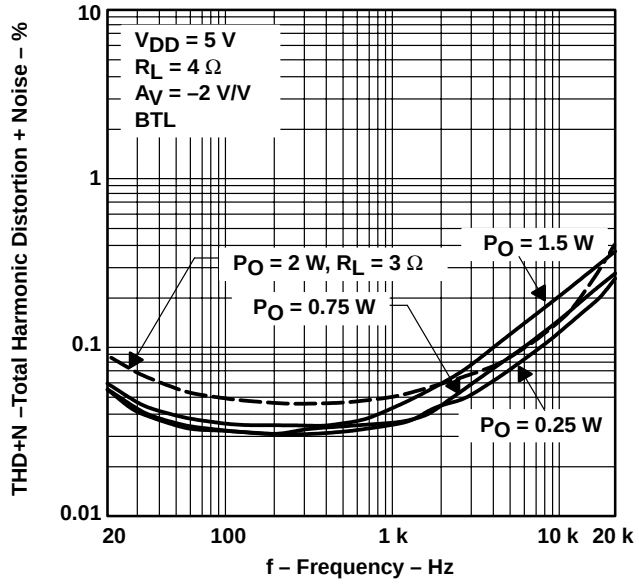


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

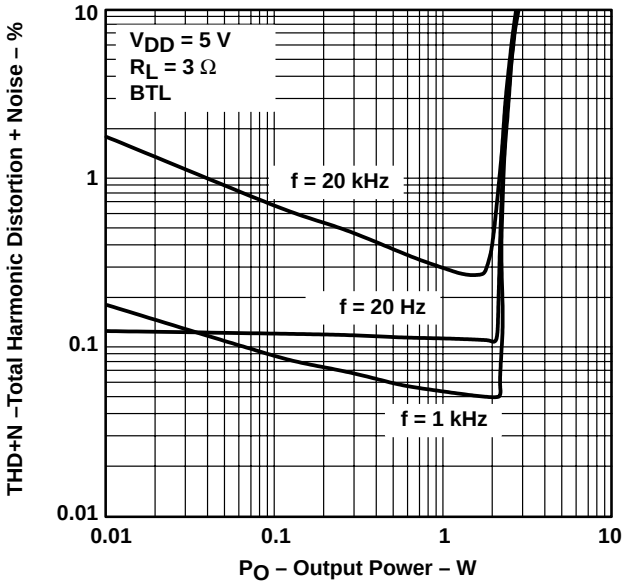


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

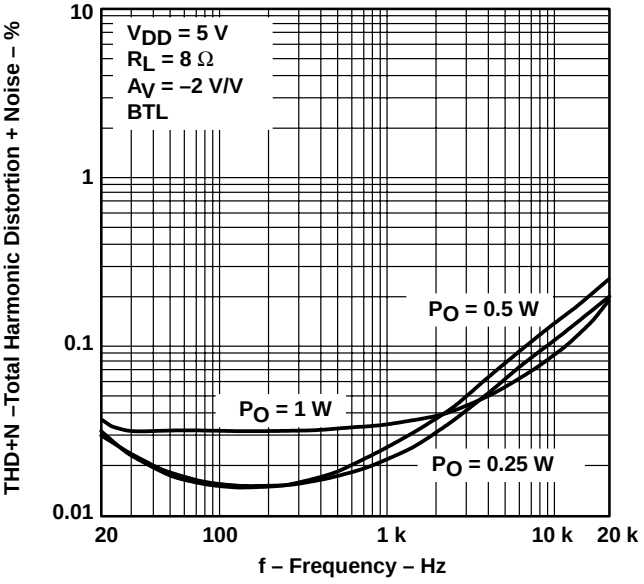


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

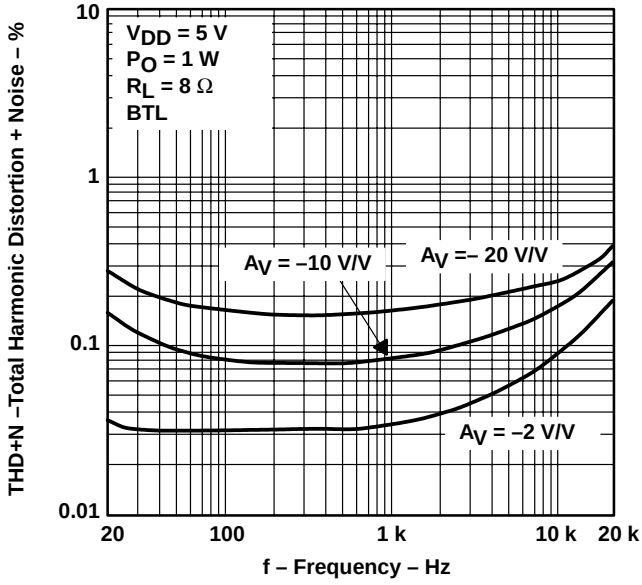


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

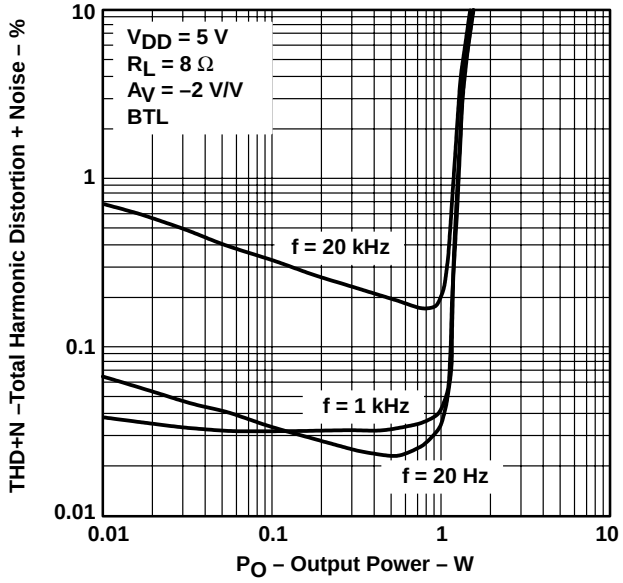


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

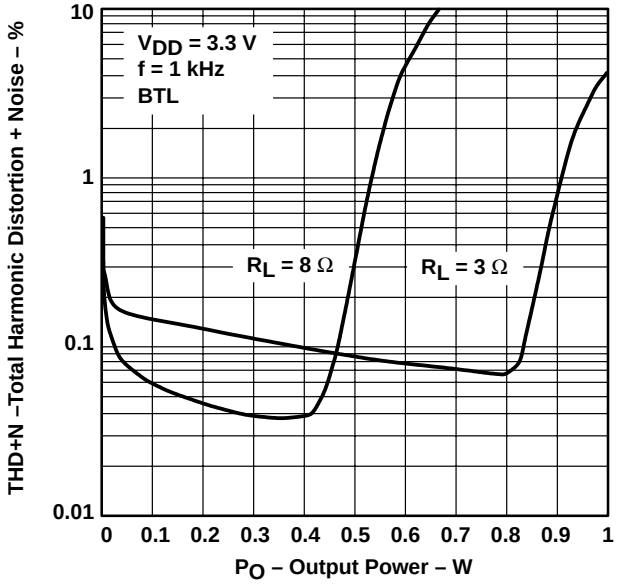


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

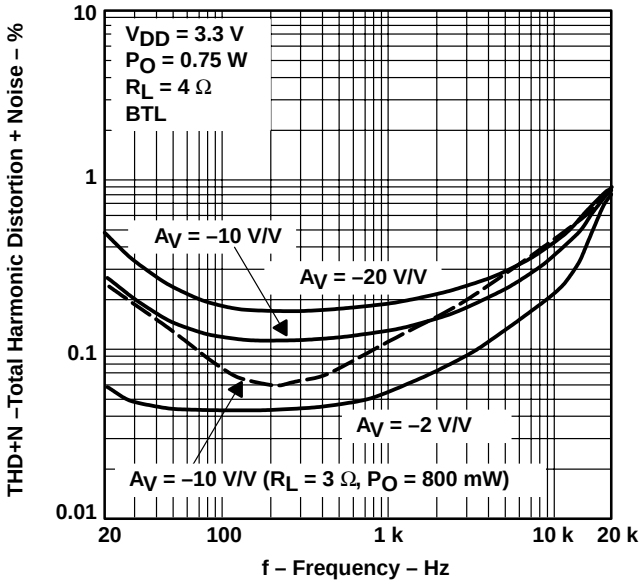


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

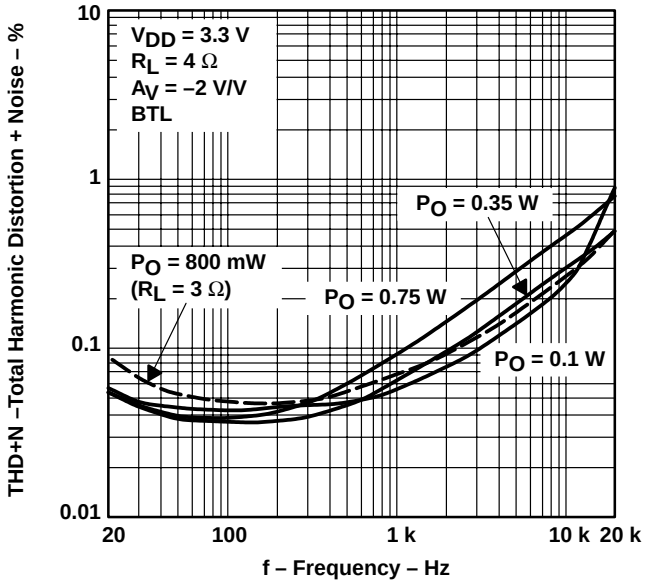


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

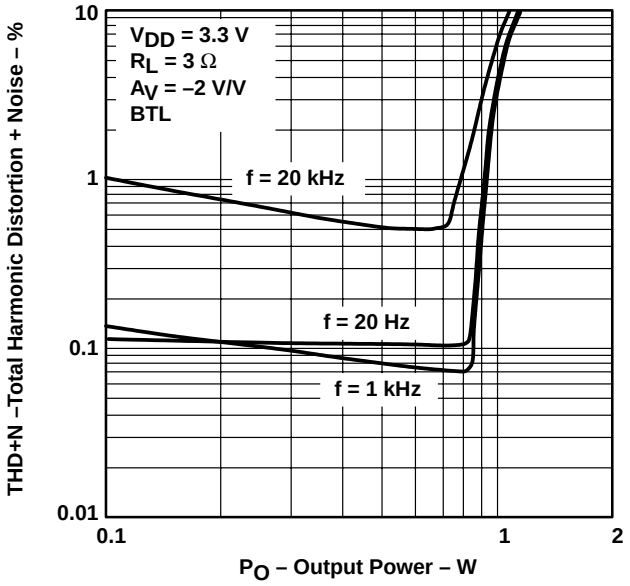


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

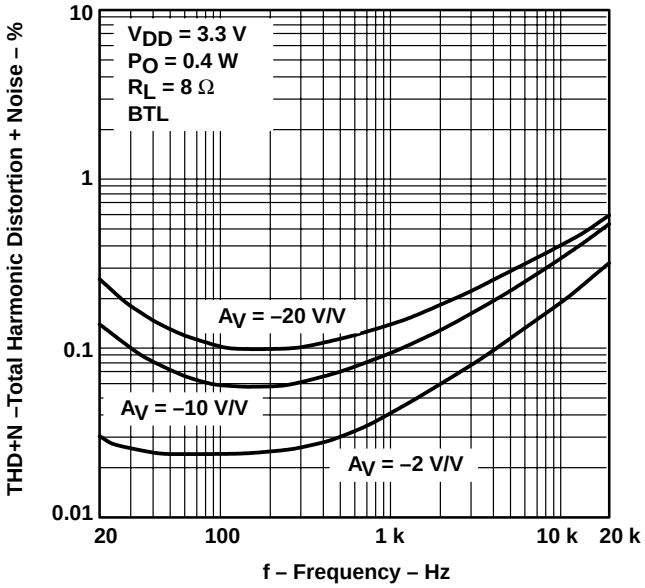


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

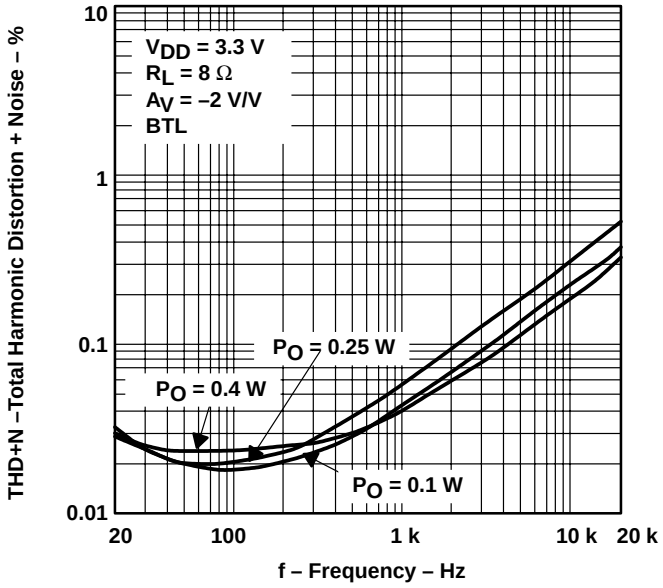


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

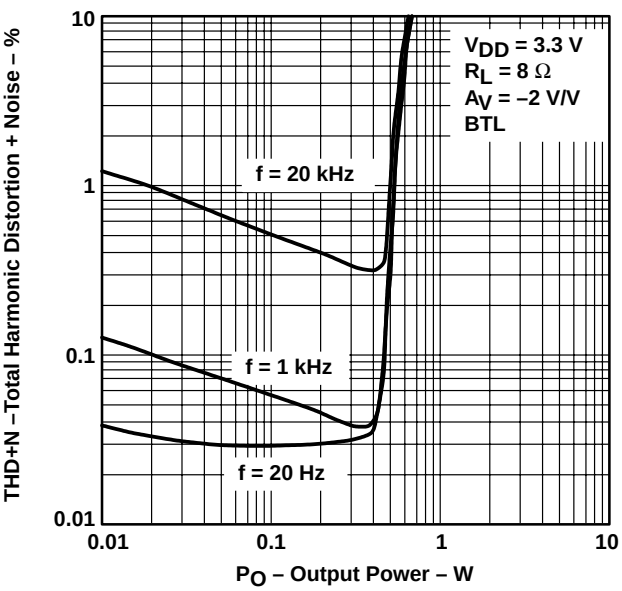


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

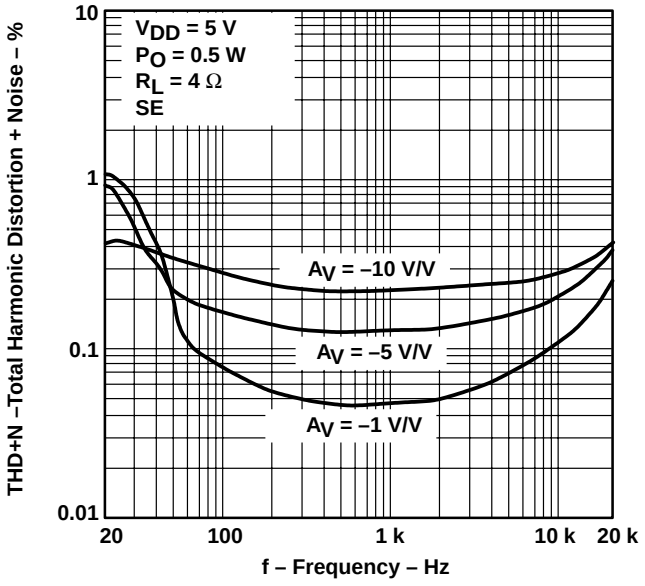


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

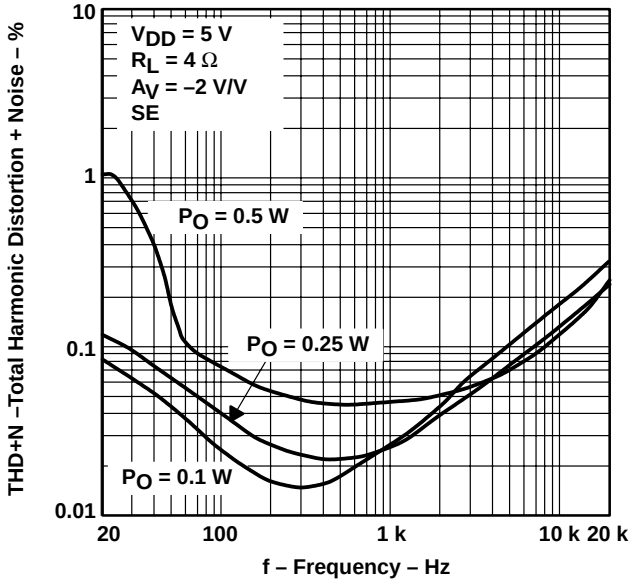


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

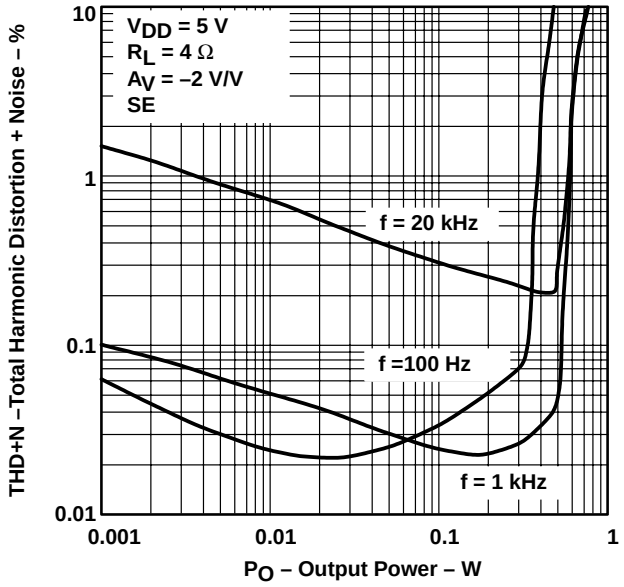


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

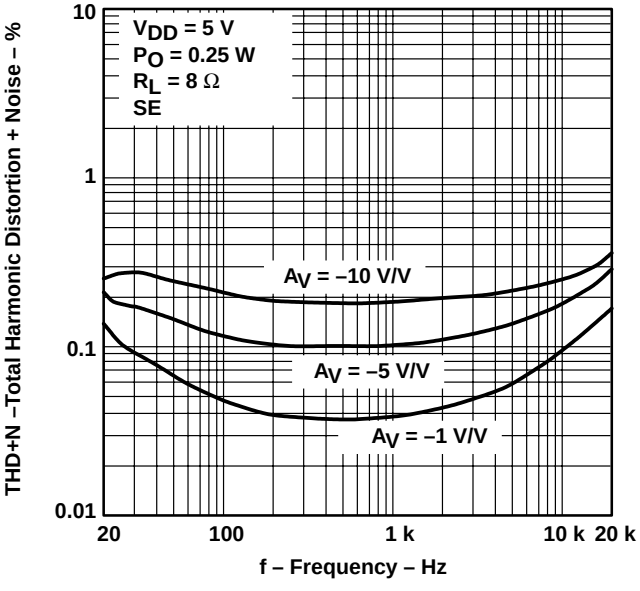


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

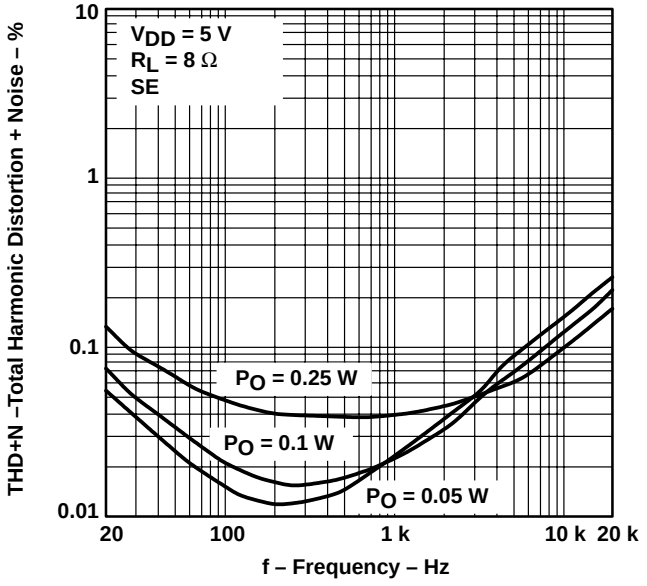


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

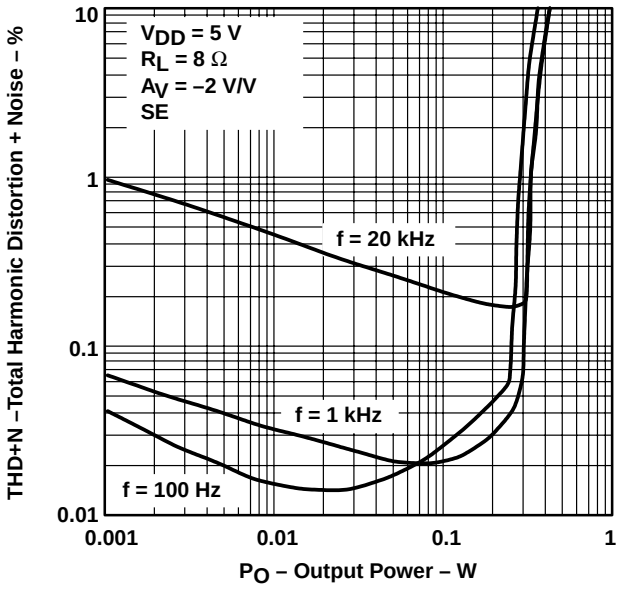


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

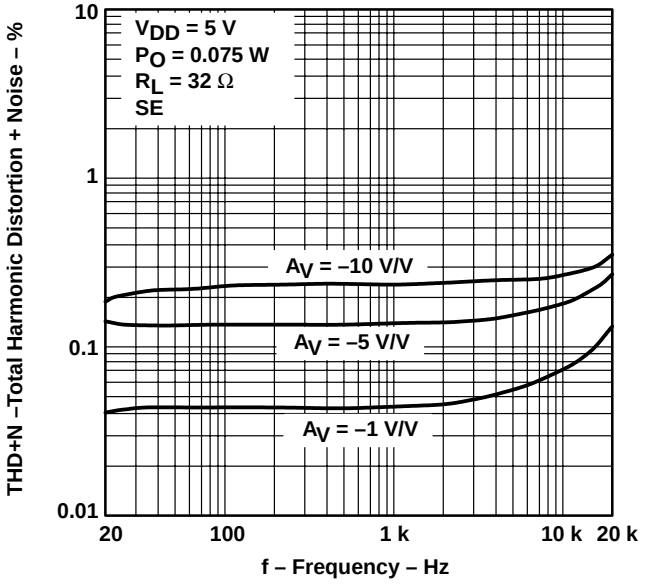


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

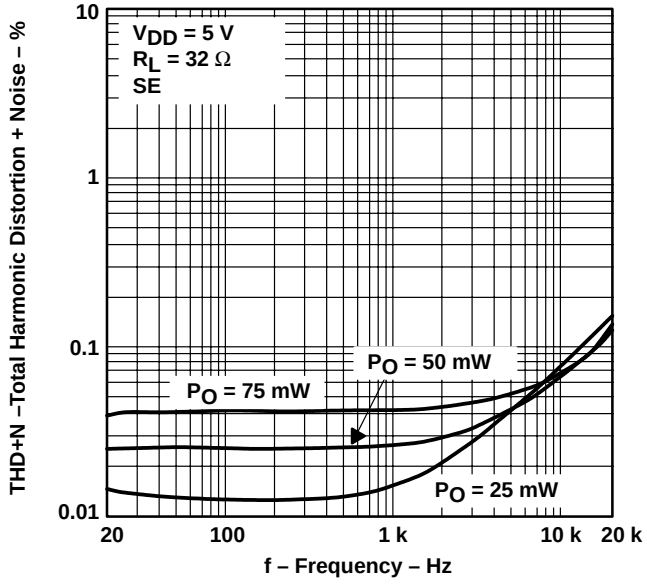


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

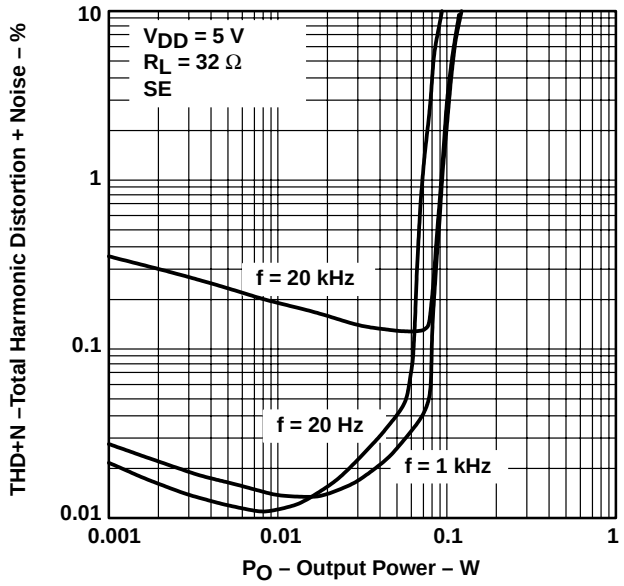


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

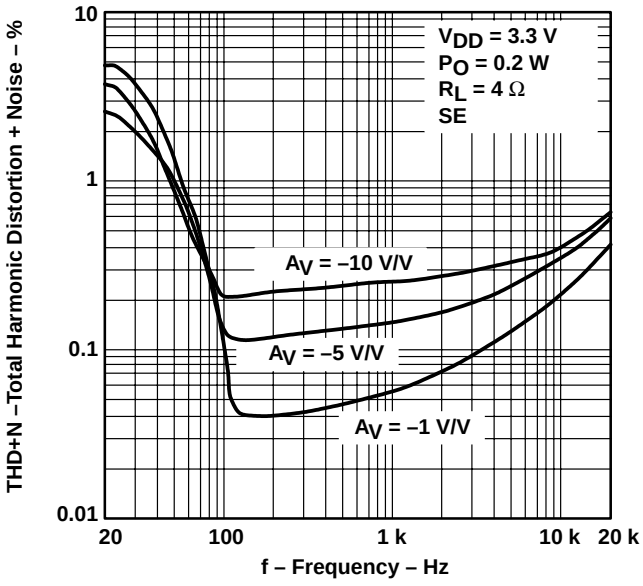


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

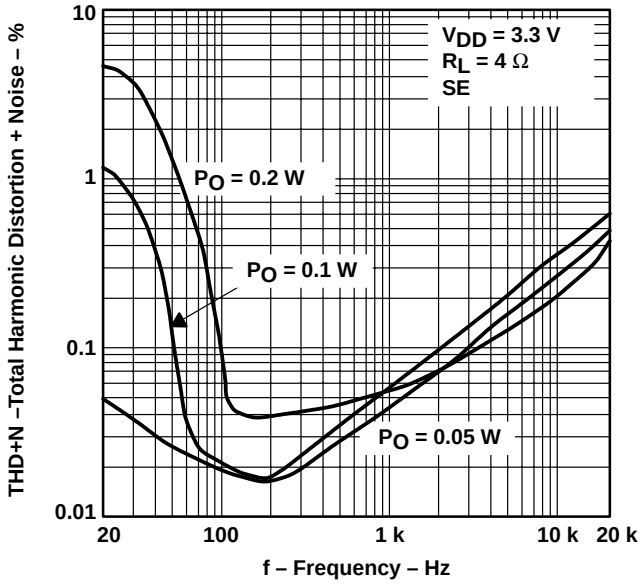


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

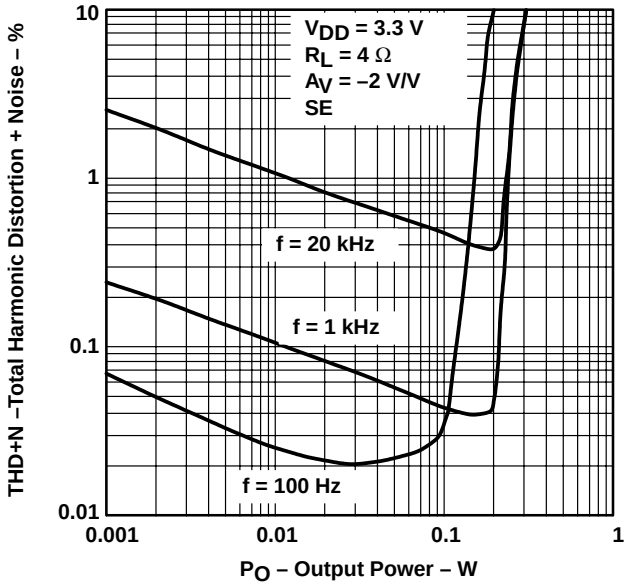


Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

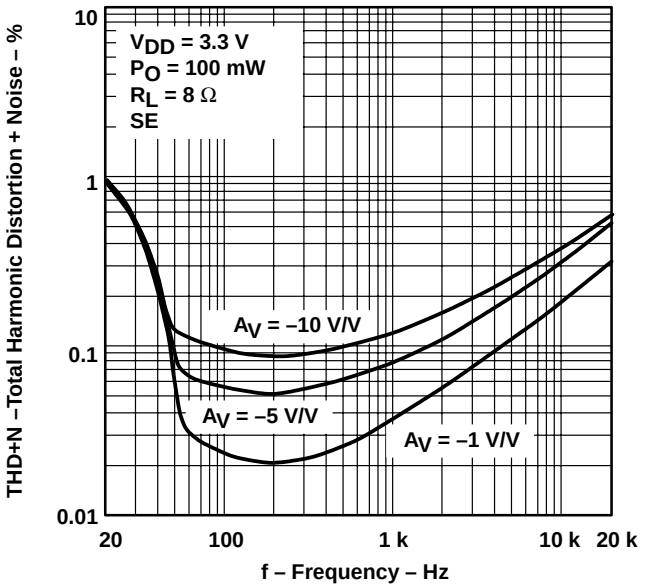


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

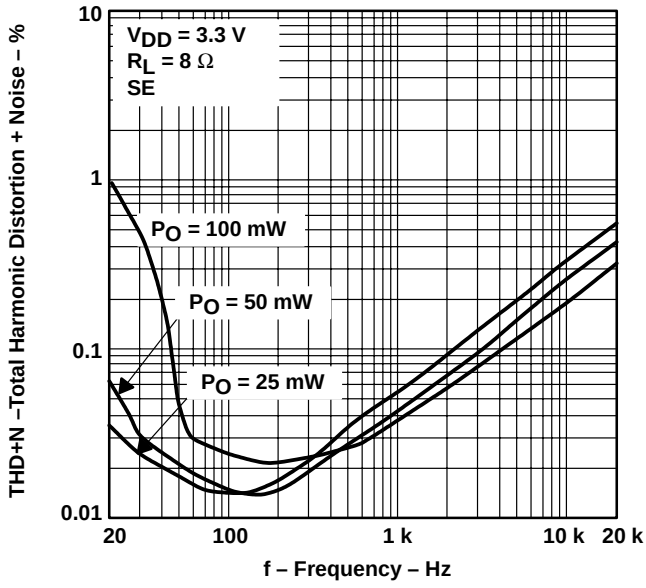


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

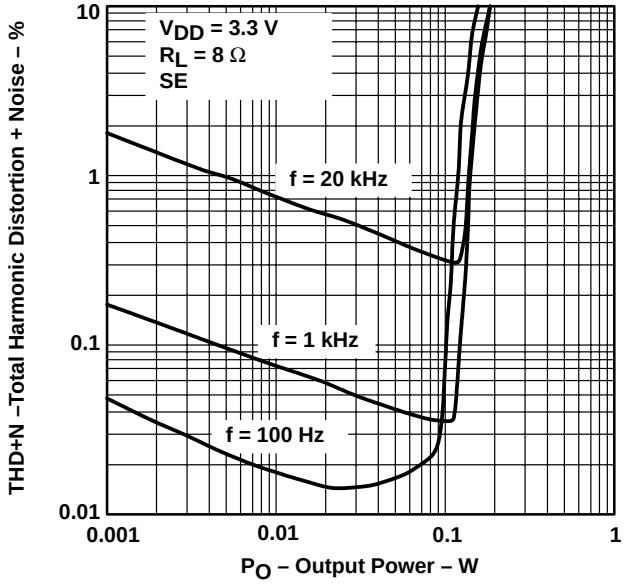


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

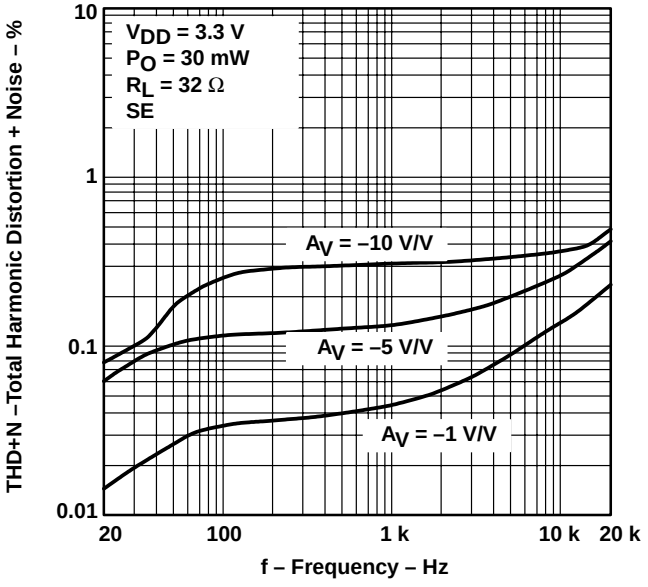


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

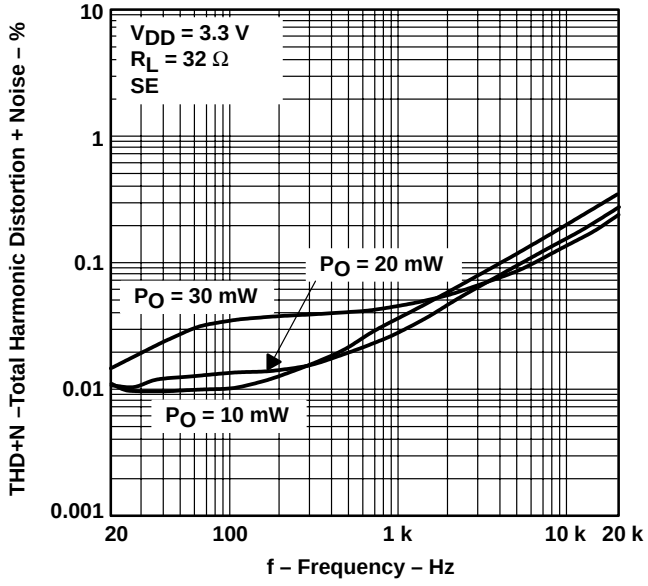


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

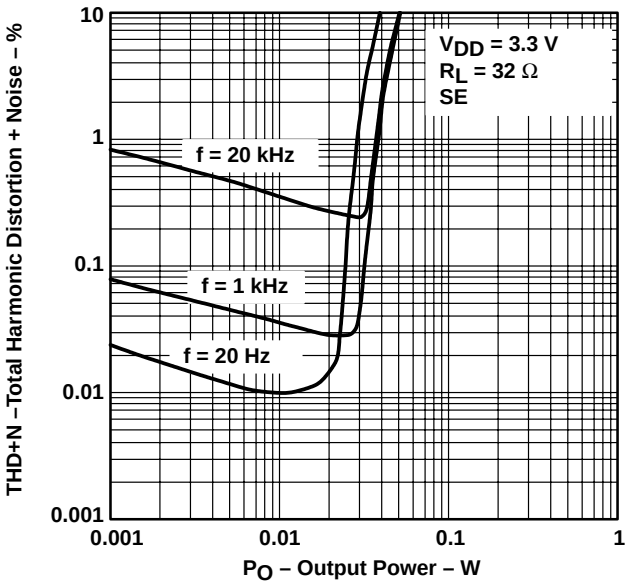


Figure 34

OUTPUT NOISE VOLTAGE vs FREQUENCY

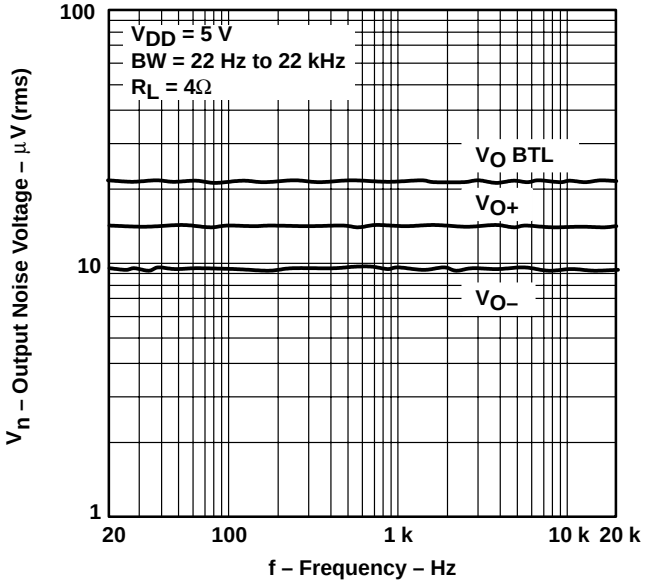


Figure 35

OUTPUT NOISE VOLTAGE vs FREQUENCY

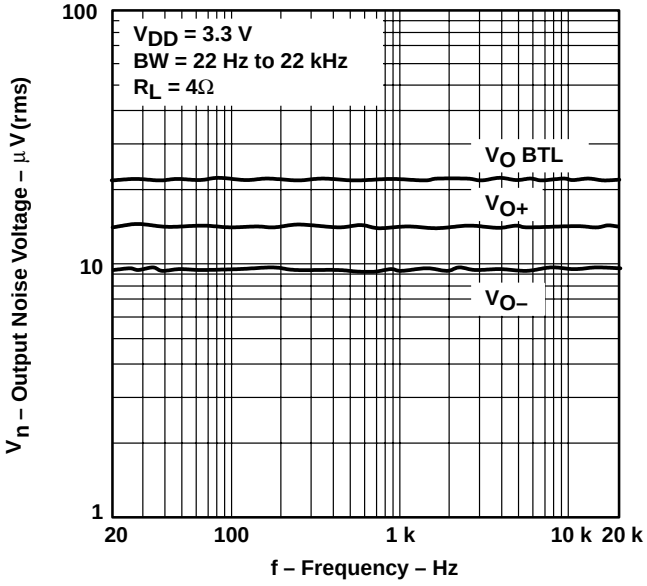


Figure 36

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

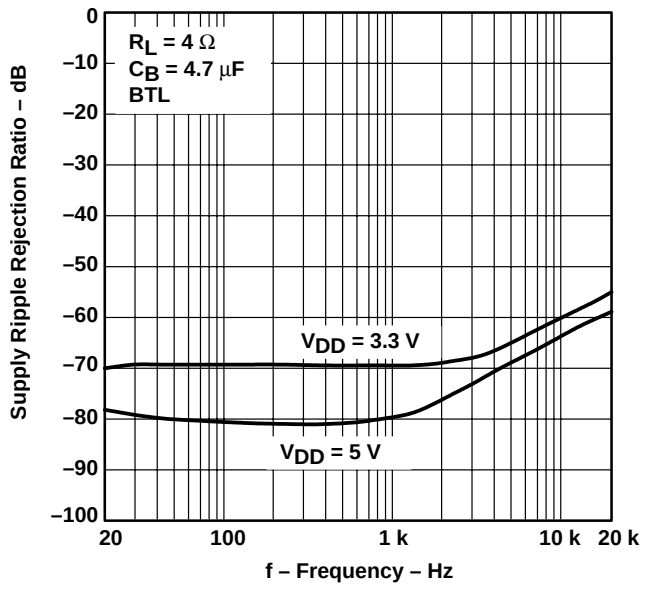


Figure 37

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

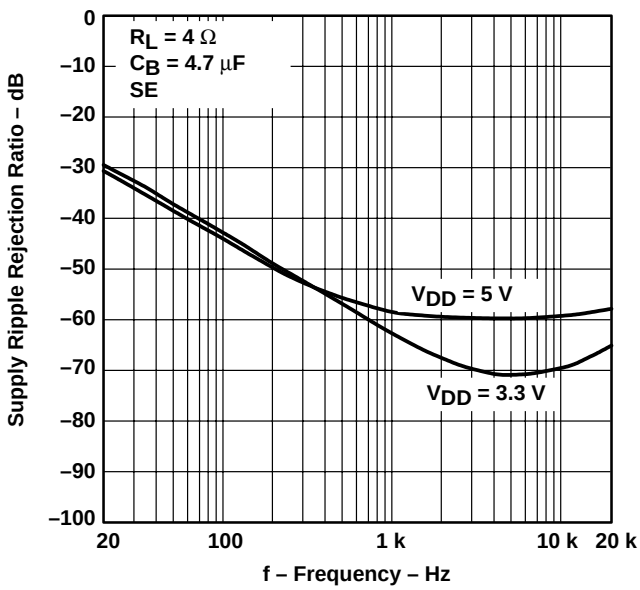


Figure 38

CROSSTALK vs FREQUENCY

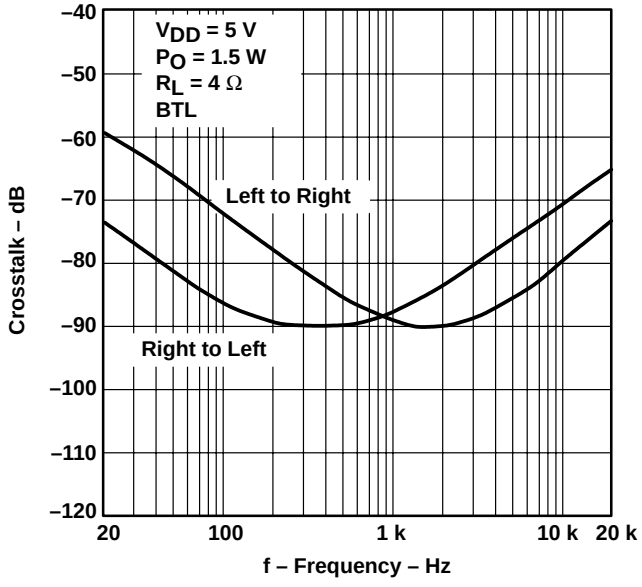


Figure 39

CROSSTALK vs FREQUENCY

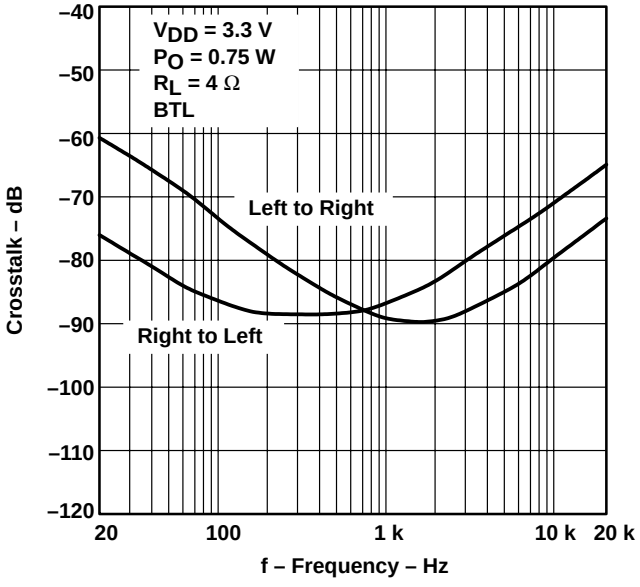


Figure 40

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

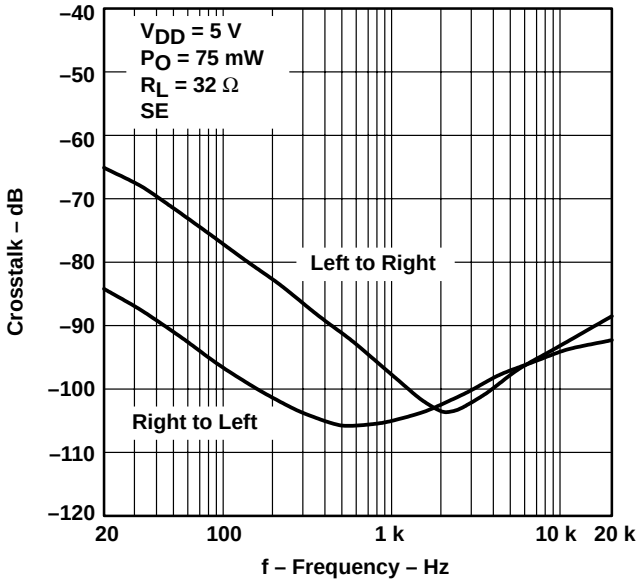


Figure 41

CROSSTALK vs FREQUENCY

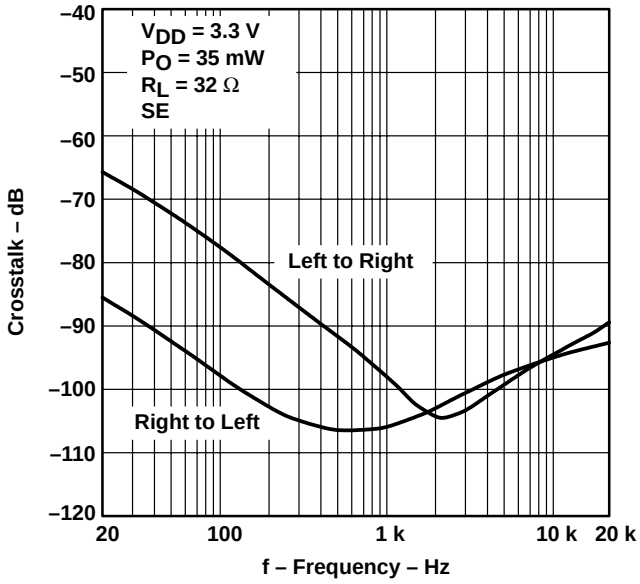


Figure 42

OPEN LOOP RESPONSE

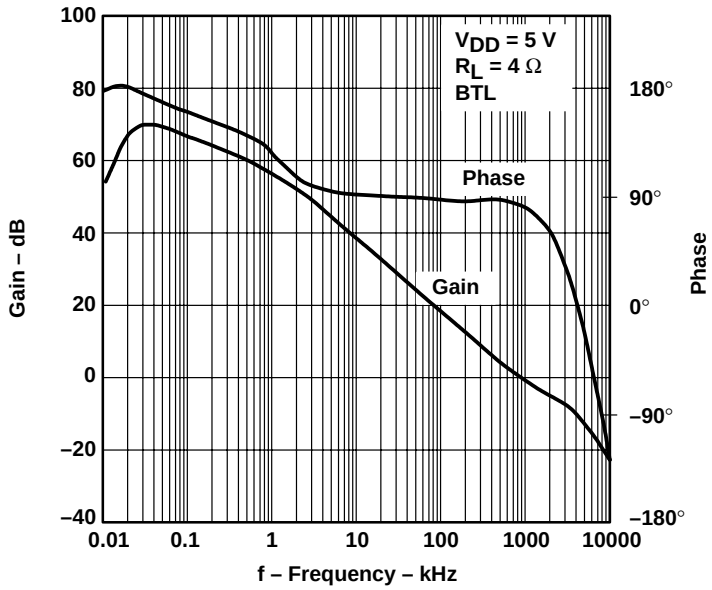


Figure 43

TYPICAL CHARACTERISTICS

OPEN LOOP RESPONSE

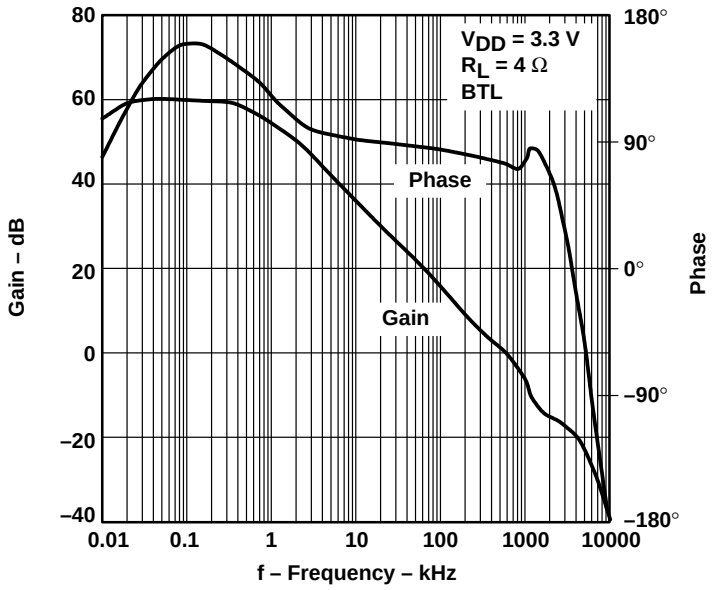


Figure 44

CLOSED LOOP RESPONSE

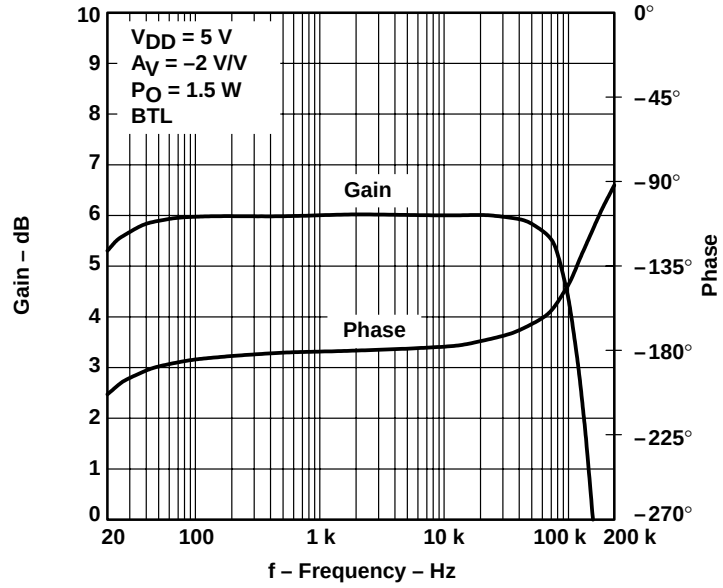


Figure 45

TYPICAL CHARACTERISTICS

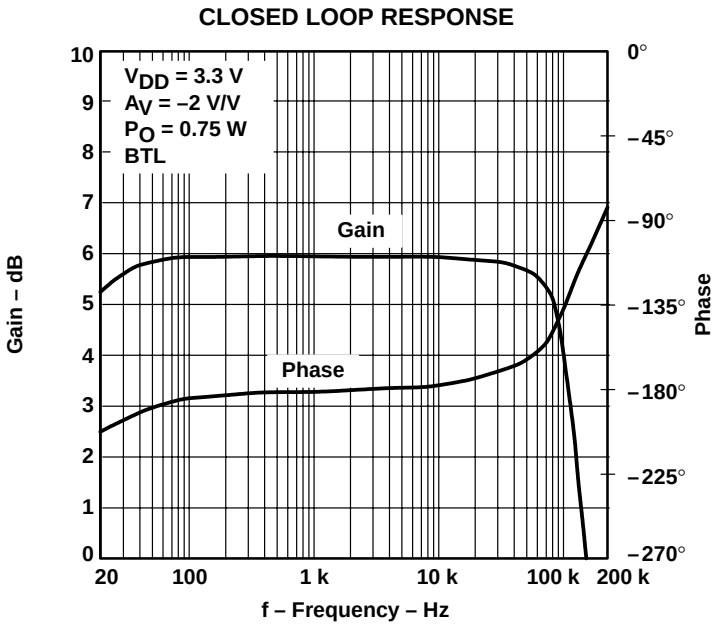


Figure 46

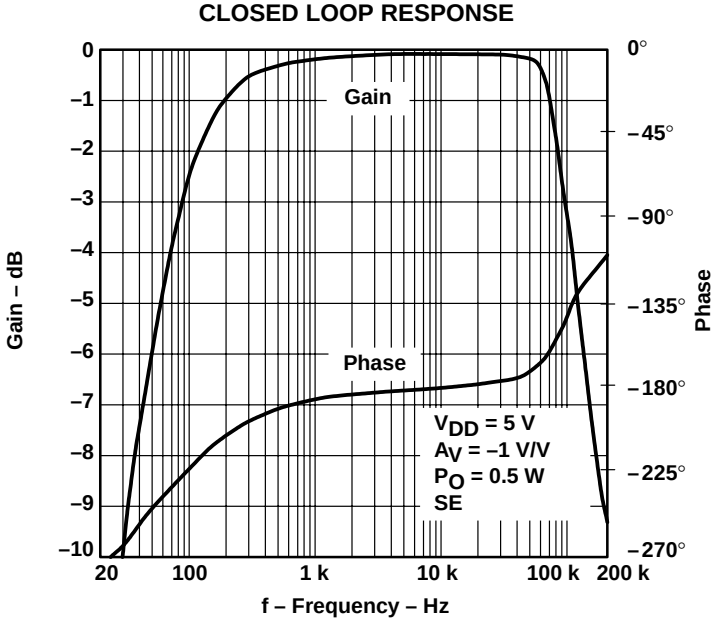


Figure 47

TYPICAL CHARACTERISTICS

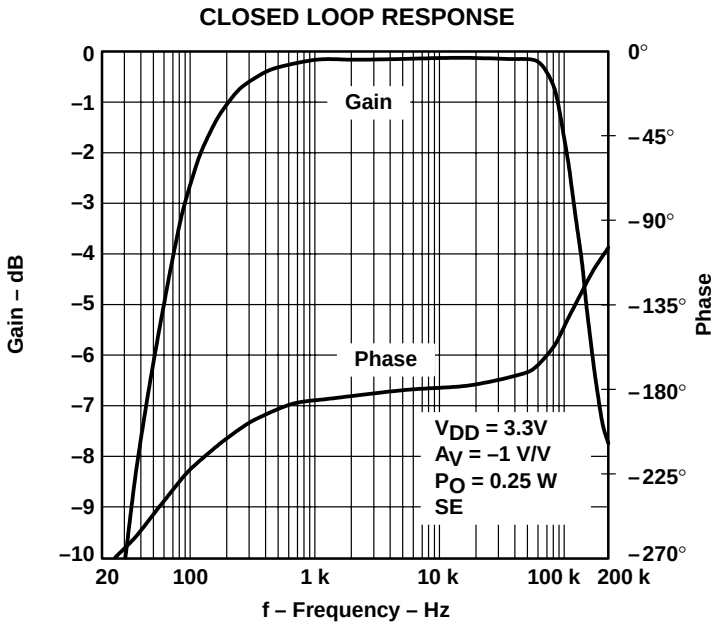


Figure 48

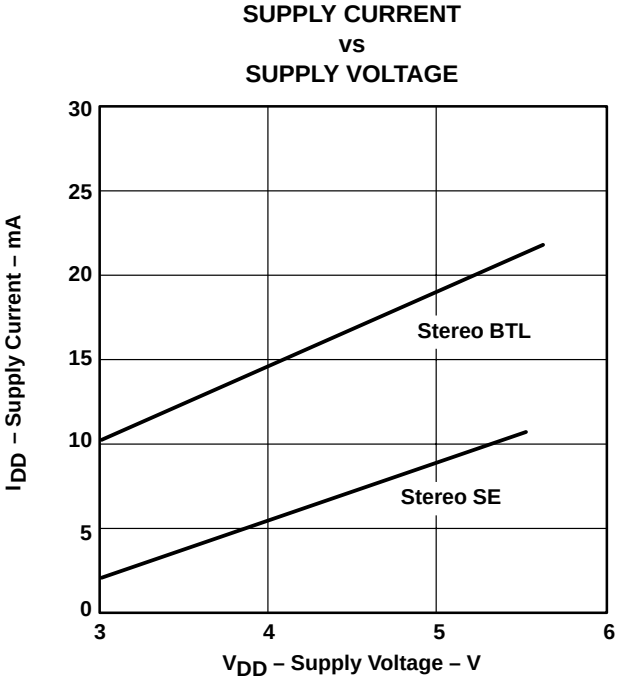


Figure 49

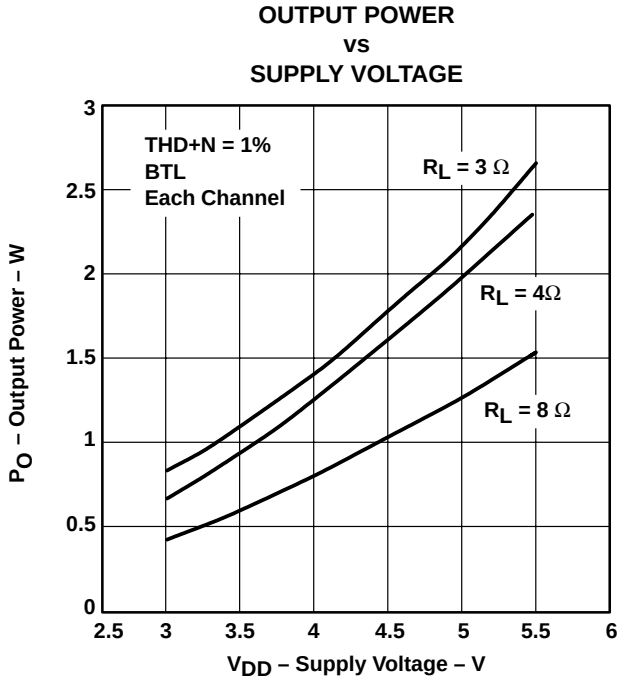


Figure 50

TYPICAL CHARACTERISTICS

OUTPUT POWER vs SUPPLY VOLTAGE

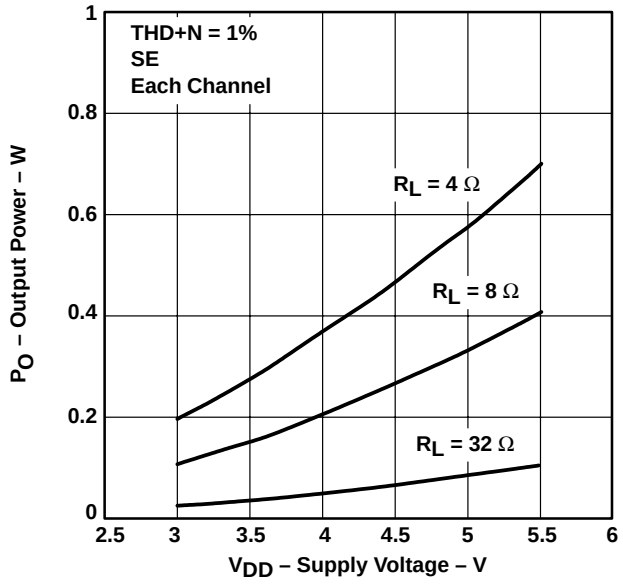


Figure 51

OUTPUT POWER vs LOAD RESISTANCE

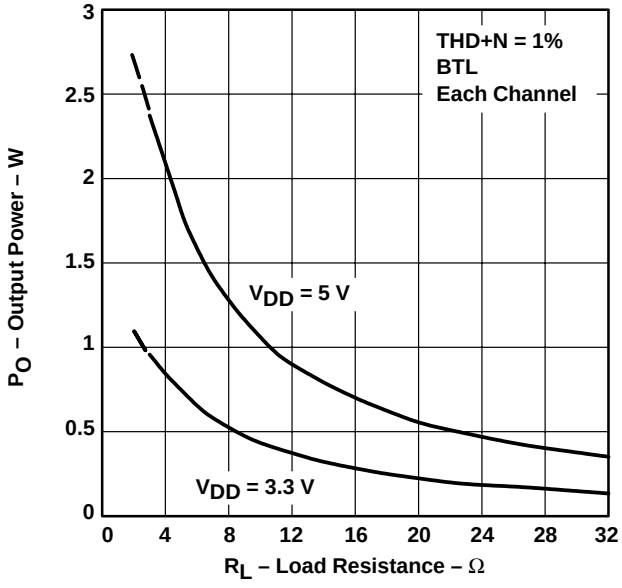


Figure 52

OUTPUT POWER vs LOAD RESISTANCE

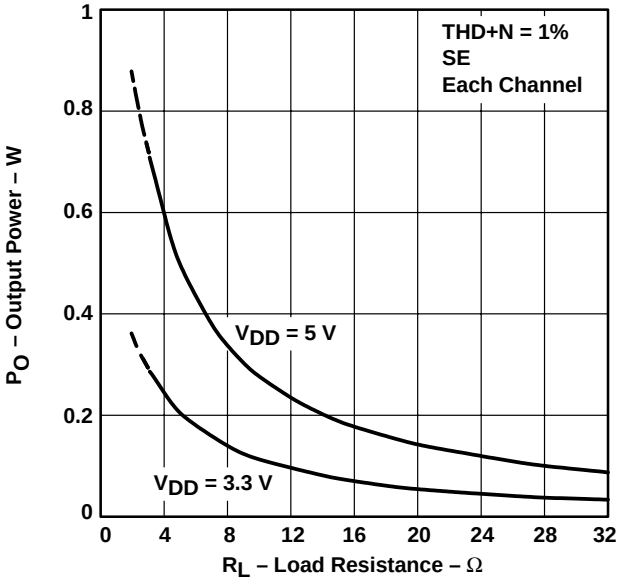


Figure 53

POWER DISSIPATION vs OUTPUT POWER

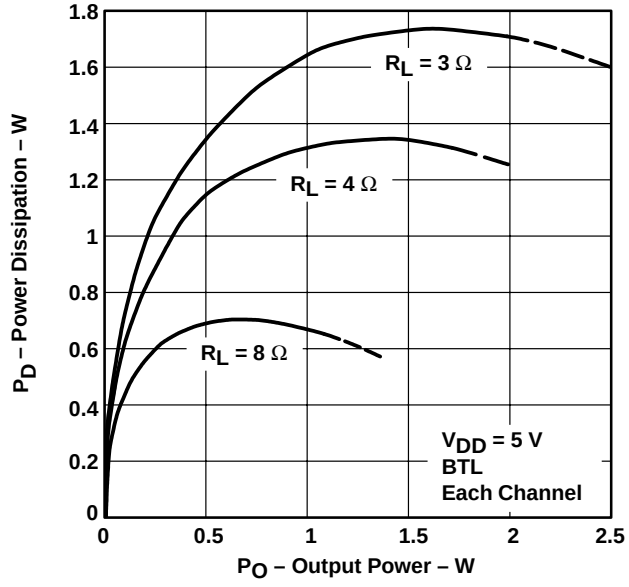


Figure 54

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs OUTPUT POWER

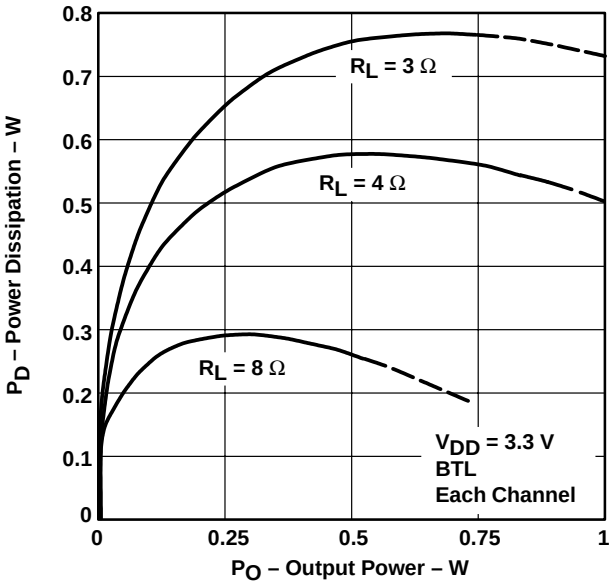


Figure 55

POWER DISSIPATION vs OUTPUT POWER

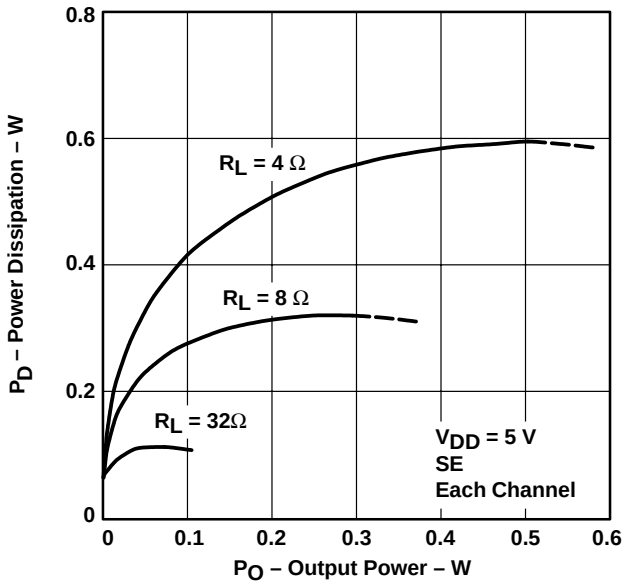


Figure 56

POWER DISSIPATION vs OUTPUT POWER

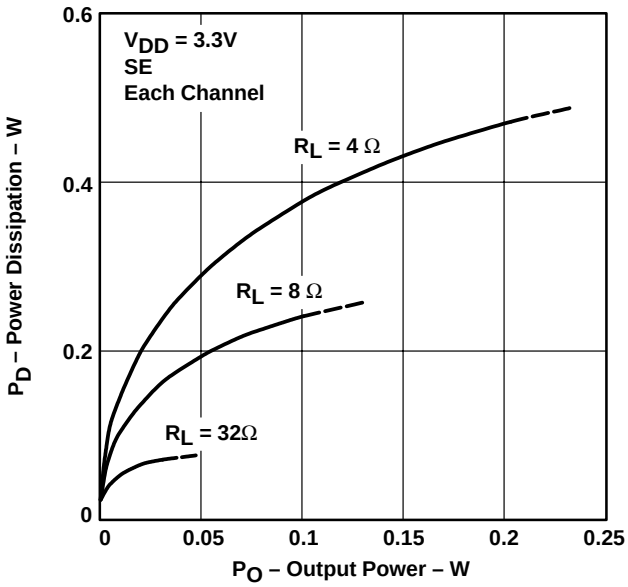


Figure 57

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface-mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

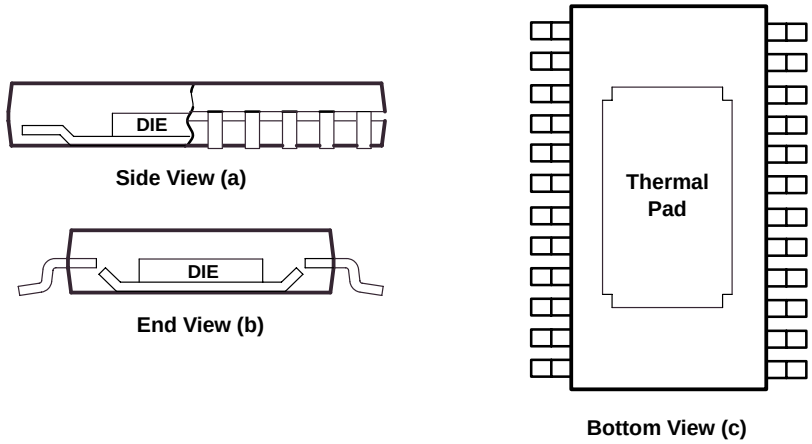


Figure 58. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0202 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (1)$$

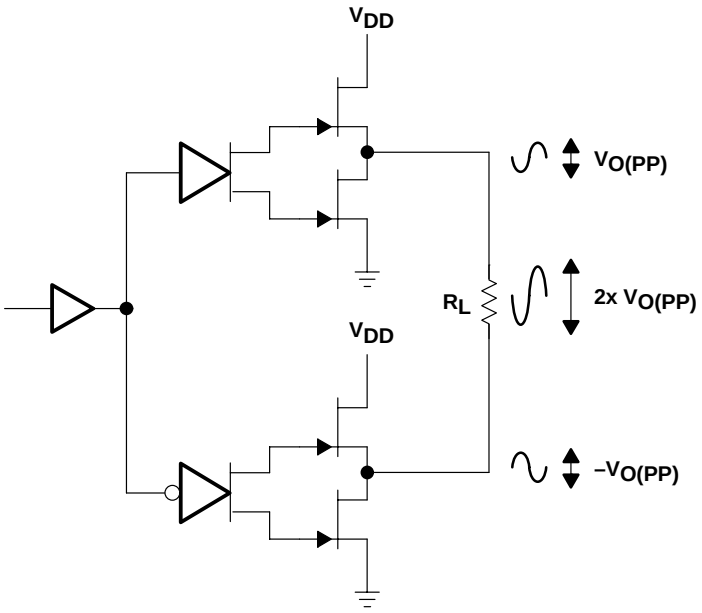


Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (2)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

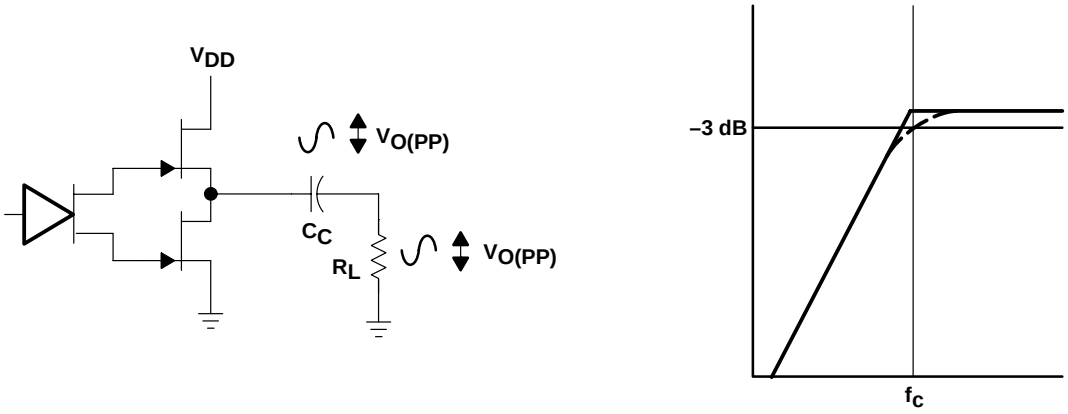


Figure 60. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).

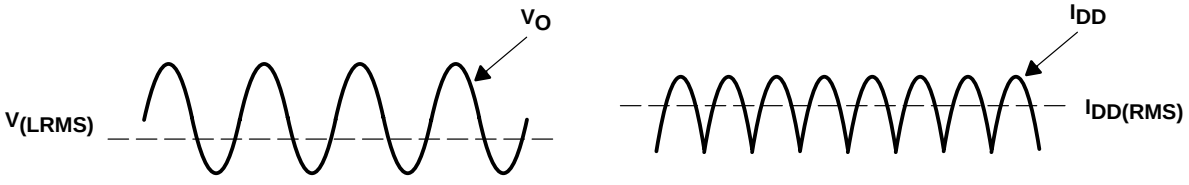


Figure 61. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

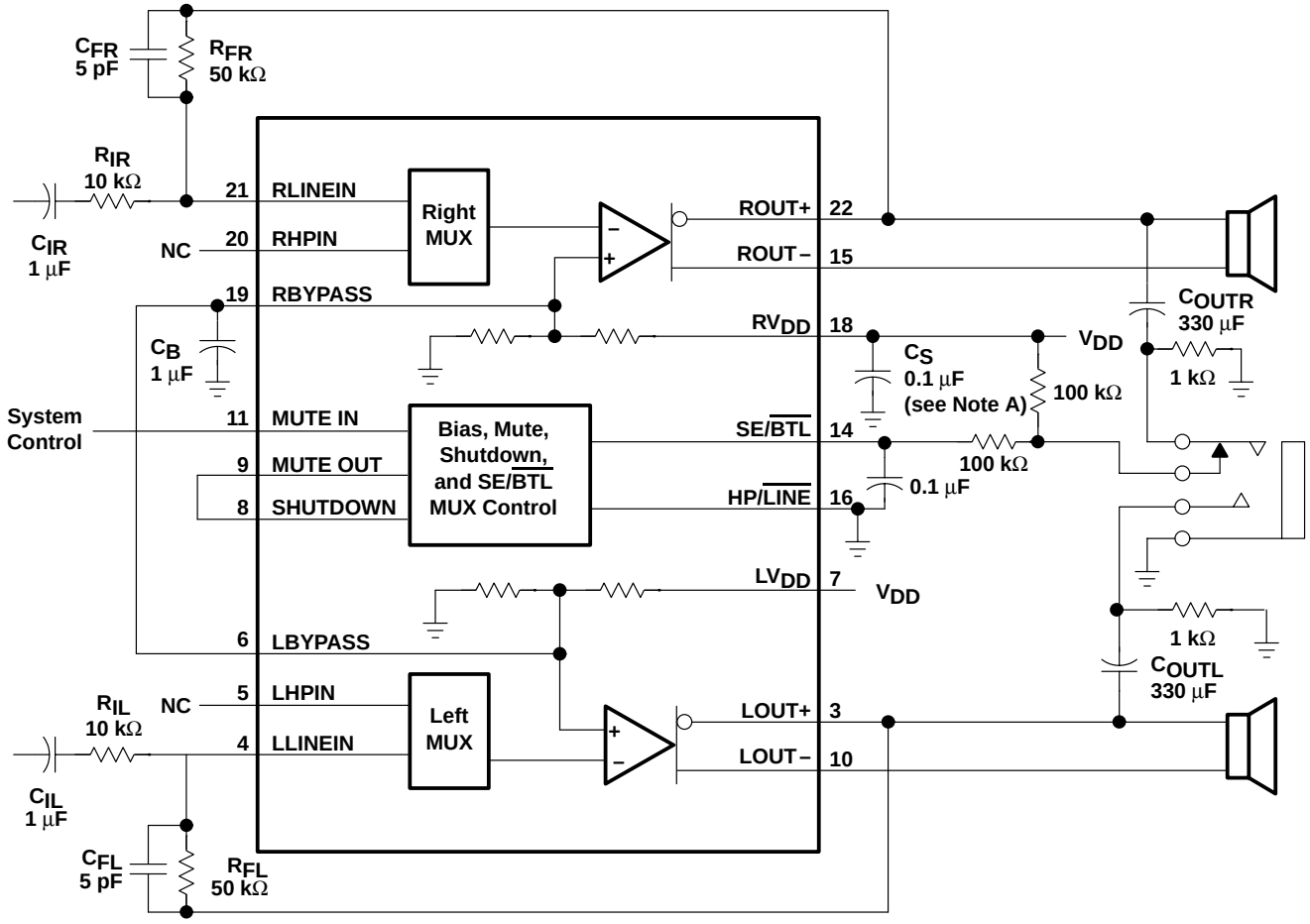
A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0202 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1, then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

selection of components

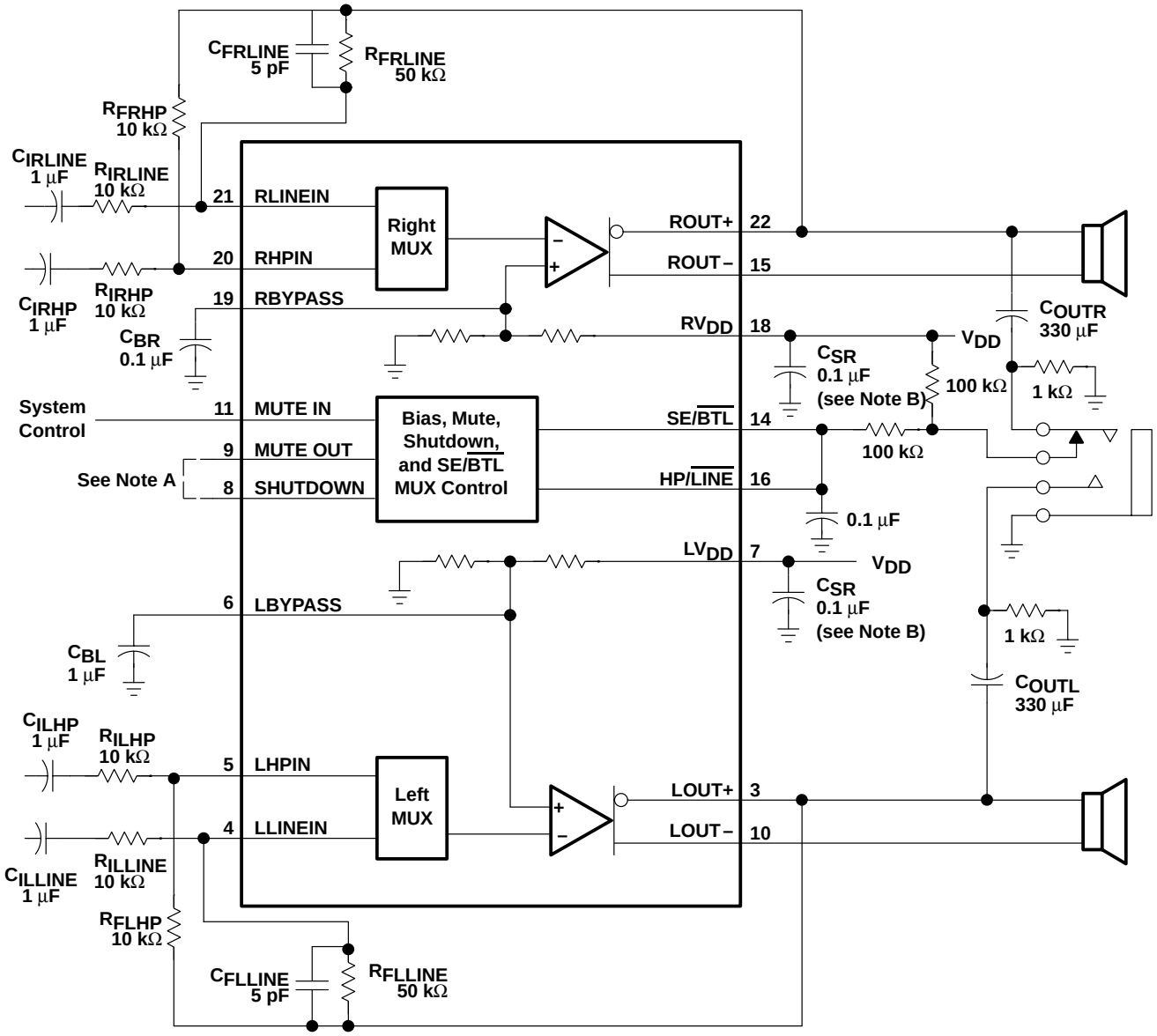
Figure 62 and Figure 63 are a schematic diagrams of a typical notebook computer application circuits.



NOTE A: A 0.1 μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

Figure 62. TPA0202 Minimum Configuration Application Circuit

APPLICATION INFORMATION



NOTES: A. This connection is for ultra-low current in shutdown mode.
B. A 0.1 μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

Figure 63. TPA0202 Full Configuration Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0202 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

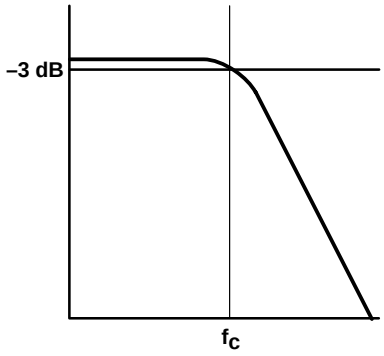
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0202 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{7}$$



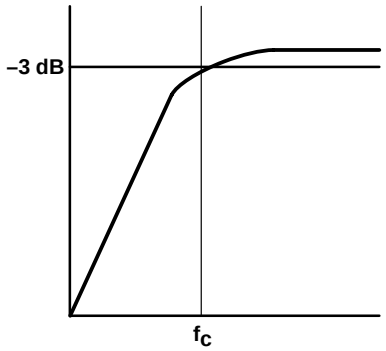
For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0202 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. The capacitor is fed from a 100-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{\left(C_B \times 100\ k\Omega\right)} \leq \frac{1}{C_I\left(R_I + R_F\right)} \tag{10}$$

As an example, consider a circuit where C_B is 1 μF, C_I is 0.22 μF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the equation 10 we get $10 \leq 75$, which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

In Figure 63, the full feature configuration, two bypass capacitors are used. This provides the maximum separation between right and left drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used as shown in Figure 62. It is critical that terminals 6 and 19 be tied together in this configuration.

load considerations

Extremely low impedance loads (below 4 Ω) coupled with certain external component selections, board layouts, and cabling can cause oscillations in the system. Using a single air-cored inductor in series with the load eliminates any spurious oscillations that might occur. An inductance of approximately 1 μH has been shown to eliminate such oscillations. There are no special considerations when using 4 Ω and above loads with this amplifier.

optimizing depop operation

Circuitry has been included in the TPA0202 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. If high impedances are used for the feedback and input resistors, it is possible for the input capacitor to drift downwards from mid-rail during mute and shutdown. A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations, and to limit the size of the gain-setting resistors. The time constant of the input coupling capacitor (C_I) and the gain-setting resistors (R_I and R_F) needs to be shorter than the time constant formed by the bypass capacitor (C_B) and the output impedance of the mid-rail generator, which is nominally 100 kΩ (see equation 10).

The effective output impedance of the mid-rail generator is actually greater than 100 kΩ due to a PNP transistor clamping the input node (see Figure 64).

APPLICATION INFORMATION

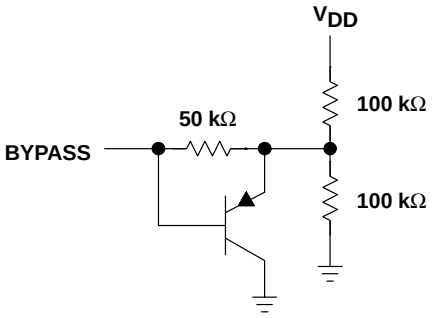


Figure 64. PNP Transistor Clamping of BYPASS Terminal

The PNP transistor limits the voltage drop across the 50 kΩ resistor by slewing the internal node slowly when power is applied. At start-up, the xBYPASS capacitor is at 0. The PNP is pulling the mid-point of the bias circuit down, so the capacitor sees a lower effective voltage, and thus charges slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

If the expression in equation 10 cannot be fulfilled or the small amount of pop is still unacceptable for the application, then external circuitry must be added that can eliminate the pop heard during power up and while transitioning out of mute or shutdown modes.

By holding the device in SE mode when the pop normally occurs, no pop can be heard through the BTL-connected speakers (as the negative output is in a high impedance state when the amplifier is in SE mode).

From a hardware point of view, the easiest way to implement this is to drive the SE/BTL terminal from the general-purpose input-output (GPIO) in the system. If the SE/BTL terminal is normally connected to a headphone socket (as shown in Figure 65), then the GPIO signal must either be taken through an OR gate (see Figure 65) or isolated with a diode (any signal diode) (see Figure 66).

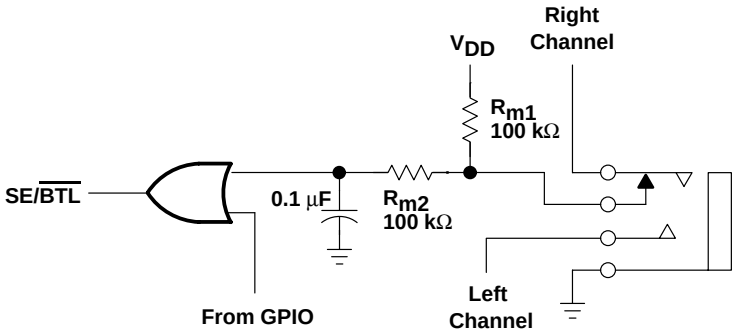


Figure 65. Implementation with an OR Gate

APPLICATION INFORMATION

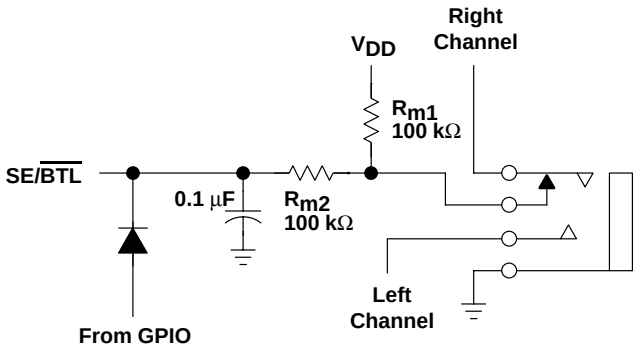


Figure 66. Implementation with a Diode

The OR gate and diode isolate the GPIO terminal from the headphone switch. In these implementations, the headphone switch has priority.

When the amplifier is in mute mode, the output stage continues to be biased. This causes the transition out of mute mode to be very fast with only a short delay (from 100 ms to 500 ms). During power up or the transition out of shutdown mode, a longer delay (from 1 s to 2 s) is required. The exact delay time required is dependent on the values of the external components used with the amplifier (see Figure 67).

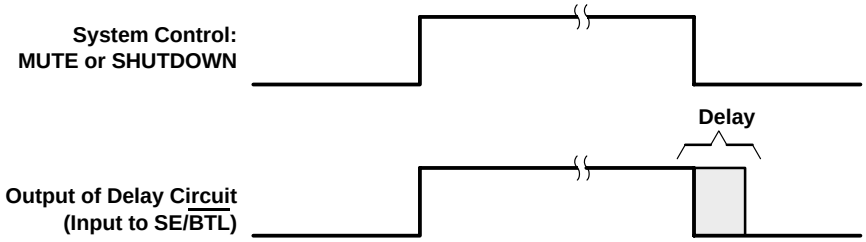


Figure 67. Transition Delay Timing

single-ended operation

In SE mode (see Figure 59 and Figure 60), the load is driven from the primary amplifier output for each channel (OUT+, terminals 22 and 3).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship (see equation 12):

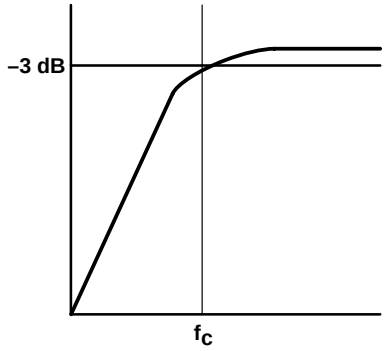
$$\frac{1}{\left(C_B \times 25\ k\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \lll \frac{1}{R_L C_C} \tag{12}$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 14.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (14)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
3 Ω	330 μF	161 Hz
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
10,000 Ω	330 μF	0.05 Hz
47,000 Ω	330 μF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0202 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0202, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 14) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 10 and 15). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0202 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0202 as an SE driver from LOUT+ and ROUT+ (terminals 3 and 22). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 68.

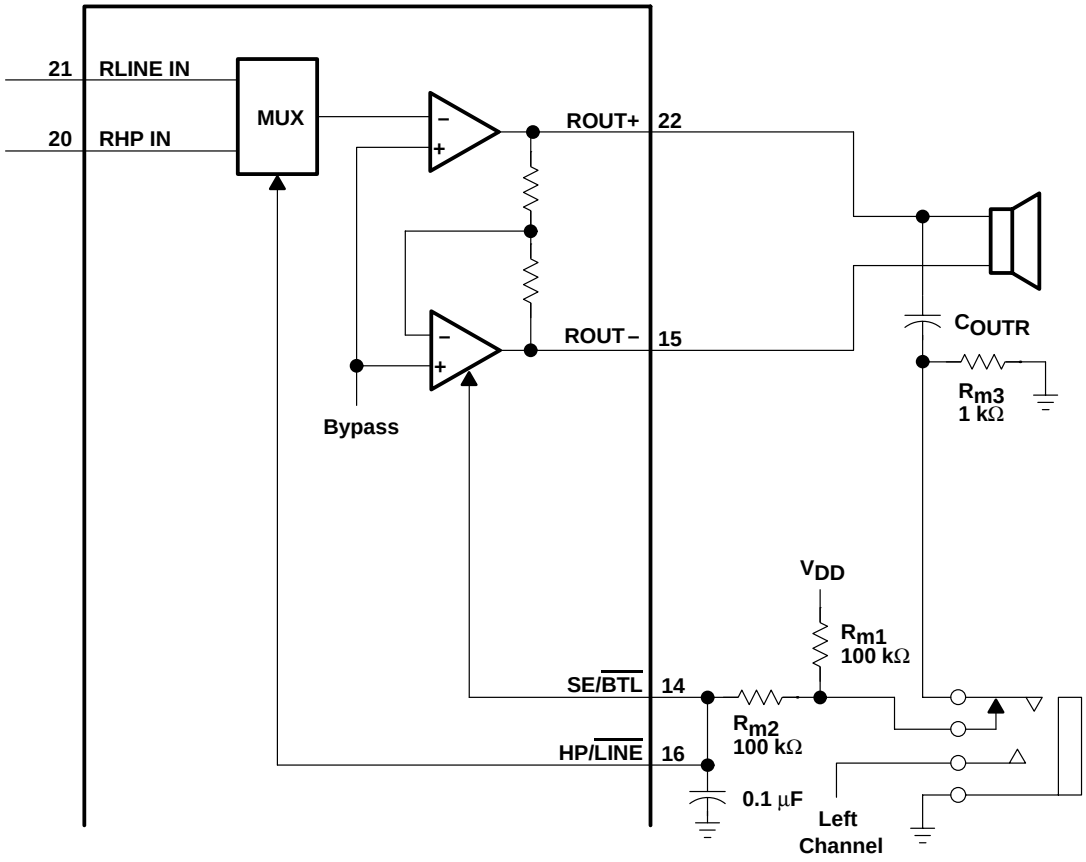


Figure 68. TPA0202 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

As shown in the full feature application (Figure 63), the input MUX control can be tied to the SE/$\overline{\text{BTL}}$ input. The benefits of doing this are described in the following input MUX operation section.

APPLICATION INFORMATION

Input MUX operation

Working in concert with the SE/$\overline{\text{BTL}}$ feature, the HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 69). The primary function of the MUX is to allow different gain settings for BTL versus SE mode. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{SE Gain}_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \quad (15)$$

If, for example $R_{I(HP)}$ = 10 kΩ and $R_{F(HP)}$ = 10 kΩ then $\text{SE Gain}_{(HP)}$ = –1

$$\text{BTL Gain}_{(LINE)} = -2\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \quad (16)$$

If, for example $R_{I(LINE)}$ = 10 kΩ and $R_{F(LINE)}$ = 50 kΩ then $\text{BTL Gain}_{(LINE)}$ = –10

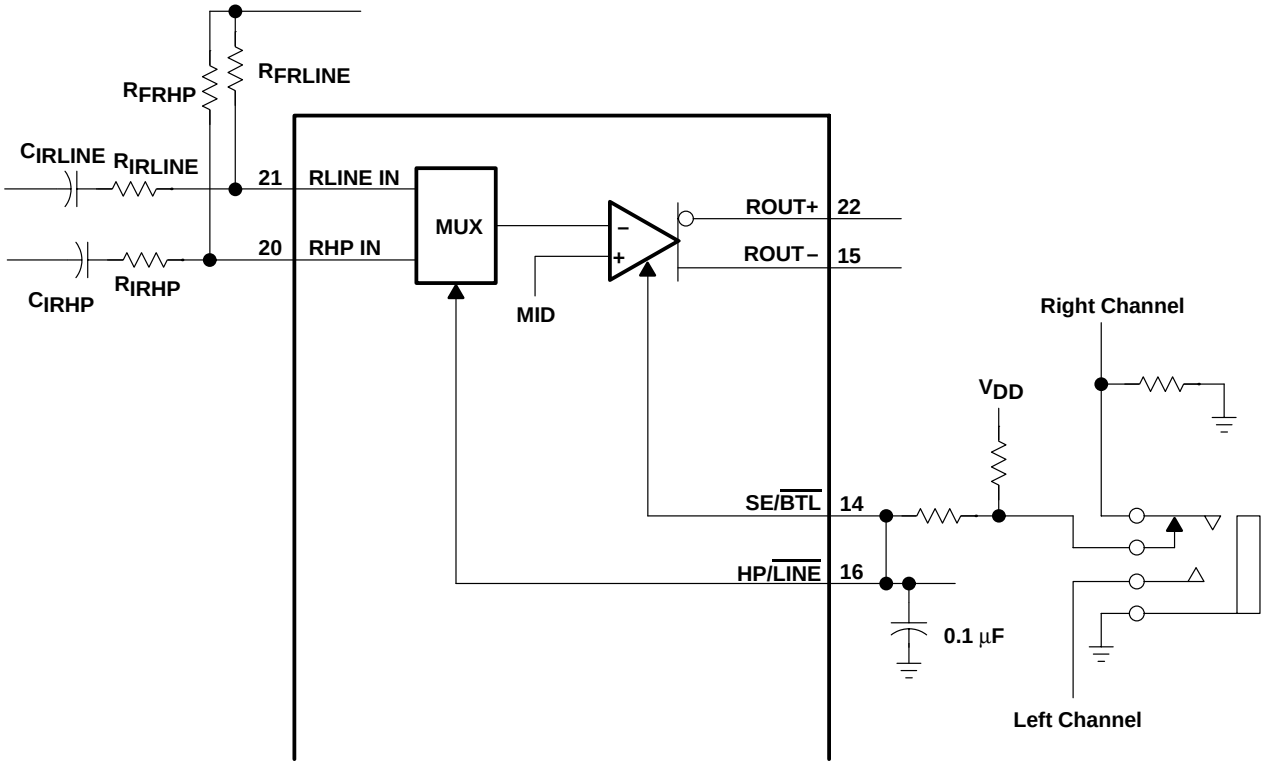


Figure 69. TPA0202 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

APPLICATION INFORMATION

mute and shutdown modes

The TPA0202 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 5 μA. SHUTDOWN or MUTE IN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces I_{DD} to 1.5 mA.

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0202 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0202 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications to improve the efficiency.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0202 data sheet, one can see that when the TPA0202 is operating from a 5-V supply into a 3-Ω speaker that 2 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\,\mathrm{Log}\left(\frac{P_W}{P_{ref}}\right) \quad (17)$$
$$= 10\,\mathrm{Log}\left(\frac{2}{1}\right)$$
$$= 3.0\ \mathrm{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

3.0 dB − 15 dB = − 12 dB (15 dB headroom)
3.0 dB − 12 dB = − 9 dB (12 dB headroom)
3.0 dB − 9 dB = − 6 dB (9 dB headroom)
3.0 dB − 6 dB = − 3 dB (6 dB headroom)
3.0 dB − 3 dB = 0 dB (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (18)$$
$$= 63\ \mathrm{mW}\ (15\ \mathrm{dB\ headroom})$$
$$= 120\ \mathrm{mW}\ (12\ \mathrm{dB\ headroom})$$
$$= 250\ \mathrm{mW}\ (9\ \mathrm{dB\ headroom})$$
$$= 500\ \mathrm{mW}\ (6\ \mathrm{dB\ headroom})$$
$$= 1000\ \mathrm{mW}\ (3\ \mathrm{dB\ headroom})$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0202 and maximum ambient temperatures is shown in Table 4.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

Table 4. TPA0202 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2	2 W	1.7	–3°C
2	1000 mW (3 dB)	1.6	6°C
2	500 mW (6 dB)	1.4	24°C
2	250 mW (9 dB)	1.1	51°C
2	120 mW (12 dB)	0.8	78°C
2	63 mW (15 dB)	0.6	96°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP‡	2.8 W	22.1 mW/°C	1.8 W	1.4 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 22 mW/°C and 54 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

For 0 CFM :

$$= \frac{1}{0.022}$$

$$= 45°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0202 is 150 °C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (20)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB headroom, 0 CFM)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB headroom per channel.

Table 4 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0202 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

junction temperature measurement

Characterizing a PCB layout with respect to thermal impedance is very difficult, as it is usually impossible to know the junction temperature of the IC in question. The TPA0202 terminal 2 (TJ) sources a current proportional to the junction temperature. The circuit internal to TJ is shown in Figure 70.

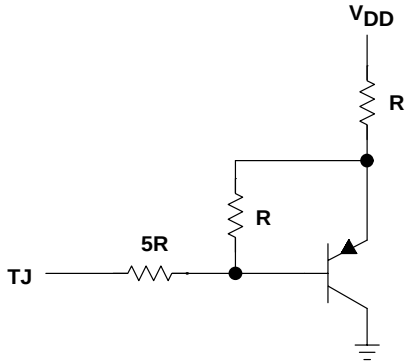


Figure 70. TJ Terminal Internal Circuit

Connect an ammeter between TJ and ground to measure the current. As the resistors have a tolerance of ±20%, this measurement must be calibrated on each device. The intent of this function is in characterization of the PCB and end equipment and not a real-time measurement of temperature. Typically a 25°C reading is –120 μA for a 3.3-V supply and –135 μA for a 5-V supply. The slope is approximately 0.25 μA/°C for both V_{DD} = 3.3 V and V_{DD} = 5 V. To reduce quiescent current, do not ground TJ in normal operation. It can be connected to V_{DD} or left floating as it has a resistor connected across the base-emitter junction.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA0202PWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-	TPA0202
TPA0202PWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPA0202PWP	TPA0202
TPA0202PWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	TPA0202
TPA0202PWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPA0202PWPR	TPA0202

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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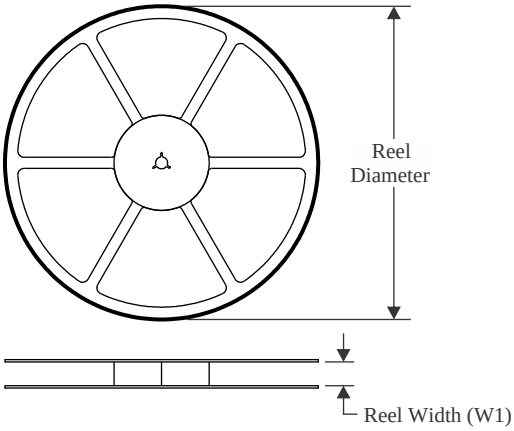
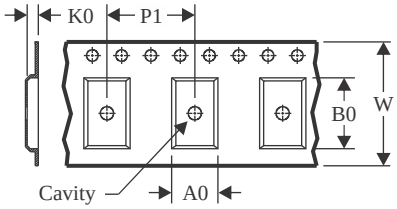
TAPE AND REEL INFORMATION

REEL DIMENSIONS

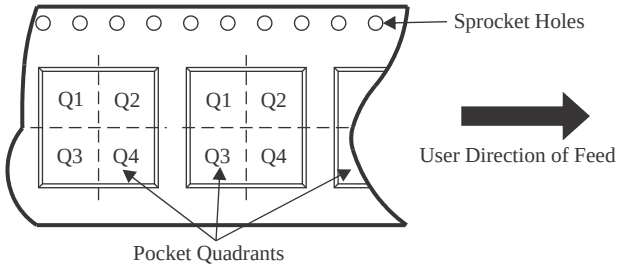


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

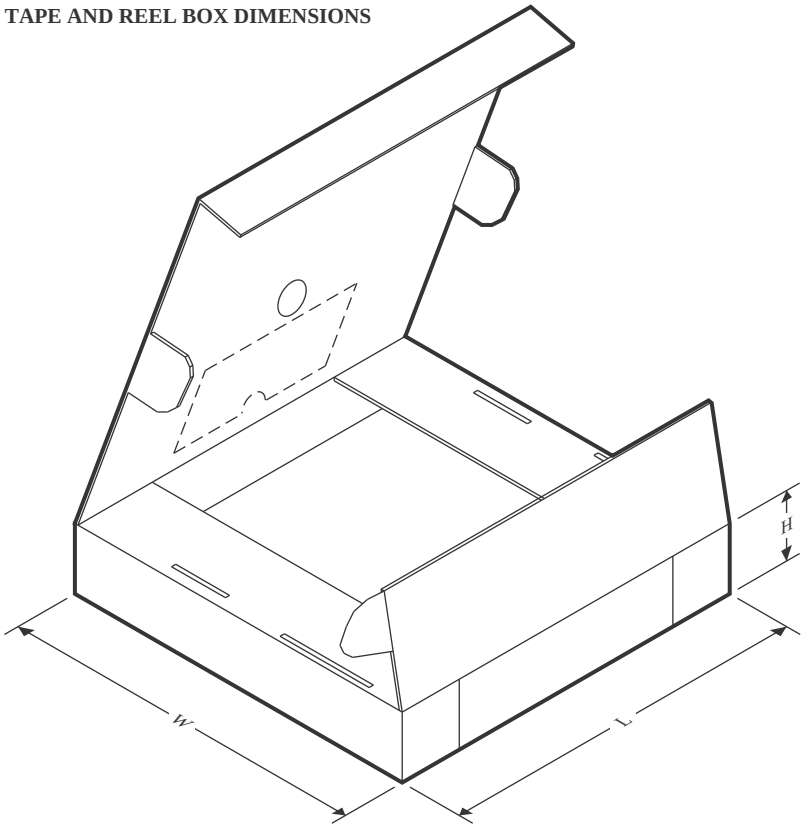
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0202PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

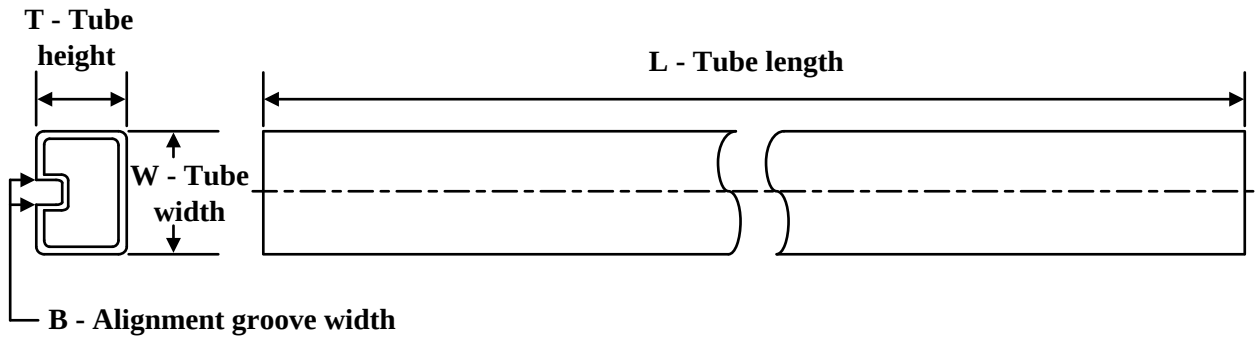
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0202PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA0202PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPA0202PWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

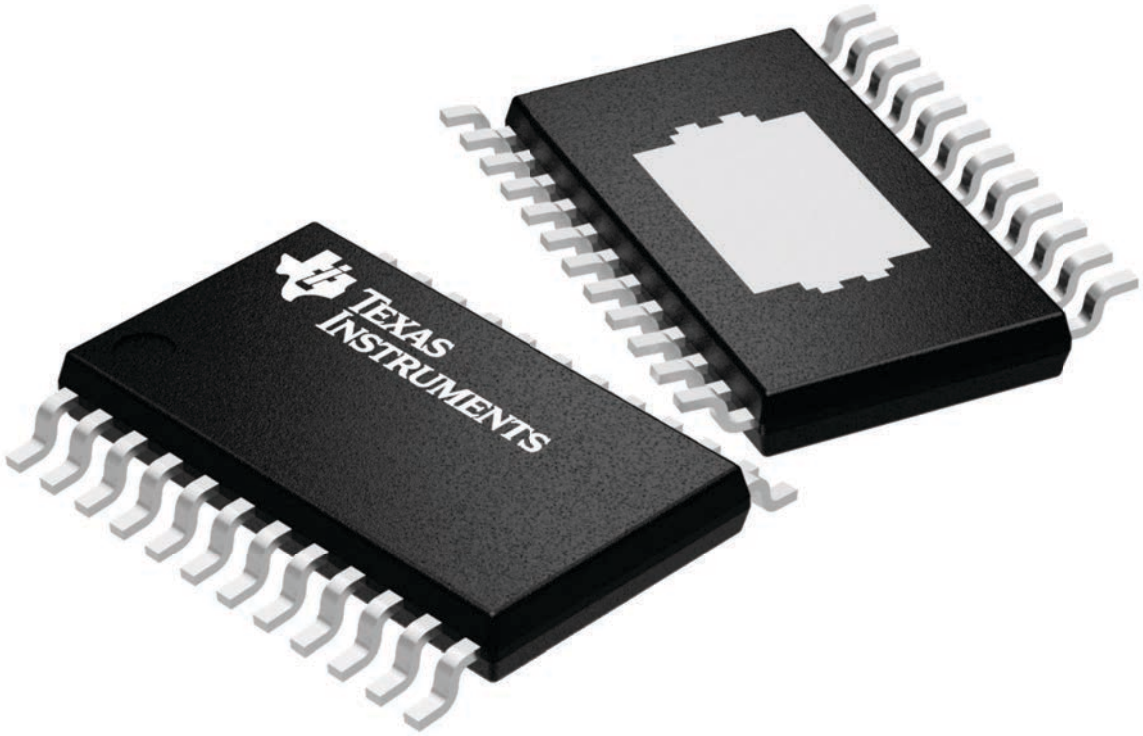
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

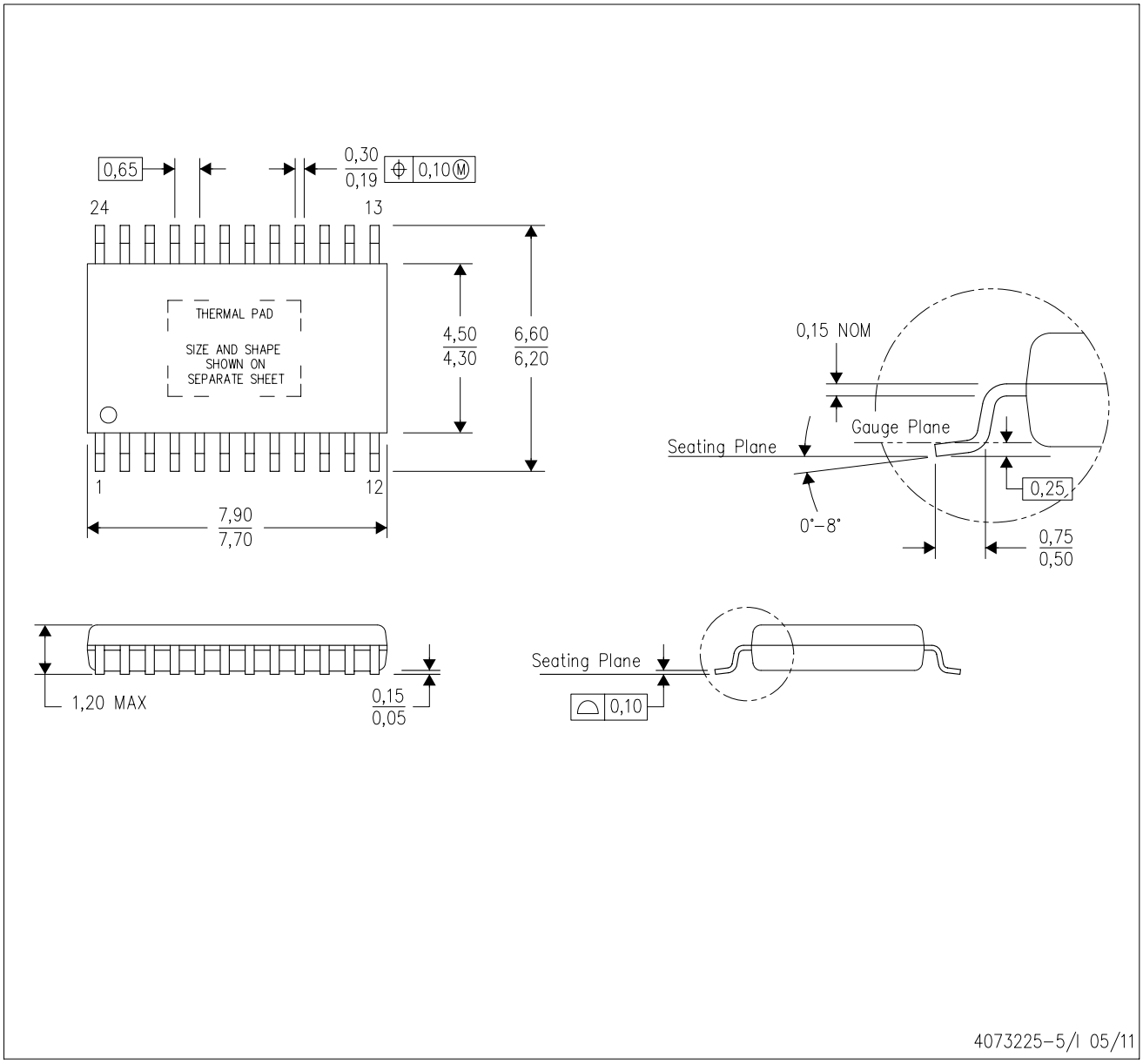
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

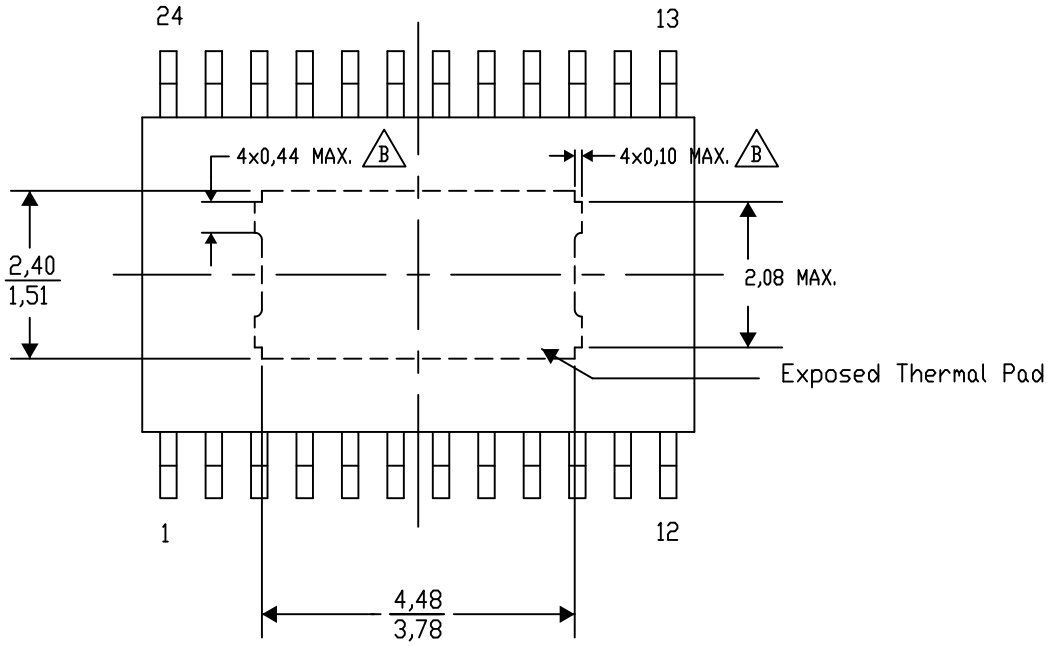
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–42/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

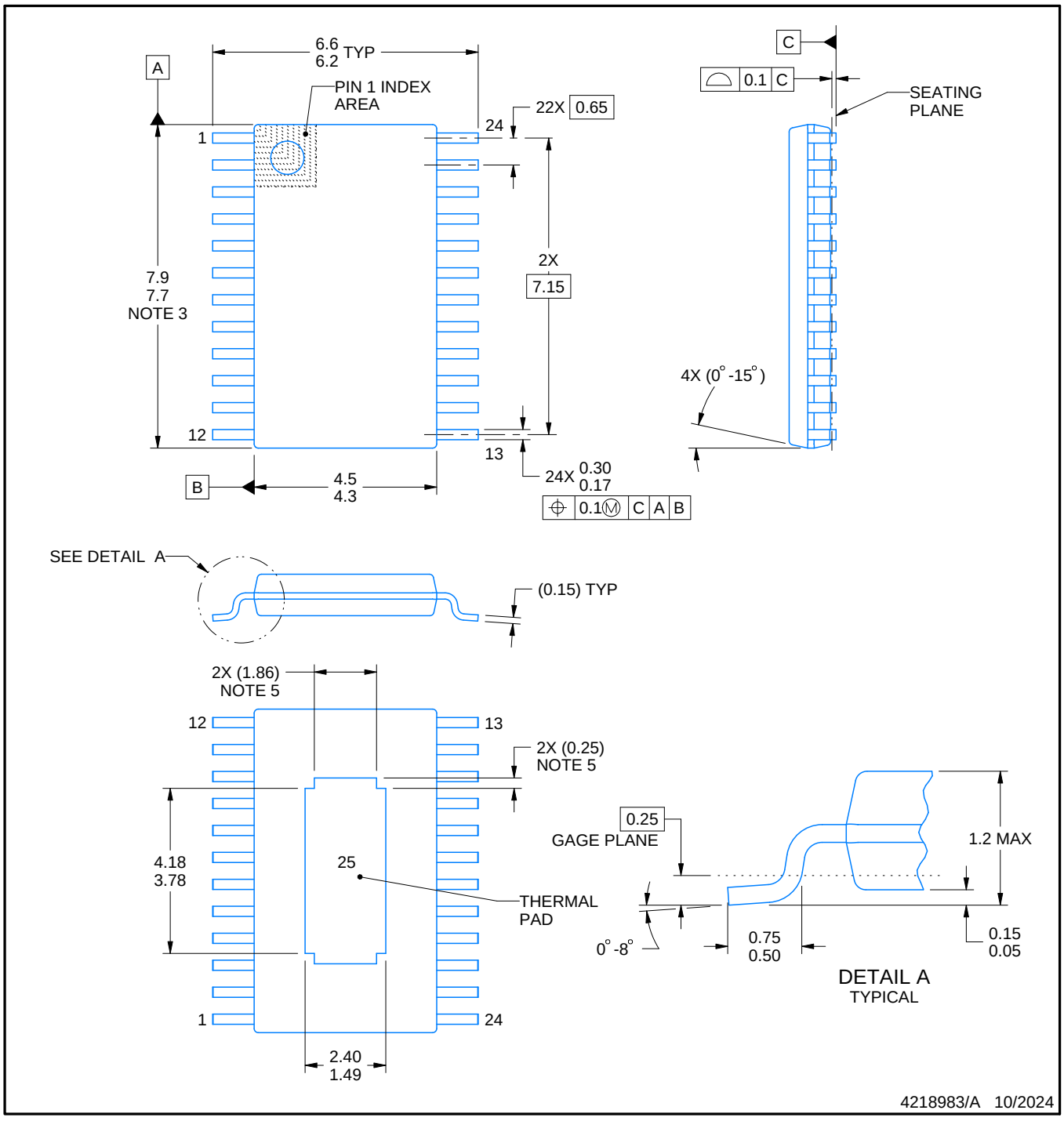
PowerPAD is a trademark of Texas Instruments

PACKAGE OUTLINE

PWP0024A

PowerPAD™ TSSOP - 1.2 mm max height

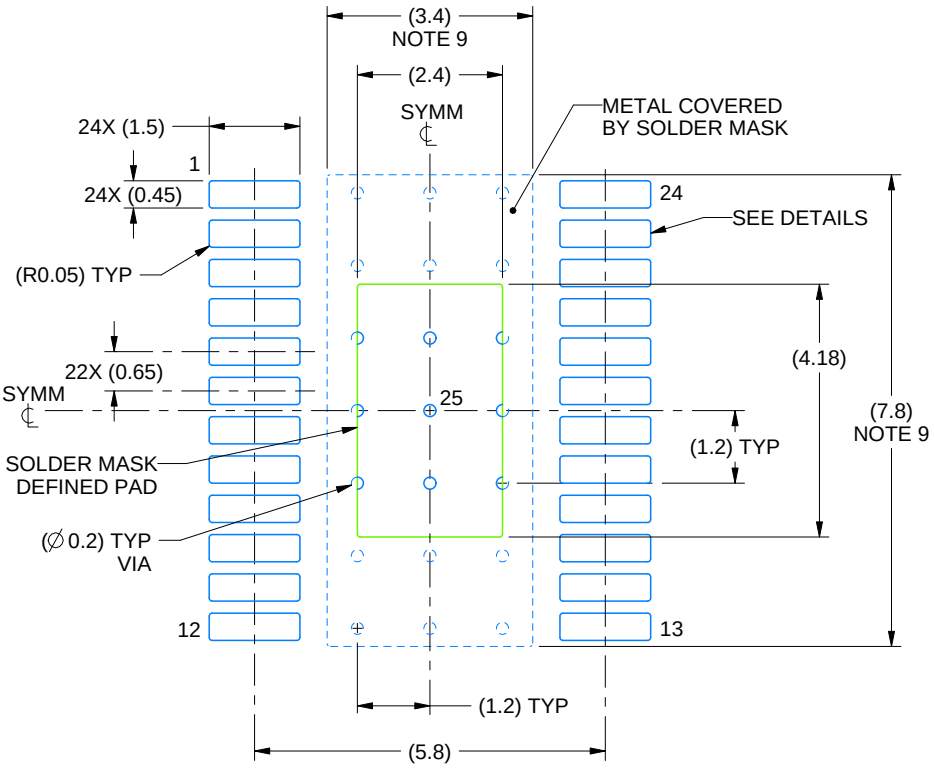
SMALL OUTLINE PACKAGE



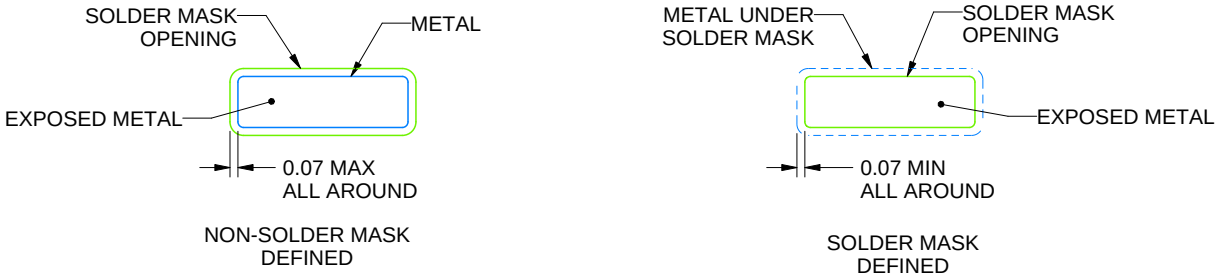
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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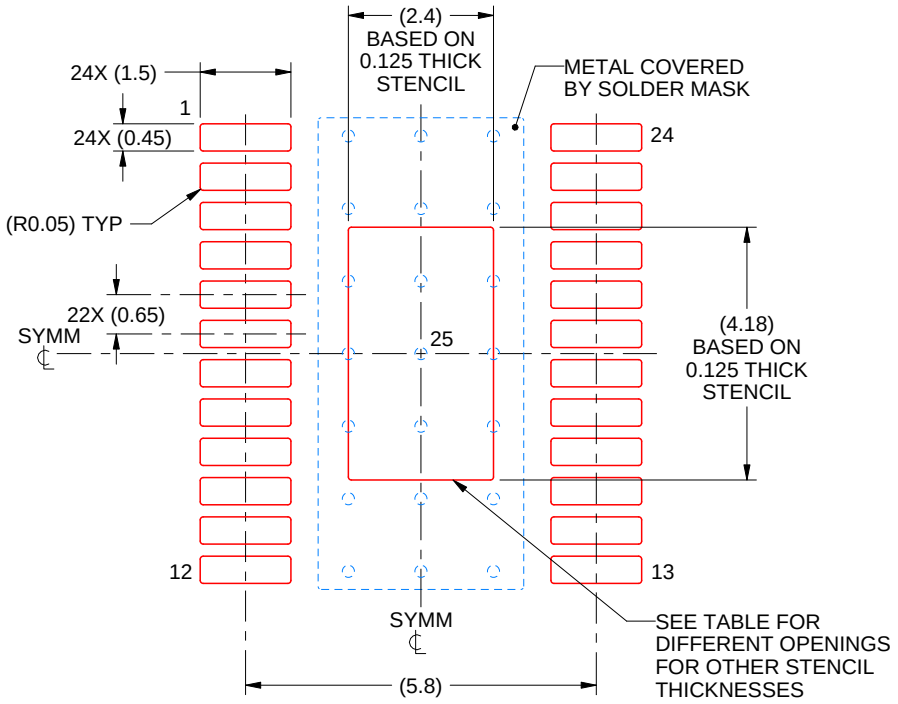
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 4.67
0.125	2.40 X 4.18 (SHOWN)
0.15	2.19 X 3.82
0.175	2.03 X 3.53

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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