

## TLV61224 采用 6 引脚 SC-70 封装的单节高效升压转换器

### 1 特性

- 典型工作条件下的效率高达 94%
- 5 $\mu$ A 静态电流
- 工作输入电压范围：0.7V 至 3V
- 关断条件下具有导通功能
- 12V 输入下的输出电流大于 40mA
- 典型开关电流的额定值为 400 mA
- 输出过压保护
- 过热保护
- 3V 固定输出电压
- 小型 6 引脚 SC-70 封装

### 2 应用

- 电池供电类应用
  - 1 至 2 节镍氢或碱性电池
  - 1 节锂原电池
- 消费类及便携式医疗产品
- 个人护理产品

### 3 说明

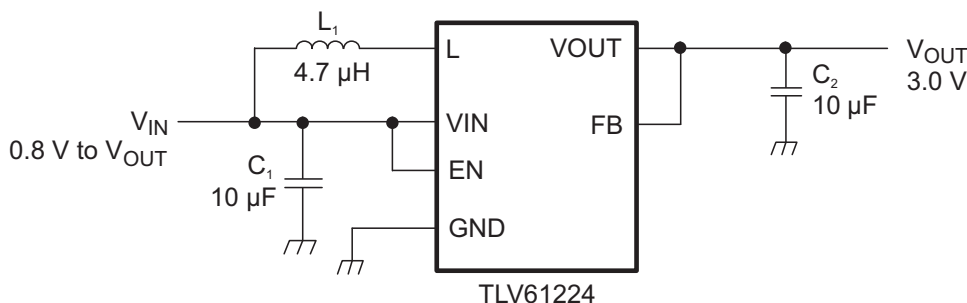
该 TLV61224 器件可以为由 1 节/2 节碱性或镍氢电池或 1 节锂原电池供电的产品提供电源解决方案。可实现的输出电流取决于输入输出电压比。升压转换器建立在采用同步整流的磁滞控制器拓扑基础之上，能够以最少的静态电流实现最高的效率。该器件可在内部设置 3V 固定输出电压。转换器可通过特有的使能引脚关断。在关断过程中，耗电量降至最低。该器件采用 2mm x 2mm 6 引脚 SC-70 封装 (DCK) 实现小型电路布局。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TLV61224	SOT (6)	2.00mm x 1.25mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型应用电路原理图



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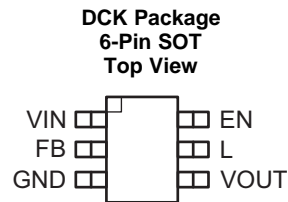
## 4 修订历史记录

### Changes from Original (March 2011) to Revision A

**Page**

- |   |                 |
|---|-----------------|
| <ul style="list-style-type: none"> <li>• 已添加 ESD 额定值表, 特性描述部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 .....</li> </ul> | <p><b>1</b></p> |
|---|-----------------|

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input (1: enabled, 0: disabled). Must be actively tied high or low.
FB	2	I	Output voltage sense input. Must be connected to $V_{OUT}$ .
GND	3	–	Control / logic and power ground
L	5	I	Connection for Inductor
VIN	1	I	Boost converter input voltage
VOUT	4	O	Boost converter output voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VIN, L, VOUT, EN, FB	–0.3	7.5	V
Temperature	Operating junction temperature, T <sub>J</sub>	–40	150	°C
	Storage, T <sub>stg</sub>	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	
	Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply voltage at VIN	0.7		3	V
T <sub>A</sub>	Operating free air temperature	–40		85	°C
T <sub>J</sub>	Operating virtual junction temperature	–40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV61224	UNIT
		DCK (SOT)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	231.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	55.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	77.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	76.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

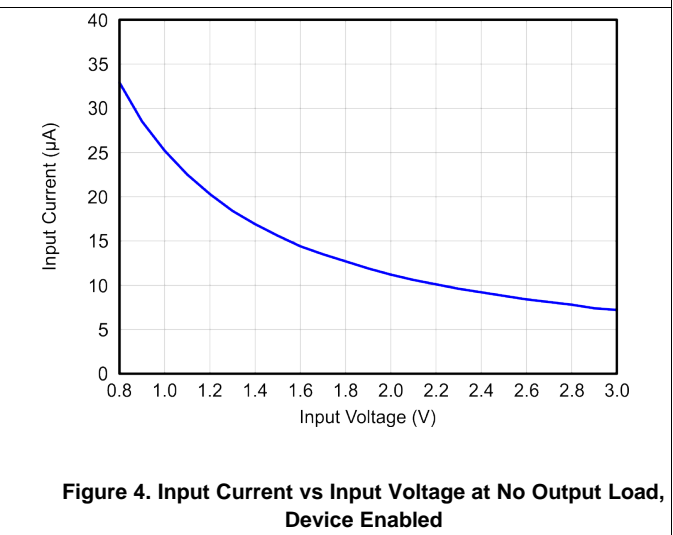
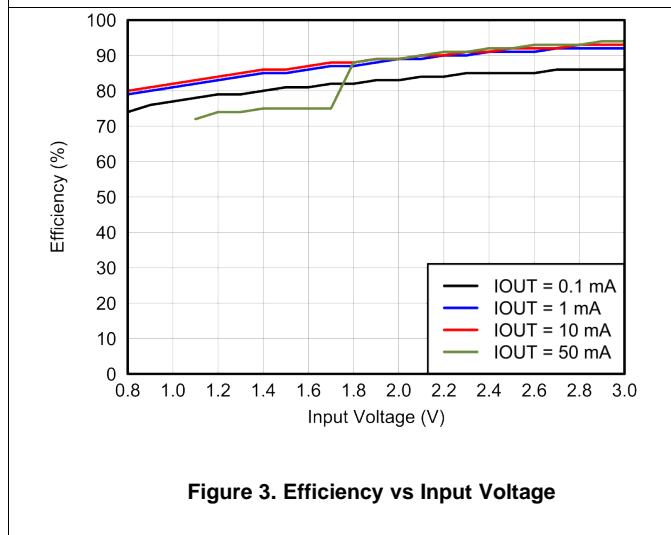
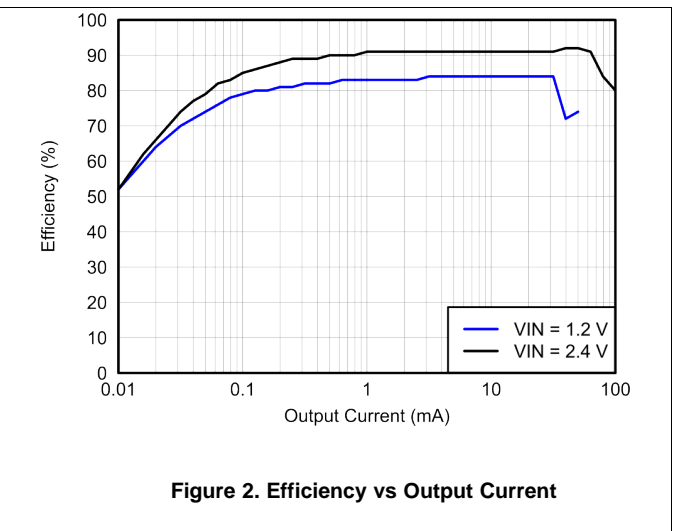
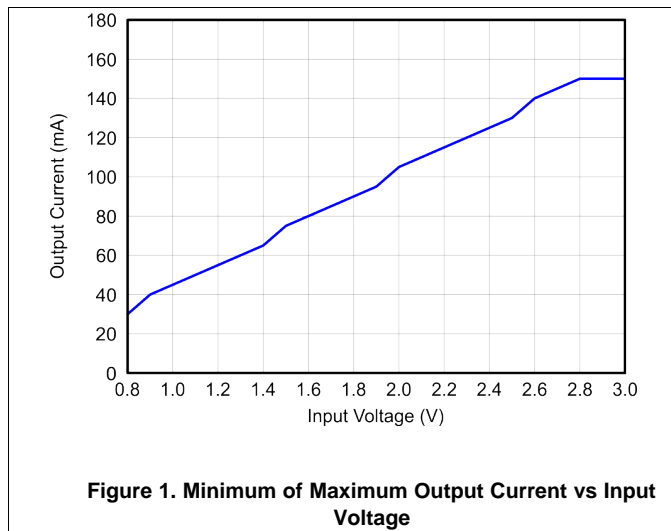
over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

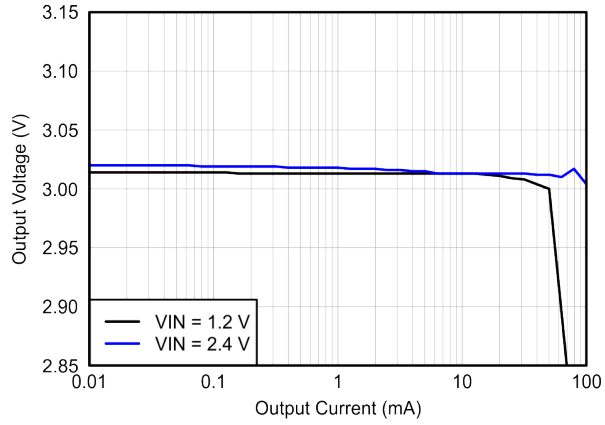
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC-DC STAGE</b>						
$V_{IN}$	Input voltage range		0.7		3	V
$V_{IN}$	Maximum minimum input voltage for start-up	$R_{Load} \geq 150 \Omega$ , $T_A = 25^\circ\text{C}$		0.7		V
$V_{OUT}$	TLV61224 output voltage	$V_{IN} < V_{OUT}$	2.85	3	3.15	V
$I_{LH}$	Inductor current ripple			200		mA
$I_{SW}$	switch current limit	$V_{OUT} = 3 \text{ V}$ , $V_{IN} = 1.2 \text{ V}$	160	400		mA
$R_{DSon\_HSD}$	Rectifying switch ON-resistance	$V_{OUT} = 3 \text{ V}$		1000		m $\Omega$
$R_{DSon\_LSD}$	Main switch ON-resistance	$V_{OUT} = 3 \text{ V}$		600		m $\Omega$
	Line regulation	$V_{IN} < V_{OUT}$		0.5%		
	Load regulation	$V_{IN} < V_{OUT}$		0.5%		
$I_Q$	Quiescent current	$V_{IN}$	$I_O = 0 \text{ mA}$ , $V_{EN} = V_{IN} = 1.2 \text{ V}$ , $V_{OUT} = 3 \text{ V}$	0.5	1	$\mu\text{A}$
		$V_{OUT}$		5	10	
$I_{SD}$	Shutdown current	$V_{IN}$	$V_{EN} = 0 \text{ V}$ , $V_{IN} = 1.2 \text{ V}$ , $V_{OUT} \geq V_{IN}$	0.2	1	$\mu\text{A}$
$I_{LKG\_VOUT}$	Leakage current into VOUT	$V_{EN} = 0 \text{ V}$ , $V_{IN} = 1.2 \text{ V}$ , $V_{OUT} = 3 \text{ V}$		1		$\mu\text{A}$
$I_{LKG\_L}$	Leakage current into L	$V_{EN} = 0 \text{ V}$ , $V_{IN} = 1.2 \text{ V}$ , $V_L = 1.2 \text{ V}$ , $V_{OUT} \geq V_{IN}$		0.01	0.7	$\mu\text{A}$
$I_{EN}$	EN input current	Clamped on GND or $V_{IN}$ ( $V_{IN} < 1.5 \text{ V}$ )		0.005	0.1	$\mu\text{A}$
<b>CONTROL STAGE</b>						
$V_{IL}$	Maximum EN input low voltage	$V_{IN} \leq 1.5 \text{ V}$	$0.2 \times V_{IN}$			V
$V_{IH}$	Minimum EN input high voltage	$V_{IN} \leq 1.5 \text{ V}$			$0.8 \times V_{IN}$	V
$V_{IL}$	Maximum EN input low voltage	$V_{IN} > 1.5 \text{ V}$		0.4		V
$V_{IH}$	Minimum EN input high voltage	$V_{IN} > 1.5 \text{ V}$		1.2		V
$V_{UVLO}$	Undervoltage lockout threshold for turnoff	$V_{IN}$ decreasing		500		mV
	Undervoltage lockout hysteresis			50		mV
	Overvoltage protection threshold		5.5		7.5	V
	Overtemperature protection			140		$^\circ\text{C}$
	Overtemperature hysteresis			20		$^\circ\text{C}$

## 6.6 Typical Characteristics

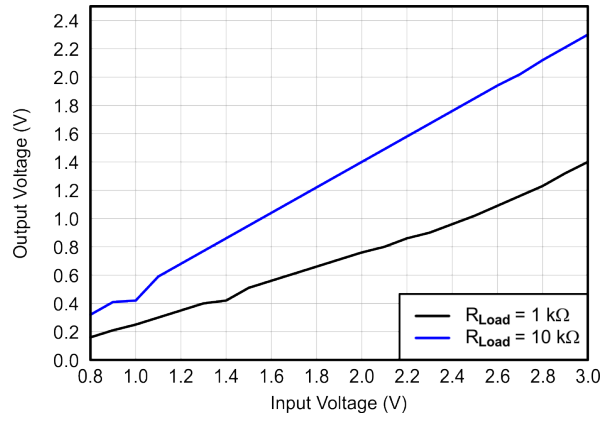
Table 1. Table of Graphs

		FIGURE
Minimum of Maximum Output Current	vs Input Voltage	Figure 1
Efficiency	vs Output Current, $V_{IN} = [1.2\text{ V}; 2.4\text{ V}]$	Figure 2
	vs Input Voltage, $I_{OUT} = [100\text{ }\mu\text{A}; 1\text{ mA}; 10\text{ mA}; 50\text{ mA}]$	Figure 3
Input Current	vs Input Voltage at No Output Load, Device Enabled	Figure 4
Output Voltage	vs Output Current, $V_{IN} = [1.2\text{ V}; 2.4\text{ V}]$	Figure 5
	vs Input Voltage, Device Disabled, $R_{LOAD} = [1\text{ k}\Omega; 10\text{ k}\Omega]$	Figure 6





**Figure 5. Output Voltage vs Output Current**



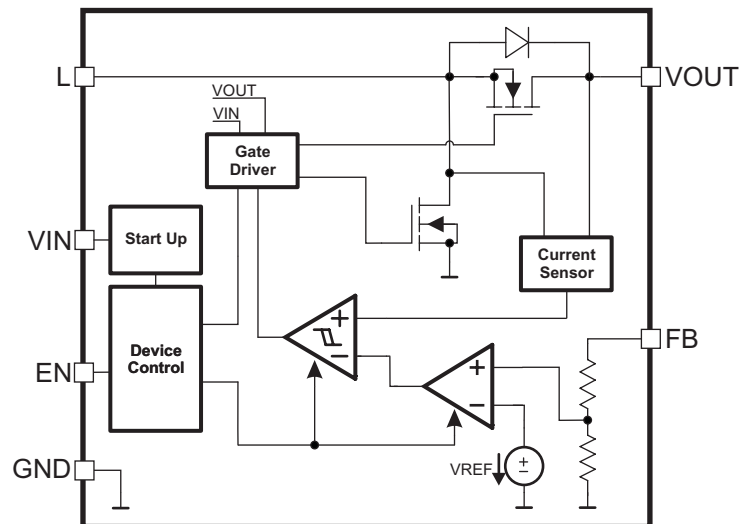
**Figure 6. Output Voltage vs input Voltage, Device Disabled**

## 7 Detailed Description

### 7.1 Overview

The TLV61224 device is a high-performance, high-efficient boost converter. To achieve high-efficiency, the power stage is implemented as a synchronous boost topology. Two actively controlled low  $R_{DS(on)}$  power MOSFETs are used to achieve power switching.

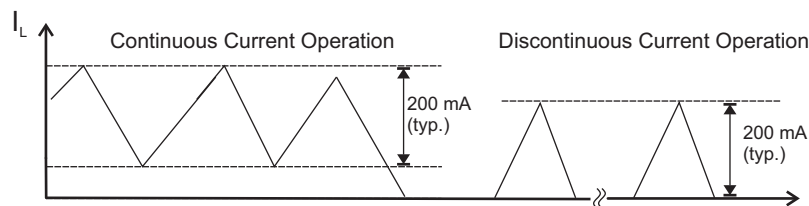
### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Controller Circuit

The device is controlled by a hysteretic current-mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current becomes discontinuous to keep the efficiency high at low-load conditions.



**Figure 7. Hysteretic Current Operation**

The output voltage  $V_{OUT}$  is monitored through the internal feedback network, which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.



## Feature Description (continued)

### 7.3.2 Start-up

After the EN pin is tied high, the device starts to operate. If the input voltage is not high enough to supply the control circuit properly, a start-up oscillator starts to operate the switches. During this phase the switching frequency is controlled by the oscillator and the maximum switch current is limited. As soon as the device has built up the output voltage to about 1.8 V (high enough for supplying the control circuit) the device switches to its normal hysteretic current mode operation. The start-up time depends on input voltage, load current, and output capacitance.

### 7.3.3 Operation at Output Overload

If the inductor current is in normal boost operation, the current reaches the internal switch current limit threshold. The main switch is turned off to stop a further increase of the input current.

In this case, the output voltage decreases because with limited input current it is no longer possible to provide sufficient power to the output to maintain the programmed output voltage.

If the output voltage drops below the input voltage, the back-gate diode of the rectifying switch gets forward-biased and current starts flowing through it. This diode cannot be turned off, so the current finally is only limited by the remaining DC resistances. As soon as the output load decreases to a value the converter can supply, the converter resumes normal operation providing the set output voltage.

### 7.3.4 Undervoltage Lockout

An implemented undervoltage lockout function (UVLO) stops the operation of the converter if the input voltage drops below the typical UVLO threshold. This function is implemented to prevent malfunctioning of the converter and protect batteries against deep discharge.

### 7.3.5 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore, overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the output voltage of the TLV61224 device is also monitored internally. If the output voltage of the device reaches the internally programmed threshold, the voltage amplifier regulates the output voltage to this value.

### 7.3.6 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC junction temperature. If the temperature exceeds the programmed threshold (see [Electrical Characteristics](#)), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. To prevent unstable operation close to the region of overtemperature threshold, a built-in hysteresis is implemented.

## 7.4 Device Functional Modes

### 7.4.1 Device Enable and Shutdown Mode

The device is enabled when EN pin is set high and shut down when EN is low. During shutdown, the converter stops switching and all internal control circuitry is turned off. In this case, the input voltage is connected to the output through the back-gate diode of the rectifying MOSFET. This means that voltage will always exist at the output, which can be as high as the input voltage or lower depending on the load.

## 8 Application and Implementation

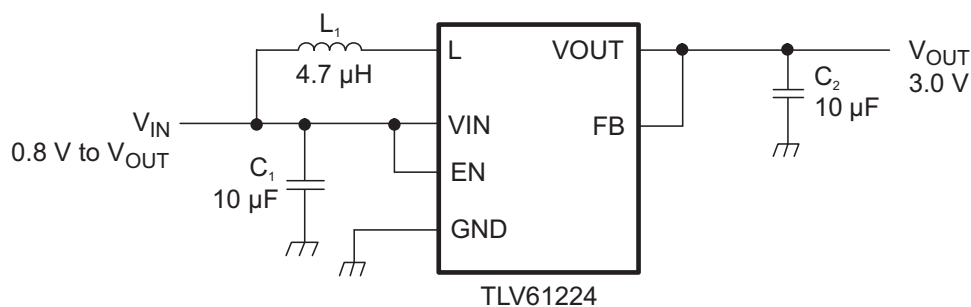
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV61224 device is intended for systems which are powered by a single-cell battery to up to two Alkaline, NiCd, or NiMH cells with a typical terminal voltage from 0.7 V to 3 V and can output 3-V voltage. Additionally, any other voltage source with a typical output voltage from 0.7 V to 3 V can be used with the TLV61224 device.

### 8.2 Typical Application



**Figure 8. Typical Application Schematic**

#### 8.2.1 Design Requirements

In this example, TLV61224 device is used to design a 3-V power supply with up to 15-mA output current capability. The TLV61224 device can be powered by a single-cell battery to up to two Alkaline, NiCd, or NiMH cells with a typical terminal voltage from 0.7 V to 3 V. The input voltage range is from 0.8 V to 1.5 V for single-cell Alkaline battery input design.

#### 8.2.2 Detailed Design Procedure

##### 8.2.2.1 Programming the Output Voltage

At fixed voltage versions, the output voltage is programmed by an internal resistor divider. The FB pin is used to sense the output voltage. To configure the devices properly, the FB pin must be connected directly to VOUT.

##### 8.2.2.2 Inductor Selection

To make sure that the TLV61224 devices can operate, a suitable inductor must be connected between pin VIN and pin L. Inductor values of 4.7 µH show good performance over the whole input and output voltage range.

Due to the fixed inductor current ripple control the switching frequency is defined by the inductor value. For a given switching frequency, input and output voltage the required inductance can be estimated using [Equation 1](#).

$$L = \frac{1}{f \times 200 \text{ mA}} \times \frac{V_{\text{IN}} \times (V_{\text{OUT}} - V_{\text{IN}})}{V_{\text{OUT}}} \quad (1)$$

Using inductor values greater than 4.7 µH can improve efficiency because greater values cause lower switching frequency and less switching losses. TI does not recommend using inductor values less than 2.2 µH.

To ensure reliable operation of the TLV61224 device under all load conditions, TI recommends using inductors with a current rating of 400 mA or higher. This will cover normal operation including current peaks during line and load transients.

**Typical Application (continued)**

Table 2 lists the inductor series from different suppliers that have been used with the TLV61224 converter:

**Table 2. List of Inductors**

VENDOR	INDUCTOR SERIES
Coilcraft	EPL3015
	EPL2010
Murata	LQH3NP
Tajo Yuden	NR3015
Würth Elektronik	WE-TPC Typ S

**8.2.2.3 Capacitor Selection**

**8.2.2.3.1 Input Capacitor**

TI recommends at least a 10-μF input capacitor to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. TI recommends placing a ceramic capacitor as close as possible to the VIN and GND pins of the IC.

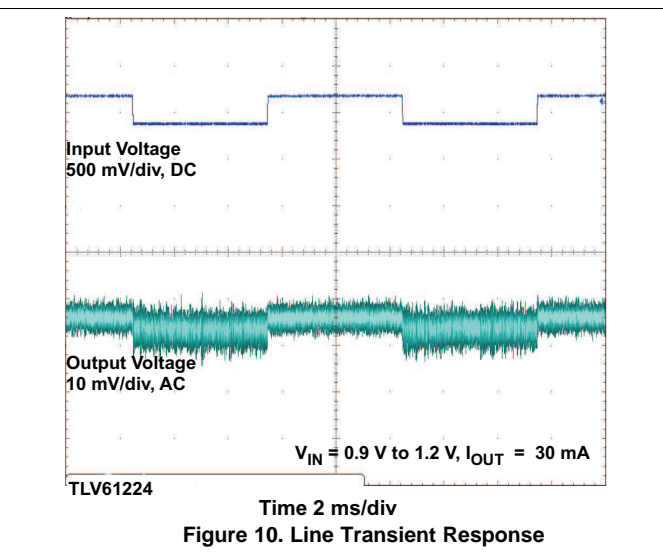
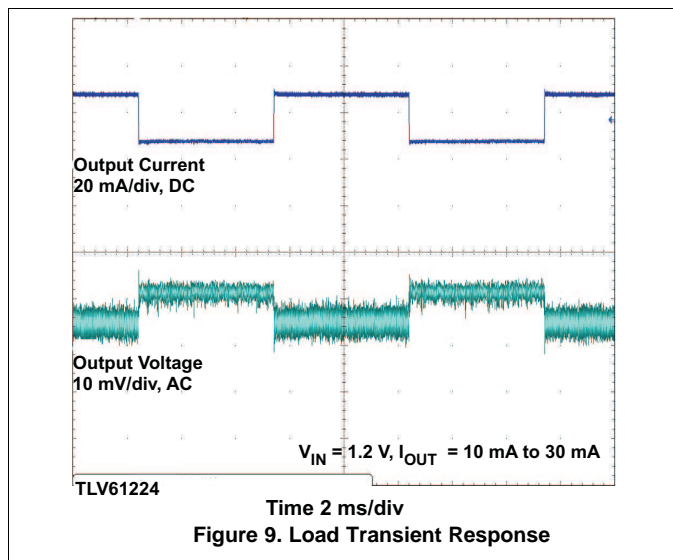
**8.2.2.3.2 Output Capacitor**

For the output capacitor C<sub>2</sub>, TI recommends placing small ceramic capacitors as close as possible to the VOUT and GND pins of the IC. There are no minimum output capacitor ESR requirements for maintaining control loop stability. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, TI recommends using a small ceramic capacitor with a capacitance value in the range of 2.2 μF in parallel to the large capacitor. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

A minimum capacitance value of 4.7 μF should be used; TI recommends a value of 10 μF. Use Equation 2 to calculate the required output capacitance in case an inductor with a value greater than 4.7 μH has been selected.

$$C_2 \geq \frac{L}{2} \times \frac{\mu\text{F}}{\mu\text{H}} \tag{2}$$

**8.2.3 Application Curves**



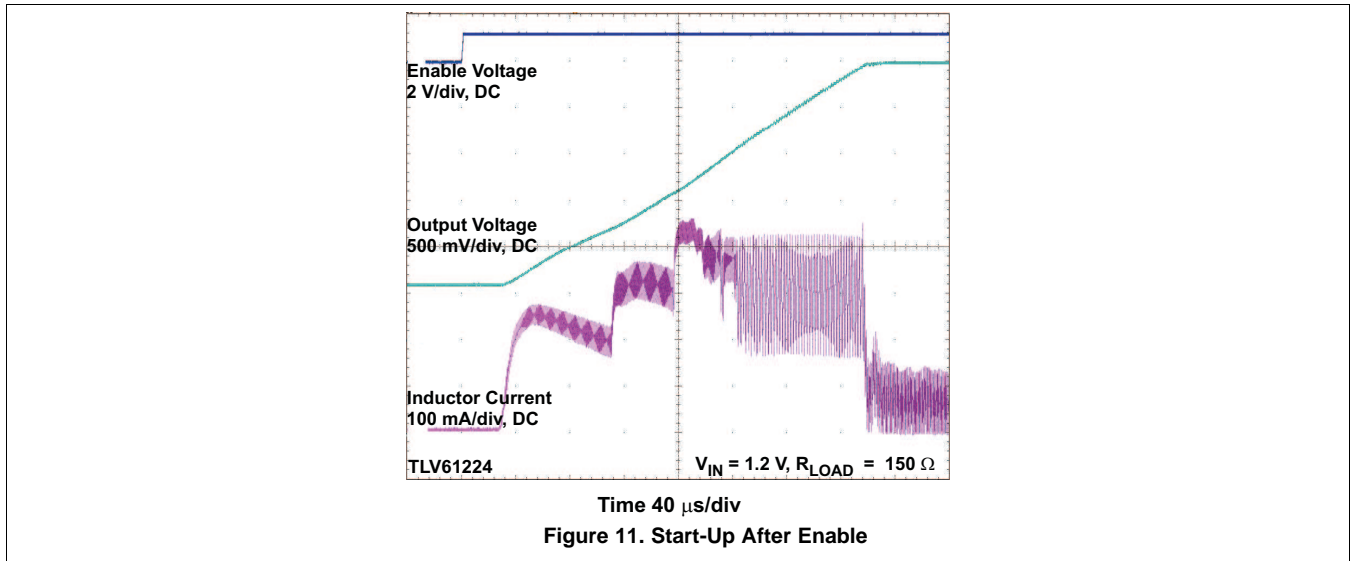


Table 3 lists the components used for the waveform measurements.

**Table 3. List of Components:**

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C <sub>1</sub>	GRM188R60J106ME84D	Murata	10 $\mu$ F, 6.3 V
C <sub>2</sub>	GRM188R60J106ME84D	Murata	10 $\mu$ F, 6.3 V
L <sub>1</sub>	EPL3015-472MLB	Coilcraft	4.7 $\mu$ H

## 9 Power Supply Recommendations

The power supply can be 1-cell or 2-cell alkaline, NiCd or NiMH batteries. The input supply should be well regulated with the rating of TLV61224 device. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47  $\mu$ F is a typical choice.

## 10 Layout

### 10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

To lay out the ground, TI recommends using short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

### 10.2 Layout Example

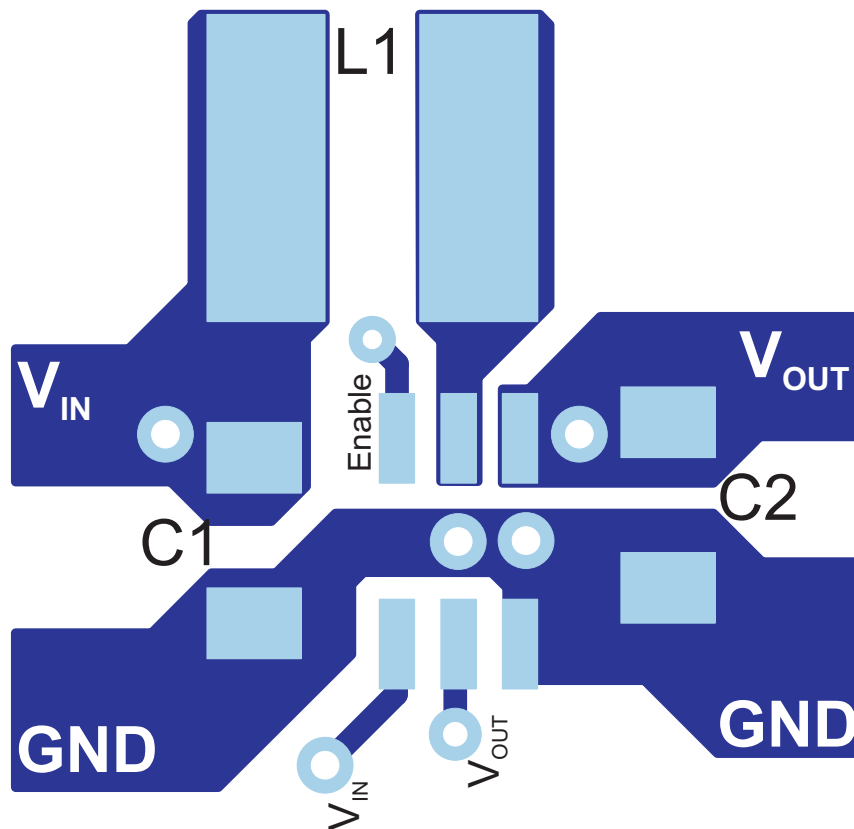


Figure 12. PCB Layout Suggestion

### 10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table, check the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note ([SZZA017](#)) and the *Semiconductor and IC Package Thermal Metrics* application note ([SPRA953](#)).

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 第三方产品免责声明

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### 11.2 文档支持

#### 11.2.1 相关文档

- 《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》，[SZZA017](#)
- 《半导体和 IC 封装热指标》，[SPRA953](#)

### 11.3 社区资源

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商标

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All other trademarks are the property of their respective owners.

### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV61224DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	QXC	<a href="#">Samples</a>
TLV61224DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	QXC	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV61224DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV61224DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV61224DCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TLV61224DCKT	SC70	DCK	6	250	200.0	183.0	25.0

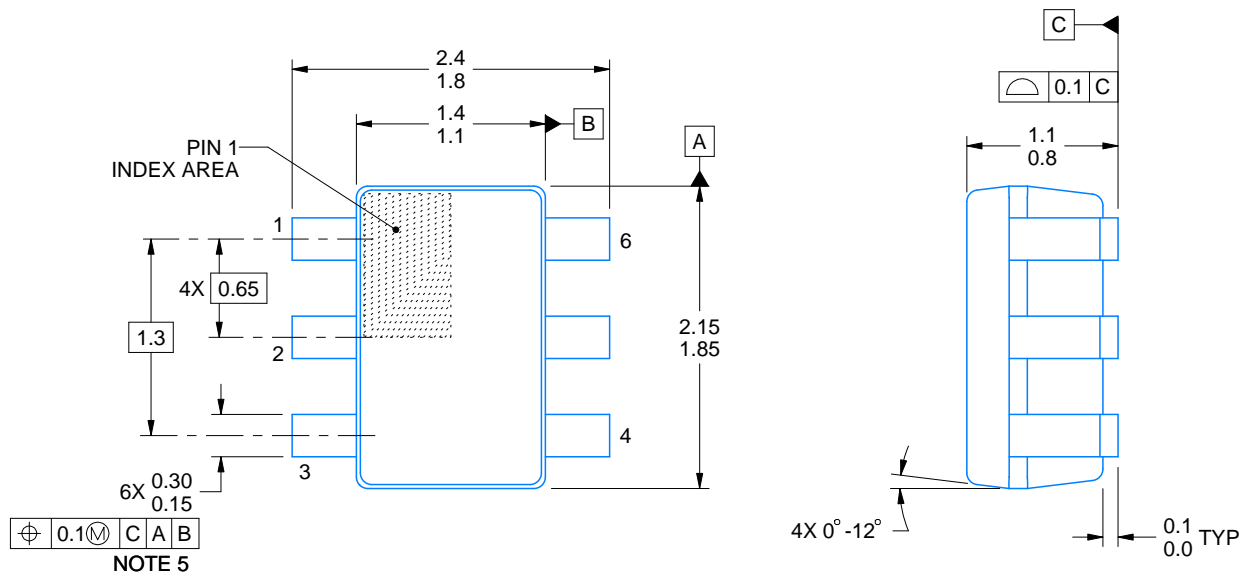


# PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



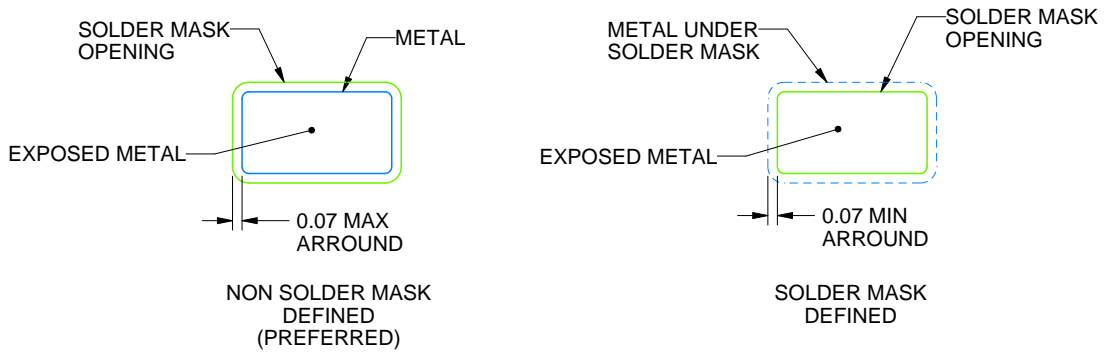
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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

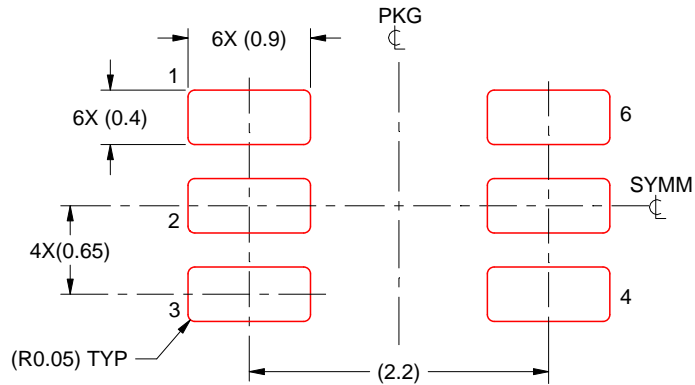


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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