

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

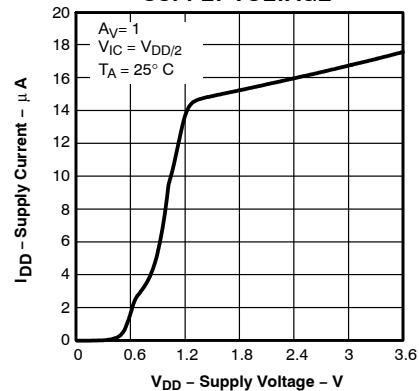
SLOS326F – JUNE 2000 – REVISED AUGUST 2013

- Low Supply Voltage . . . 1.8 V to 3.6 V
- Very Low Supply Current . . . 20  $\mu\text{A}$  (per channel)
- Ultralow Power Shut-Down Mode
  - $I_{\text{DD(SHDN)}} = 10 \text{ nA/Channel}$
- CMOS Rail-to-Rail Input/Output
- Input Common-Mode Voltage Range . . .  $-0.2 \text{ V}$  to  $V_{\text{DD}} + 0.2 \text{ V}$
- Input Offset Voltage . . . 550  $\mu\text{V}$
- Wide Bandwidth . . . 500 kHz
- Slew Rate . . . 0.20  $\text{V}/\mu\text{s}$
- Specified Temperature Range:
  - $0^\circ\text{C}$  to  $70^\circ\text{C}$  . . . Commercial Grade
  - $-40^\circ\text{C}$  to  $85^\circ\text{C}$  . . . Industrial Grade
- Ultrasmall Packaging
  - 5 or 6 Pin SOT-23 (TLV2760/1)
  - 8 or 10 Pin MSOP (TLV2762/3)
- Universal Op-Amp EVM

Operational Amplifier



SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE



## description

The TLV276x single supply operational amplifiers provide 500 kHz bandwidth from only 20  $\mu\text{A}$  while operating down to 1.8 V over the industrial temperature range. The maximum recommended supply voltage is 3.6 V, which allows the devices to be operated from ( $\pm 1.8 \text{ V}$  supplies down to  $\pm 0.9 \text{ V}$ ) two AA or AAA cells. The devices have been characterized at 1.8 V (end of life of 2 AA(A) cells) and at 2.4 V (nominal voltage of 2 NiCd/NiMH cells). The TLV276x have rail-to-rail input and output capability which is a necessity at 1.8 V.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-ohm resistors. Low shutdown current of only 10 nA make these devices ideal for low frequency measurement applications desiring long active battery life.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

### SELECTION OF SINGLE SUPPLY AMPLIFIER PRODUCTS

DEVICE	$V_{\text{DD}}$ (V)	$V_{\text{IO}}$ ( $\mu\text{V}$ )	$I_{\text{DD/Ch}}$ ( $\mu\text{A}$ )	$I_{\text{IB}}$ (pA)	GBW (MHz)	SR ( $\text{V}/\mu\text{s}$ )	$V_n, 1\text{kHz}$ ( $\text{nV}/\sqrt{\text{Hz}}$ )	$I_o$ (mA)	SHUT- DOWN	RAIL-TO- RAIL
TLV224x	2.5 – 12	600	1	100	0.0055	0.002	NA	0.2	—	I/O
TLV2211	2.7 – 10	450	13	1	0.065	0.025	21	0.4	—	O
TLV276x	1.8 – 3.6	550	20	3	0.5	0.23	95	5	Y	I/O
TLV245x(A)	2.7 – 6	20	23	500	0.22	0.11	49	2.5	Y	I/O
TLV246x(A)	2.7 – 6	150	550	1300	6.4	1.6	11	25	Y	I/O
TLV278x(A)	1.8 – 3.6	250	650	2.5	8	5	18	10	Y	I/O



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TLV2760 and TLV2761 AVAILABLE OPTIONS<sup>(1)</sup>

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D) <sup>†</sup>	SOT-23		PLASTIC DIP (P)
			(DBV) <sup>‡</sup>	SYMBOL	
0°C to 70°C	3500 μV	TLV2760CD TLV2761CD	— —	— —	— —
–40°C to 85°C	3500 μV	TLV2760ID TLV2761ID	TLV2760IDBV TLV2761IDBV	VANI VAXI	TLV2760IP TLV2761IP

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2760CDR).

<sup>‡</sup> This package is only available taped and reeled. For standard quantities (3,000 pieces per reel), add an **R** suffix (i.e., TLV2760CDBVR). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g., TLV2760CDBVT).

## TLV2762 and TLV2763 AVAILABLE OPTIONS<sup>(1)</sup>

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE (D) <sup>†</sup>	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
			DGK <sup>†</sup>	SYMBOL	DGS <sup>†</sup>	SYMBOL		
0°C to 70°C	3500 μV	TLV2762CD TLV2763CD	— TLV2762CDGK	— AJO	— —	— —	— —	
–40°C to 85°C	3500 μV	TLV2762ID TLV2763ID	TLV2762IDGK —	xxTIAJP —	— TLV2763IDGS	— xxTIAJR	— TLV2762IP —	

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2762CDR).

## TLV2764 and TLV2765 AVAILABLE OPTIONS<sup>(1)</sup>

T <sub>A</sub>	V <sub>IOmax</sub> AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D) <sup>†</sup>	PLASTIC DIP (N)	TSSOP (PW) <sup>†</sup>
0°C to 70°C	3500 μV	TLV2764CD TLV2765CD	— —	— —
–40°C to 85°C	3500 μV	TLV2764ID TLV2765ID	TLV2764IN TLV2765IN	TLV2764IPW TLV2765IPW

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2764CDR).

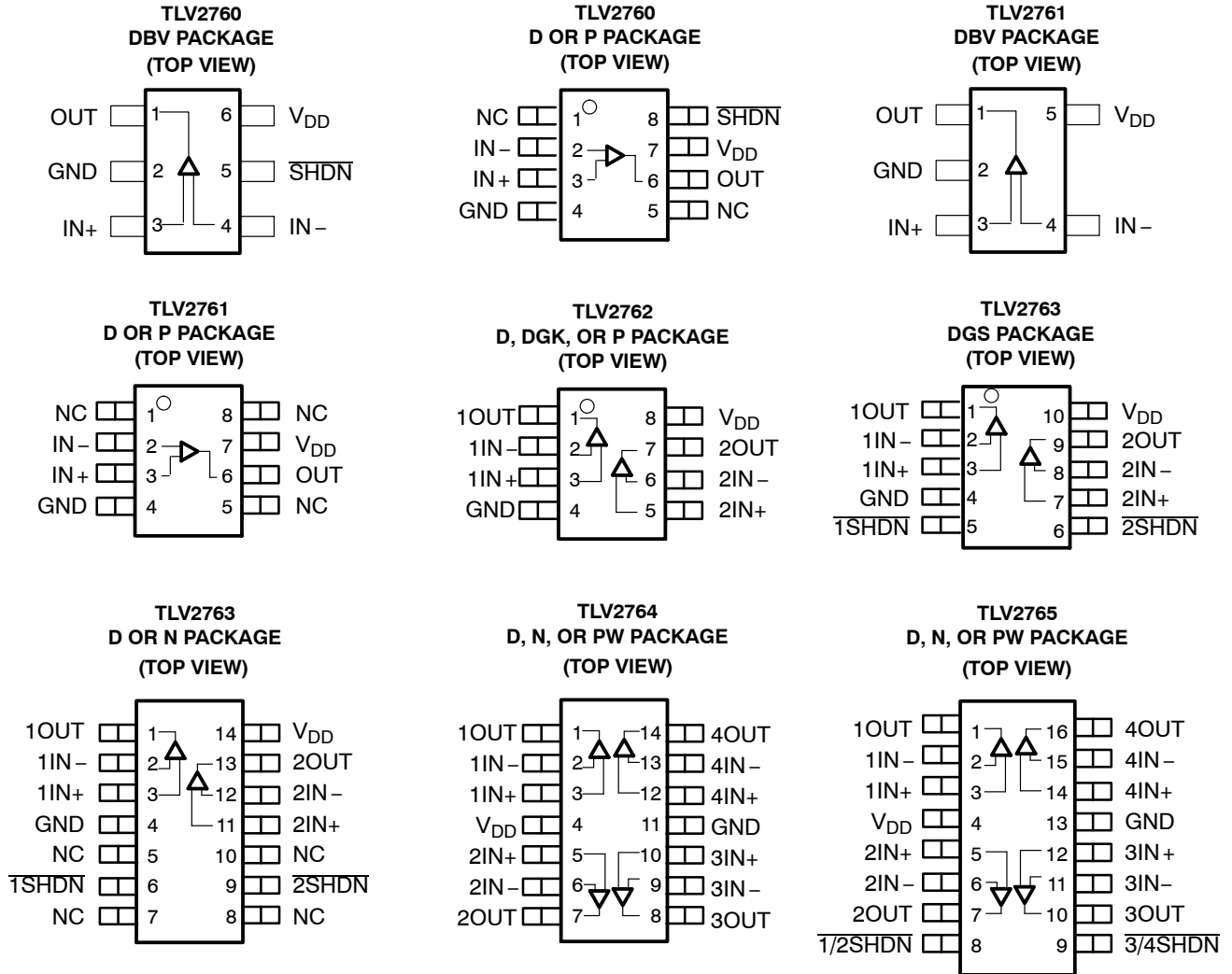
1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TLV276x PACKAGE PINOUTS



NC – No internal connection

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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{DD}$ (see Note 1)	4 V
Differential input voltage range, $V_{ID}$	$\pm V_{DD}$
Input current range, $I_I$	$\pm 10$ mA
Output current range, $I_O$	$\pm 10$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C-suffix	0°C to 70°C
I-suffix	-40°C to 85°C
Maximum junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	$\Theta_{JC}$ (°C/W)	$\Theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	369 mW
D (14)	26.9	122	1022 mW	531 mW
D (16)	25.7	114	1090 mW	567 mW
DBV (5)	55	324	385 mW	201 mW
DBV (6)	55	294	425 mW	221 mW
DGK(8)	54.2	260	481 mW	250 mW
DGS(10)	54.1	258	485 mW	252 mW
N (14,16)	32	78	1600 mW	833 mW
P	41	104	1200 mW	625 mW
PW (14)	29.3	174	720 mW	374 mW
PW (16)	28.7	161	774 mW	403 mW

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$	Single supply	1.8	3.6	V
	Split supply	$\pm 0.8$	$\pm 1.8$	
Common-mode input voltage range, $V_{ICR}$		-0.2	$V_{DD} + 0.2$	V
Operating free-air temperature, $T_A$	C-suffix	0	70	°C
	I-suffix	-40	85	
Shutdown on/off voltage level (see Note 2)	$V_{IH}$	$V_{DD} < 2.7$ V	$0.75 V_{DD}$	V
		$V_{DD} = 2.7$ to $3.6$ V	2	
	$V_{IL}$		0.6	

NOTE 2: Relative to GND



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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}, 2.4\text{ V}$  (unless otherwise noted)

## dc performance

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = V_{DD}/2,$ $V_O = V_{DD}/2,$ $R_L = 300\text{ k}\Omega,$ $R_S = 50\ \Omega$	TLV276x	25°C	550	3500	$\mu\text{V}$
				Full range	6800		
$\alpha_{VIO}$	Offset voltage drift			9		$\mu\text{V}/^\circ\text{C}$	
CMRR	Common-mode rejection ratio	$V_{ICR} = 0\text{ V to }V_{DD},$ $R_S = 50\ \Omega$	$V_{DD} = 1.8\text{ V}$	25°C	50	70	dB
				Full range	48		
			$V_{DD} = 2.4\text{ V}$	25°C	53	72	dB
				Full range	50		
			$V_{DD} = 3.6\text{ V}$	25°C	55	76	dB
				Full range	55		
			$V_{DD} = 2.4\text{ V}, 3.6\text{ V}$	25°C	63	82	dB
				Full range	60		
$A_{VD}$	Large-signal differential voltage amplification	$R_L = 10\text{ k}\Omega,$ $V_{O(PP)} = V_{DD}/2$	$V_{DD} = 1.8\text{ V}$	25°C	20	60	V/mV
				Full range	18		
			$V_{DD} = 2.4\text{ V}$	25°C	28	78	V/mV
				Full range	23		
			$V_{DD} = 3.6\text{ V}$	25°C	45	120	V/mV
				Full range	37		

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and –40°C to 85°C for the I-suffix. If not specified, full range is –40°C to 85°C.

## input characteristics

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{IO}$	Input offset current	$V_{IC} = V_{DD}/2,$ $V_O = V_{DD}/2,$ $R_L = 300\text{ k}\Omega,$ $R_S = 50\ \Omega$	25°C	3		15	pA
			TLV276xC	Full range	100		
				TLV276xI	Full range	200	
$I_{IB}$	Input bias current		25°C	3		15	pA
			TLV276xC	Full range	100		
				TLV276xI	Full range	200	
$r_{i(d)}$	Differential input resistance		25°C	1000		G $\Omega$	
$C_{i(c)}$	Common-mode input capacitance	$f = 16\text{ kHz}$	25°C	10		pF	

$^\dagger$  Full range is 0°C to 70°C for the C-suffix and –40°C to 85°C for the I-suffix. If not specified, full range is –40°C to 85°C.

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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}, 2.4\text{ V}$  (unless otherwise noted) (continued)

**output characteristics**

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IC} = V_{DD}/2,$ $I_{OH} = -100\ \mu\text{A}$	$V_{DD} = 1.8\text{ V}$	25°C	1.77	1.79		V
			Full range	1.76			
		$V_{DD} = 2.4\text{ V}$	25°C	2.38	2.39		
			Full range	2.37			
		$V_{DD} = 3.6\text{ V}$	25°C	3.58	3.59		
			Full range	3.57			
	$V_{IC} = V_{DD}/2,$ $I_{OH} = -500\ \mu\text{A}$	$V_{DD} = 1.8\text{ V}$	25°C	1.725	1.75		
			Full range	1.7			
		$V_{DD} = 2.4\text{ V}$	25°C	2.325	2.35		
			Full range	2.3			
		$V_{DD} = 3.6\text{ V}$	25°C	3.525	3.55		
			Full range	3.5			
$V_{OL}$ Low-level output voltage	$V_{IC} = V_{DD}/2,$ $I_{OL} = 100\ \mu\text{A}$	25°C		10	20	mV	
		Full range			30		
	$V_{IC} = V_{DD}/2,$ $I_{OL} = 500\ \mu\text{A}$	25°C		50	75		
		Full range			100		
$I_O$ Output current	$V_{DD} = 1.8\text{ V},$ $V_O = 0.5\text{ V from}$	Positive rail	25°C	4.8		mA	
		Negative rail		7.2			
	$V_{DD} = 2.4\text{ V},$ $V_O = 0.5\text{ V from}$	Positive rail	25°C	7.3			
		Negative rail		10.2			
$I_{OS}$ Short-circuit output current	$V_{DD} = 1.8\text{ V}$	Sourcing	25°C	7		mA	
		Sinking		10			
	$V_{DD} = 2.4\text{ V}$	Sourcing	25°C	15			
		Sinking		19			

† Full range is 0°C to 70°C for the C-suffix and -40°C to 85°C for the I-suffix. If not specified, full range is -40°C to 85°C.

**power supply,  $V_{DD} = 1.8\text{ V}, 2.4\text{ V}, 3.6\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{DD}$ Supply current (per channel)	$V_O = V_{DD}/2,$ $\overline{\text{SHDN}} = V_{DD}$		25°C		20	28	$\mu\text{A}$
			Full range			30	
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 1.8\text{ V to } 2.4\text{ V},$ $V_{IC} = V_{DD}/2$	No load	25°C	65	85	dB	
			Full range	63			
	$V_{DD} = 2.4\text{ V to } 3.6\text{ V},$ $V_{IC} = V_{DD}/2$		25°C	65	85		
			Full range	63			
	$V_{DD} = 1.8\text{ V to } 3.6\text{ V},$ $V_{IC} = V_{DD}/2$		25°C	65	85		
			Full range	63			

† Full range is 0°C to 70°C for the C-suffix and -40°C to 85°C for the I-suffix. If not specified, full range is -40°C to 85°C.



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**OPERATIONAL AMPLIFIERS WITH SHUTDOWN**

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

electrical characteristics at recommended operating conditions,  $V_{DD} = 1.8\text{ V}, 2.4\text{ V}$  (unless otherwise noted) (continued)

**dynamic performance**

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 300\text{ k}\Omega,$	$C_L = 10\text{ pF}$	$25^\circ\text{C}$		500		kHz
SR+	Positive slew rate at unity gain	$V_{O(PP)} = 1\text{ V}, R_L = 300\text{ k}\Omega,$ $C_L = 50\text{ pF},$	$V_{DD} = 1.8\text{ V}$	$25^\circ\text{C}$	0.11	0.20		V/ $\mu\text{s}$
				Full range	0.09			
			$V_{DD} = 2.4\text{ V}$	$25^\circ\text{C}$	0.11	0.22		V/ $\mu\text{s}$
				Full range	0.09			
			$V_{DD} = 3.6\text{ V}$	$25^\circ\text{C}$	0.11	0.23		V/ $\mu\text{s}$
				Full range	0.09			
SR-	Negative slew rate at unity gain	$V_{O(PP)} = 1\text{ V}, R_L = 300\text{ k}\Omega,$ $C_L = 50\text{ pF},$	$V_{DD} = 1.8\text{ V}$	$25^\circ\text{C}$	0.08	0.15		V/ $\mu\text{s}$
				Full range	0.07			
			$V_{DD} = 2.4\text{ V}$	$25^\circ\text{C}$	0.10	0.18		V/ $\mu\text{s}$
				Full range	0.09			
			$V_{DD} = 3.6\text{ V}$	$25^\circ\text{C}$	0.10	0.22		V/ $\mu\text{s}$
				Full range	0.09			
$\phi_m$	Phase margin	$R_L = 300\text{ k}\Omega,$	$C_L = 100\text{ pF}$	$25^\circ\text{C}$		63		$^\circ$
	Gain margin			$25^\circ\text{C}$		20		dB
$t_s$	Settling time	$V_{DD} = 1.8\text{ V}, V_{(STEP)PP} = 1\text{ V},$ $A_V = -1, C_L = 10\text{ pF}, R_L = 300\text{ k}\Omega$	$25^\circ\text{C}$	0.1%		6.4		$\mu\text{s}$
				0.01%		13.7		
		$V_{DD} = 2.4\text{ V}, V_{(STEP)PP} = 1\text{ V},$ $A_V = -1, C_L = 10\text{ pF}, R_L = 300\text{ k}\Omega$	$25^\circ\text{C}$	0.1%		6		
				0.01%		13.9		

$^\dagger$  Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the C-suffix and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the I-suffix. If not specified, full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**noise/distortion**

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{DD} = 1.8\text{ V},$ $V_{O(PP)} = V_{DD}/2\text{ V},$ $R_L = 300\text{ k}\Omega,$ $f = 1\text{ kHz}$	$A_V = 1$	$25^\circ\text{C}$		0.08%		
			$A_V = 10$			0.10%		
			$A_V = 100$			0.27%		
		$V_{DD} = 2.4\text{ V},$ $V_{O(PP)} = V_{DD}/2\text{ V},$ $R_L = 300\text{ k}\Omega,$ $f = 1\text{ kHz}$	$A_V = 1$	$25^\circ\text{C}$		0.06%		
			$A_V = 10$			0.08%		
			$A_V = 100$			0.24%		
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	$25^\circ\text{C}$		95		nV/ $\sqrt{\text{Hz}}$	
		$f = 10\text{ kHz}$	$25^\circ\text{C}$		75			
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	$25^\circ\text{C}$		0.8		fA/ $\sqrt{\text{Hz}}$	

**shutdown characteristics**

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current, all channels in shutdown mode (TLV2760, TLV2763, TLV2765) (per channel)	$\overline{\text{SHDN}} = 0\text{ V}$	$25^\circ\text{C}$		10	50	nA
			Full range			400	
$t_{(on)}$	Amplifier turnon time (see Note 3)	$R_L = 300\text{ k}\Omega$	$25^\circ\text{C}$		5		$\mu\text{s}$
$t_{(off)}$	Amplifier turnoff time (see Note 3)	$R_L = 300\text{ k}\Omega$	$25^\circ\text{C}$		0.8		$\mu\text{s}$

$^\dagger$  Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the C-suffix and  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the I-suffix. If not specified, full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 3: Disable time and enable time are defined as the interval between application of the logic signal to  $\overline{\text{SHDN}}$  and the point at which the supply current has reached half its final value.



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SLOS326F – JUNE 2000 – REVISED AUGUST 2013

**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			<b>FIGURE</b>
$V_{IO}$	Input offset voltage	vs Common-mode input voltage	1, 2
CMRR	Common-mode rejection ratio	vs Frequency	3
$V_{OH}$	High-level output voltage	vs High-level output current	4, 6
$V_{OL}$	Low-level output voltage	vs Low-level output current	5, 7
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	8
$I_{DD}$	Supply current	vs Supply voltage	9
$I_{DD}$	Supply current	vs Free-air temperature	10
PSRR	Power supply rejection ratio	vs Frequency	11
$A_{VD}$	Differential voltage amplification & phase	vs Frequency	12
	Gain-bandwidth product	vs Temperature	13
		vs Supply voltage	14
SR	Slew rate	vs Supply voltage	15
		vs Free-air temperature	16, 17
$\phi_m$	Phase margin	vs Load capacitance	18
$V_n$	Equivalent input noise voltage	vs Frequency	19
	Supply current and output voltage	vs Time	20
	Voltage-follower large-signal pulse response	vs Time	21
	Voltage-follower small-signal pulse response	vs Time	22
	Inverting large-signal response	vs Time	23
	Inverting small-signal response	vs Time	24
	Crosstalk	vs Frequency	25
	Shutdown forward & reverse isolation	vs Frequency	26
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	27
$I_{DD(SHDN)}$	Shutdown supply current	vs Free-air temperature	28
$I_{DD(SHDN)}$	Shutdown pin leakage current	vs Shutdown pin voltage	29
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	30

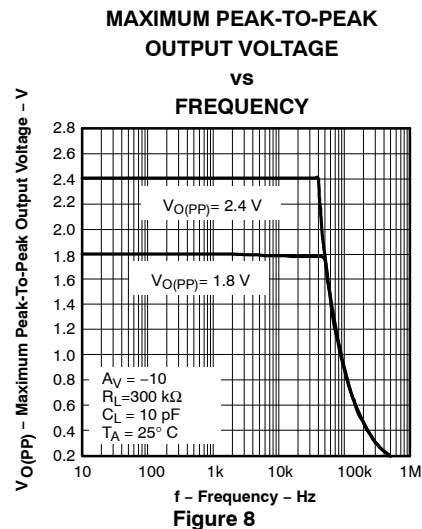
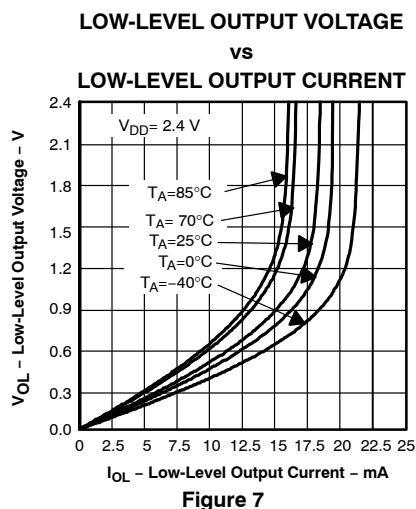
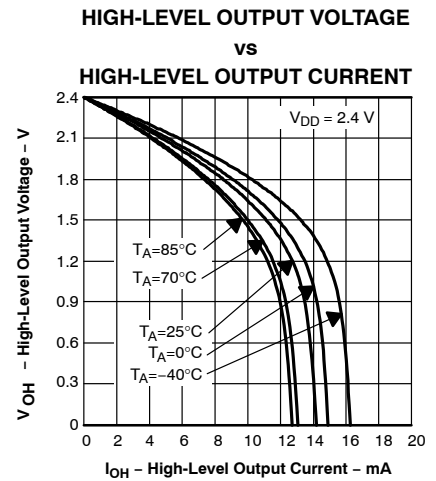
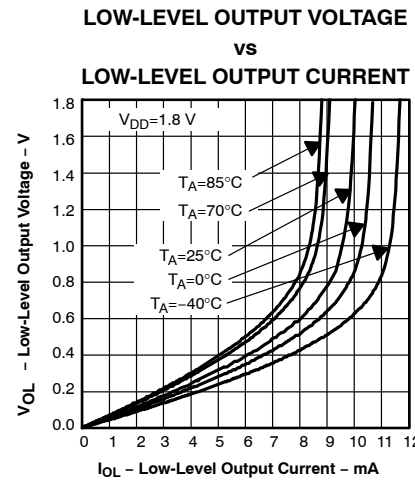
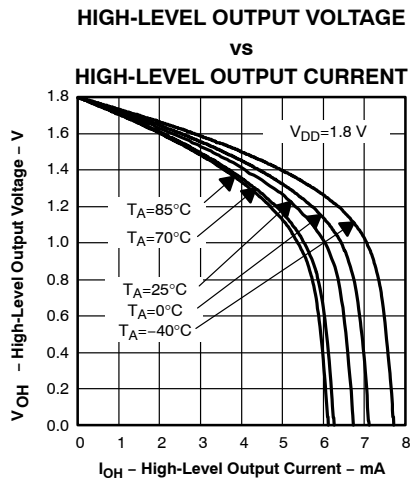
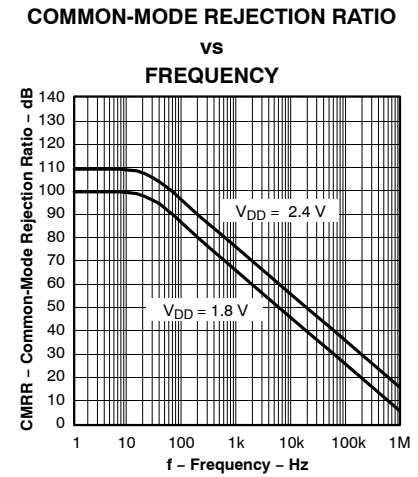
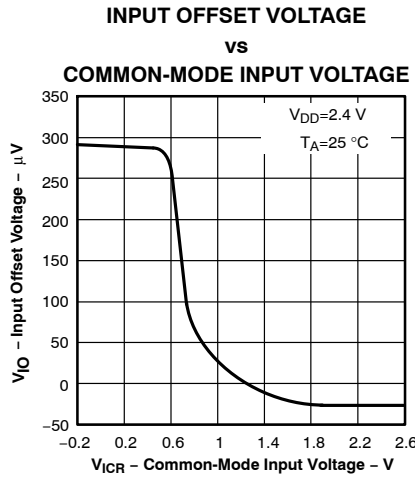
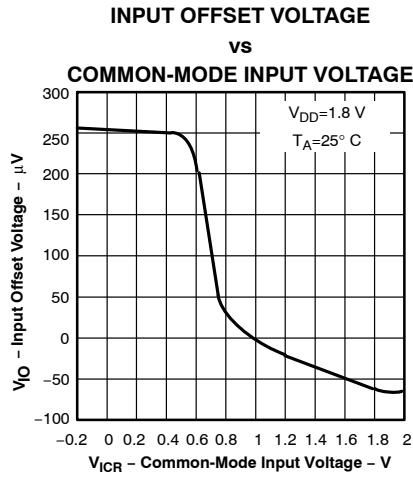




# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROWPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TYPICAL CHARACTERISTICS



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TYPICAL CHARACTERISTICS

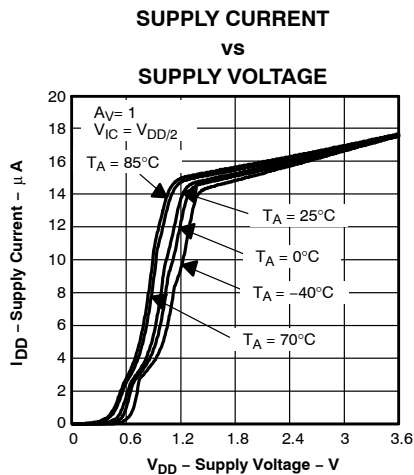


Figure 9

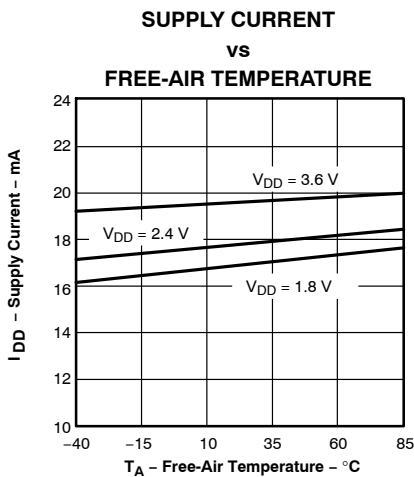


Figure 10

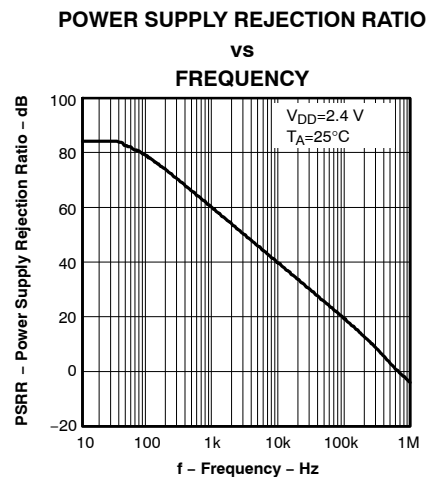


Figure 11

### DIFFERENTIAL VOLTAGE GAIN AND PHASE

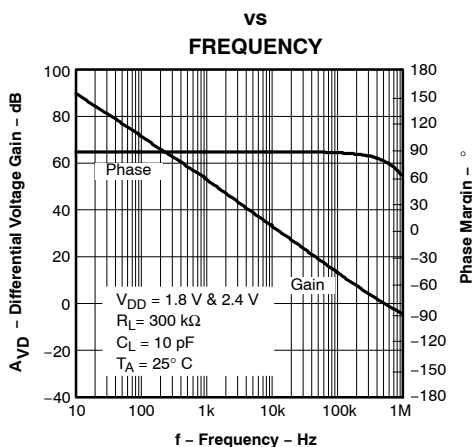


Figure 12

### GAIN BANDWIDTH PRODUCT

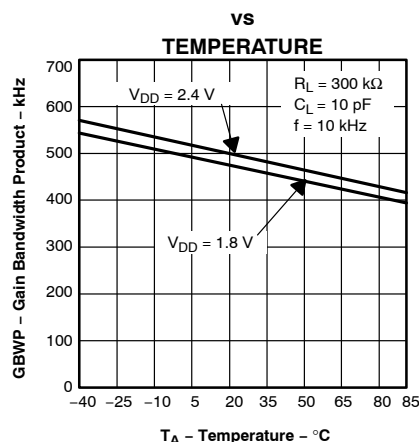


Figure 13

### GAIN-BANDWIDTH PRODUCT

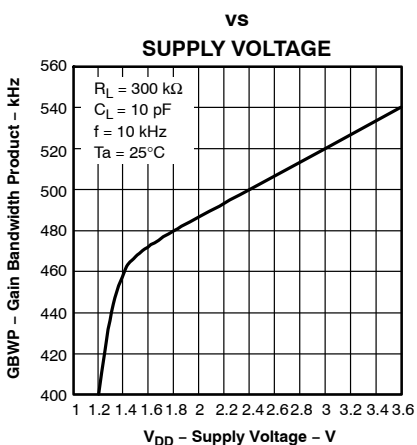


Figure 14

### SLEW RATE

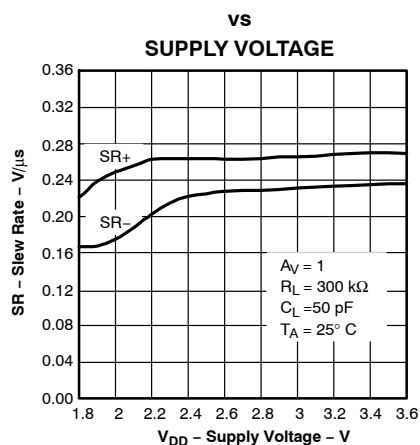


Figure 15



# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TYPICAL CHARACTERISTICS

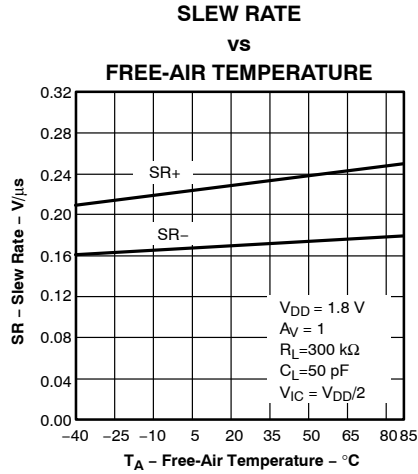


Figure 16

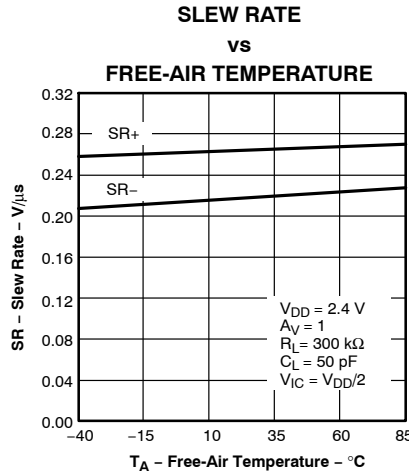


Figure 17

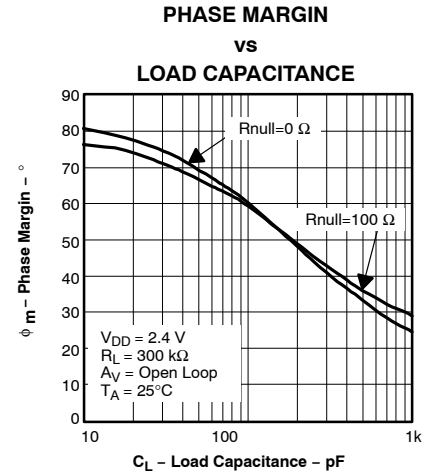


Figure 18

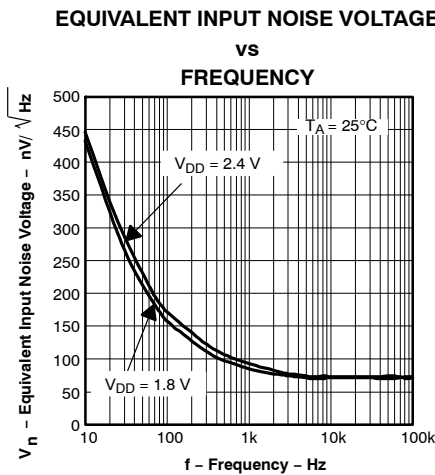


Figure 19

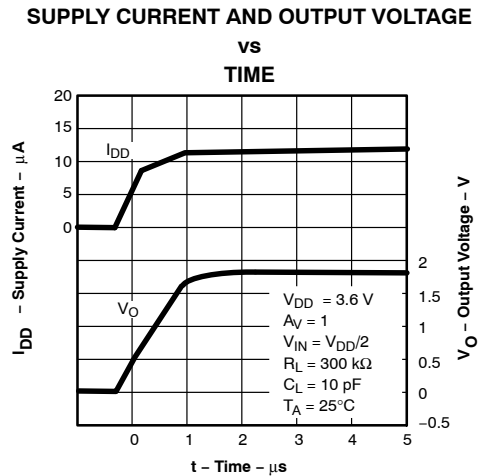


Figure 20

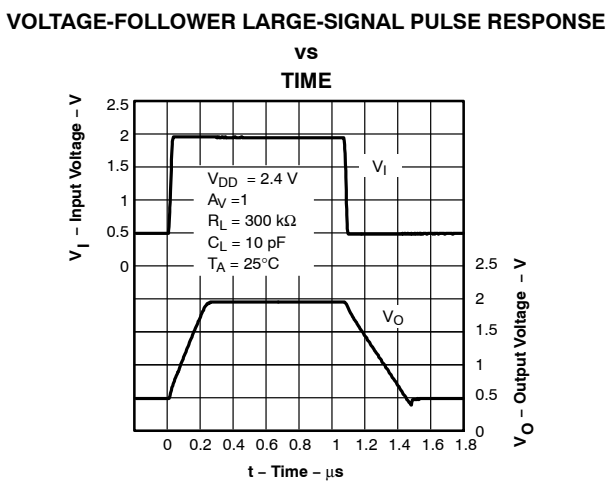


Figure 21

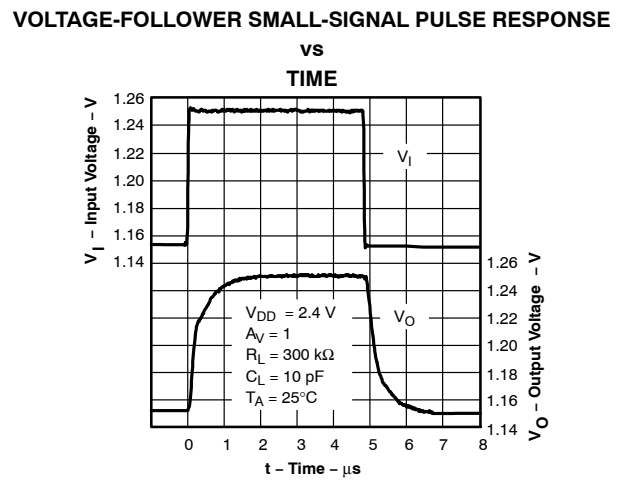


Figure 22

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL RESPONSE

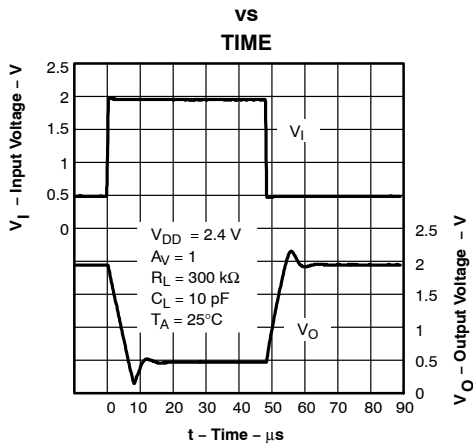


Figure 23

INVERTING SMALL-SIGNAL PULSE RESPONSE

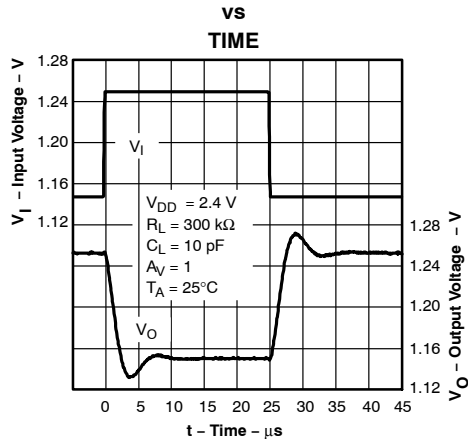


Figure 24

CROSSTALK

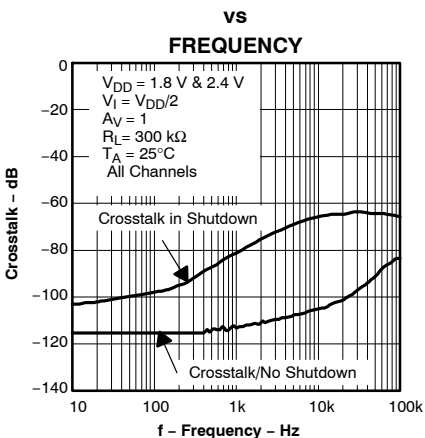


Figure 25

SHUTDOWN FORWARD AND REVERSE ISOLATION

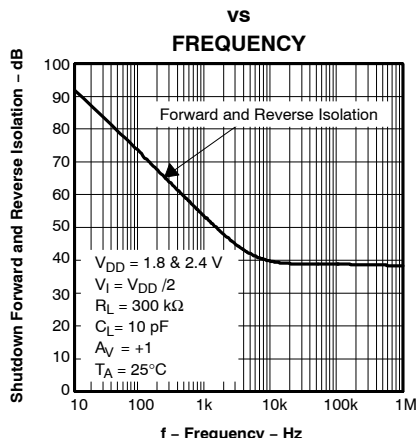


Figure 26

SHUTDOWN SUPPLY CURRENT

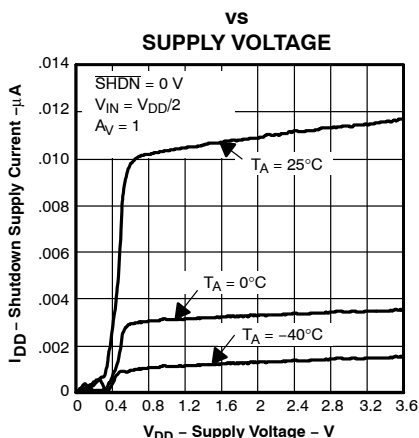


Figure 27

SHUTDOWN SUPPLY CURRENT

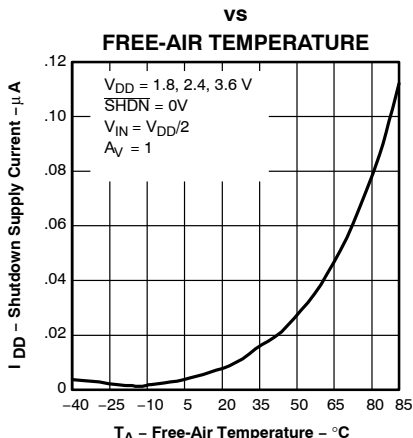


Figure 28

SHUTDOWN PIN LEAKAGE CURRENT

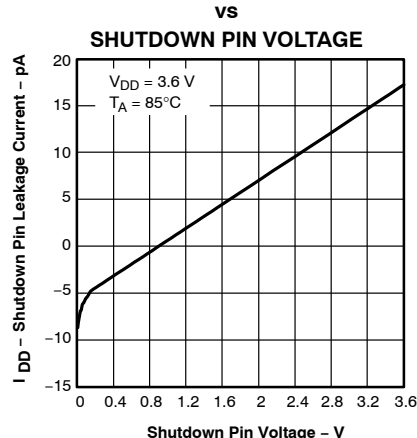


Figure 29

TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765  
FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT  
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F - JUNE 2000 - REVISED AUGUST 2013

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE  
vs  
TIME



Figure 30

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## APPLICATION INFORMATION

### driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ( $R_{NULL}$ ) with the output of the amplifier, as shown in Figure 31. A minimum value of 20  $\Omega$  should work well for most applications.



Figure 31. Driving a Capacitive Load

### offset voltage

The output offset voltage, ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

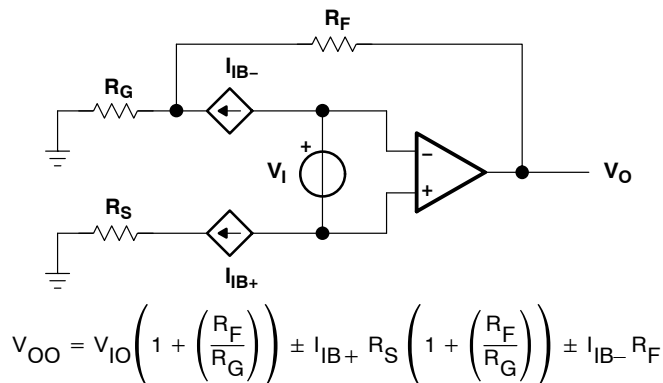


Figure 32. Output Offset Voltage Model

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 33).

APPLICATION INFORMATION

general configurations (continued)



Figure 33. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



Figure 34. 2-Pole Low-Pass Sallen-Key Filter

circuit layout considerations

To achieve the levels of high performance of the TLV276x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

## APPLICATION INFORMATION

### circuit layout considerations (continued)

- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

### shutdown function

Three members of the TLV276x family (TLV2760/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is pulled low, the supply current is reduced to 10 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal must be pulled high. The shutdown terminal should never be left floating. If the shutdown feature is not desired, directly tie the shutdown terminal to the positive rail. The shutdown terminal threshold is always referenced to the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g.  $\pm 1.8$  V), the shutdown terminal needs to be pulled to the negative rail, not the system ground, to disable the operational amplifier.

The amplifier is powered with a single 2.4-V supply and configured as a noninverting configuration with a unity gain. Turnon and turnoff times are defined as the interval between application of the logic signal to the shutdown pin and the point at which the supply current has reached half its final value. The times for the single, dual, and quad are listed in the data tables.

### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 35 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$  = Maximum power dissipation of TLV276x IC (watts)

$T_{MAX}$  = Absolute maximum junction temperature (150°C)

$T_A$  = Free-ambient air temperature (°C)

$\theta_{JA}$  =  $\theta_{JC} + \theta_{CA}$

$\theta_{JC}$  = Thermal coefficient from junction to case

$\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)



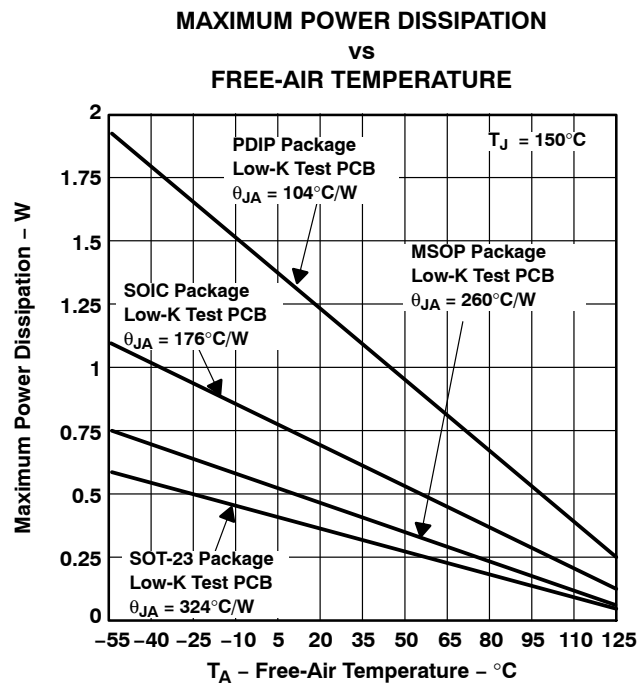


TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765  
FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT  
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

APPLICATION INFORMATION

general power dissipation considerations (continued)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 35. Maximum Power Dissipation vs Free-Air Temperature

# TLV2760, TLV2761, TLV2762, TLV2763, TLV2764, TLV2765 FAMILY OF 1.8 V MICROPOWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS326F – JUNE 2000 – REVISED AUGUST 2013

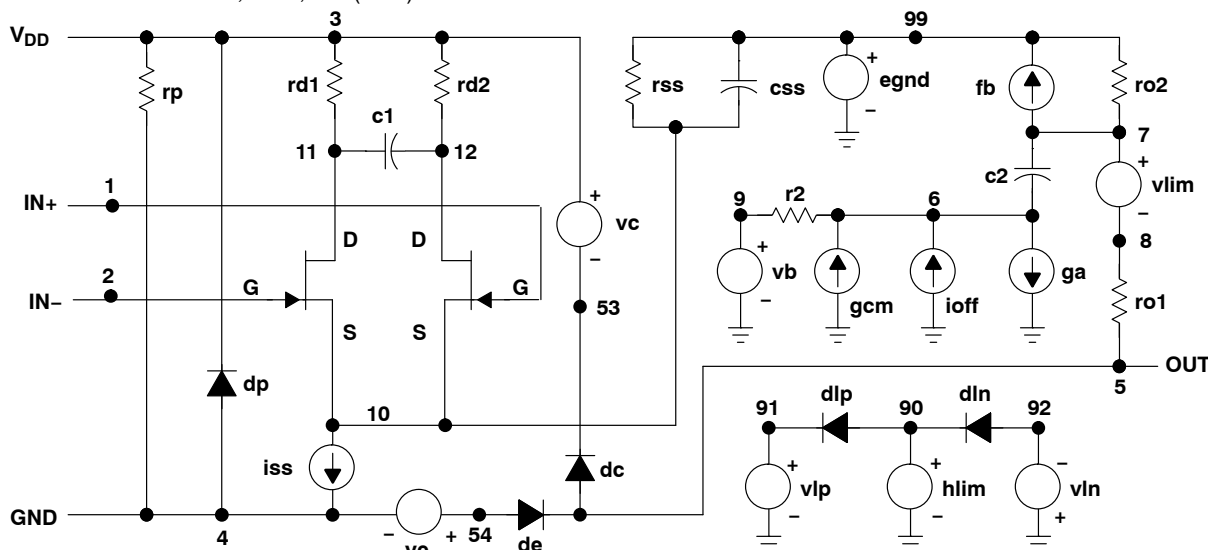
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 9.1, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 36 are generated using TLV276x typical electrical and operating characteristics at T<sub>A</sub> = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



\*DEVICE=amp\_tlv276x\_highVdd,OPAMP,NJF,INT  
\* amp\_tlv\_276x\_highVdd operational amplifier "macromodel"  
\* subcircuit updated using Model Editor release 9.1 on 05/15/00  
\* at 14:40 Model Editor is an OrCAD product.  
\*

\* connections:

non-inverting input  
inverting input  
positive power supply  
negative power supply  
output

.subckt amp\_tlv276x\_highVdd

c1	11	12	457.48E-15
c2	6	7	5.0000E-12
css	10	99	1.1431E-12
dc	5	53	dy
de	54	5	dy
dip	90	91	dx
dln	92	90	dx
dp	4	3	dx
egnd	99	0	poly(2) (3,0) (4,0) 0 .5 .5
fb	7	99	poly(5) vb vc ve vlp vln 0 176.02E6 -1E3 1E3 180E6 -180E6

ga	6	0	11 12 16.272E-6
gcm	0	6	10 99 6.8698E-9
iss	10	4	dc 1.3371E-6
hlim	90	0	vlim 1K
j1	11	2	10 jx1
J2	12	1	10 jx2
r2	6	9	100.00E3
rd1	3	11	61.456E3
rd2	3	12	61.456E3
ro1	8	5	10
ro2	7	99	10
rp	3	4	150.51E3
rss	10	99	149.58E6
vb	9	0	dc 0
vc	3	53	dc .78905
ve	54	4	dc .78905
vlim	7	8	dc 0
vlp	91	0	dc 14.200
vln	0	92	dc 14.200
.model	dx		D(Is=800.00E-18)
.model	dy		D(Is=800.00E-18 Rs=1m Cjo=10p)
.model	jx1		NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)
.model	jx2		NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)
.ends			

Figure 36. Boyle Macromodel and Subcircuit

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**Revision History**

DATE	REV	PAGE	SECTION	DESCRIPTION
8/2013	F	2	2nd Available Options Table	Added TLVZ762CDGK and AJO to Available Options Table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DRAFT ONLY

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2760ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T2760I	<a href="#">Samples</a>
TLV2760IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VANI	<a href="#">Samples</a>
TLV2760IDBVT	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 85	VANI	
TLV2760IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	T2760I	<a href="#">Samples</a>
TLV2761CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T2761C	<a href="#">Samples</a>
TLV2761ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T2761I	<a href="#">Samples</a>
TLV2761IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VAXI	<a href="#">Samples</a>
TLV2761IDBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	VAXI	
TLV2761IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	T2761I	<a href="#">Samples</a>
TLV2762CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	2762C	
TLV2762CDGK	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	0 to 70	AJO	
TLV2762CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	0 to 70	AJO	<a href="#">Samples</a>
TLV2762CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2762C	<a href="#">Samples</a>
TLV2762ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	2762I	
TLV2762IDGK	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 85	AJP	
TLV2762IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	AJP	<a href="#">Samples</a>
TLV2762IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2762I	<a href="#">Samples</a>
TLV2763IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJR	<a href="#">Samples</a>
TLV2763IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJR	<a href="#">Samples</a>
TLV2764CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TLV2764C	
TLV2764ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TLV2764I	
TLV2764IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2764I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2764IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLV2764I	<a href="#">Samples</a>
TLV2764IPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	2764I	
TLV2764IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2764I	<a href="#">Samples</a>
TLV2764IPWRG4	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
TLV2765CDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2765C	<a href="#">Samples</a>
TLV2765IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2765I	<a href="#">Samples</a>
TLV2765IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2765I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2760IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2761IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2762CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV2762CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2762IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV2762IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2763IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2763IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2764IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2764IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2764IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2765CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2765IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2760IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV2761IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2762CDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2762CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2762IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2762IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2763IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2763IDGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
TLV2764IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2764IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2764IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2765CDR	SOIC	D	16	2500	353.0	353.0	32.0
TLV2765IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2760ID	D	SOIC	8	75	507	8	3940	4.32
TLV2760IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2761CD	D	SOIC	8	75	507	8	3940	4.32
TLV2761ID	D	SOIC	8	75	507	8	3940	4.32
TLV2761IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2763IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88
TLV2764IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2765IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



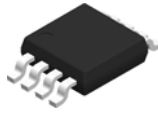
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

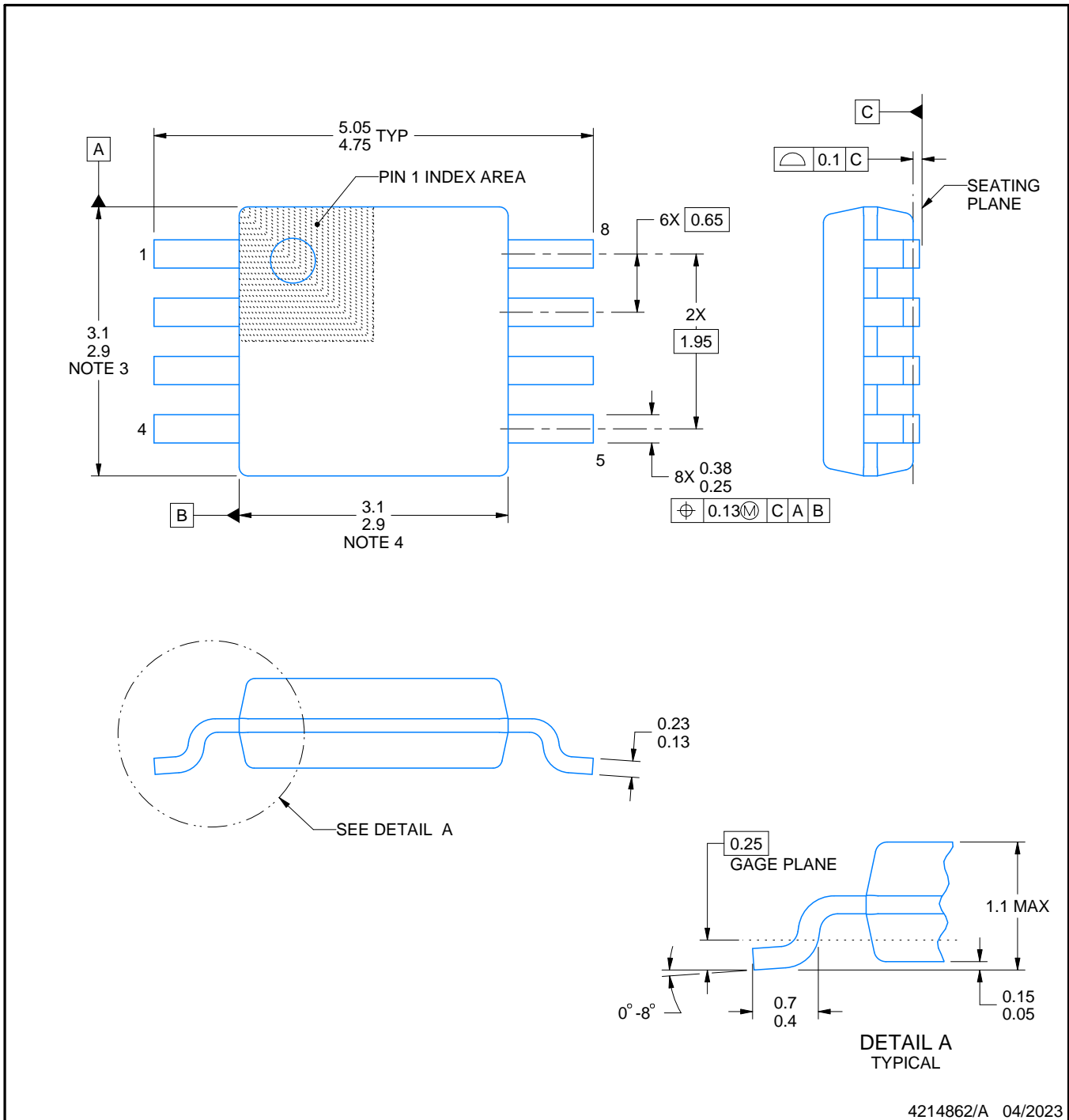
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE  
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



# EXAMPLE BOARD LAYOUT

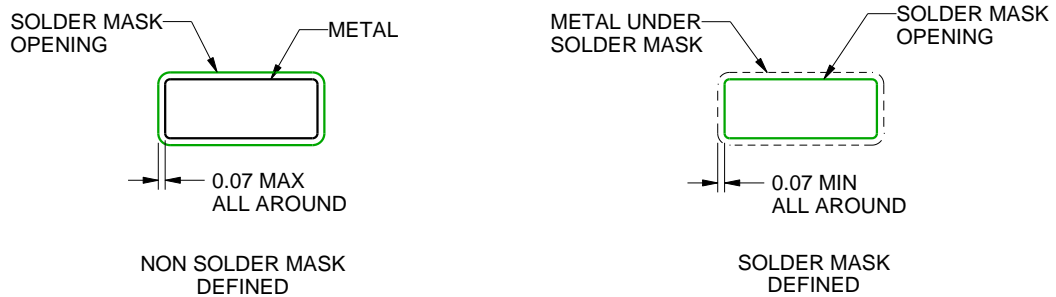
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DBV0006A



## PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

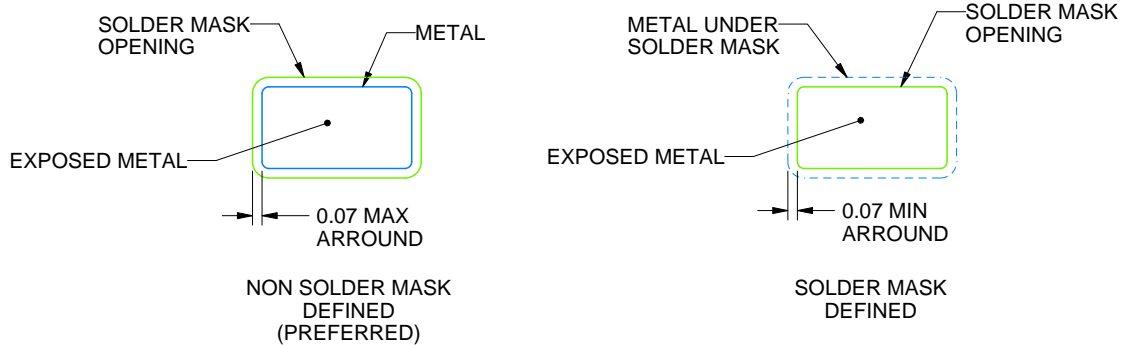
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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