

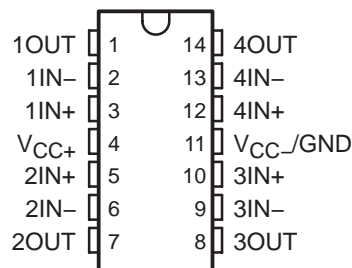
# TL3474, TL3474A

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

SLVS461B – JANUARY 2003 – REVISED JULY 2003

- Low Offset . . . 3 mV (Max) for A-Grade
- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/ $\mu$ s
- Fast Settling Time . . . 1.1  $\mu$ s to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground ( $V_{CC-}$ )
- Low Total Harmonic Distortion . . . 0.02%
- Large-Capacitance Drive Capability . . . 10,000 pF
- Output Short-Circuit Protection
- Alternative to MC33074/A and MC34074/A

D, N, OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

### ORDERING INFORMATION

$T_A$	$V_{IOmax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474ACN	TL3474ACN	
		SOIC (D)	Tube of 50	TL3474ACD	TL3474A	
			Reel of 2500	TL3474ACDR		
		TSSOP (PW)	Tube of 90	TL3474ACPW	T3474A	
	Reel of 2000		TL3474ACPWR			
	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474CN	TL3474CN	
SOIC (D)			Tube of 50	TL3474CD	TL3474C	
			Reel of 2500	TL3474CDR		
TSSOP (PW)		Tube of 90	TL3474CPW	TL3474		
		Reel of 2000	TL3474CPWR			
-40°C to 105°C		A-grade: 3 mV	PDIP (N)	Tube of 25	TL3474AIN	Z3474A
	SOIC (D)		Tube of 50	TL3474AID	TL3474AI	
			Reel of 2500	TL3474AIDR		
	TSSOP (PW)		Tube of 90	TL3474AIPW	Z3474A	
		Reel of 2000	TL3474AIPWR			
	Standard grade: 10 mV	PDIP (N)	Tube of 25	TL3474IN	TL3474IN	
			SOIC (D)	Tube of 50	TL3474ID	TL3474I
				Reel of 2500	TL3474IDR	
		TSSOP (PW)	Tube of 90	TL3474IPW	Z3474	
			Reel of 2000	TL3474IPWR		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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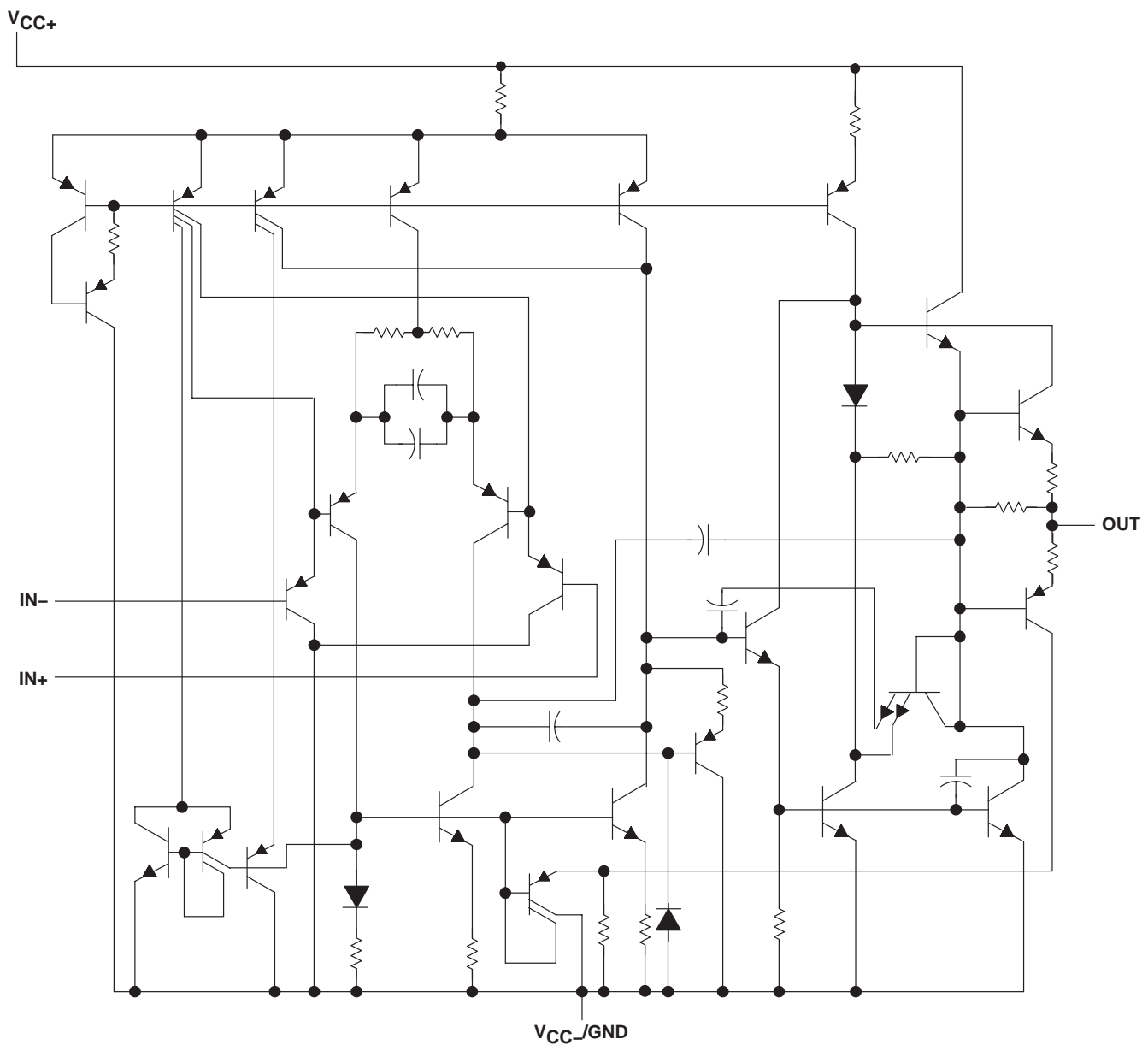
# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## description/ordering information (continued)

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3474, TL3474A operational amplifiers. These devices offer 4 MHz of gain-bandwidth product, 13-V/ $\mu$ s slew rate, and fast settling time without the use of JFET device technology. Although the TL3474 and TL3474A can be operated from split supplies, they are particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, these devices exhibit high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. These low-cost amplifiers are an alternative to the MC34074/A and MC33074/A operational amplifiers.

## schematic (each amplifier)



# TL3474, TL3474A

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: $V_{CC+}$ (see Note 1) .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 36$ V
Input voltage, $V_I$ (any input) .....	$V_{CC\pm}$
Input current, $I_I$ (each input) .....	$\pm 1$ mA
Output current, $I_O$ .....	$\pm 80$ mA
Total current into $V_{CC+}$ .....	80 mA
Total current out of $V_{CC-}$ .....	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5): D package .....	86°C/W
N package .....	80°C/W
PW package .....	113°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}/GND$ .
  2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than  $V_{CC-} - 0.3$  V.
  3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  4. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  5. The package thermal impedance is calculated in accordance with JEDEC 51-7.

### recommended operating conditions

		MIN	MAX	UNIT	
$V_{CC\pm}$	Supply voltage	4	36	V	
$V_{IC}$	Common-mode input voltage	$V_{CC} = 5$ V	0	2.8	V
		$V_{CC\pm} = \pm 15$ V	-15	12.8	
$T_A$	Operating free-air temperature	TL3474C, TL3474AC	0	70	°C
		TL3474I, TL3474AI	-40	105	



# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	TL3474			TL3474A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$	$V_{CC} = 5\text{ V}$	25°C	1.5	10	1.5	3	mV	
		$V_{CC} = \pm 15\text{ V}$	25°C	1.0	10	1.0	3		
			Full range‡			12			5
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$	$V_{CC} = \pm 15\text{ V}$	Full range‡	10		10		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$ Input offset current		$V_{CC} = \pm 15\text{ V}$	25°C	6	75	6	75	nA	
			Full range‡		300		300		
$I_{IB}$ Input bias current	$V_{CC} = \pm 15\text{ V}$	25°C	100	500	100	500	nA		
		Full range‡		700		700			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 12.8		-15 to 12.8		V		
		Full range‡	-15 to 12.8		-15 to 12.8				
$V_{OH}$ High-level output voltage	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0$ , $R_L = 2\text{ k}\Omega$	25°C	3.7	4	3.7	4	V		
	$R_L = 10\text{ k}\Omega$	25°C	13.6	14	13.6	14			
	$R_L = 2\text{ k}\Omega$	Full range‡	13.4		13.4				
$V_{OL}$ Low-level output voltage	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0$ , $R_L = 2\text{ k}\Omega$	25°C	0.1	0.3	0.1	0.3	V		
	$R_L = 10\text{ k}\Omega$	25°C	-14.7	-14.3	-14.7	-14.3			
	$R_L = 2\text{ k}\Omega$	Full range‡		-13.5		-13.5			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	25	100	25	100	V/mV		
		Full range‡	20		20				
$I_{OS}$ Short-circuit output current	Source: $V_{ID} = 1\text{ V}$ , $V_O = 0$	25°C	-10	-34	-10	-34	mA		
	Sink: $V_{ID} = -1\text{ V}$ , $V_O = 0$		20	27	20	27			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$ , $R_S = 50\ \Omega$	25°C	65	97	80	97	dB		
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 13.5\text{ V}$ to $\pm 16.5\text{ V}$ , $R_S = 100\ \Omega$	25°C	70	97	70	97	dB		
$I_{CC}$ Supply current (per channel)	$V_O = 0$ , No load	25°C	3.5	4.5	3.5	4.5	mA		
		Full range‡	4.5	5.5	4.5	5.5			
	$V_{CC+} = 5\text{ V}$ , $V_O = 2.5\text{ V}$ , $V_{CC-} = 0$ , No load	25°C	3.5	4.5	3.5	4.5			

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the TL3474C, TL3474AC devices and  $-40^\circ\text{C}$  to  $105^\circ\text{C}$  for the TL3474I, TL3474AI devices.



# TL3474, TL3474A

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TL3474			TL3474A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_I = -10\text{ V to } 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$	$A_V = 1$	8	10		8	10	$\text{V}/\mu\text{s}$	
SR-	Negative slew rate		$A_V = -1$		13		13			
$t_s$	Settling time	$A_{VD} = -1$ , 10-V step	To 0.1%		1.1		1.1	$\mu\text{s}$		
			To 0.01%		2.2		2.2			
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ ,	$R_S = 100\ \Omega$		49		49	$\text{nV}/\sqrt{\text{Hz}}$		
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.22		0.22	$\text{pA}/\sqrt{\text{Hz}}$		
THD	Total harmonic distortion	$V_{O(PP)} = 2\text{ V to } 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$			0.02		0.02	%		
GBW	Gain-bandwidth product	$f = 100\text{ kHz}$		3	4		3	4	MHz	
BW	Power bandwidth	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 1$ , THD = 5.0%			160		160	kHz		
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$ ,	$C_L = 0$		70		70	deg		
		$R_L = 2\text{ k}\Omega$ ,	$C_L = 300\text{ pF}$		50		50			
	Gain margin	$R_L = 2\text{ k}\Omega$ ,	$C_L = 0$		12		12	dB		
		$R_L = 2\text{ k}\Omega$ ,	$C_L = 300\text{ pF}$		4		4			
$r_i$	Differential input resistance	$V_{IC} = 0$			150		150	$\text{M}\Omega$		
$C_i$	Input capacitance	$V_{IC} = 0$			2.5		2.5	pF		
	Channel separation	$f = 10\text{ kHz}$			101		101	dB		
$z_o$	Open-loop output impedance	$f = 1\text{ MHz}$ ,	$A_V = 1$		20		20	$\Omega$		

# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

**OUTPUT IMPEDANCE  
VS  
FREQUENCY**

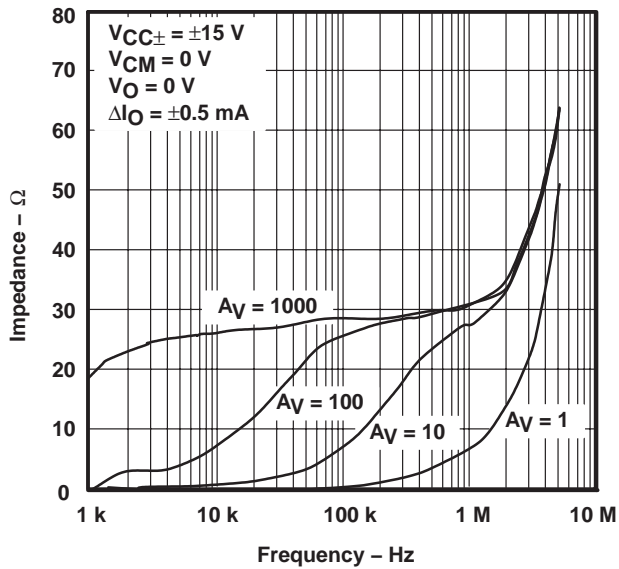


Figure 1

**TOTAL HARMONIC DISTORTION  
VS  
FREQUENCY**

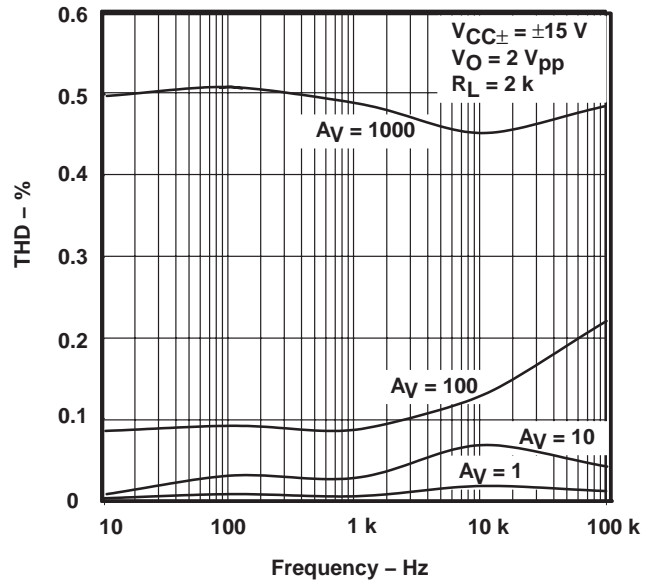


Figure 2

**GAIN AND PHASE  
VS  
FREQUENCY**

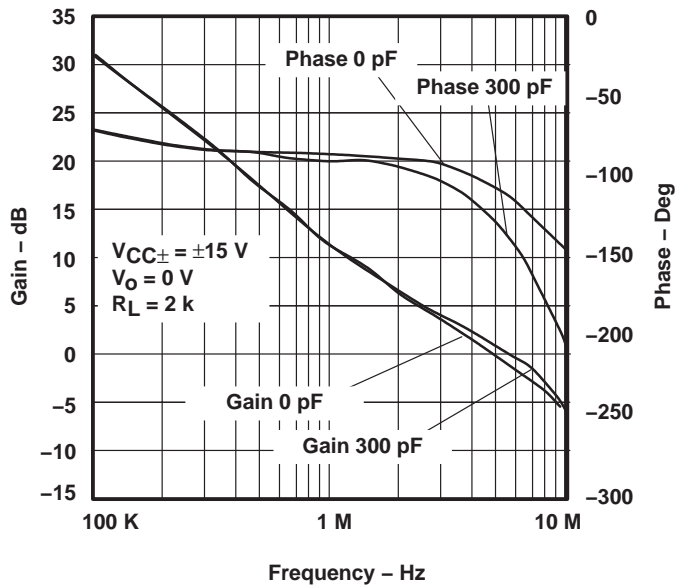


Figure 3

**NORMALIZED INPUT BIAS CURRENT  
VS  
TEMPERATURE**

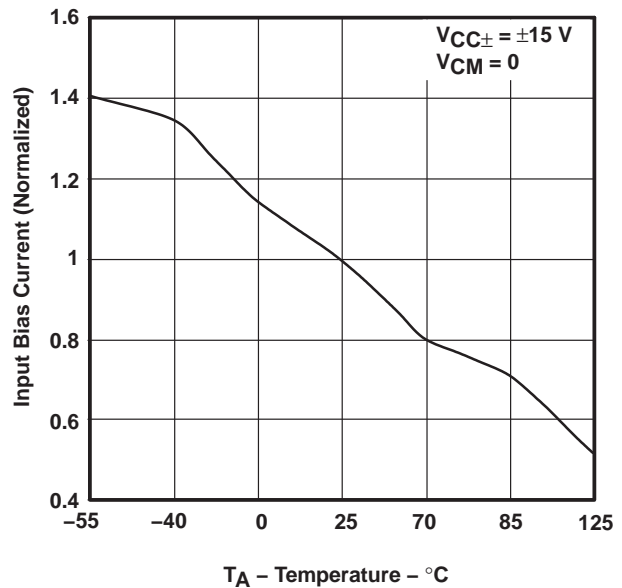


Figure 4



**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

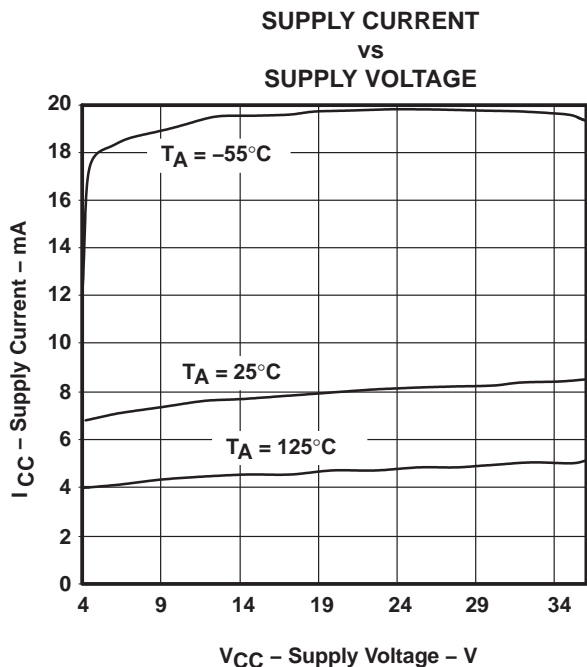


Figure 5

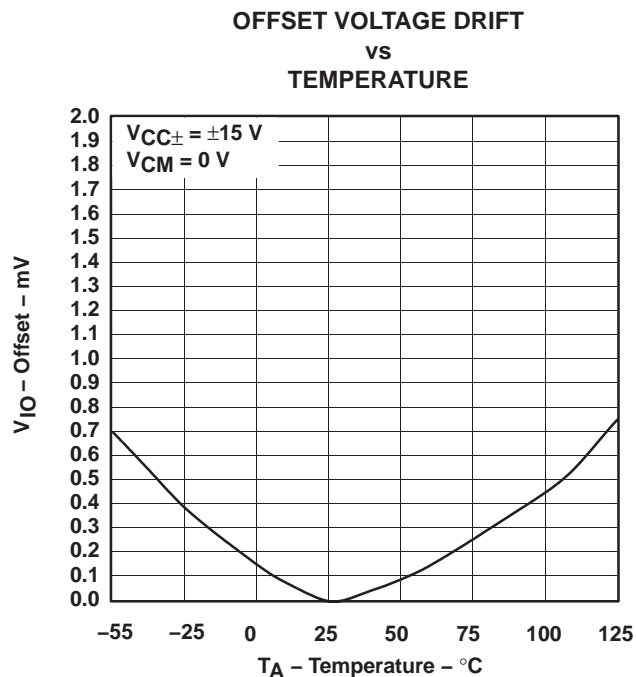


Figure 6

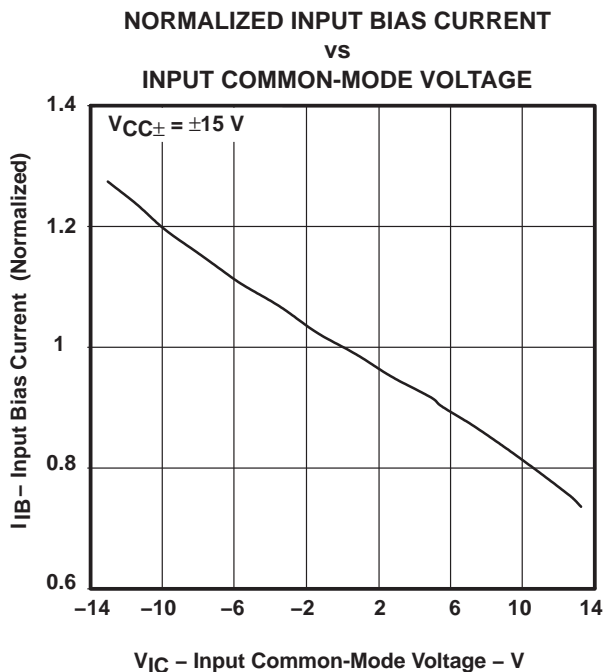


Figure 7

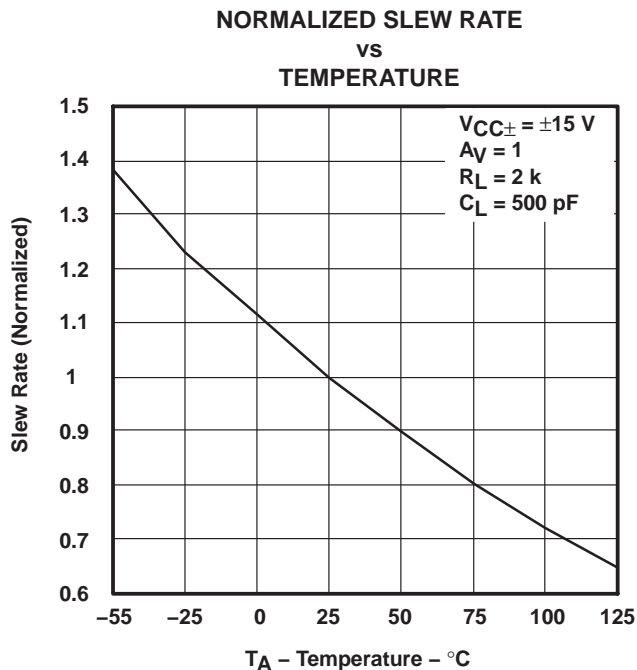


Figure 8

# TL3474, TL3474A HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

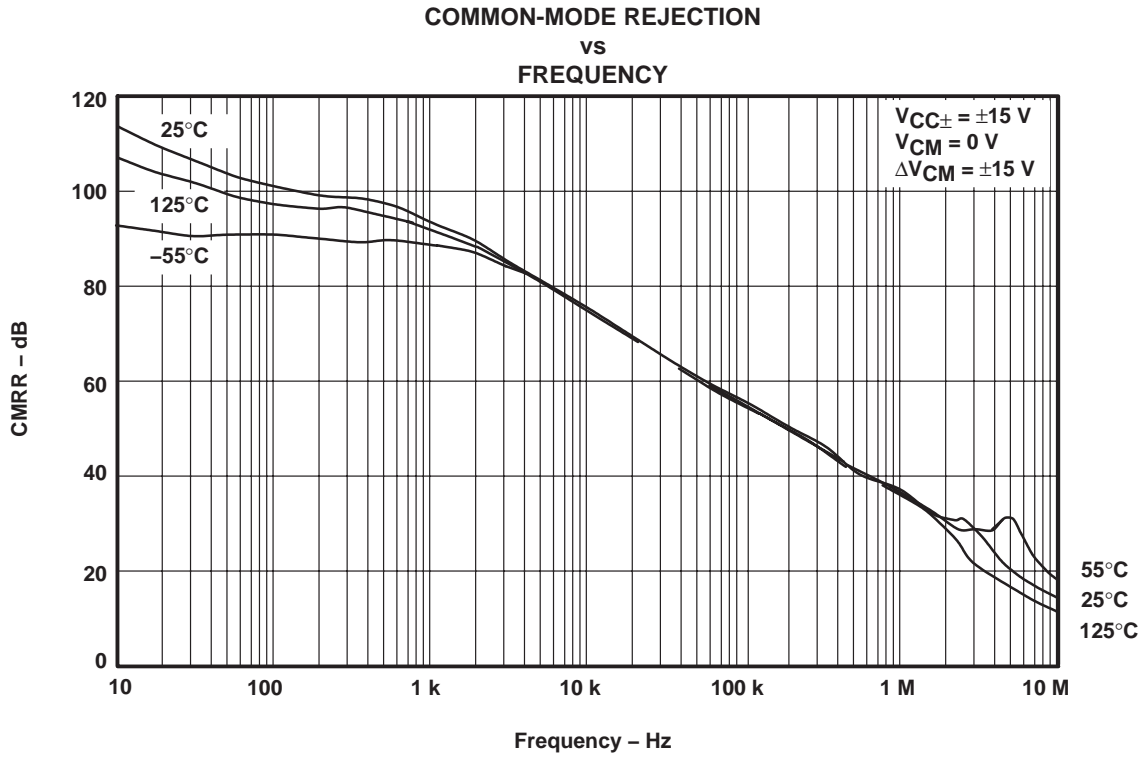


Figure 9



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TL3474ACDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474A
<a href="#">TL3474ACN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474ACN
<a href="#">TL3474ACPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T3474A
<a href="#">TL3474AID</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 105	TL3474AI
<a href="#">TL3474AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474AI
<a href="#">TL3474AIN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474AIN
<a href="#">TL3474AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474A
<a href="#">TL3474CD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	TL3474C
<a href="#">TL3474CDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3474C
<a href="#">TL3474CN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3474CN
<a href="#">TL3474CPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	T3474
<a href="#">TL3474ID</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 105	TL3474I
<a href="#">TL3474IDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TL3474I
<a href="#">TL3474IN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3474IN
<a href="#">TL3474IPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3474

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3474ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL3474IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3474ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474ACPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL3474ACPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474AIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IDR	SOIC	D	14	2500	356.0	356.0	35.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL3474IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL3474ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474CN	N	PDIP	14	25	506	13.97	11230	4.32
TL3474IN	N	PDIP	14	25	506	13.97	11230	4.32



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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