

TCA9543A 具有中断逻辑电路和复位功能的低压 2 通道 I²C 总线开关

1 特性

- 2 选 1 双向转换开关
- 与 I²C 总线和系统管理总线 (SMBus) 兼容
- 两个低电平有效中断输入
- 低电平有效中断输出
- 低电平有效复位输入
- 两个地址引脚，允许在 I²C 总线上支持多达四个 TCA9543A 器件
- 通过 I²C 总线进行通道选择，可任意组合
- 上电时所有开关通道取消选定
- 低 R_{ON} 开关
- 支持在 1.8V、2.5V、3.3V 和 5V 总线间进行电压电平转换
- 上电时无干扰
- 支持热插入
- 低待机电流
- 工作电源电压范围为 1.65V 至 5.5V
- 5.5V 耐压输入
- 0 至 400kHz 时钟频率
- 闩锁性能超过 100mA，符合 JESD78 规范
- ESD 保护性能超过 JESD 22 规范要求
 - 4000V 人体放电模型 (A114-A)
 - 1500V 充电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 工厂自动化
- 具有 I²C 从器件地址冲突（多个完全一样的温度传感器）的产品

3 说明

TCA9543A 是一款由 I²C 总线控制的双路双向转换开关。串行时钟/串行数据 (SCL/SDA) 上行对扩展到 2 个下行对，或者通道。根据可编程控制寄存器的内容，可选择任一单独的 SC_n/SD_n 通道或者这两个通道。提供两个中断输入 ($\overline{INT1}$ - $\overline{INT0}$)，每个中断输入针对一个下行对。一个中断输出 (\overline{INT}) 可作为两个中断输入的与 (AND) 操作。

一个低电平有效复位 (\overline{RESET}) 输入使得 TCA9543A 能够在其中一个下行 I²C 总线长时间处于低电平的情况下恢复。将 \overline{RESET} 下拉为低电平会使 I²C 状态机复位，并且使这两个通道取消选中，这一功能与内部加电复位功能的作用一样。

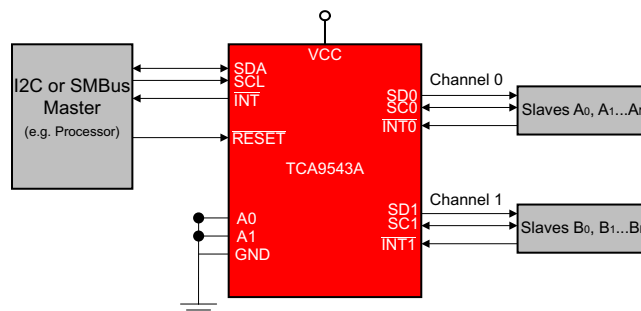
在开关上建有导通栅极，这样的话，VCC 引脚可被用于限制将由 TCA9543A 传递的最大高压。这允许在每个对上使用不同的总线电压，以便 1.8V、2.5V 或 3.3V 部件可以在没有任何额外保护的情况下与 5V 部件通信。对于每个通道，外部上拉电阻器将总线电压上拉至所需的电压水平。所有 I/O 引脚可耐受 5.5V 电压。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|----------|------------|-----------------|
| TCA9543A | TSSOP (14) | 5.00mm × 4.40mm |
| | SOIC (14) | 8.65mm × 3.91mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用示意图



目录

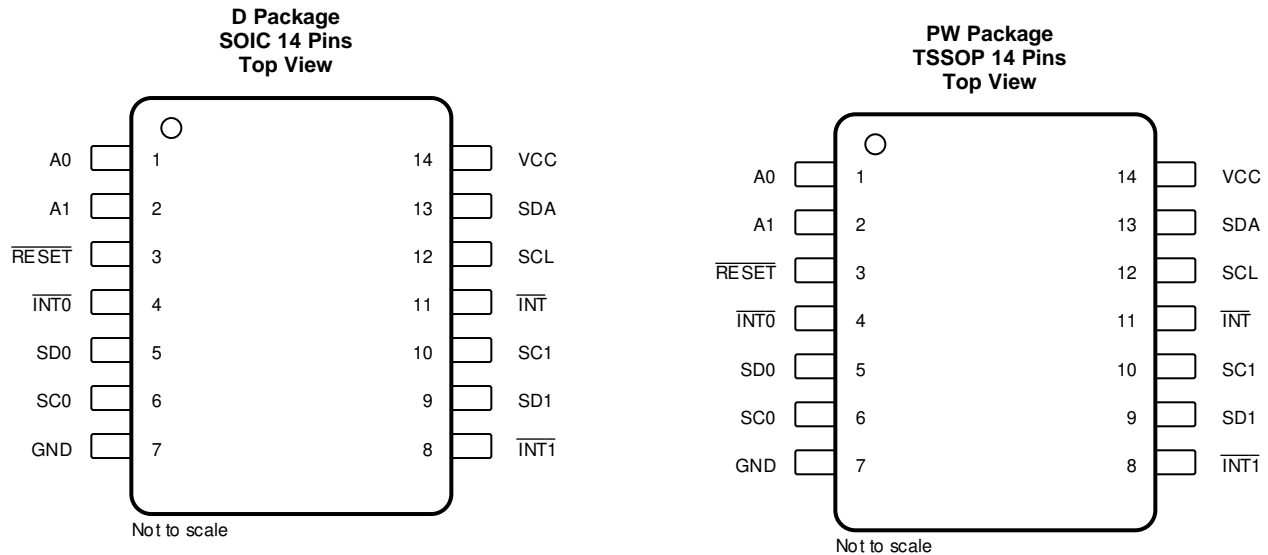
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4 修订历史记录

| Changes from Revision A (February 2015) to Revision B | Page |
|---|-------------|
| • Changed the Pin Configuration images appearance | 3 |
| • Changed $V_{CC} = 3.3\text{ V}$ to $V_{CC} = 2.5\text{ V}$ in Figure 16 | 17 |

| Changes from Original (September 2012) to Revision A | Page |
|--|-------------|
| • 已添加 添加了引脚配置和功能 部分、ESD 额定值表、特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 | 1 |
| • 已添加 向数据表添加了 D 封装 | 1 |
| • Changed Handling Ratings table to ESD Ratings | 4 |
| • Added D package to the Thermal Information table. | 4 |

5 Pin Configuration and Functions



Pin Functions

| PIN | | DESCRIPTION |
|-----|---------------------------|--|
| NO. | NAME | |
| 1 | A0 | Address input 0. Connect directly to V_{CC} or ground. |
| 2 | A1 | Address input 1. Connect directly to V_{CC} or ground. |
| 3 | $\overline{\text{RESET}}$ | Active-low reset input. Connect to V_{CC} or $V_{DPUM}^{(1)}$ through a pull-up resistor, if not used. |
| 4 | $\overline{\text{INT0}}$ | Active-low interrupt input 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor. |
| 5 | SD0 | Serial data 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor. |
| 6 | SC0 | Serial clock 0. Connect to $V_{DPU0}^{(1)}$ through a pull-up resistor. |
| 7 | GND | Ground |
| 8 | $\overline{\text{INT1}}$ | Active-low interrupt input 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor. |
| 9 | SD1 | Serial data 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor. |
| 10 | SC1 | Serial clock 1. Connect to $V_{DPU1}^{(1)}$ through a pull-up resistor. |
| 11 | $\overline{\text{INT}}$ | Active-low interrupt output. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor. |
| 12 | SCL | Serial clock line. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor. |
| 13 | SDA | Serial data line. Connect to $V_{DPUM}^{(1)}$ through a pull-up resistor. |
| 14 | VCC | Supply power |

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I²C reference voltage while V_{DPU0} and V_{DPU1} are the slave channel reference voltages.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--------------------------------------|------|------|------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| I _I | Input current | | ±20 | mA |
| I _O | Output current | | ±25 | mA |
| | Continuous current through VCC | | ±100 | mA |
| | Continuous current through GND | | ±100 | mA |
| P _{tot} | Total power dissipation | | 400 | mW |
| T _A | Operating free-air temperature range | -40 | 85 | °C |
| T _{stg} | Storage temperature range | -60 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±4000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------|---------------------------|-----------------------|-----------------------|
| V _{CC} | Supply voltage | 1.65 | 5.5 | V |
| V _{IH} | High-level input voltage | SCL, SDA | 0.7 × V _{CC} | 6 |
| | | A1, A0, INT1, INT0, RESET | 0.7 × V _{CC} | V _{CC} + 0.5 |
| V _{IL} | Low-level input voltage | SCL, SDA | -0.5 | 0.3 × V _{CC} |
| | | A1, A0, INT1, INT0, RESET | -0.5 | 0.3 × V _{CC} |
| T _A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | TCA9543A | | UNIT | |
|-------------------------------|--|---------|-------|------|
| | PW | D | | |
| | 14 PINS | 14 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 130.9 | 102.8 | °C/W |
| R _{θJctop} | Junction-to-case (top) thermal resistance | 59.2 | 63.9 | |
| R _{θJB} | Junction-to-board thermal resistance | 72.7 | 57.1 | |
| ψ _{JT} | Junction-to-top characterization parameter | 10.5 | 26.7 | |
| ψ _{JB} | Junction-to-board characterization parameter | 72.1 | 56.8 | |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽²⁾ | MAX | UNIT | | | |
|-------------------|---|---|--|--|--------------------|-------|------|------|------|-----|
| V _{PORR} | Power-on reset voltage, VCC rising | No load: V _I = V _{CC} or GND ⁽³⁾ | | | 1.2 | 1.5 | V | | | |
| V _{PORF} | Power-on reset voltage, VCC falling ⁽⁴⁾ | No load: V _I = V _{CC} or GND ⁽³⁾ | | 0.8 | 1 | | V | | | |
| V _{pass} | Switch output voltage | V _{SWin} = V _{CC} , I _{SWout} = -100 μA | 5 V | | 3.6 | | V | | | |
| | | | 4.5 V to 5.5 V | | 2.6 | 4.5 | | | | |
| | | | 3.3 V | | 1.9 | | | | | |
| | | | 3 V to 3.6 V | | 1.6 | 2.8 | | | | |
| | | | 2.5 V | | 1.4 | | | | | |
| | | | 2.3 V to 2.7 V | | 1.0 | 1.8 | | | | |
| | | | 1.8 V | | 0.8 | | | | | |
| | | | 1.65 V to 1.95 V | 0.5 | | 1.1 | | | | |
| I _{OH} | $\overline{\text{INT}}$ | V _O = V _{CC} | 1.65 V to 5.5 V | | | 10 | μA | | | |
| I _{OL} | SDA | V _{OL} = 0.4 V | 1.65 V to 5.5 V | 3 | 7 | | mA | | | |
| | | V _{OL} = 0.6 V | | 6 | 10 | | | | | |
| | $\overline{\text{INT}}$ | V _{OL} = 0.4 V | | 3 | | | | | | |
| I _I | SCL, SDA | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | -1 | | 1 | μA | | | |
| | SC1–SC0, SD1–SD0 | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | -1 | | 1 | | | | |
| | A1, A0 | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | -1 | | 1 | | | | |
| | $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | -1 | | 1 | | | | |
| | $\overline{\text{RESET}}$ | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | -1 | | 1 | | | | |
| I _{CC} | Operating mode | f _{SCL} = 400 kHz | V _I = V _{CC} or GND ⁽³⁾ | 5.5 V | | 50 | μA | | | |
| | | | I _O = 0 | 3.6 V | | 20 | | | | |
| | | | t _{r,max} = 300 ns | 2.7 V | | 11 | | | | |
| | | | | 1.65 V | | 6 | | | | |
| | | | f _{SCL} = 100 kHz | V _I = V _{CC} or GND ⁽³⁾ | 5.5 V | | | 35 | | |
| | | | | I _O = 0 | 3.6 V | | | 14 | | |
| | | | | t _{r,max} = 1 μs | 2.7 V | | | 5 | | |
| | | 1.65 V | | | 2 | | | | | |
| | Standby mode | Low inputs | V _I = GND ⁽³⁾ | I _O = 0 | 5.5 V | | | 1.6 | 2 | |
| | | | | | 3.6 V | | | 1.0 | 1.3 | |
| | | | | | 2.7 V | | | 0.7 | 1.1 | |
| | | | | | 1.65 V | | | 0.4 | 0.55 | |
| | | High inputs | V _I = V _{CC} | I _O = 0 | | 5.5 V | | | 1.6 | 2 |
| | | | | | | 3.6 V | | | 1.0 | 1.3 |
| | | | | | 2.7 V | | 0.7 | 1.1 | | |
| | | | | | 1.65 V | | 0.4 | 0.55 | | |
| ΔI _{CC} | Supply-current change | $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ | One $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ input at 0.6 V, Other inputs at V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | | 3 | 20 | | | |
| | | | One $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND ⁽³⁾ | | | 3 | 20 | | | |
| | | SCL, SDA | SCL or SDA input at 0.6 V, Other inputs at V _{CC} or GND ⁽³⁾ | | | 2 | 15 | | | |
| | | | SCL or SDA input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND ⁽³⁾ | | | 2 | 15 | | | |

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.

(3) $\overline{\text{RESET}}$ = V_{CC} (held high) when all other input voltages, V_I = GND

(4) The power-on reset circuit resets the I²C bus logic when V_{CC} < V_{PORF}.

Electrical Characteristics⁽¹⁾ (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-------------------------------------|---|---|------------------|-----|--------------------|-----|------|
| C _i | A1, A0 | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | 4.5 | 6 | | pF |
| | $\overline{\text{INT1}}\text{--}\overline{\text{INT0}}$ | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | 4.5 | 6 | | |
| | $\overline{\text{RESET}}$ | V _I = V _{CC} or GND ⁽³⁾ | 1.65 V to 5.5 V | 4.5 | 5.5 | | |
| C _{io(OFF)} ⁽⁵⁾ | SCL, SDA | V _I = V _{CC} or GND ⁽³⁾ , Switch OFF | 1.65 V to 5.5 V | 15 | 19 | | pF |
| | SC1–SC0, SD1–SD0 | | | 6 | 8 | | |
| R _{ON} | Switch on-state resistance | V _O = 0.4 V, I _O = 15 mA | 4.5 V to 5.5 V | 4 | 10 | 16 | Ω |
| | | | 3 V to 3.6 V | 5 | 13 | 20 | |
| | | V _O = 0.4 V, I _O = 10 mA | 2.3 V to 2.7 V | 7 | 16 | 45 | |
| | | | 1.65 V to 1.95 V | 10 | 25 | 70 | |

 (5) C_{io(ON)} depends on the device capacitance and load that is downstream from the device.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| | | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNIT |
|------------------------|--|---|------|---------------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{scl} | I ² C clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{sch} | I ² C clock high time | 4 | | 0.6 | | μs |
| t _{scl} | I ² C clock low time | 4.7 | | 1.3 | | μs |
| t _{sp} | I ² C spike time | | 50 | | 50 | ns |
| t _{sds} | I ² C serial-data setup time | 250 | | 100 | | ns |
| t _{sdh} | I ² C serial-data hold time | 0 ⁽¹⁾ | | 0 ⁽¹⁾ | | μs |
| t _{icr} | I ² C input rise time | | 1000 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{icf} | I ² C input fall time | | 300 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{ocf} | I ² C output fall time | 10-pF to 400-pF bus | 300 | 20 + 0.1C _b ⁽²⁾ | 300 | ns |
| t _{buf} | I ² C bus free time between stop and start | 4.7 | | 1.3 | | μs |
| t _{sts} | I ² C start or repeated start condition setup | 4.7 | | 0.6 | | μs |
| t _{sth} | I ² C start or repeated start condition hold | 4 | | 0.6 | | μs |
| t _{sps} | I ² C stop condition setup | 4 | | 0.6 | | μs |
| t _{vdL(Data)} | Valid-data time (high to low) ⁽³⁾ | SCL low to SDA output low valid | 1 | | 1 | μs |
| t _{vdH(Data)} | Valid-data time (low to high) ⁽³⁾ | SCL low to SDA output high valid | 0.6 | | 0.6 | μs |
| t _{vd(ack)} | Valid-data time of ACK condition | ACK signal from SCL low to SDA output low | 1 | | 1 | μs |
| C _b | I ² C bus capacitive load | | 400 | | 400 | pF |

 (1) A device internally must provide a hold time of at least 300-ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

 (2) C_b = total bus capacitance of one bus line in pF

(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 5)

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see [Figure 7](#))

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|----------------|---|-----------------------------------|------------------|-----|-----|---------|
| $t_{pd}^{(1)}$ | Propagation delay time | $R_{ON} = 20 \Omega, C_L = 15$ pF | SDA or SCL | | 0.3 | ns |
| | | $R_{ON} = 20 \Omega, C_L = 50$ pF | | | 1 | |
| t_{iv} | Interrupt valid time ⁽²⁾ | \overline{INTn} | \overline{INT} | | 4 | μ s |
| t_{ir} | Interrupt reset delay time ⁽²⁾ | \overline{INTn} | \overline{INT} | | 2 | μ s |

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) Data taken using a 4.7-k Ω pullup resistor and 100-pF load (see [Figure 7](#))

6.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7](#))

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|---|-----|-----|---------|
| t_{PWRL} | Required low-level pulse duration of \overline{INTn} inputs ⁽¹⁾ | 1 | | μ s |
| t_{PWRH} | Required high-level pulse duration of \overline{INTn} inputs ⁽¹⁾ | 0.5 | | μ s |
| t_{WL} | Pulse duration, \overline{RESET} low | 4 | | ns |
| $t_{rst}^{(2)}$ | \overline{RESET} time (SDA clear) | | 500 | ns |
| t_{REC} | Recovery time from \overline{RESET} to start | 0 | | ns |

(1) The device has interrupt input rejection circuitry for pulses less than the listed minimum.

(2) t_{rst} is the propagation delay measured from the time the \overline{RESET} terminal is first asserted low to the time the SDA terminal is asserted high, signaling a stop condition. It must be a minimum of t_{WL} .

6.9 Typical Characteristics

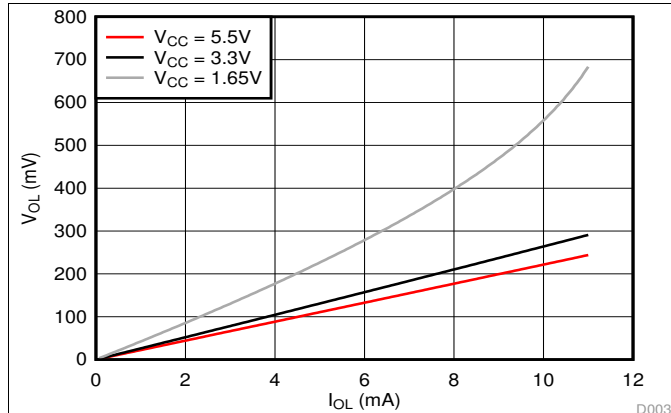


Figure 1. SDA Output Low Voltage (V_{OL}) vs Load Current (I_{OL}) at Three V_{CC} Levels

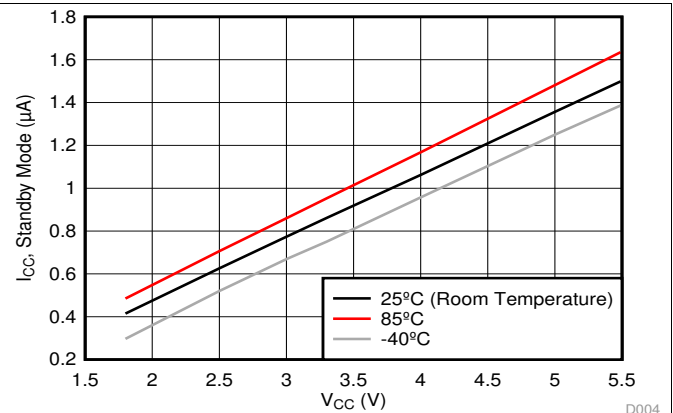


Figure 2. Standby Current (I_{CC}) vs Supply Voltage (V_{CC}) at Three Temperature Points

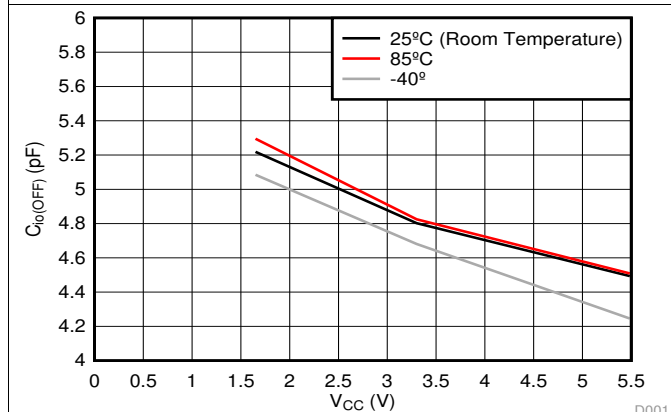


Figure 3. Slave channel (SCn/SDn) capacitance ($C_{io(OFF)}$) vs. Supply Voltage (V_{CC}) at Three Temperature Points

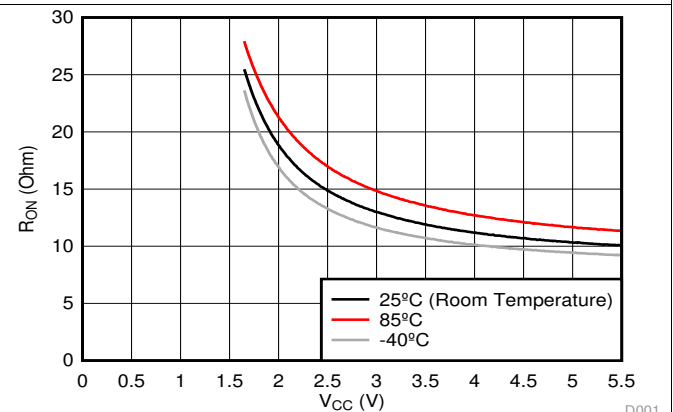
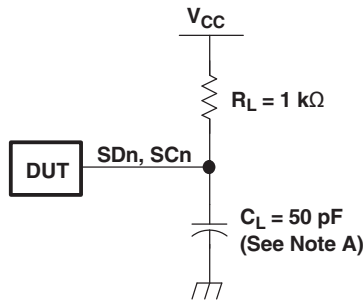
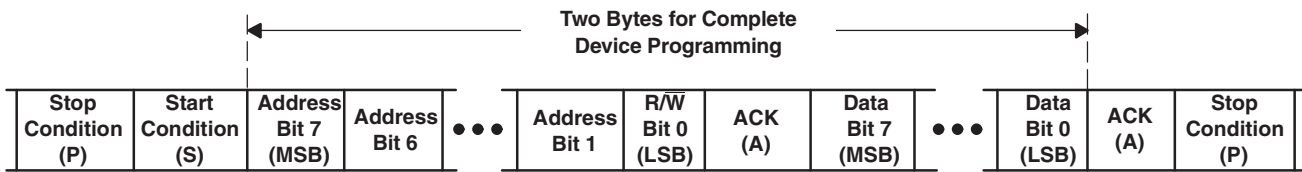


Figure 4. ON-Resistance (R_{ON}) vs Supply Voltage (V_{CC}) at Three Temperatures

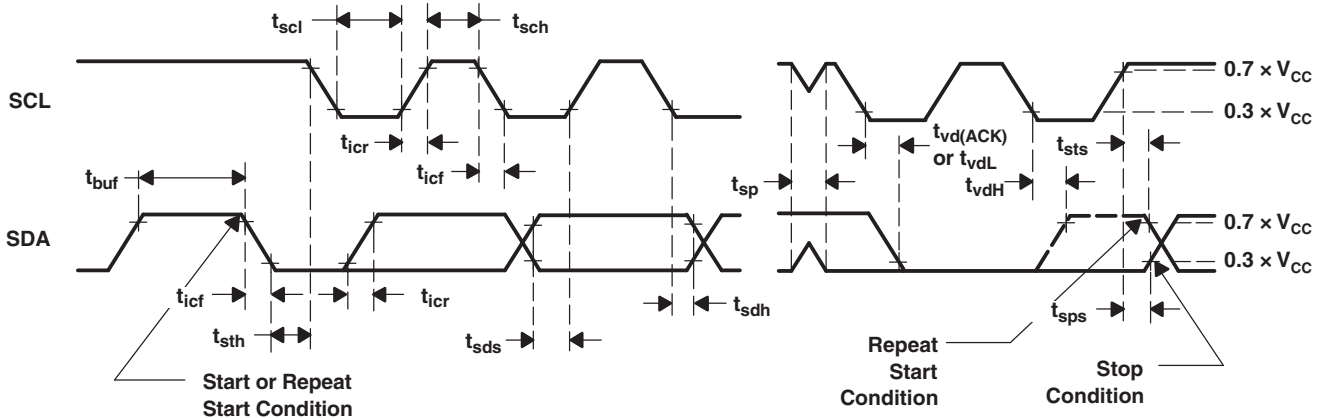
7 Parameter Measurement Information



I²C PORT LOAD CONFIGURATION



| BYTE | DESCRIPTION |
|------|--------------------------------|
| 1 | I ² C address + R/W |
| 2 | Control register data |



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 30 \text{ ns}$.
- C. The outputs are measured one at a time, with one transition per measurement.

Figure 5. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

Parameter Measurement Information (continued)

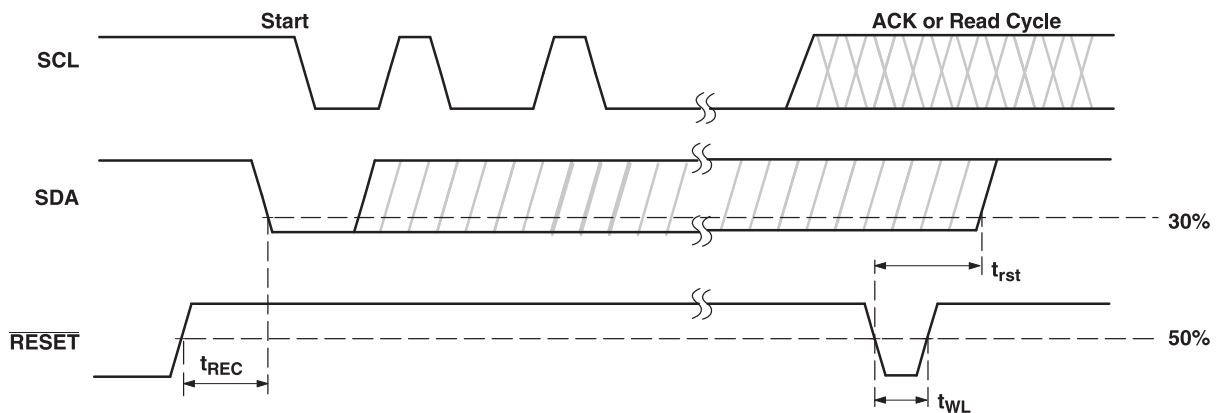
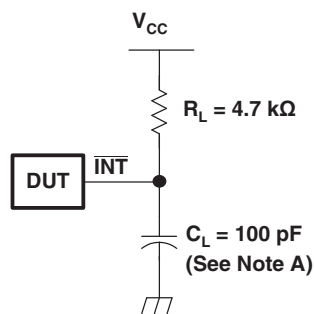
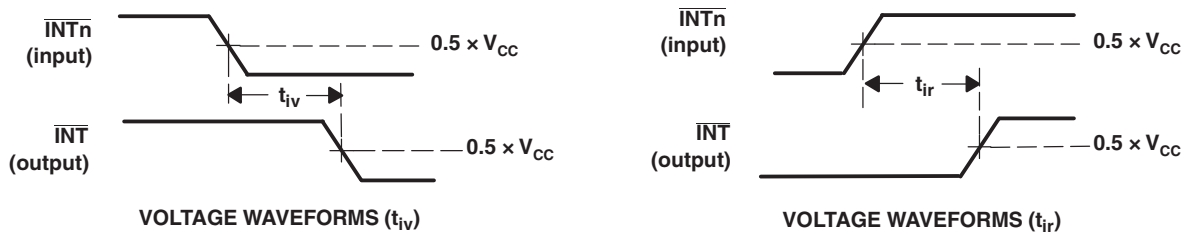


Figure 6. Reset Timing



INTERRUPT LOAD CONFIGURATION



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 30\text{ ns}$.

Figure 7. Interrupt Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

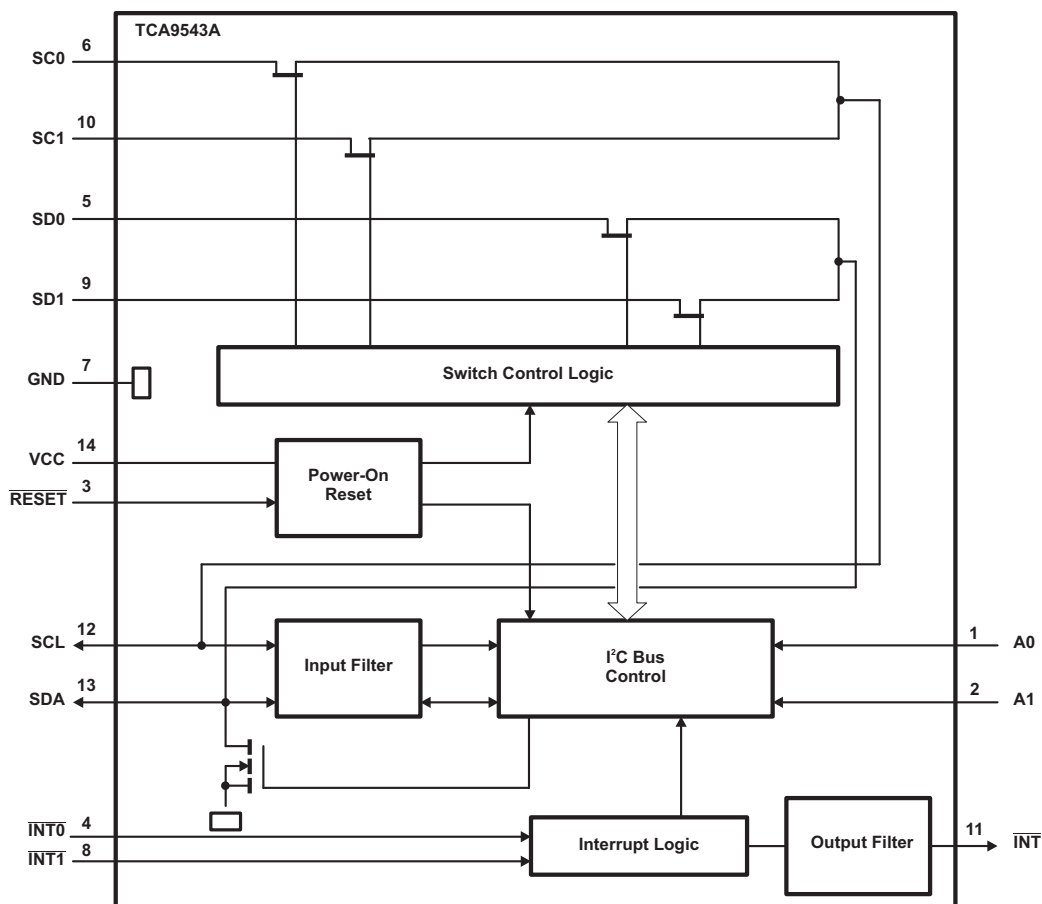
The TCA9543A is a 2-channel, bidirectional translating I²C switch. The master SCL/SDA signal pair is directed to two channels of slave devices, SC0/SD0-SC1/SD1. Either individual downstream channel can be selected as well as both channels. The TCA9543A also supports interrupt signals in order for the master to detect an interrupt on the $\overline{\text{INT}}$ output terminal that can result from any of the slave devices connected to the $\overline{\text{INT1}}$ - $\overline{\text{INT0}}$ input terminals.

The device offers an active-low $\overline{\text{RESET}}$ input which resets the state machine and allows the TCA9543A to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Either using the $\overline{\text{RESET}}$ function or causing a POR will cause both channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with multiple I²C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The TCA9543A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

8.2 Functional Block Diagram



8.3 Feature Description

The TCA9543A is a dual channel bidirectional translating switch for I²C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9543A features I²C control using a single 8-bit control register in which bits 1 and 0 control the enabling and disabling of the two switch channels of I²C data flow. The TCA9543A also supports interrupt signals for each slave channel and this data is held in bits 5 and 4 of the control register. Depending on the application, voltage translation of the I²C bus can also be achieved using the TCA9543A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the TCA9543A can be reset to resume normal operation using the RESET terminal feature or by a power-on reset which results from cycling power to the device.

8.4 Device Functional Modes

8.4.1 RESET Input

The RESET input can be used to recover the TCA9543A from a bus-fault condition. The registers and the I²C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL} . Both channels also are deselected in this case. RESET must be connected to V_{CC} through a pull-up resistor.

8.4.2 Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the TCA9543A in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the TCA9543A registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{PORF} to reset the device.

8.5 Programming

8.5.1 I²C Interface

The I²C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time is interpreted as control signals (see Figure 8).

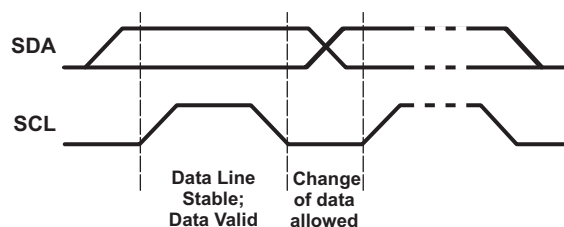


Figure 8. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 9).

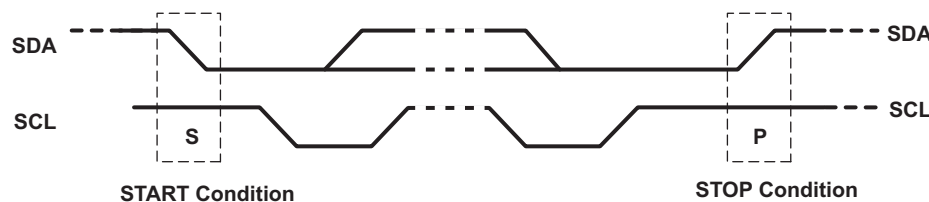


Figure 9. Definition of Start and Stop Conditions

Programming (continued)

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see Figure 10).

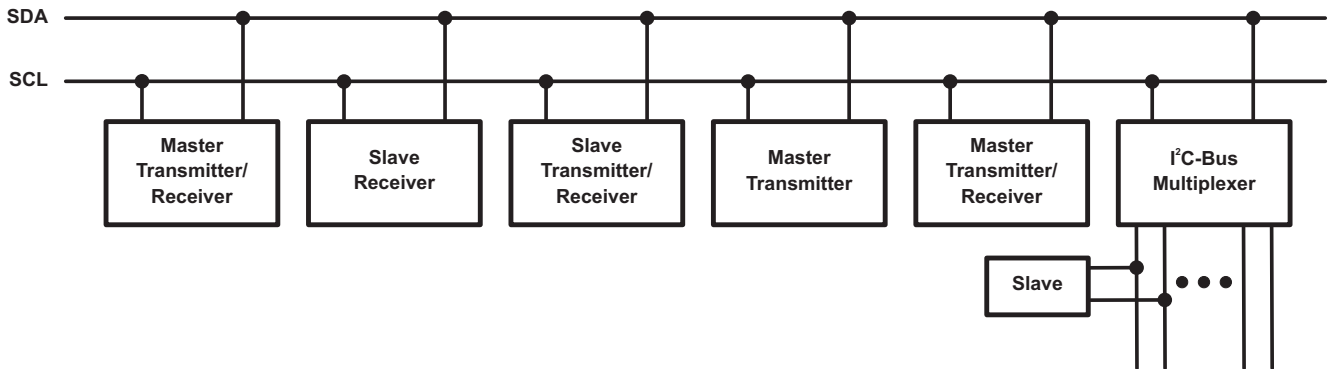


Figure 10. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 11). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

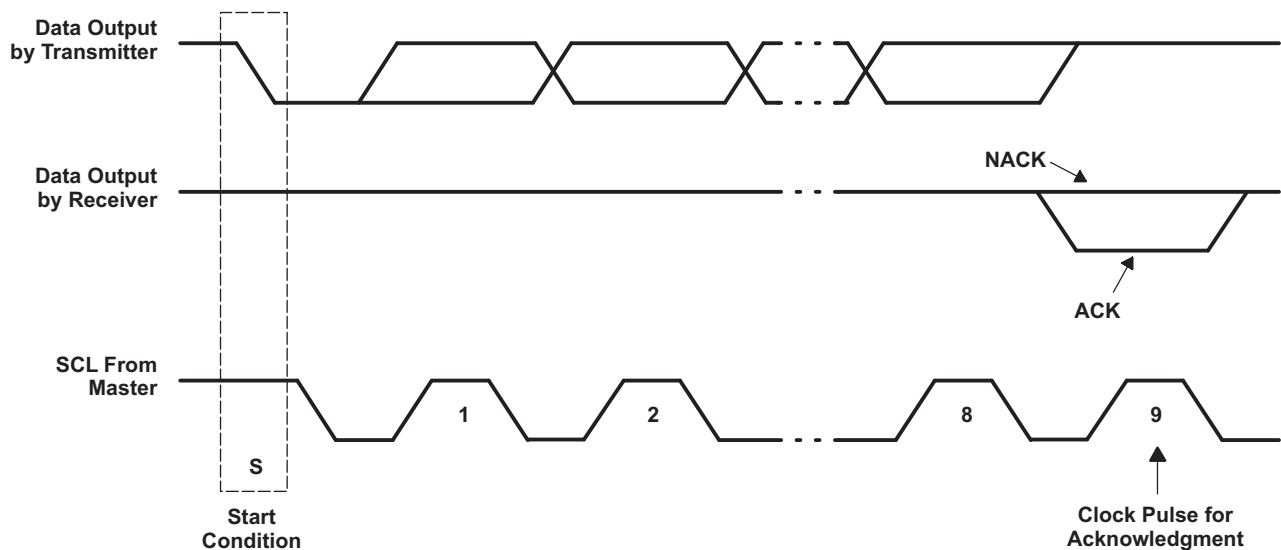


Figure 11. Acknowledgment on I²C Bus

Data is transmitted to the TCA9543A control register using the write mode shown in Figure 12.

Programming (continued)

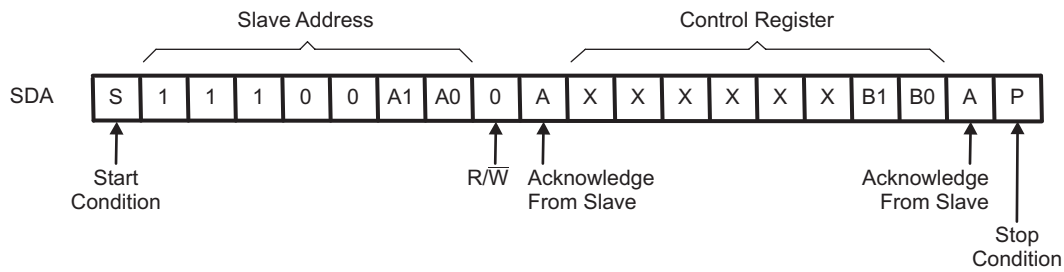


Figure 12. Write Control Register

Data is read from the TCA9543A control register using the read mode shown in Figure 13.

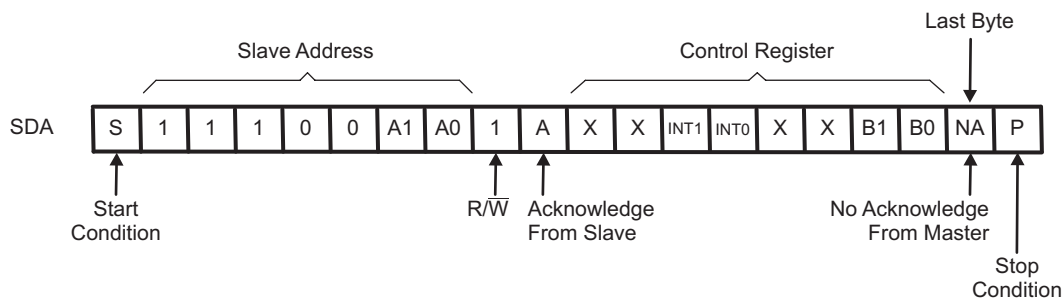


Figure 13. Read Control Register

8.6 Register Maps

8.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the TCA9543A is shown in Figure 14. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address terminals and they must be pulled high or low.

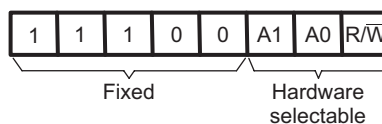


Figure 14. Slave Address TCA9543A

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

8.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TCA9543A, which is stored in the control register (see Figure 15). If multiple bytes are received by the TCA9543A, it saves the last byte received. This register can be written and read via the I²C bus.

Register Maps (continued)

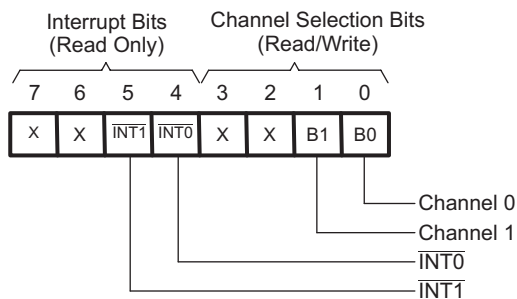


Figure 15. Control Register

8.6.3 Control Register Definition

One or both SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the TCA9543A has been addressed, the control register is written. The two LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)⁽¹⁾

| D7 | D6 | $\overline{\text{INT1}}$ | $\overline{\text{INT0}}$ | D3 | D2 | B1 | B0 | COMMAND |
|----|----|--------------------------|--------------------------|----|----|----|----|---|
| X | X | X | X | X | X | X | 0 | Channel 0 disabled |
| | | | | | | | 1 | Channel 0 enabled |
| X | X | X | X | X | X | 0 | X | Channel 1 disabled |
| | | | | | | 1 | | Channel 1 enabled |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No channel selected; power-up/reset default state |

(1) Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

8.6.4 Interrupt Handling

The TCA9543A provides two interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the TCA9543A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bit 4 and Bit 5 of the control register correspond to the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ inputs of the TCA9543A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the TCA9543A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the TCA9543A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC} through a pull-up resistor.

Table 2. Control Register Read (Interrupt)⁽¹⁾

| D7 | D6 | $\overline{\text{INT1}}$ | $\overline{\text{INT0}}$ | D3 | D2 | B1 | B0 | COMMAND |
|----|----|--------------------------|--------------------------|----|----|----|----|---|
| X | X | X | 0 | X | X | X | X | No interrupt on channel 0 |
| | | | 1 | | | | | Interrupt on channel 0 |
| X | X | 0 | X | X | X | X | X | No interrupt on channel 1 |
| | | 1 | | | | | | Interrupt on channel 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No channel selected; power-up/reset default state |

(1) Two interrupts can be active at the same time.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Applications of the TCA9543A will contain an I²C (or SMBus) master device and up to two I²C slave devices. The downstream channels are ideally used to resolve I²C slave address conflicts. For example, if two identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0 and 1. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and the other channel switched off, the data can be retrieved, and the I²C master can move on and read the next channel.

In an application where the I²C bus will contain many additional slave devices that do not result in I²C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across both channels. If both switches will be enabled simultaneously, additional design requirements must be considered (See [Design Requirements](#) and [Detailed Design Procedure](#)).

9.2 Typical Application

A typical application of the TCA9543A contains anywhere from 1 to 3 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} and V_{DPU1}). In the event where the master device and both slave devices operate at the same voltage, then the pass voltage, $V_{PASS} = V_{DPUX}$. Once the maximum V_{PASS} is known, V_{CC} can be selected easily using [Figure 17](#). In an application where voltage translation is necessary, additional design requirements must be considered (See [Design Requirements](#)).

[Figure 16](#) shows an application in which the TCA9543A can be used.

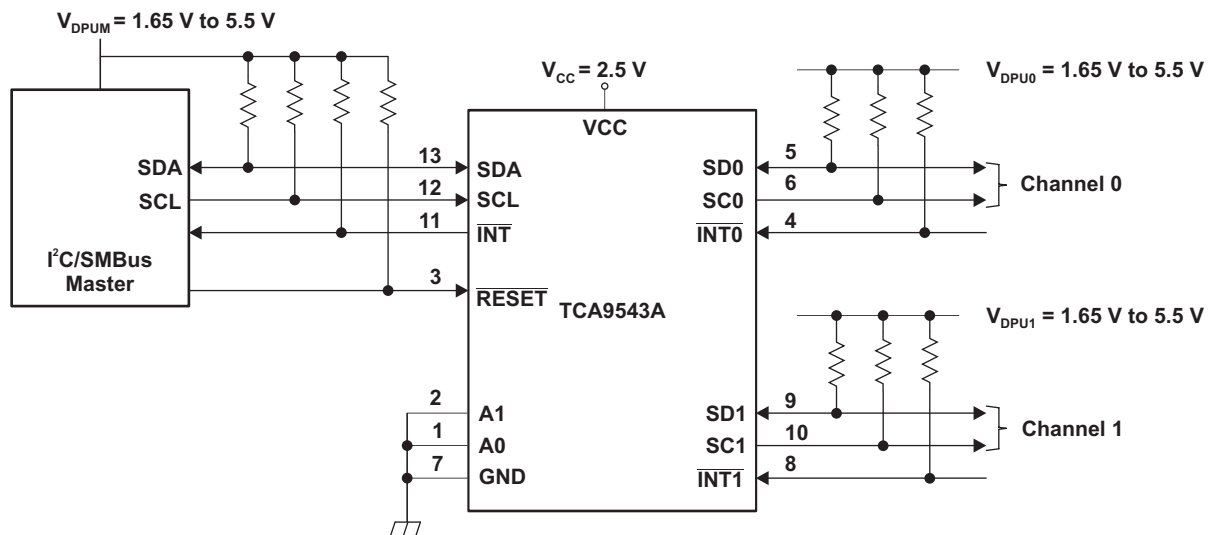


Figure 16. Typical Application Schematic

9.2.1 Design Requirements

The pull-up resistors on the $\overline{INT1}$ - $\overline{INT0}$ terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

Typical Application (continued)

The A0 and A1 terminals are hardware selectable to control the slave address of the TCA9543A. These terminals may be tied directly to GND or V_{CC} in the application.

If both slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p .

The pass-gate transistors of the TCA9543A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

Figure 17 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the TCA9543A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 17, $V_{pass(max)}$ is 2.7 V when the TCA9543A supply voltage is 4 V or lower, so the TCA9543A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 16).

9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX} , $V_{OL(max)}$, and I_{OL} :

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9543A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If both channels will be activated simultaneously, each of the slaves on both channels will contribute to total bus capacitance.

Typical Application (continued)

9.2.3 Application Curves

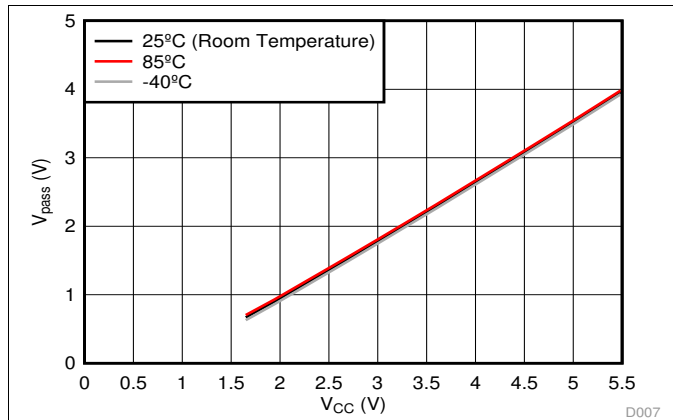
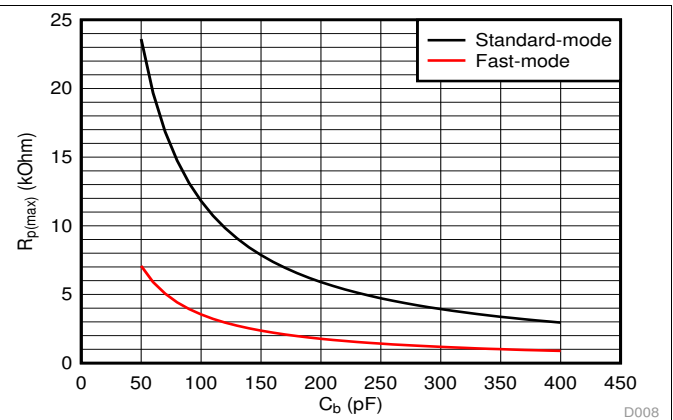
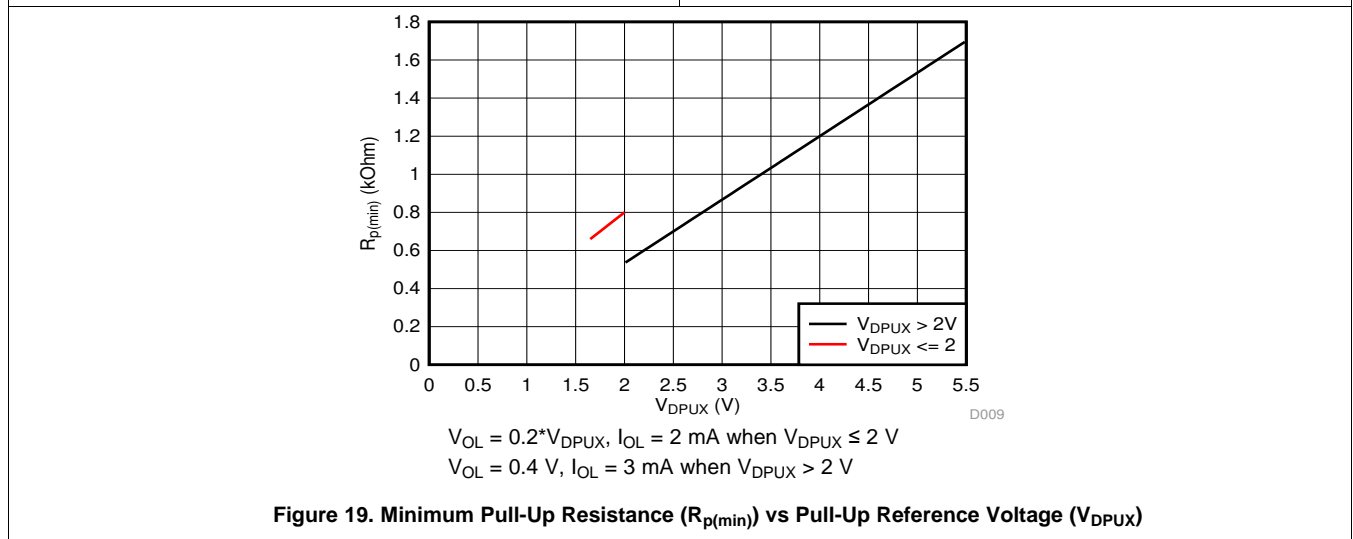


Figure 17. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode (f_{SCL} = 100 kHz, t_r = 1 μs) Fast-mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 18. Maximum Pull-Up Resistance (R_{p(max)}) vs Bus Capacitance (C_b)



V_{OL} = 0.2 * V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
 V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 19. Minimum Pull-Up Resistance (R_{p(min)}) vs Pull-Up Reference Voltage (V_{DPUX})

10 Power Supply Recommendations

The operating power-supply voltage range of the TCA9543A is 1.65-V to 5.5-V applied at the VCC terminal. When the TCA9543A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I²C bus logic is initialized properly.

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9543A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 20.

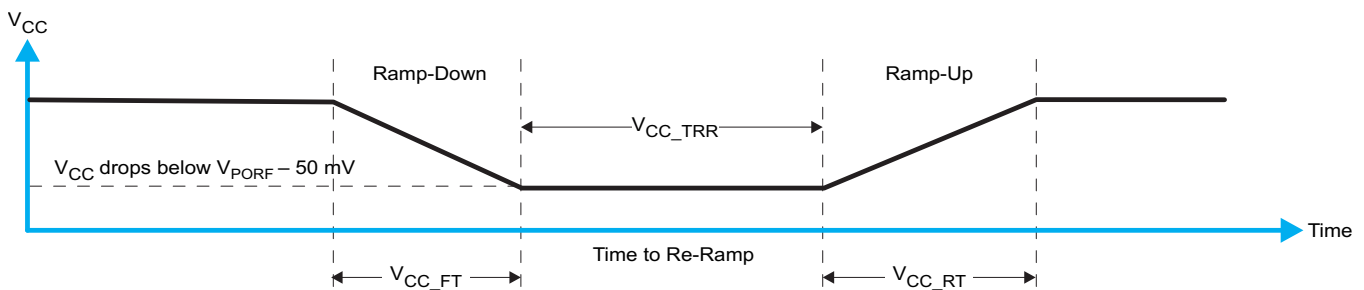


Figure 20. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 3 specifies the performance of the power-on reset feature for TCA9543A for both types of power-on reset.

Table 3. Recommended Supply Sequencing And Ramp Rates⁽¹⁾

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|--|------|-----|------|------|
| V _{CC_FT} | Fall time | 1 | | 100 | ms |
| V _{CC_RT} | Rise time | 0.1 | | 100 | ms |
| V _{CC_TRR} | Time to re-ramp (when V _{CC} drops below V _{PORF(min)} – 50 mV or when V _{CC} drops to GND) | 40 | | | μs |
| V _{CC_GH} | Level that V _{CC} can glitch down to, but not cause a functional disruption when V _{CC_GW} = 1 μs | | | 1.2 | V |
| V _{CC_GW} | Glitch width that will not cause a functional disruption when V _{CC_GH} = 0.5 × V _{CC} | | | 10 | μs |
| V _{PORF} | Voltage trip point of POR on falling V _{CC} | 0.8 | | 1.25 | V |
| V _{PORR} | Voltage trip point of POR on rising V _{CC} | 1.05 | | 1.5 | V |

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 21 and Table 3 provide more information on how to measure these specifications.

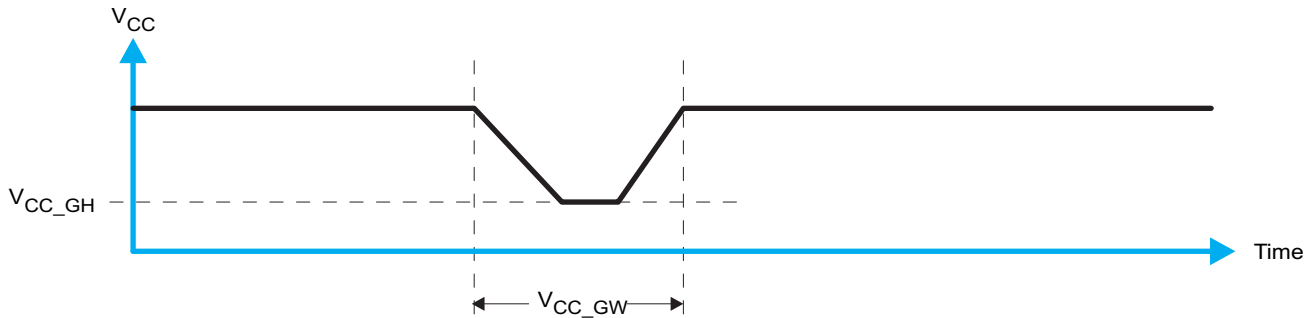


Figure 21. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 22 and Table 3 provide more details on this specification.

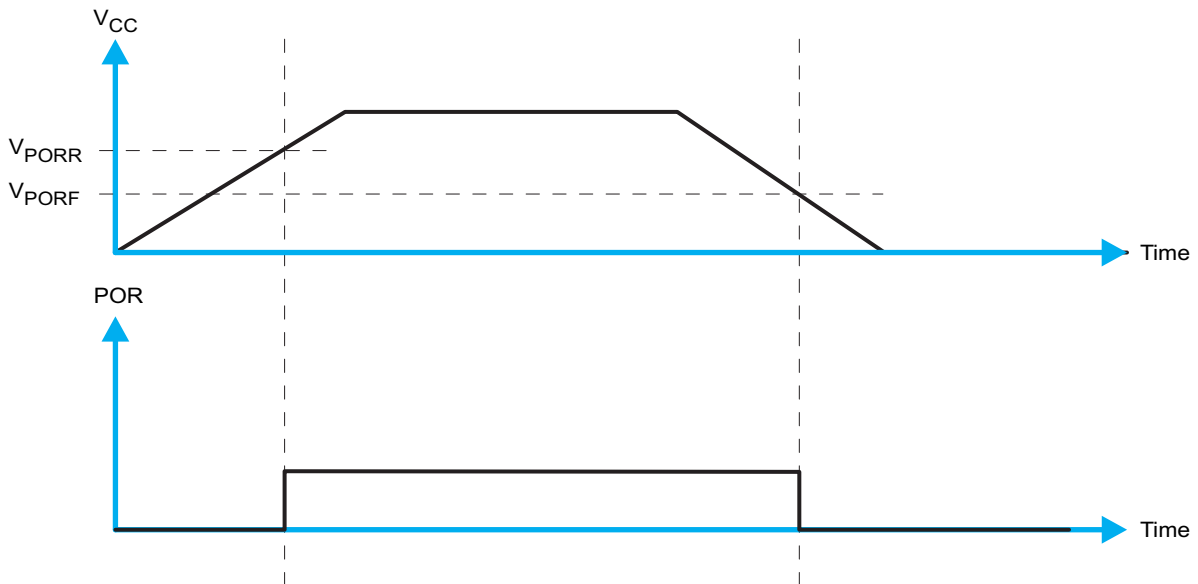


Figure 22. V_{POR}

11 Layout

11.1 Layout Guidelines

For PCB layout of the TCA9543A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane can connect all of the pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM} , V_{DPU0} , and V_{DPU1} , may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn, SDn and \overline{INTn}) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

11.2 Layout Example

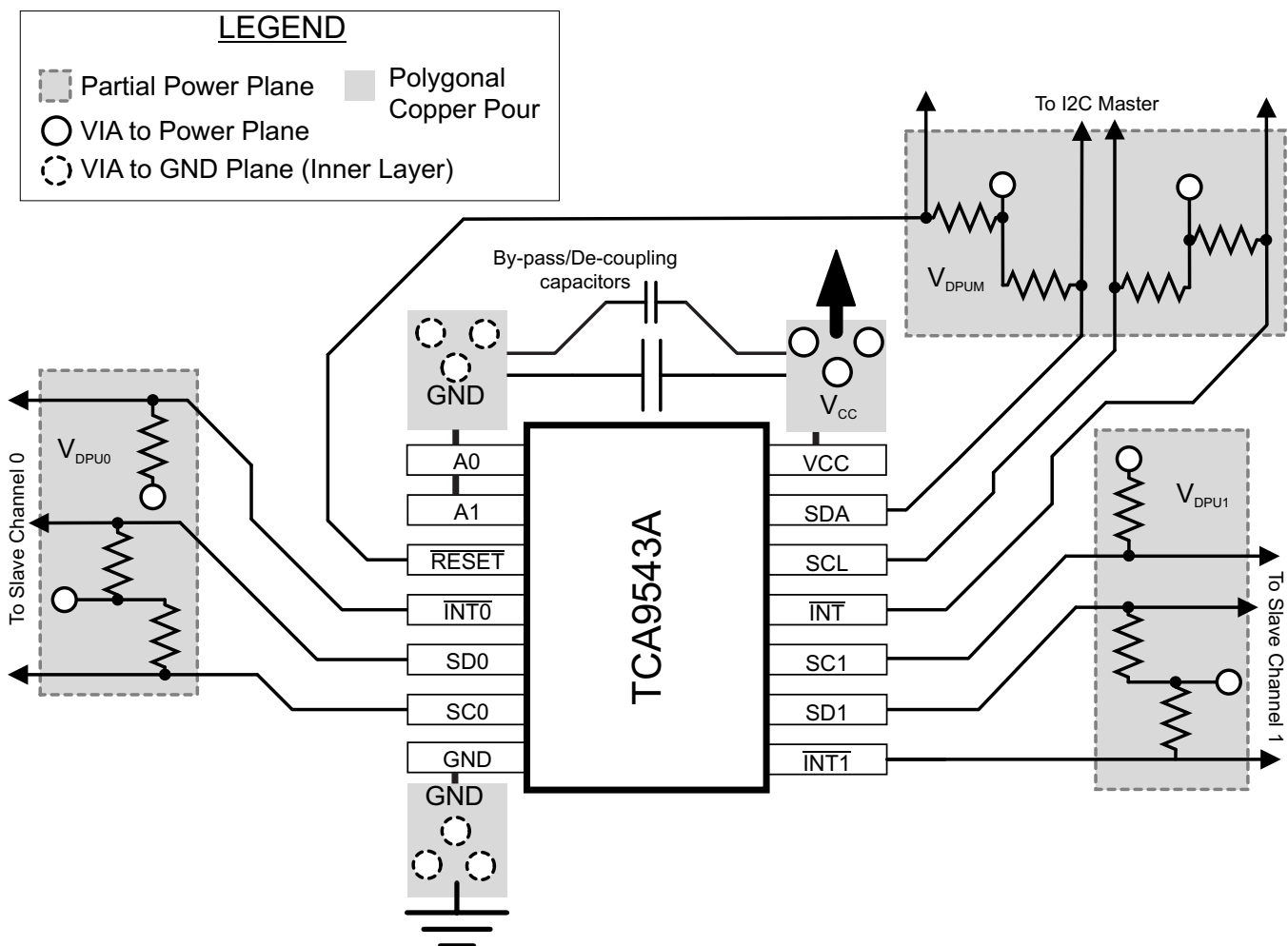


Figure 23. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TCA9543ADR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TCA9543A | Samples |
| TCA9543APWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PW543A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TCA9543ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TCA9543APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TCA9543ADR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TCA9543APWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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