SN65LBC175、SN75LBC175 四通道低功耗差分线路接收器

1 特性

- 符合或超出 EIA 标准 RS-422-A、RS-423-A、RS-485 和 CCITT 建议 V.11
- 可以低至 20ns 的脉冲持续时间运行
- 适用于嘈杂环境中长总线上的多点传输
- 输入灵敏度：±200mV
- 低功耗：20 mA（最大值）
- 开路失效防护设计
- -7 V 至 12V 的共模输入电压范围
- 与 SN75175 和 LTC489 引脚兼容

2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动器

3 说明

SN65LBC175 和 SN75LBC175 是具有三态输出的单片四通道差分线路接收器，旨在满足 EIA 标准 RS-422-A、RS-423-A、RS-485 和 CCITT 建议 V.11 的要求。这个器件针对数据速率高达和超过每秒 10 兆位的平衡多点总线传输进行了优化。接收器采用高电平有效使能输入成对启用。每个差分接收器都输入具有高阻抗、用于提高抗噪性的迟滞，以及在 –12V 至 -7V 共模输入电压范围内 ±200mV 的灵敏度。失效防护设计可确保在输入处于开路状态时，输出始终处于高电平状态。这两款器件都采用 TI 专有 LinBiCMOS™ 技术进行设计，可实现低功耗、高开关速度和稳健性。

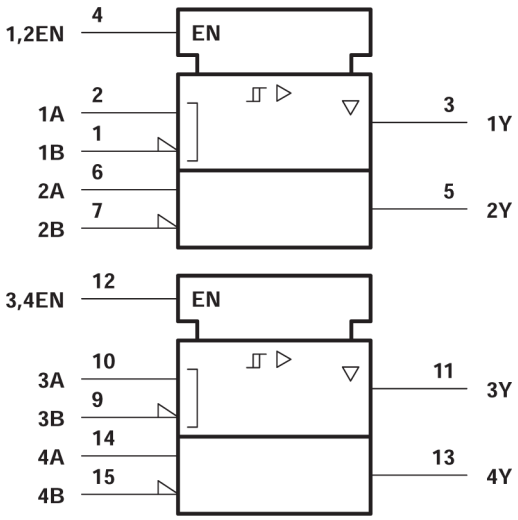
这些器件会在与 SN75LBC172 或 SN75LBC174 四通道线路驱动器配合使用时提供卓越性能。SN65LBC175 采用 16 引脚 DIP (N)、小外形封装 (D) 和宽外形封装 (DW)。SN75LBC175 采用 16 引脚 DIP (N) 和小外形封装 (D)。

SN65LBC175 可在 -40°C 至 85°C 的工业温度范围内运行。SN75LBC175 可在 0°C 至 70°C 的商用温度范围内运行。

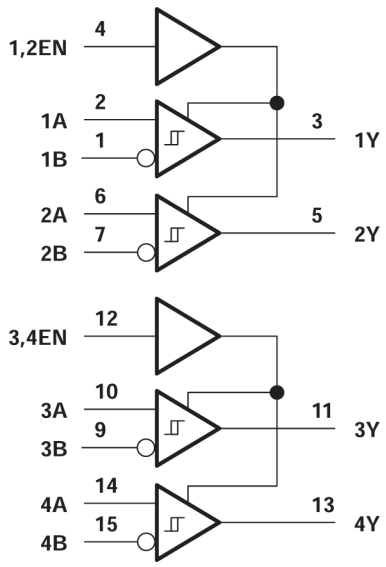
封装信息

器件型号	封装(1)	封装尺寸(2)
SN65LBC175 SN75LBC175	D（SOIC，16）	9.9mm × 6mm
	DW（SOIC，16）	10.3mm × 10.3mm
	N（PDIP、16）	19.3mm × 9.4mm

(1) 有关详细信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

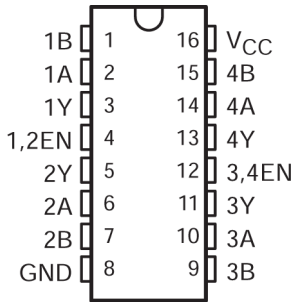

图 4-1. D, DW, or N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Inverting Differential Input
1A	2	I	Channel 1 Non-Inverting Differential Input
1Y	3	O	Channel 1 Output
1,2 EN	4	I	Channel 1 and 2 Active High Enable
2Y	5	O	Channel 2 Output
2A	6	I	Channel 2 Non-Inverting Differential Input
2B	7	I	Channel 2 Inverting Differential Input
GND	8	GND	Device Ground
3B	9	I	Channel 3 Inverting Differential Input
3A	10	I	Channel 3 Non-Inverting Differential Input
3Y	11	O	Channel 3 Output
3,4 EN	12	I	Channel 3 and 4 Active High Enable
4Y	13	O	Channel 4 Output
4A	14	I	Channel 4 Non-Inverting Differential Input
4B	15	I	Channel 4 Inverting Differential Input
V_{CC}	16	POW	Device Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage range		−0.3	7	V
V_I	Input voltage	(A or B inputs)		±25	V
V_{ID} (see (3))	Differential input voltage			±25	V
	Voltage range at Y, 1/2EN, 3/4EN		−0.3	V_{CC} + 0.5	V
	Continuous total dissipation		See Dissipation Rating Table		
T_A	Operating free-air temperature range:	SN65LBC175	−40	85	°C
		SN75LBC175	0	70	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)

5.3 Dissipation Rating Table

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	1100 mW	8.7 mW/°C	709 mW	578 mW
DW	1200 mW	9.6 mW/°C	770 mW	625 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

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5.4 Thermal Information

THERMAL METRIC[1]		SOIC (D)	SOIC (DW)	PDIP (N)	UNIT
		16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.1	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.3	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	EN inputs	2			V
Low-level input voltage, V_{IL}	EN inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A	SN65LBC175	−40		85	°C
	SN75LBC175	0		70	

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5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$V_{IT}+$	Positive-going input threshold voltage		I_O = −8 mA			0.2			V
$V_{IT}-$	Negative-going input threshold voltage		I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT}+ - V_{IT}-$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 8 mA			0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V	0.7		1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V	0.8		1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V	−0.5		−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V	−0.4		−0.8	
I_{IH}	High-level enable input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level enable input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0			−80		−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.7 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See 图 6-1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	30	ns
t_{PZH}	Output enable time to high level	See 图 6-2		17	30	ns
t_{PZL}	Output enable time to low level	See 图 6-3		18	30	ns
t_{PHZ}	Output disable time from high level	See 图 6-2		30	40	ns
t_{PLZ}	Output disable time from low level	See 图 6-3		23	30	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See 图 6-2		4	6	ns
t_t	Transition time	See 图 6-1		3	10	ns

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5.8 Typical Characteristics

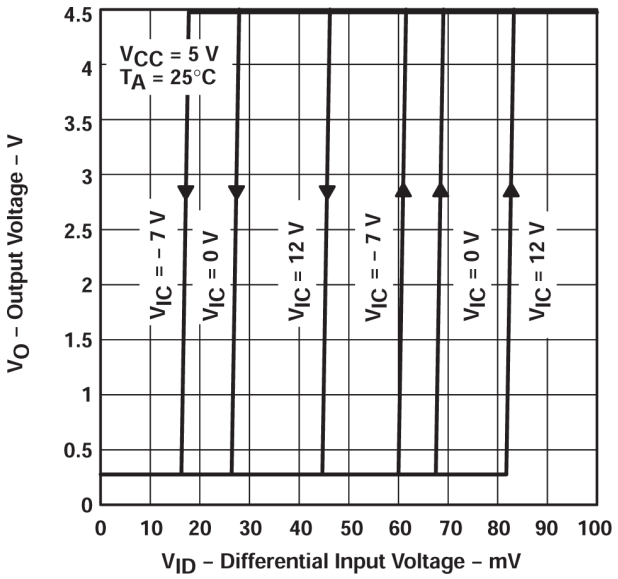

图 5-1. Output Voltage vs Differential Input Voltage

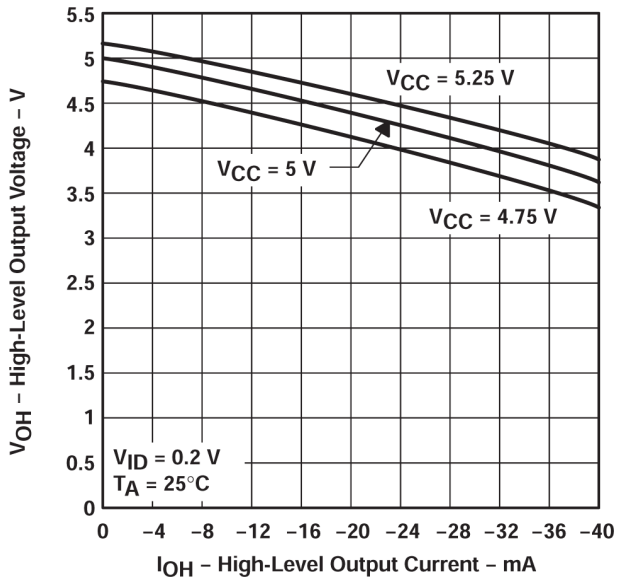

图 5-2. High-level Output Voltage vs High-level Output Current

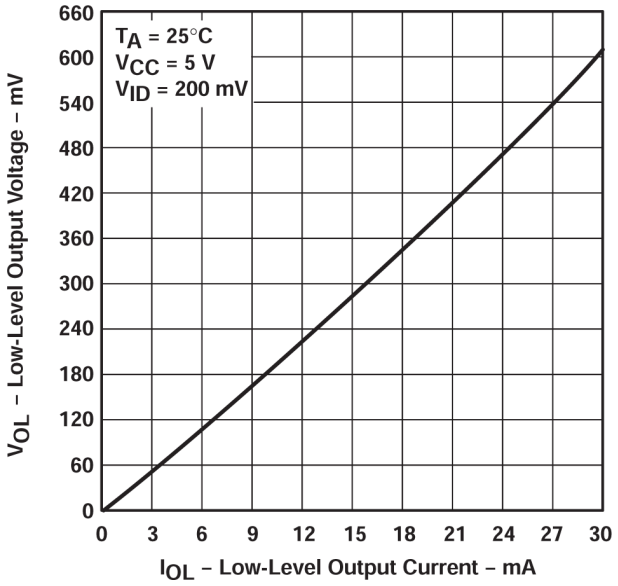

图 5-3. Low-level Output Voltage vs Low-level Output Current

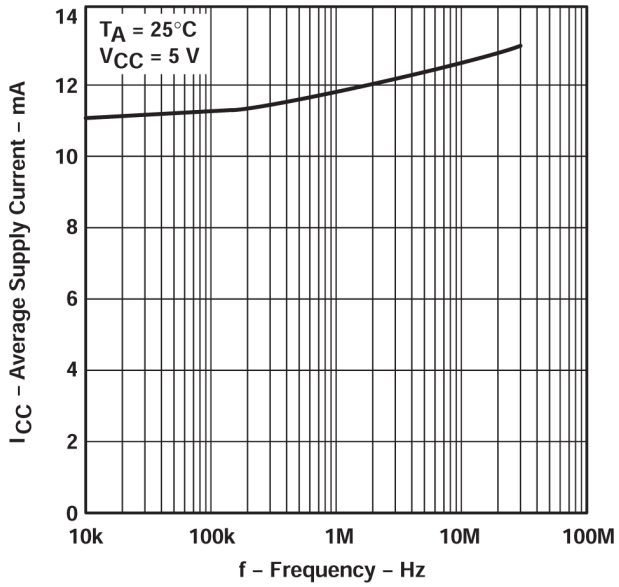

图 5-4. Average Supply Current vs Frequency

5.8 Typical Characteristics (continued)

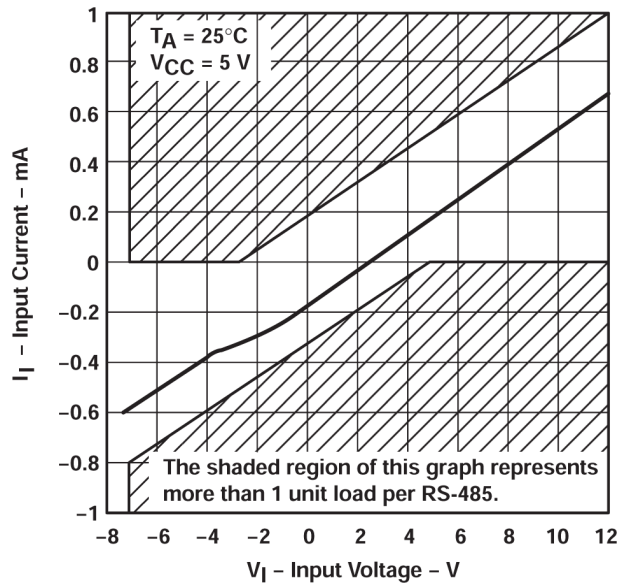

图 5-5. Input Current vs Input Voltage (Complementary Input at 0 v)

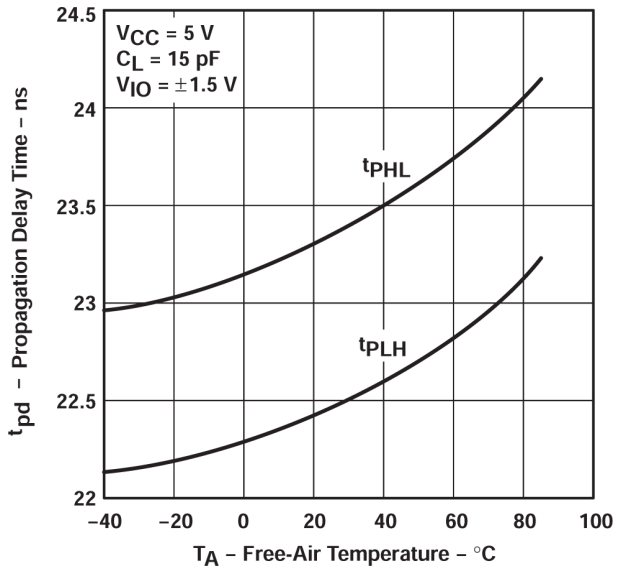

图 5-6. Propagation Delay Time vs Free-air Temperature

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6 Parameter Measurement Information

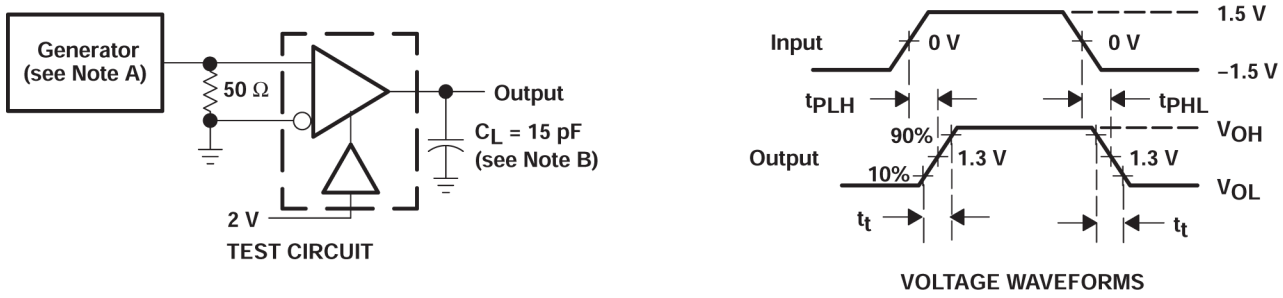
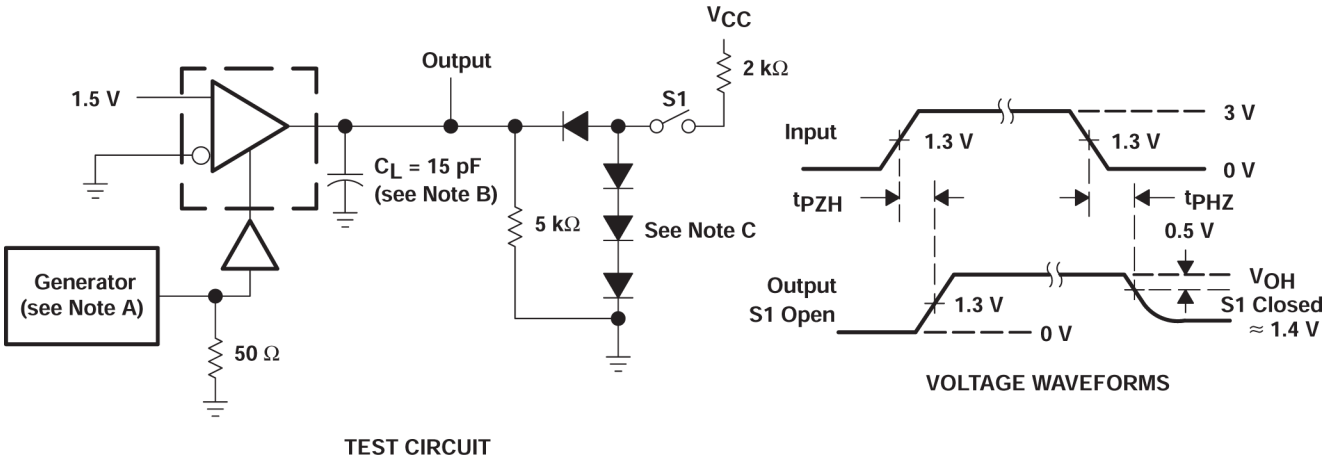


图 6-1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

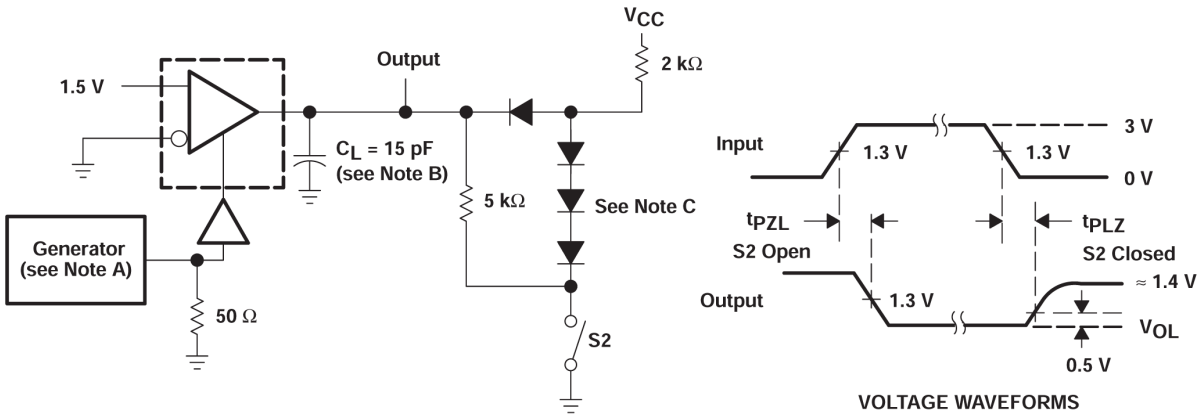


A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

图 6-2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

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C. All diodes are 1N916 or equivalent.

图 6-3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS	ENABLE(1)	OUTPUT
A−B		Y
$V_{ID} \geq 0.2$ V	H	H
−0.2 V < V_{ID} < 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

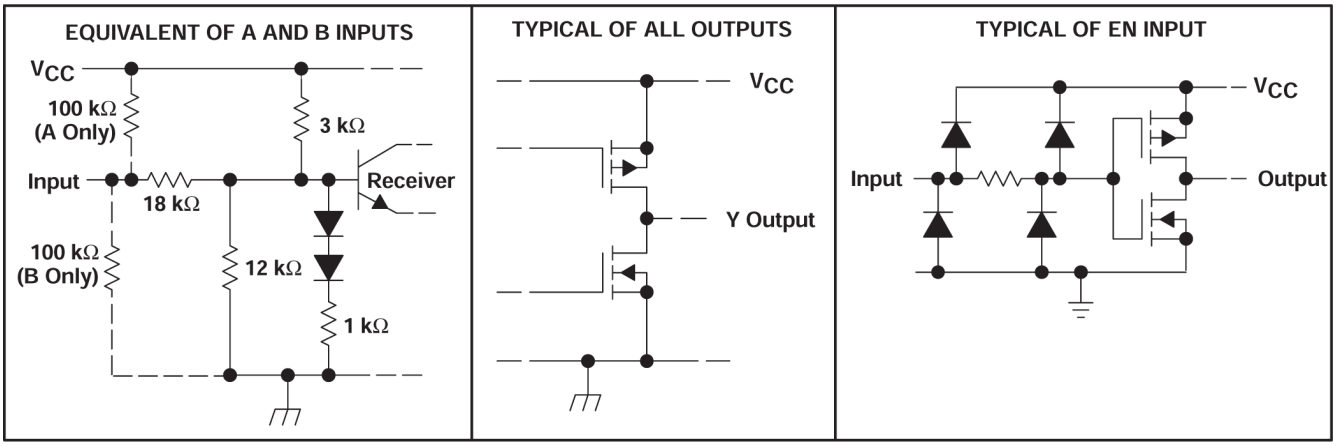

图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (March 2009) to Revision H (November 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC175D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	65LBC175
SN65LBC175DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175DRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175DRG4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175DW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-40 to 85	65LBC175
SN65LBC175DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175
SN65LBC175N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC175N
SN65LBC175N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC175N
SN65LBC175NG4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC175N
SN65LBC175NG4.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC175N
SN75LBC175N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC175N
SN75LBC175N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC175N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN75LBC175 :

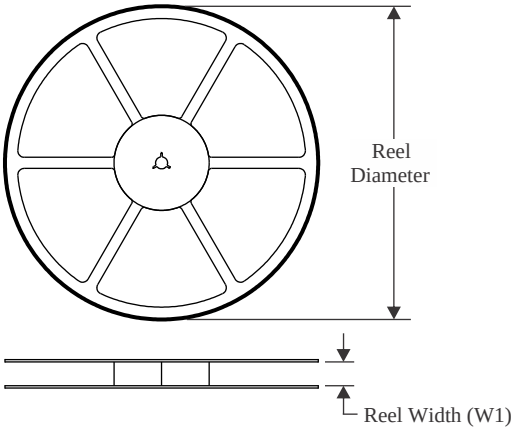
- Military : SN55LBC175

NOTE: Qualified Version Definitions:

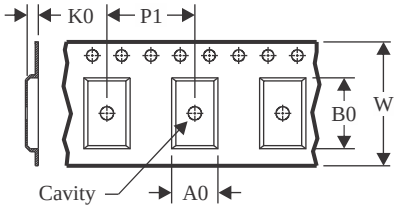
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

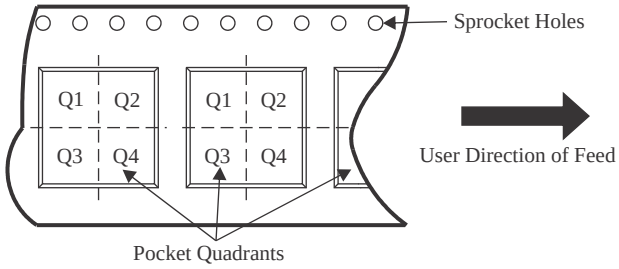


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

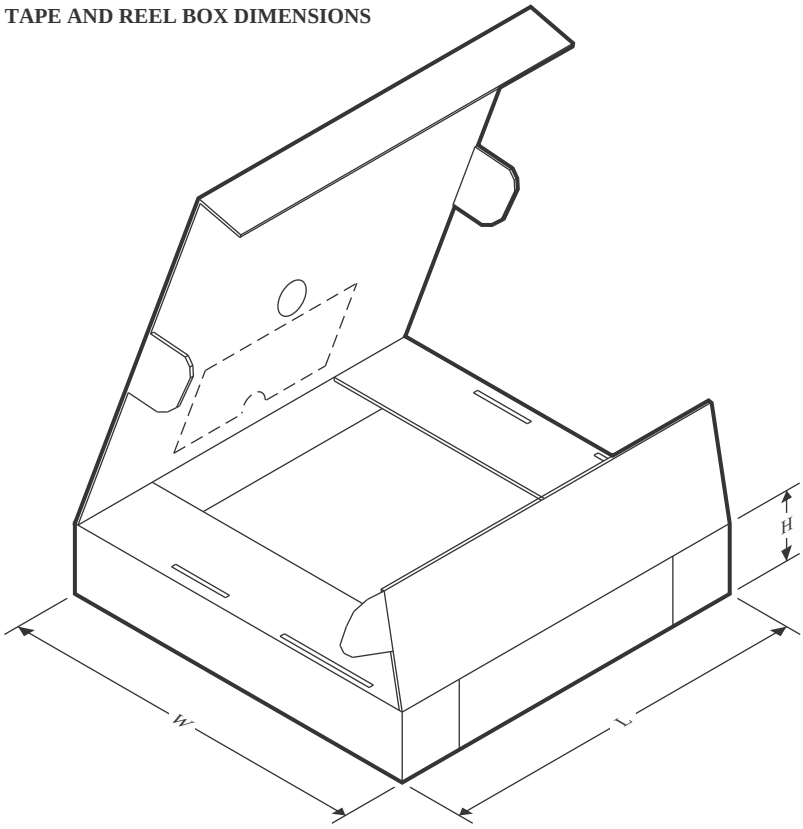
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LBC175DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LBC175DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

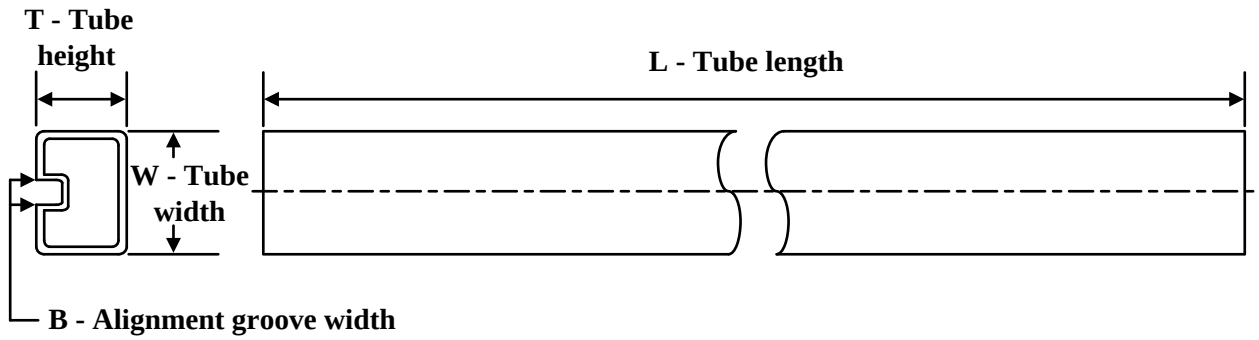
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC175DR	SOIC	D	16	2500	340.5	336.1	32.0
SN65LBC175DRG4	SOIC	D	16	2500	353.0	353.0	32.0
SN65LBC175DWR	SOIC	DW	16	2000	350.0	350.0	43.0

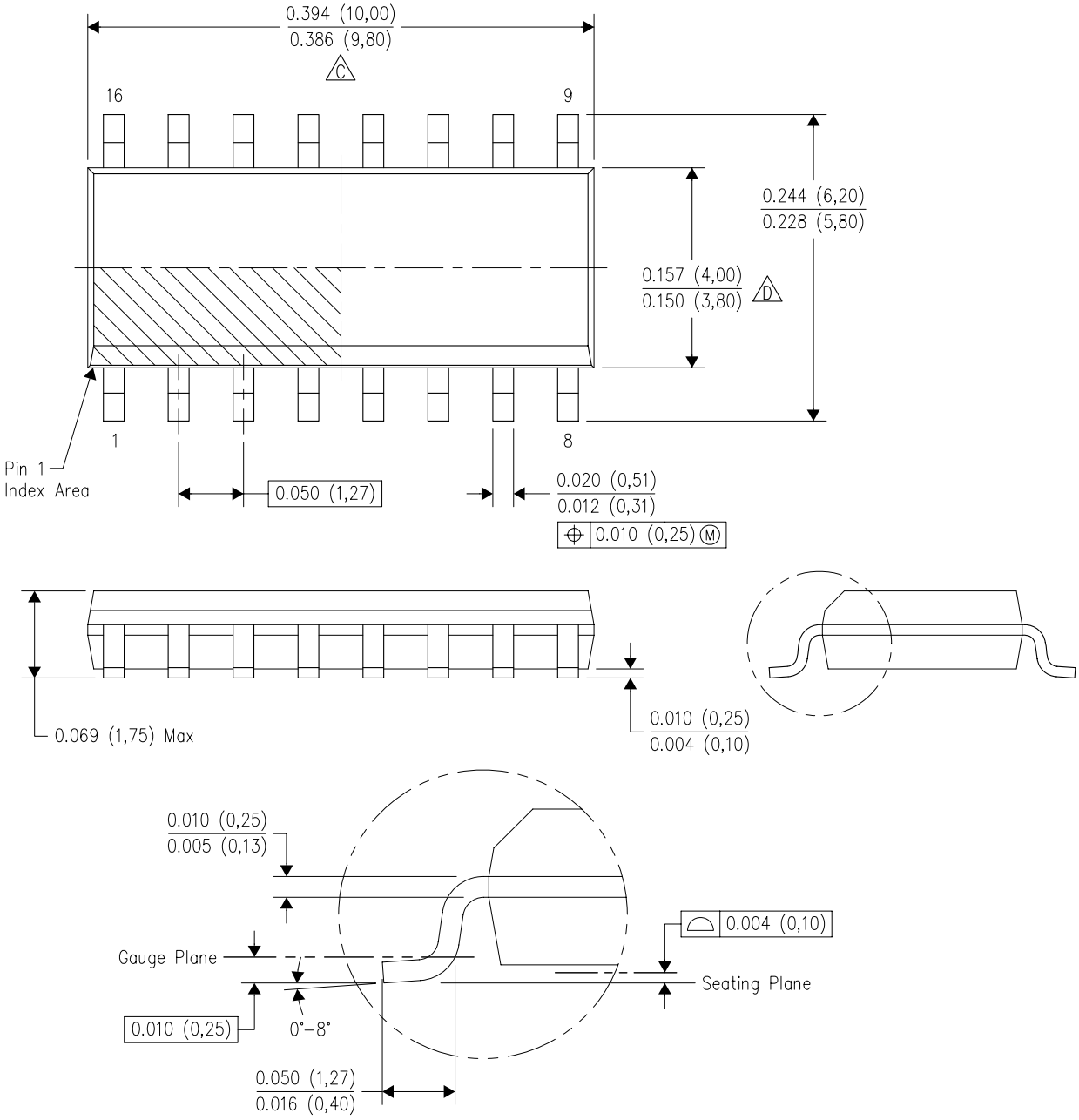
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC175N	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC175N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC175NG4	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC175NG4.A	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC175N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC175N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

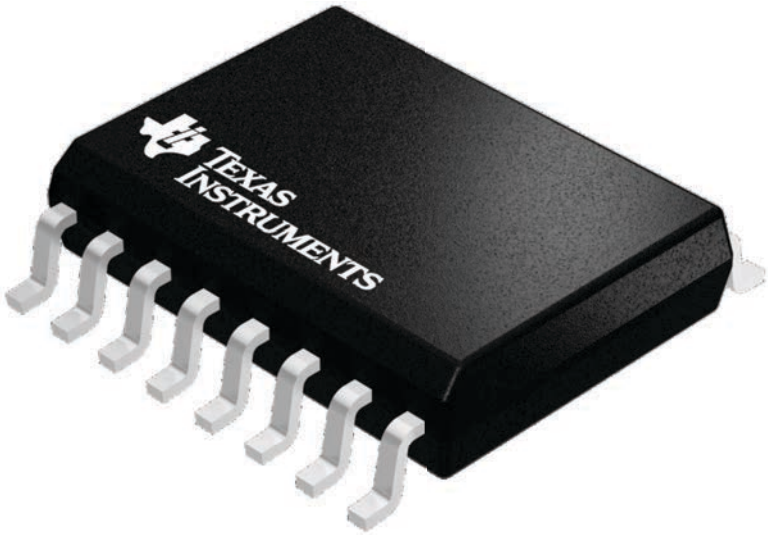
DW 16

SOIC - 2.65 mm max height

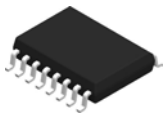
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

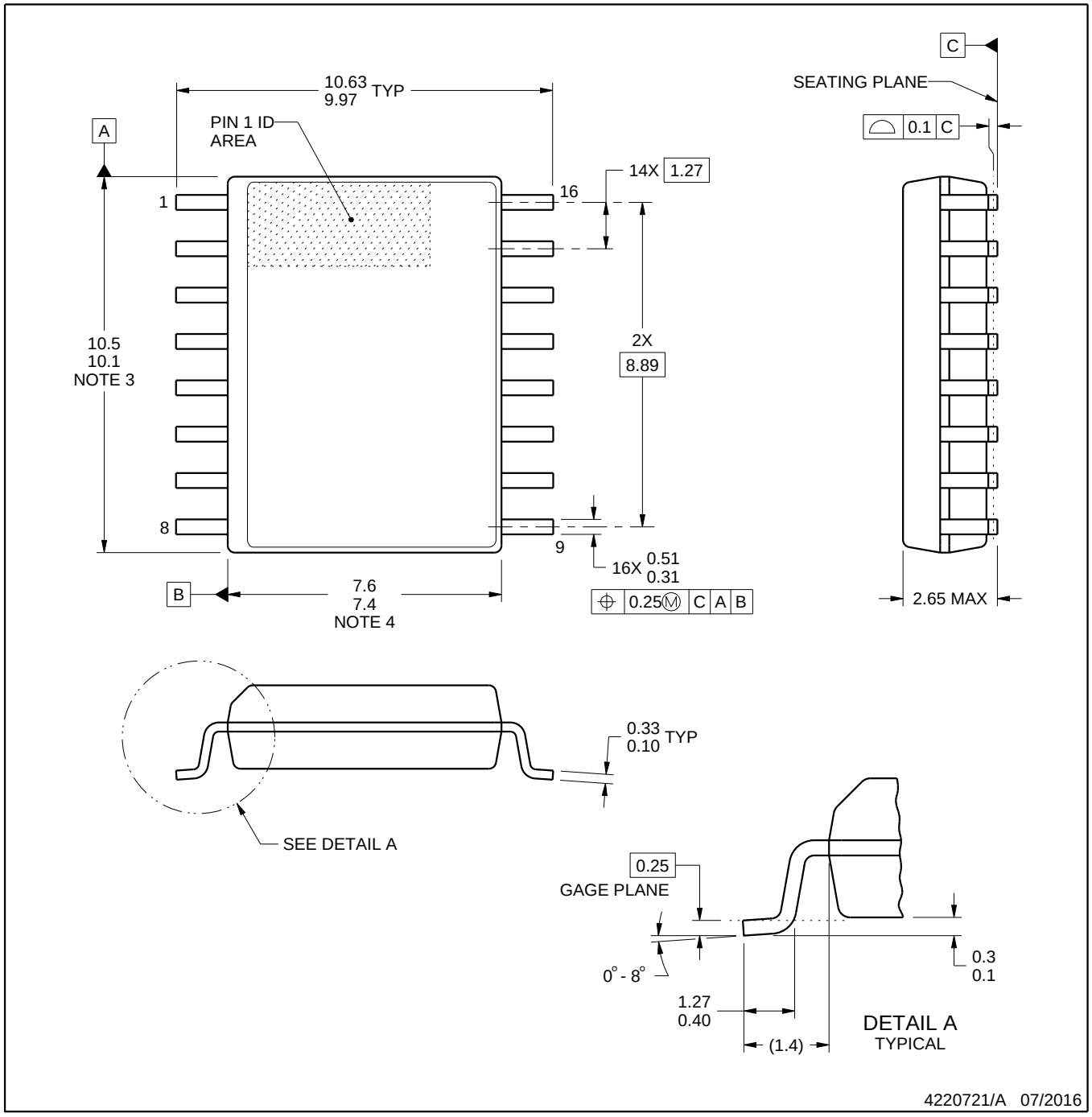


PACKAGE OUTLINE

DW0016A

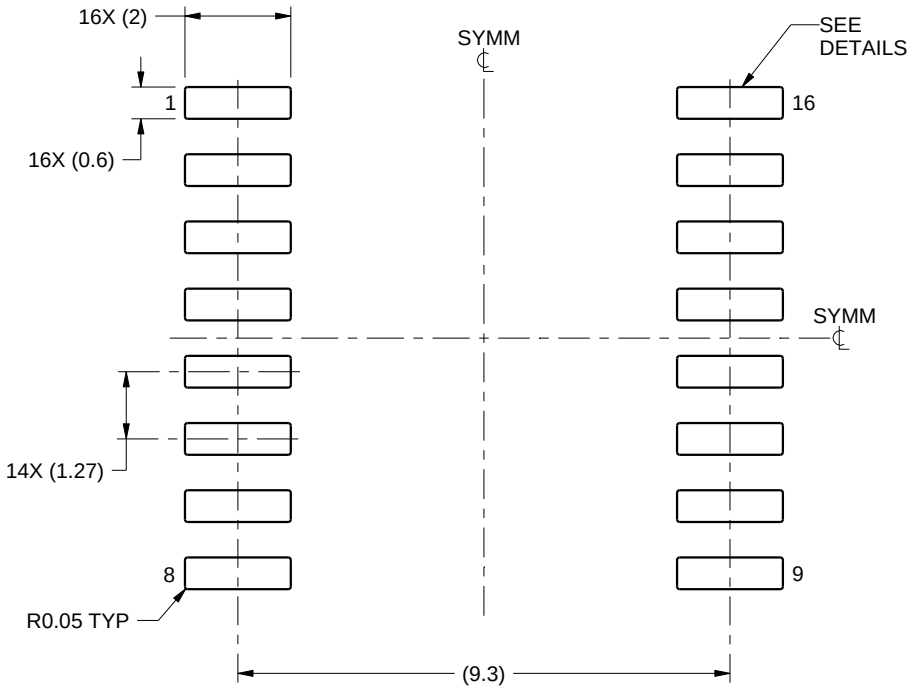
SOIC - 2.65 mm max height

SOIC

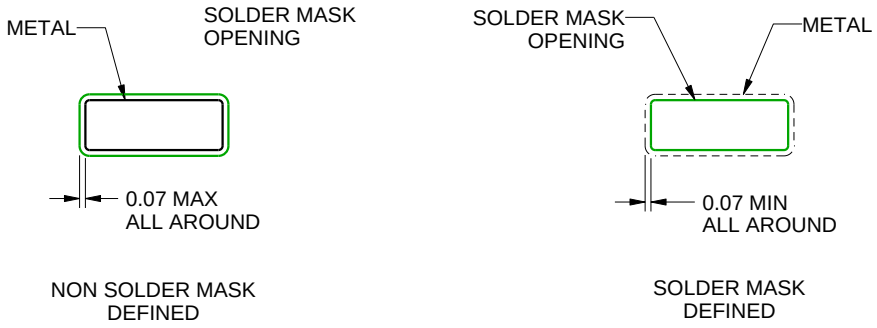


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

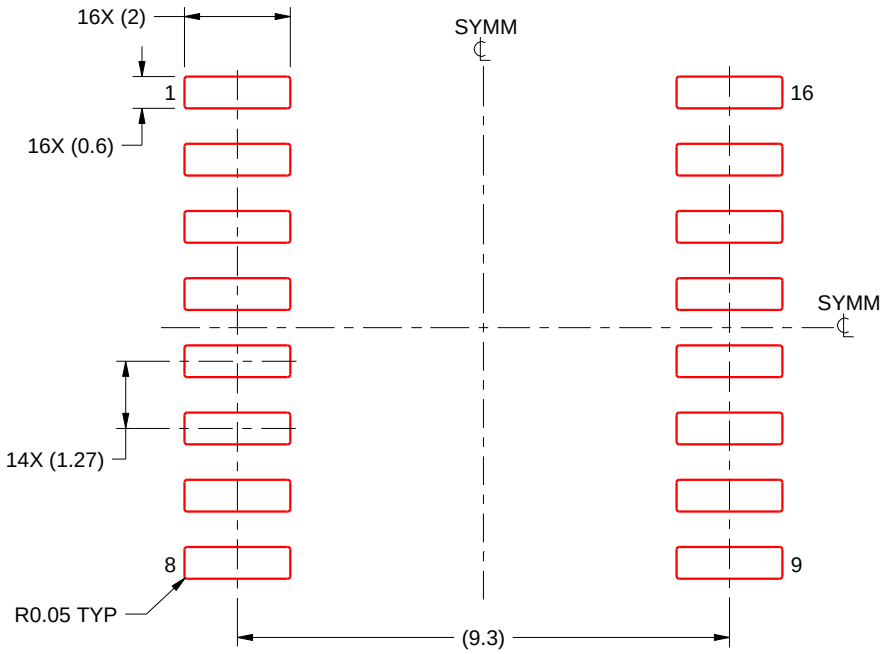


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

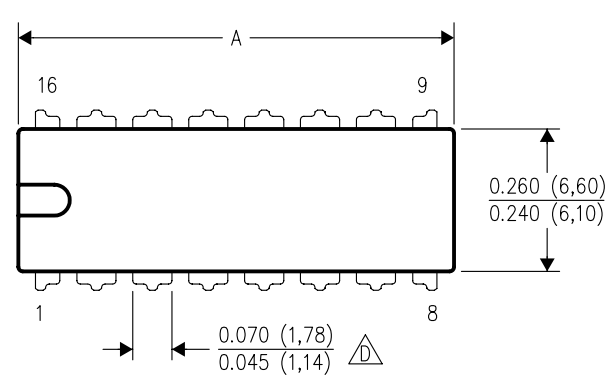
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

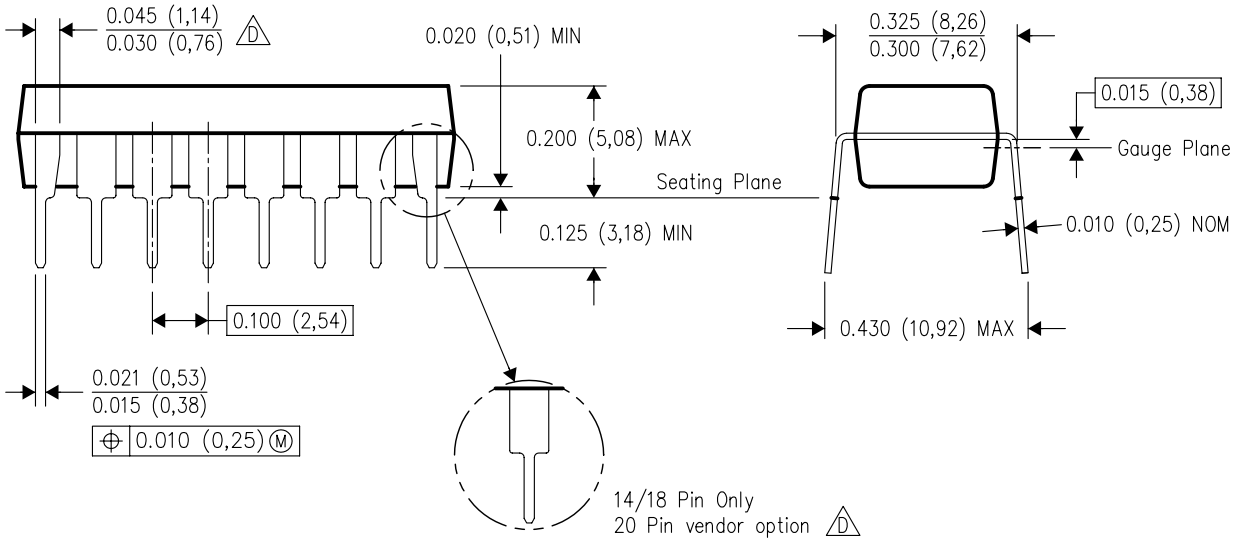
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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