1 特性

- 交流耦合 TMDS 或 DisplayPort 双模物理电平输入到 HDMI2.0a TMDS 物理电平输出支持高达 6Gbps 的数据速率且与 HDMI2.0a 电气参数兼容
- 支持 DisplayPort 双模标准版本 1.1
- 高达 16.5dB 的自适应接收器均衡器和可编程固定均衡器
- 高速通道控制、预加重和发送摆幅以及转换率控制
- I²C 或引脚搭接可编程
- 支持 2 类 I²C-over-AUX 转 DDC 电桥
- 集成了 TMDS 电平转换器和时钟和数据恢复 (CDR) 功能
- 有源 I²C[4] 缓冲器
- 主信道输入交换
- 低功耗
- 低功耗
  - 6Gbps 时的工作功耗为 435mW, 关断状态下的功耗为 10mW
- 面向商业和工业应用的扩展温度器件选项
- 采用 40 引脚、0.4mm 间距、5mm x 5mm QFN 封装, 与 TPD158 转接驱动器引脚兼容
- 40 引脚、0.5mm 间距、7mm x 7mm VQFN 封装

2 应用

- 笔记本、台式机、一体机、平板电脑、游戏机和工业电脑
- 音频/视频设备
- Blu-Ray™DVD
- 游戏系统
- HDMI 适配器或软件狗
- 扩展基座

3 说明

SNx5DP159 器件是一款双模[1] DisplayPort 转最小化传输差分信号 (TMDS) 重定时器, 支持数字视频接口 (DVI) 1.0 以及高清多媒体接口 (HDMI) 1.4b 和 2.0 输出信号。SNx5DP159 器件通过 DDC 链路或 AUX 通道支持双模标准版本 1.1 的 1 类和 2 类应用。SNx5DP159 器件的每条数据信道支持的数据速率为 6Gbps。可支持超高清 (4K × 2K/60Hz) 8 位彩色高分辨率视频和 1080p 16 位色深的高清电视 (1920 × 1080/60Hz)。SNx5DP159 器件在数据速率为 1Gbps 时可自动配置为转接驱动器, 在超过该数据速率后可自动配置为重定时器。此特性可通过 I²C[4] 编程来关闭。

为确保信号完整性, SNx5DP159 器件实现了多个特性。SNx5DP159 接收器支持自适应和固定均衡, 以便消除电路板走线或电缆因带宽受限而引起的码间串扰 (ISI) 抖动或损耗。用作重定时器时, 内置的时钟数据恢复 (CDR) 功能可清除输入端高频和视频源的随机抖动。发送器提供多种功能不仅有利于达到合规要求, 还能够减少系统设计问题, 例如去加重功能可补偿驱动长电缆或高损耗电路板走线时的衰减。SNx5DP159 器件还包括使用 Vsadj 引脚上的外部电阻器实现的 TMDS 输出幅度调节功能, 以及源端选择功能和输出转换速率控制功能。器件的运行和配置可通过引脚设置或 I²C[4] 编程。

SNx5DP159 器件采用多种方法来进行电源管理和降低有功功率。

<table>
<thead>
<tr>
<th>器件型号</th>
<th>封装</th>
<th>封装尺寸 (标称值)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65DP159</td>
<td>VQFN (48)</td>
<td>7.00mm × 7.00mm</td>
</tr>
<tr>
<td>SN75DP159</td>
<td>WQFN (40)</td>
<td>5.00mm × 5.00mm</td>
</tr>
</tbody>
</table>

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

本文档旨在为方便起见, 提供有关 TI 产品中文版本的信息, 以确认产品的概要。有关适用的官方英文版本的最新信息, 请访问 www.ti.com。其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前, 请务必参考最新版本的英文版本。
目录

4 修订历史记录
注：之前版本的页码可能与当前版本有所不同。

<table>
<thead>
<tr>
<th>Changes from Revision E (April 2018) to Revision F</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 将“SN75DP159的工作温度范围为-40°C至85°C”更改为“SN65DP159的工作温度范围为-40°C至85°C”（说明（续））</td>
<td>4</td>
</tr>
<tr>
<td>• 将“SN65DP159的工作温度范围为0°C至85°C”更改为“SN75DP159的工作温度范围为0°C至85°C”（说明（续））</td>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changes from Revision D (June 2017) to Revision E</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed the pinout images appearance in the Pin Configuration and Functions section.</td>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changes from Revision C (July 2016) to Revision D</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 将标题从“SNx5DP159 6-Gbps DP++ 到 HDMI 重定时器”更改为“SNx5DP159 6-Gbps 交流耦合 TMDS™ 到 HDMI™ 电平转换器重定时器”</td>
<td>1</td>
</tr>
<tr>
<td>• 更改了特性列表</td>
<td>1</td>
</tr>
<tr>
<td>• 更改了应用列表</td>
<td>1</td>
</tr>
<tr>
<td>• V_BADJ: Added Note: &quot;Best transmit eye ..&quot;, added MIN and Max values in the Recommended Operating Conditions table</td>
<td>8</td>
</tr>
<tr>
<td>• Changed the description of tชน in 表1</td>
<td>26</td>
</tr>
<tr>
<td>• Changed read procedures in the I²C Control Behavior section</td>
<td>34</td>
</tr>
<tr>
<td>• Added paragraph: &quot;DP159 is designed...&quot; to the Application and Implementation section</td>
<td>40</td>
</tr>
<tr>
<td>• Added 2 paragraphs to the Application Information section</td>
<td>40</td>
</tr>
</tbody>
</table>
Changes from Revision B (April 2016) to Revision C  

- **Recommended Operating Conditions**, Changed the CONTROL PINS section ............................................................... 8
- Changed the **AUX, DDC, and *FC Electrical Characteristics** table ............................................................................... 12
- Added text to 图31 Note: "The SCL_SRC and SDA_SRC pins must be pulled to ground." ...................................................... 42

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- Added "Low-level input voltage at OE" to VIL in the **Recommended Operating Conditions table** .................................................. 8
- Added OE to VIL "High-level input voltage" in the **Recommended Operating Conditions table** ............................................. 8
- Changed 图22 ........................................................................................................................................................................ 25
- Deleted the VDD_ramp and VCC_ramp MIN values in 表1 .................................................................................................. 26
- Changed text "through the *C interface" To: "through the *C access on the DDC interface" in **DDC Functional Description** .......... 31
- Changed the HDMI and DVI value for 1Ah 表3 ....................................................................................................................... 32
- Added Note to 11–400-kbps in 表7 .......................................................................................................................................... 36
- Changed the note in the DEV_FUNC_MODE section of 表7 ................................................................................................ 36
- Changed Note in the DDC_TRAIN_SET section of 表8 ..................................................................................................... 37

Changes from Original (July 2015) to Revision A  

- 将器件状态从“产品预览”更改为“生产数据” ...................................................................................................................... 1
- 更新了典型电源数 ............................................................................................................................................................... 1
- 删除了备用电源数 ............................................................................................................................................................... 1
- 将“预览”更改为“生产数据” ............................................................................................................................................... 1
- Replaced SIG_EN with NC in pinout drawing and **Pin Functions** table ........................................................................ 4
- Removed lane swap from description of SWAP/POL = H ...................................................................................................... 7
- Updated swing data ................................................................................................................................................................. 8
- Changed DDC link into its pin names between SNK and SRC and updated min value .......................................................... 8
- Added new line for SCL_SNK, SDA_SNK .................................................................................................................................. 8
- Removed standby power and standby current rows and updated active power and current numbers ................................. 9
- Changed term control to no source termination ................................................................................................................... 11
- Increased ILEAK max value from 10 μA to 45 μA...................................................................................................................... 11
- Updated redriver mode max jitter value .............................................................................................................................. 13
- Clarified polarity swap to input signals .................................................................................................................................. 27
- Added more information on compliance in redriver mode ................................................................................................... 31
- Added note to **DDC Functional Description** section describing DDC snoop function ................................................... 31
- Removed bit 4 SIG_EN and made reserved ........................................................................................................................... 36
- Removed SIG_EN Pin and added Note 1 for DDC Snoop ..................................................................................................... 42
- Updated schematic to replace SIG_EN pin with NC ................................................................................................................ 43
- Updated VID swing .................................................................................................................................................................. 46
- Changed Title to better match table. Removed Standby and redundant rows ................................................................. 48
- Updated drawing with pin 17 changed to NC ........................................................................................................................ 51
说明（续）

SNx5DP159 接收器使用多种方法来确定支持 HDMI1.4b[2] 还是 HDMI2.0[3] 数据速率。SNx5DP159 接收器采用两种封装：40 引脚 RSB 封装（支持空间受限的应用）和 48 引脚 RGZ 封装（支持软件狗等应用中的 DisplayPort 双模标准版本 1.1 的全部特性）。

SN65DP159 器件可在 –40°C 至 85°C 的工业级温度范围内运行。
SN75DP159 器件可在 0°C 至 85°C 的扩展商业级温度范围内运行。

6 Pin Configuration and Functions
Pin Functions

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_D2p</td>
<td>I</td>
<td>Channel 2 differential input</td>
</tr>
<tr>
<td>IN_D2n</td>
<td>I</td>
<td>Channel 2 differential input</td>
</tr>
<tr>
<td>IN_D1p</td>
<td>I</td>
<td>Channel 1 differential input</td>
</tr>
<tr>
<td>IN_D1n</td>
<td>I</td>
<td>Channel 1 differential input</td>
</tr>
<tr>
<td>IN_D0p</td>
<td>I</td>
<td>Channel 0 differential input</td>
</tr>
<tr>
<td>IN_D0n</td>
<td>I</td>
<td>Channel 0 differential input</td>
</tr>
<tr>
<td>HPD_SRC</td>
<td>I</td>
<td>Channel 0 differential input</td>
</tr>
<tr>
<td>IN_CLKp</td>
<td>I</td>
<td>Clock differential input</td>
</tr>
<tr>
<td>IN_CLKn</td>
<td>I</td>
<td>Clock differential input</td>
</tr>
<tr>
<td>OUT_D2n</td>
<td>O</td>
<td>TMDS data 2 differential output</td>
</tr>
<tr>
<td>OUT_D2p</td>
<td>O</td>
<td>TMDS data 2 differential output</td>
</tr>
<tr>
<td>OUT_D1n</td>
<td>O</td>
<td>TMDS data 1 differential output</td>
</tr>
<tr>
<td>OUT_D1p</td>
<td>O</td>
<td>TMDS data 1 differential output</td>
</tr>
</tbody>
</table>

(1) Blue pin names are only in the SNx5DP159 RGZ package.
(2) (H) Logic high (pin strapped to VCC through 65-kΩ resistor); (L) logic low (pin strapped to GND through 65-kΩ resistor); (for mid-level, no connect)
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>PIN NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT_D0n</td>
<td>28</td>
<td>TMDS data 0 differential output</td>
</tr>
<tr>
<td>OUT_D0p</td>
<td>29</td>
<td>TMDS data clock differential output</td>
</tr>
<tr>
<td>OUT_CLKn</td>
<td>25</td>
<td>TMDS data clock differential output</td>
</tr>
<tr>
<td>OUT_CLKp</td>
<td>26</td>
<td></td>
</tr>
</tbody>
</table>

### HOT PLUG DETECT PINS

- **HPD_SRC**: Hot plug detect output
- **HPD_SNK**: Hot plug detect input

### AUXILIARY/DDC DATA PINS

- **AUX_SRCp**: Source side bidirectional DisplayPort auxiliary for I2C-over-AUX (DP159RGZ only)
- **AUX_SRCn**: Source side TMDS port bidirectional DDC data line
- **SDA_SRC**: Sink side TMDS port bidirectional DDC data line
- **SCL_SRC**: Sink side TMDS port bidirectional DDC data line

### CONTROL PINS

- **OE**: Operation enable/reset pin
  - OE = Low: Power-down mode
  - OE = High: Normal operation
  - Internal weak pullup: Resets device when transitions from H to L
- **NC**: No connect
- **CEC_EN**: CEC control pin for Dongle applications

### I2C EN/PIN

- **I2C_EN/PIN**: I2C clock signal
  - I2C_EN/PIN = Low: pin signal
  - I2C_EN/PIN = High: I2C control mode

### TX TERM_CTL

- **TX_TERM_CTL**: Transmit Termination Control when I2C_EN/PIN = Low
  - TX_TERM_CTL = L: No transmit termination
  - TX_TERM_CTL = H: Transmit termination
  - Data rate (DR) < 3.4 Gbps – 75- to 150-Ω differential near end termination
  - Data rate (DR) > 3.4 Gbps – 75- to 150-Ω differential near end termination
  - Note: If left floating will be in automatic select mode.
Pin Functions (continued)

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>RGZ</th>
<th>RSB</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWAP/POL (^{(1)})</td>
<td>1</td>
<td>N/A</td>
<td>Input lane SWAP and polarity control pin when I2C_EN/PIN = Low (\text{SWAP/POL} = \text{H}) receive lane polarity swap (retimer mode only) (\text{SWAP/POL} = \text{L}) receive lanes swap (retimer and redriver mode) (\text{SWAP/POL} = \text{No Connect}) normal working</td>
</tr>
</tbody>
</table>

SUPPLY AND GROUND PINS

<table>
<thead>
<tr>
<th>V(_{CC})</th>
<th>V(_{DD})</th>
<th>GND</th>
<th>Thermal Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>13, 43</td>
<td>14, 23, 24, 37, 48</td>
<td>7, 19, 41, 30, 15, 35</td>
<td>Connected to ground</td>
</tr>
</tbody>
</table>

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) \(^{(1)}\)\(^{(2)}\)

### Minimum and Maximum Values

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{CC})</td>
<td>–0.3</td>
<td>4</td>
</tr>
<tr>
<td>V(_{DD})</td>
<td>–0.3</td>
<td>1.4</td>
</tr>
<tr>
<td>Supply voltage (^{(3)})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Main link input (IN(_)Dx AC-coupled mode), AUX_Srcp, AUX_Srcn</td>
<td>1.56</td>
<td>V</td>
</tr>
<tr>
<td>TMDS outputs (OUT(_)Dx)</td>
<td>–0.3</td>
<td>4</td>
</tr>
<tr>
<td>HPD_SRC, Vsadj, SDA_CTL, SCL_CTL, OE, HDMI_SEL/A1, EQ_SEL/A0, I2C_EN/PIN, SLEW_CTL, TX_TERM_CTL, SDA_SRC, SCL_SRC</td>
<td>–0.3</td>
<td>4</td>
</tr>
<tr>
<td>HPD_SNK, SDA_SNK, SCL_SNK</td>
<td>–0.3</td>
<td>6</td>
</tr>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Continuous power dissipation

<table>
<thead>
<tr>
<th>Storage temperature, (T_{stg})</th>
<th>See Thermal Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-65)</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)}) Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (^{(1)})</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (^{(2)})</td>
<td>±2000</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC} (Supply voltage)</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V_{DD}</td>
<td>1.00</td>
<td>1.1</td>
<td>1.27</td>
<td>V</td>
</tr>
<tr>
<td>T_{CASE} (Case temperature for RSB package)</td>
<td>93.5</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{CASE} (Case temperature for RGZ package)</td>
<td>92.7</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_{A} (Operating free-air temperature)</td>
<td>SN75DP159</td>
<td>0</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>SN65DP159</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

**MAIN LINK DIFFERENTIAL PINS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{ID_PP} (Peak-to-peak input differential voltage)</td>
<td>75</td>
<td>1200</td>
<td>mv</td>
<td></td>
</tr>
<tr>
<td>V_{IC} (Input common mode voltage)</td>
<td>0</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>C_{AC} (AC coupling capacitance)</td>
<td>75</td>
<td>100</td>
<td>200</td>
<td>nF</td>
</tr>
<tr>
<td>d_{a} (Data rate)</td>
<td>0.25</td>
<td>5</td>
<td>Gbps</td>
<td></td>
</tr>
<tr>
<td>V_{SADJ} (TMDS-compliant swing voltage bias resistor)</td>
<td>4.5</td>
<td>7.06</td>
<td>7.5</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

**CONTROL PINS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{I_DC} (DC input voltage)</td>
<td>−0.3</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IL} (Low-level input voltage at OE)</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IM} (No connect input voltage at SLEW_CTL, PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL)</td>
<td>1</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>V_{IN} (High-level input voltage at SLEW_CTL, OE[10], PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL)</td>
<td>2.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OL} (Low-level output voltage)</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OH} (High-level output voltage)</td>
<td>2.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{H} (High-level input current)</td>
<td>−30</td>
<td>30</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_{L} (Low-level input current)</td>
<td>−10</td>
<td>10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_{QO} (Short circuit output current)</td>
<td>−50</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{QZ} (High impedance output current)</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{OEPU} (Pullup resistance on OE pin)</td>
<td>150</td>
<td>250</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) Best transmit eye with minimum intra-pair skew, largest vertical and horizontal eye opening, maintaining HDMI compliant output swing can be achieved with resistors around 6.4k. Using smaller resistors may lead to compliance failures.

(2) These values are based upon a microcontroller driving the control pins. The pullup/pulldown/floating resistor configuration will set the internal bias to the proper voltage level which will not match the values shown here.

(3) This value is based upon a microcontroller driving the OE pin. A passive reset circuit using an external capacitor and the internal pullup resistor will set OE pin properly, but may have a different value than shown due to internal biasing.

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>SN65DP159</th>
<th>SN75DP159</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{UA} (Junction-to-ambient thermal resistance)</td>
<td>31.1</td>
<td>37.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{UC(top)} (Junction-to-case (top) thermal resistance (High-K board))</td>
<td>18.2</td>
<td>23.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{UB} (Junction-to-board thermal resistance (High-K board))</td>
<td>8.1</td>
<td>9.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>\Psi_{JT} (Junction-to-top characterization parameter)</td>
<td>0.4</td>
<td>0.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>\Psi_{JB} (Junction-to-board characterization parameter)</td>
<td>8.1</td>
<td>3.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{UBC(bot)} (Junction-to-case (bottom) thermal resistance)</td>
<td>3.2</td>
<td>3.2</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Test conditions for \Psi_{JB} and \Psi_{JT} are clarified in TI document Semiconductor and IC Package Thermal Metrics.
## 7.5 Power Supply Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{D1} ) Device power dissipation (Retimer operation)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.6 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V} ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( V_i = 3.3 \text{ V}, ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}_{\text{CTL}}} = 0 \text{ V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega )</td>
<td></td>
<td>435</td>
<td>600</td>
<td>mW</td>
</tr>
<tr>
<td>( P_{D2} ) Device power dissipation (Redriver operation)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.6 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V} ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( V_i = 3.3 \text{ V}, ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}_{\text{CTL}}} = 0 \text{ V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega )</td>
<td></td>
<td>215</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>( P_{SD1} ) Device power in power down</td>
<td>( \text{OE} = \text{L}, \quad V_{\text{CC}} = 3.3 \text{ V/3.6 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega )</td>
<td></td>
<td>10</td>
<td>30</td>
<td>mW</td>
</tr>
<tr>
<td>( I_{CC1} ) VCC supply current (TMDS 6Gbps retimer mode)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.6 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}<em>{\text{CTL}}} = 0 \text{ V}, \quad \text{SLEW}</em>{\text{CTL}} = \text{H} )</td>
<td></td>
<td>35</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD1} ) VDD supply current (TMDS 6Gbps retimer mode)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.6 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}<em>{\text{CTL}}} = 0 \text{ V}, \quad \text{SLEW}</em>{\text{CTL}} = \text{H} )</td>
<td></td>
<td>295</td>
<td>325</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{CC2} ) VCC supply current (TMDS 6Gbps redriver mode)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.465 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}<em>{\text{CTL}}} = 0 \text{ V}, \quad \text{SLEW}</em>{\text{CTL}} = \text{H} )</td>
<td></td>
<td>8</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD2} ) VDD supply current (TMDS 6Gbps redriver mode)</td>
<td>( \text{OE} = \text{H}, \quad V_{\text{CC}} = 3.3 \text{ V/3.465 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( \text{IN}<em>{\text{Dx}}: \quad V</em>{\text{ID}<em>{\text{PP}}} = 1200 \text{ mV}, \quad 6\text{Gbps TMDS pattern} ) ( I</em>{2\text{C}<em>{\text{EN/PIN}}} = \text{L}, \quad \text{PRE}</em>{\text{SEL}} = \text{H}, \quad \text{EQ}<em>{\text{CTL}} = \text{H}, ) ( \text{SDA}</em>{\text{CLK/CLK}<em>{\text{CTL}}} = 0 \text{ V}, \quad \text{SLEW}</em>{\text{CTL}} = \text{H} )</td>
<td></td>
<td>170</td>
<td>250</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{SD1} ) Power-down current</td>
<td>( \text{OE} = \text{L}, \quad V_{\text{CC}} = 3.3 \text{ V/3.465 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( 3.3\text{-V rail} )</td>
<td>2</td>
<td>5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{SD1} ) Power-down current</td>
<td>( \text{OE} = \text{L}, \quad V_{\text{CC}} = 3.3 \text{ V/3.465 V}, \quad V_{\text{DD}} = 1.1 \text{ V/1.27 V}, \quad \text{VSadj} = 7.06 \text{ k}\Omega ) ( 1.1\text{-V rail} )</td>
<td>3.5</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) The typical rating is simulated at 3.3-V \( V_{\text{CC}} \) and 1.1-V \( V_{\text{DD}} \) and at 27°C temperature unless otherwise noted.

(2) The maximum rating is simulated at 3.6-V \( V_{\text{CC}} \) and 1.27-V \( V_{\text{DD}} \) and at 85°C temperature unless otherwise noted.
### 7.6 Differential Input Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{R_RX_DATA}$</td>
<td>Ddata lanes data rate</td>
<td>0.25</td>
<td>6</td>
<td>Gbps</td>
<td></td>
</tr>
<tr>
<td>$D_{R_RX_CLK}$</td>
<td>Clock lanes clock rate</td>
<td>25</td>
<td>340</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$t_{RX_DUTY}$</td>
<td>Input clock duty circle</td>
<td>40%</td>
<td>50%</td>
<td>60%</td>
<td></td>
</tr>
<tr>
<td>$t_{CLK_JIT}$</td>
<td>Input clock jitter tolerance</td>
<td>0.3</td>
<td></td>
<td>Tbit</td>
<td></td>
</tr>
<tr>
<td>$t_{DATA_JIT}$</td>
<td>Input data jitter tolerance</td>
<td>Test the TTP2, see 图 10</td>
<td>150</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$T_{RX_INTRA}$</td>
<td>Input intra-pair skew tolerance</td>
<td>Test at TTP2 when DR = 1.6-Gbps, see 图10</td>
<td>112</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$T_{RX_INTER}$</td>
<td>Input inter-pair skew tolerance</td>
<td>1.8</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$E_{QH(D)}$</td>
<td>Fixed EQ gain for data lane IN_D(0,1,2)n/p</td>
<td>EQ_SEL/A0 = H; Fixed EQ gain, test at 6-Gbps</td>
<td>15</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$E_{QL(D)}$</td>
<td>Fixed EQ gain for data lane IN_D(0,1,2)n/p</td>
<td>EQ_SEL/A0 = L; Fixed EQ gain, test at 6-Gbps</td>
<td>7.5</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$E_{QZ(D)}$</td>
<td>Adaptive EQ gain for data lane IN_D(0,1,2)n/p</td>
<td>EQ_SEL/A0 = Z; adaptive EQ</td>
<td>2</td>
<td>15</td>
<td>dB</td>
</tr>
<tr>
<td>$E_{Q(c)}$</td>
<td>EQ gain for clock lane IN_CLKn/p</td>
<td>EQ_SEL/A0 = H,L,NC</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{INT}$</td>
<td>Input differential termination impedance</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{TERM}$</td>
<td>Input termination voltage</td>
<td>OE = H</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ID_PP}$</td>
<td>Input differential voltage (peak to peak)</td>
<td>Tested at TTP2, check 图 10</td>
<td>75</td>
<td>1200</td>
<td>mVpp</td>
</tr>
</tbody>
</table>
### 7.7 HDMI and DVI TMDS Output Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} )</td>
<td>Single-ended high level output voltage</td>
<td>( V_{CC} - 10 )</td>
<td>( V_{CC} + 10 )</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Single-ended high level output voltage</td>
<td>( V_{CC} - 200 )</td>
<td>( V_{CC} + 10 )</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Single-ended low level output voltage</td>
<td>( V_{CC} - 600 )</td>
<td>( V_{CC} - 400 )</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Single-ended low level output voltage</td>
<td>( V_{CC} - 700 )</td>
<td>( V_{CC} - 400 )</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{SWING_DA} )</td>
<td>Single-ended output voltage swing on data lane</td>
<td>400</td>
<td>500</td>
<td>600</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{SWING_CLK} )</td>
<td>Single-ended output voltage swing on clock lane</td>
<td>400</td>
<td>500</td>
<td>600</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{SWING} )</td>
<td>Change in single-end output voltage swing per 100 ( \Omega ) ( \Delta V_{\text{Sadj}} )</td>
<td>20</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{\text{OCM(SS)}} )</td>
<td>Change in steady state output common mode voltage between logic levels</td>
<td>-5</td>
<td>5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{DD_PP} )</td>
<td>Output differential voltage before pre-emphasis</td>
<td>( V_{\text{Sadj}} = 7.06-k\Omega ); ( \text{PRE_SEL} = Z ), See 图 8</td>
<td>800</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{DD_SS} )</td>
<td>Steady-state output differential voltage</td>
<td>( V_{\text{Sadj}} = 7.06-k\Omega ); ( \text{PRE_SEL} = L ), See 图 9</td>
<td>600</td>
<td>1050</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{\text{LEAK}} )</td>
<td>Failsafe condition leakage current</td>
<td>( V_{CC} = 0-V ); ( V_{DD} = 0-V ); output pulled to 3.3 V through 50-( \Omega ) resistors</td>
<td>45</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Short circuit current limit</td>
<td>Main link output shorted to GND</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( R_{TERM} )</td>
<td>Source termination resistance for HDMI 2.0</td>
<td>75</td>
<td>150</td>
<td>( \Omega )</td>
<td></td>
</tr>
</tbody>
</table>
### 7.8 AUX, DDC, and I²C Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sub&gt;ID&lt;/sub&gt;</td>
<td>Input capacitance</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;AC&lt;/sub&gt;</td>
<td>AUX AC coupling capacitance</td>
<td>75</td>
<td>200</td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>D&lt;sub&gt;R(AUX)&lt;/sub&gt;</td>
<td>Data rate of the AUX channel input</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>Mbps</td>
</tr>
<tr>
<td>V&lt;sub&gt;I-DC(AUX)&lt;/sub&gt;</td>
<td>DC input voltage on AUX channel, AUX&lt;sub&gt;_SRC&lt;/sub&gt;p/n: 100-kΩ pull up to 3.6 V but differential common mode is 2 V or less.</td>
<td>-0.5</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IS_DIFF_PP_TX&lt;/sub&gt;</td>
<td>Peak-to-peak differential voltage at TX pins</td>
<td>0.29</td>
<td>1.38</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IS_DIFF_PP_RX&lt;/sub&gt;</td>
<td>Peak-to-peak differential voltage at RX pins</td>
<td>0.14</td>
<td>1.36</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IS_DC_CM&lt;/sub&gt;</td>
<td>AUX channel DC common mode voltage</td>
<td>0</td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;ISSHORT&lt;/sub&gt;</td>
<td>AUX channel short circuit current limit</td>
<td>90</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;I-DC&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_SNK&lt;/sub&gt; DC input voltage</td>
<td>-0.3</td>
<td>5.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;I-DC&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_CTL&lt;/sub&gt;, SCL/SDA&lt;sub&gt;_SRC&lt;/sub&gt; DC input voltage</td>
<td>-0.3</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_SNK&lt;/sub&gt;, SCL/SDA&lt;sub&gt;_SRC&lt;/sub&gt; Low level input voltage</td>
<td>0.3 x V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_CTL&lt;/sub&gt; Low level input voltage</td>
<td>0.3 x V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IIH&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_SNK&lt;/sub&gt; high level input voltage</td>
<td>3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IIH&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_SRC&lt;/sub&gt; high level input voltage</td>
<td>0.7 x V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IIH&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_CTL&lt;/sub&gt; high level input voltage</td>
<td>0.7 x V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IDL&lt;/sub&gt;</td>
<td>SCL/SDA&lt;sub&gt;_CTL&lt;/sub&gt;, SCL/SDA&lt;sub&gt;_SRC&lt;/sub&gt; low-level output voltage</td>
<td>I&lt;sub&gt;0&lt;/sub&gt; = 3-mA and V&lt;sub&gt;CC&lt;/sub&gt; &gt; 2-V</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>t&lt;sub&gt;sCL&lt;/sub&gt;</td>
<td>SCL clock frequency fast I²C mode for local I²C control</td>
<td>400</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>C&lt;sub&gt;bus&lt;/sub&gt;</td>
<td>Total capacitive load for each bus line (DDC and local I²C pins)</td>
<td>400</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### 7.9 HPD Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IIH&lt;/sub&gt;</td>
<td>High-level input voltage</td>
<td>2.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;III&lt;/sub&gt;</td>
<td>Low-level input voltage</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub,IDH&lt;/sub&gt;</td>
<td>High-level output voltage</td>
<td>2.4</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub,IDL&lt;/sub&gt;</td>
<td>Low-level output voltage</td>
<td>0</td>
<td>0.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;LEAK&lt;/sub&gt;</td>
<td>Failsafe condition leakage current</td>
<td>40</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IIIHPD&lt;/sub&gt;</td>
<td>High-level input current</td>
<td>40</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IIIHPD&lt;/sub&gt;</td>
<td>Low-level input current</td>
<td>30</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>R&lt;sub&gt;pdHPD&lt;/sub&gt;</td>
<td>HPD input termination to GND</td>
<td>150</td>
<td>190</td>
<td>220</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

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## 7.10 HDMI and DVI Main Link Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REDRIVER MODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$D_R$</td>
<td>Data rate (Automatic Mode)</td>
<td>250</td>
<td>1000</td>
<td>Mbps</td>
<td></td>
</tr>
<tr>
<td>$D_R$</td>
<td>Data rate (full redriver mode)</td>
<td>250</td>
<td>6000</td>
<td>Mbps</td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Propagation delay time (low to high)</td>
<td>250</td>
<td>600</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Propagation delay time (high to low)</td>
<td>250</td>
<td>800</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_{T1}$</td>
<td>Transition time (rise and fall time); measured at 20% and 80% levels for data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lanes. TMDS clock meets $t_{T3}$ for all three times.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = H; \ TX_TERM_CNT = L; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps$</td>
<td>45</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = L; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps$</td>
<td>65</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = NC; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps; \ CLK = 150MHz$</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SK1(T)}$</td>
<td>Intra-pair output skew</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = NC; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps; \ $</td>
<td>40</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{SK2(T)}$</td>
<td>Inter-pair output skew</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = NC; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps; \ $</td>
<td>100</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{JITD1(1.4b)}$</td>
<td>Total output data jitter</td>
<td></td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$DR = 2.97 \ Gbps, \ HDMI_SEL/A1 = NC, \ EQ_SEL/A0 = NC; \ SLEW_CNT = H \ OE = H$.</td>
<td>0.2</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$3.4Gbps &lt; Rbit &lt; 3.712Gbps \ SLEW_CNT = H; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; \ OE = H$.</td>
<td>0.4</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$3.712Gbps &lt; Rbit &lt; 5.94Gbps \ SLEW_CNT = H; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; \ OE = H$.</td>
<td>0.23</td>
<td>12</td>
<td>0.1998</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$5.94Gbps \leq Rbit &lt; 6.0Gbps \ SLEW_CNT = H; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; \ OE = H$.</td>
<td>0.8</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>$t_{JITD1(2.0)}$</td>
<td>Total output data jitter</td>
<td></td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$DR = 6Gbps; \ CLK = 297 \ MHz$</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>$t_{JITC1(1.4b)}$</td>
<td>Total output clock jitter</td>
<td></td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$CLK = 297 \ MHz$</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>$t_{JITC1(2.0)}$</td>
<td>Total output clock jitter</td>
<td></td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>$DR = 6Gbps; \ CLK = 150 \ MHz$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td><strong>RETIMER MODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$d_R$</td>
<td>Data rate (Full retimer mode)</td>
<td>0.25</td>
<td>6</td>
<td>Gbps</td>
<td></td>
</tr>
<tr>
<td>$d_o$</td>
<td>Data rate (Automatic mode)</td>
<td>1.0</td>
<td>6</td>
<td>Gbps</td>
<td></td>
</tr>
<tr>
<td>$d_{XVR}$</td>
<td>Automatic redriver to retimer crossover</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Measured with input signal applied from 0 to 200 mVpp</td>
<td>.75</td>
<td>1.0</td>
<td>1.25</td>
<td>Gbps</td>
</tr>
<tr>
<td>$i_{CROSSOVER}$</td>
<td>Crossover frequency hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$P_{LLBW}$</td>
<td>Data retimer PLL bandwidth</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Default loop bandwidth setting</td>
<td>.4</td>
<td>1</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$i_{ACQ}$</td>
<td>Input clock frequency detection and retimer acquisition time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tested when data rate &gt; 1.0 Gbps</td>
<td>180</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$i_{JT1}$</td>
<td>Input clock jitter tolerance</td>
<td></td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>$t_{T1}$</td>
<td>Transition time (rise and fall time); measured at 20% and 80% levels for data</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>lanes. TMDS clock meets $t_{T3}$ for all three times.</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = H; \ TX_TERM_CNT = L; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps$</td>
<td>45</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = L; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps$</td>
<td>65</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>$SLEW_CNT = NC; \ TX_TERM_CNT = NC; \ PRE_SEL = NC; OE = H; DR = 6 \ Gbps; \ CLK = 150MHz$</td>
<td>100</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$i_{DCD}$</td>
<td>OUT_CLK ± duty cycle</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>40%</td>
<td>50%</td>
<td>60%</td>
<td></td>
</tr>
</tbody>
</table>
HDMI and DVI Main Link Switching Characteristics (接下页)

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tSK_INTER</td>
<td>Inter-pair output skew</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Default setting for internal inter-pair skew adjust, HDMI_SEL/A1 = NC</td>
<td>0.2</td>
<td></td>
<td></td>
<td>Tch</td>
</tr>
<tr>
<td>tSK_INTRA</td>
<td>Inter-pair output skew</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Default setting for internal inter-pair skew adjust, HDMI_SEL/A1 = NC</td>
<td>0.15</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>tJITC1(1.4b)</td>
<td>Total output clock jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLK = 297 MHz</td>
<td>0.25</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>tJITC1(2.0)</td>
<td>Total output clock jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DR = 6Gbps: CLK = 150 MHz</td>
<td>0.3</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td>tJITD2</td>
<td>Total output data jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.4 Gbps &lt; R_bit ≤ 3.712 Gbps</td>
<td>0.4</td>
<td></td>
<td></td>
<td>Tbit</td>
</tr>
<tr>
<td></td>
<td>3.712 Gbps &lt; R_bit &lt; 5.94 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.94 Gbps ≤ R_bit ≤ 6.0 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOD_range</td>
<td>Total TMDS data lanes output differential voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.4 Gbps &lt; R_bit ≤ 3.712 Gbps</td>
<td>335</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>3.712 Gbps &lt; R_bit &lt; 5.94 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.94 Gbps ≤ R_bit ≤ 6.0 Gbps</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) \(-0.0332R_{bit}^2 + 0.2312 R_{bit} + 0.1998\)
(2) \(-19.66 \times (R_{bit}^2) + (106.74 \times R_{bit}) + 209.58\)
### 7.11 AUX Switching Characteristics (Only for RGZ Package)

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_{I_{MAN}}$</td>
<td>Manchester transaction unit interval</td>
<td>0.4</td>
<td>0.6</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{AUXjitter_{TX}}$</td>
<td>Cycle-to-cycle jitter time at transmit pins</td>
<td>0.08</td>
<td></td>
<td></td>
<td>$U_{I_{MAN}}$</td>
</tr>
<tr>
<td>$t_{AUXjitter_{RX}}$</td>
<td>Cycle-to-cycle jitter time receive pins</td>
<td>0.05</td>
<td></td>
<td></td>
<td>$U_{I_{MAN}}$</td>
</tr>
</tbody>
</table>

### 7.12 HPD Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD(HPD)}$</td>
<td>Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge</td>
<td>See 图 14; not valid during switching time</td>
<td>40</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{T(HPD)}$</td>
<td>HPD logical disconnected timeout</td>
<td>See 图 15</td>
<td>2</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

### 7.13 DDC and I²C Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{r}$</td>
<td>Rise time of both SDA and SCL signals</td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Fall time of both SDA and SCL signals</td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HIGH}$</td>
<td>Pulse duration, SCL high</td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{LOW}$</td>
<td>Pulse duration, SCL low</td>
<td>1.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{SU1}$</td>
<td>Setup time, SDA to SCL</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ST, STA}$</td>
<td>Setup time, SCL to start condition</td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{HD, STA}$</td>
<td>Hold time, start condition to SCL</td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{ST, STO}$</td>
<td>Setup time, SCL to stop condition</td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{(BUF)}$</td>
<td>Bus free time between stop and start condition.</td>
<td>1.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{PLH1}$</td>
<td>Propagation delay time, low-to-high-level output</td>
<td>Source-to-sink: 100-kbps pattern; $C_b(Sink) = 400$-pF$^{(1)}$; See 图 18</td>
<td>360</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PHL1}$</td>
<td>Propagation delay time, high-to-low-level output</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PHL2}$</td>
<td>Propagation delay time, low-to-high-level output</td>
<td>Sink to Source: 100-kbps pattern; $C_b(Source) = 100$-pF$^{(1)}$; See 图 19</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PHL2}$</td>
<td>Propagation delay time, high-to-low-level output</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) $C_b =$ total capacitance of one bus line in pF.
7.14 Typical Characteristics

8 Parameter Measurement Information

图 1. Current vs Data Rate in Retimer Mode
图 2. Current vs Data Rate in Redriver Mode
图 3. $V_{\text{OD}}$ vs $V_{\text{sadj}}$
图 4. TMDS Main Link Test Circuit
Parameter Measurement Information (接下页)

图 5. Input and Output Timing Measurements

图 6. HDMI and DVI Sink TMDS Output Skew Measurements

图 7. TMDS Main Link Common Mode Measurements
Parameter Measurement Information (接下页)

图 8. Output Differential Waveform 0 dB De-Emphasis

图 9. PRE_SEL = L for –2-dB De-Emphasis
Parameter Measurement Information

(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8” of FR4, AC coupling cap, connector and another 1-2” of FR4. Trace width – 4 mils. 100-Ω differential impedance.

(2) All jitter is measured at a BER of 10^-9.

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1.

(4) AVCC = 3.3-V

(5) RT = 50-Ω

(6) The input signal from parallel bit error rate tester (BERT) does not have any pre-emphasis. Refer to Recommended Operating Conditions.

图 10. TMDS Output Jitter Measurement

图 11. Post EQ Input Eye Mask at TTP2_EQ
Parameter Measurement Information (接下页)

<table>
<thead>
<tr>
<th>TMDS DATA RATE (Gbps)</th>
<th>H (Tbit)</th>
<th>V (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.4 &lt; DR &lt; 3.712</td>
<td>0.6</td>
<td>335</td>
</tr>
<tr>
<td>3.712 &lt; DR &lt; 5.94</td>
<td>(-0.0332R_{\text{b}}^2 + 0.2312R_{\text{b}} + 0.1998)</td>
<td>(-19.66R_{\text{b}}^2 + 106.74R_{\text{b}} + 209.58)</td>
</tr>
<tr>
<td>5.94 ≤ DR ≤ 6.0</td>
<td>0.4</td>
<td>150</td>
</tr>
</tbody>
</table>

图 12. Output Eye Mask at TTP4_EQ
图 13. HPD Test Circuit

图 14. HPD Timing Diagram Number 1

图 15. HPD Logic Disconnect Timeout
图 16. Start and Stop Condition Timing

图 17. SCL and SDA Timing
图 18. DDC Propagation Delay – Source to Sink

图 19. DDC Propagation Delay – Sink to Source
9 Detailed Description

9.1 Overview
The SNx5DP159 device is a Dual Mode[1] DisplayPort retiming level shifter that supports data rates up to 6-Gbps for HDMI2.0a. The device takes in AC coupled HDMI/DVI signals and level shifts them to TMDS signals while compensating for loss and jitter through its receiver equalizer and retiming functions. The SNx5DP159 in default configuration should meet most system needs but also provides features that allow the system implementer flexibility in design. Programming can be accomplished through I2C[4] or pin strapping.

9.2 Functional Block Diagram

NOTE: Black pin names are common to both packages. Blue pin names are only in the SNx5DP159 RGZ package.
9.3 Feature Description

9.3.1 Reset Implementation

When OE is de-asserted, control signal inputs are ignored; the Dual Mode[1] DisplayPort inputs and outputs are high impedance. It is critical to transition the OE input from a low level to a high level after the \( V_{CC} \) supply has reached the minimum recommended operating voltage. Achieve this transition by a control signal to the OE input, or by an external capacitor connected between OE and GND. To ensure that the SNx5DP159 device is properly reset, the OE pin must be de-asserted for at least 100-\( \mu \)s before being asserted. When OE is toggled in this manner the device is reset. This requires the device to be reprogrammed if it was originally programmed through \( \text{I}^2\text{C} \) for configuration. When implementing the external capacitor, the size of the external capacitor depends on the power-up ramp of the \( V_{CC} \) supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for SNx5DP159; consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor. Both OE implementations are shown in 图 20 and 图 21.

![图 20. External Capacitor Controlled OE](image1)

![图 21. OE Input from Active Controller](image2)

9.3.2 Operation Timing

SNx5DP159 starts to operate after the OE signal goes high (see 图 22, 图 23, and 表 1). Keeping OE low until \( V_{DD} \) and \( V_{CC} \) become stable avoids any timing requirements as shown in 图 22.

![图 22. Power-Up Timing for SSNx5DP159](image3)
Feature Description (接下页)

图 23. CDR Timing for SNx5DP159

表 1. SNx5DP159 Operation Timing

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_d1</td>
<td>V_DD/V_CC stable before V_CC/V_DD</td>
<td>0</td>
<td>200</td>
</tr>
<tr>
<td>t_d2</td>
<td>V_DD and V_CC stable before OE deassertion</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>t_d3</td>
<td>CDR active operation after retimer mode initial</td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td>t_d4</td>
<td>CDR turn off time after retimer mode de-assert</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>VDD_ramp</td>
<td>V_DD supply ramp-up requirements</td>
<td>100</td>
<td>ms</td>
</tr>
<tr>
<td>VCC_ramp</td>
<td>V_CC supply ramp-up requirements</td>
<td>100</td>
<td>ms</td>
</tr>
</tbody>
</table>

9.3.3 I²C-over-AUX to DDC Bridge (SNx5DP159 48-Pin Package Version Only)

The SNx5DP159 device incorporates the I²C-over-AUX to DDC bridge to support the DisplayPort Dual-Mode standard version 1.1. It enables the communication between source device and sink device through AUX channel. The bridge receives the request from source device in the I²C-over-AUX format and transfers it into DDC signal to sink device. When the sink device responds, the request in the DDC channel and bridge packages it into I²C-over-AUX and sends it back to the source device.

9.3.4 Input Lane Swap and Polarity Working

The SNx5DP159 device incorporates the swap function, which can set the input lanes in swap mode. The IN_D2 routes to the OUT_CLK position. The IN_D1 swaps with IN_D0. The swap function only changes the input pins; EQ setup follows new mapping. The SWAP/POL is pin 1 in the 48-pin RGZ package. For the RSB version, the user needs to control the register 0x09h bit 7 for SWAP enable. Lane swap is operational in both redriver and retimer mode.

表 2. Lane Swap(1)

<table>
<thead>
<tr>
<th>NORMAL OPERATION</th>
<th>SWAP = L OR CSR 0x09h BIT 7 IS 1'b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_D2 → OUT_D2</td>
<td>IN_D2 → OUT_CLK</td>
</tr>
<tr>
<td>IN_D1 → OUT_D1</td>
<td>IN_D1 → OUT_D0</td>
</tr>
<tr>
<td>IN_D0 → OUT_D0</td>
<td>IN_D2 → OUT_D1</td>
</tr>
<tr>
<td>IN_CLK → OUT_CLK</td>
<td>IN_CLK → OUT_D2</td>
</tr>
</tbody>
</table>

(1) The output lanes never change. Only the input lanes change. See 图 24 and 图 25.
The SNx5DP159 can also change the polarity of the input signals. When SWAP/POL is high, the n and p pins on each lane will swap. Use Register 0x9h bit 6 to swap polarity using \( I^2C \). Polarity swap only works for retimer mode. When the device is in automatic redriver to retimer mode this only works when device is in retimer stage. If set and data rate falls below 1.0-Gbps in this mode the polarity function will be lost.
9.3.5 Main Link Inputs

Standard Dual Mode [1] DisplayPort terminations are integrated on all inputs with expected AC coupling capacitors on board prior to input pins. External terminations are not required. Each input data channel contains an adaptive or fixed equalizer to compensate for cable or board losses. The voltage at the input pins must be limited below the absolute maximum ratings. The input pins have incorporated failsafe circuits. The input pins can be polarity changed through the local I2C register or pin strapping.

9.3.6 Main Link Inputs Debug Tools

There are two methods for debugging a system making sure the inputs to the SNx5DP159 are valid. A TMDS error checker is implemented that will increment an error counter per data lane. This allows the system implementer to determine how the link between the source and SNx5DP159 is performing on all three data lanes. See CSR Bit Field Definitions – RX PATTERN VERIFIER CONTROL/STATUS register in 表 10.

If a high error count is evident, the SNx5DP159 has the ability to provide the general eye quality. A tool is available that uses the I2C [4] link to download data that can be plotted for an eye diagram. This is available per data lane.

9.3.7 Receiver Equalizer

Equalizers are used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. The SNx5DP159 device supports both fixed receiver equalizer (redriver and retimer mode) and adaptive receive equalizer (retimer mode) by setting the EQ_SEL/A0 pin or through I2C using reg0Ah[5]. When the EQ_SEL/A0 pin is high, the EQ gain is fixed to 14-dB. The EQ gain will be 7.5-dB if the EQ_SEL/A0 pin is set low. The SNx5DP159 device operates in adaptive equalizer mode when EQ_SEL/A0 left floating. Using adaptive equalization the gain will be automatically adjusted based on the data rate to compensate for variable trace or cable loss. Using the local I2C[4] control, reg0Dh[5:1], the fixed EQ gain can be selected for both data and clock.

![Adaptive EQ Gain Curve](image)

图 26. Adaptive EQ Gain Curve

9.3.8 Termination Impedance Control

HDMI2.0 [3] standard requires the transmitter termination impedance should be between 75 to 150-Ω. Older versions of the HDMI standard required no source termination. For HDMI1.4b [2] when data rate over 2 Gbps, the output performance could be better if the termination value between 150 to 300-Ω which was allowed. The SNx5DP159 supports three different source termination impedances for HDMI1.4b [2] and HDMI2.0 [3]. Pin 36, TX_TERM_CTL, offers a selection option to choose the output termination impedance value. This can be adjusted by I2C[4]; reg0Bh[4:3] TX_TERM_CTL.
9.3.9 TMDS Outputs

An 1% precision resistor, 7.06-kΩ, is recommended to be connected from Vsadj pin to ground to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability when no source term is enabled, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor. As compliance testing is system dependant this resistor value can be adjusted.

Referring to 图 27, if both Vcc (device supply) and AVCC (sink termination supply) are powered, the TMDS output signals are high impedance when OE = low. The normal operating condition is that both supplies are active. A total of 33-mW of power is consumed by the terminations independent of the OE logical selection. When AVCC is powered on, normal operation (OE controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the IO(off) (output leakage current) specification ensures the leakage current is limited 45-μA or less.

The clock and data lanes VOD can be changed through I²C[4] (see VSWING_CLK and VSWING_DATA in 表 8 for details). 图 3 shows the different output voltage based on different Vsadj resistor values.

9.3.9.1 Pre-Emphasis/De-Emphasis

The SNx5DP159 provides De-emphasis as a way to compensate for the ISI loss between the TMDS outputs and the receiver it is driving. There are two methods to implement this function. When in pin strapping mode the PRE_SEL pin controls this. The PRE_SEL pin provides −2-dB, or 0-dB de-emphasis, which allows output signal pre-conditioning to offset interconnect losses from the SNx5DP159 device outputs to a TMDS receiver. TI recommends setting PRE_SEL at 0 dB while connecting to a receiver through a short PCB route. When pulled to ground with a 65-kΩ resistor −2-dB can be realized, see 图 9. When using I²C, Reg0Ch[1:0] is used to make these adjustments.

As there are times true pre-emphasis may be the best solution there are two ways to accomplish this. If pin strapping is being use the best method is to reduce the Vsadj resistor value increasing the VOD and then pulling the PRE_SEL pin to ground using the 65-kΩ resistor, see 图 28. If using I²C this can be accomplished using two methods. First is similar to pin strapping by adjusting the Vsadj resistor value and then implementing −2-dB de-emphasis. Second method is to set Reg0Ch[7:5] = 011 and the set Reg0Ch[1:0] = 01 which accomplishes the same pre-emphasis setting. See 图 29.
PRE_SEL = Z  
Vsadj = 7.06KΩ

PRE_SEL = L  
Vsadj = 4.5KΩ

1st bit

2nd to N bit

VOD(PP) = 1400mVpp  
VOD(SS) = 1150mVpp

PRE_SEL = Z  
Vsadj = 7.06KΩ

Vsadj = 7.06KΩ  
I2C Reg0Ch[7:5] = 011  
Reg0C[1:0] = 01

1st bit

2nd to N bit

VOD(PP) = 1200mVpp  
VOD(SS) = 1020mVpp

图 28. Pre-Emphasis Using Pin Strapping Method

图 29. Pre-Emphasis Using I2C Method
9.4 Device Functional Modes

9.4.1 Retimer Mode

Clock and data recovery circuits (CDR) are used to track, sample and retime the equalized data bit streams. The CDRs are designed with loop bandwidth to minimize the amount of jitter transfer from the video source to the TMDS outputs. Input jitter within the CDR’s PLL bandwidth, < 1-MHz, will be transferred to the TMDS outputs. Higher frequency jitter above the CDR loop bandwidth is attenuated, providing a jitter cleaning function to reduce the amount of high frequency jitter from the video source. The retimer is automatically activated at pixel clock above approximately 100-MHz when jitter cleaning is needed for robust operation. The retimer operates at about 1.0 to 6-Gbps DR supporting HDMI2.0[3]. At pixel clock frequency below about 100 MHz, the SNx5DP159 automatically bypasses the internal retimer and operates as a redriver. When the video source changes resolution, the internal retimer starts the acquisition process to determine the input clock frequency and acquire lock to the new data bit streams. During the clock frequency detection period and the retimer acquisition period (that last approximately 7-ms), the TMDS drivers can be kept active (default) or programmed to be disabled to avoid sending invalid clock or data to the downstream receiver.

9.4.2 Redriver Mode

The SNx5DP159 also has a redriver mode that can be enabled through I2C[4]; at offset address 0Ah bits 1:0 DEV_FUNC_MODE. When in this mode, the CDR and PLL are shut off, thus reducing power. Jitter performance is degraded as the device will now only compensate for ISI loss in the link. In redriver mode HDMI2.0[3] compliance is not guaranteed as skew compensation and retiming functions are disabled. Excessive random or phase jitter will not be compensated.

9.4.3 DDC Training for HDMI2.0 Data Rate Monitor

As part of discovery, the source reads the sink’s E-EDID information to understand the sink’s capabilities. Part of this read is HDMI forum vendor specific data block (HF-VSDB) MAX_TMDS_Character_Rate byte to determine the data rate supported. Depending upon the value, the source will write to slave address 0xA8 offset 0x20 bit1, TMDS_CLOCK_RATIO_STATUS. The SNx5DP159 snoops this write to determine the TMDS clock ratio and thus sets its own TMDS_CLOCK_RATIO_STATUS bit accordingly. If a 1 is written, then the TMDS clock is 1/40 of TMDS bit period. If a 0 is written, then the TMDS clock is 1/10 of TMDS bit period. The SNx5DP159 will always default to 1/10 of TMDS bit period unless a 1 is written to address 0xA8 offset 0x20 bit 1. When HPD_SNK is de-asserted, this bit is reset to default values. If the source does not write this bit the SNx5DP159 will not be configured for TMDS clock 1/40 mode in support of HDMI2.0. As the SNx5DP159 is in link but not recognized as part of the link it is possible that the source could read the sink EDID where this bit is set and does not re-write this bit. If the SNx5DP159 has entered a power down state this bit is cleared and does not re-set on a read. To work properly the bit has to be set again with a write by the source.

9.4.4 DDC Functional Description

The SNx5DP159 solves sink- or source-level issues by implementing a master/slave control mode for the DDC bus. When the SNx5DP159detects the start condition on the DDC bus from the SDA_SRC/SCL_SRC, it will transfer the data or clock signal to the SDA_SNK/SCL_SNK with little propagation delay. When SDA_SNK detects the feedback from the downstream device, the SNx5DP159 will pull up or pull down the SDA_SRC bus and deliver the signal to the source.

The DDC link defaults to 100 kbps, but can be set to various values including 400 kbps by setting the correct value to address 22h (see 表3) through the I2C access on the DDC interface. The DDC lines are 5-V tolerant. The HPD_SRC goes to high impedance when VCC is under low power conditions, < 1.5-V.

注

The SNx5DP159 uses clock stretching for DDC transactions. As there are sources and sinks that do not perform this function correctly a system may not work correctly as DDC transactions are incorrectly transmitted/received. To overcome this a snoop configuration can be implemented where the SDA/SCL from the source is connected directly to the SDA/SCL sink. The SNx5DP159 will need its SDA_SNK and SCL_SNK pins connected to this link in order to the SNx5DP159 to configure the TMDS_CLOCK_RATIO_STATUS bit. Care must be taken when this configuration is being implemented as the voltage levels for DDC between the source and sink may be different, 3.3 V vs 5 V.
9.5 Register Maps

9.5.1 DP-HDMI Adaptor ID Buffer

The SNx5DP159 device includes the DP-HDMI adapter ID buffer for HDMI/DVI adaptor recognition, defined by the VESA DisplayPort Dual-Mode Standard Version 1.1, accessible by standard I^2C protocols through the DDC interface when the HDMI_SEL/A1 pin is low. The DP-HDMI adapter buffer and extended DDC register for Type 2 capability is accessed at target addresses 80h (Write) and 81h (Read).

The DP-HDMI adapter buffer contains a read-only phrase DP-HDMI ADAPTOR<EOT> converted to ASCII characters, as shown in 表 3, and supports the WRITE command procedures (accessed at target address 80h) to select the subaddress, as recommended in the VESA DisplayPort Interoperability Guideline Adaptor Checklist Version 1.0 section 2.3.

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
<th>Value HDMI</th>
<th>Value DVI</th>
<th>Read or Read/Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>HDMI ID code</td>
<td>44h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>01h</td>
<td>Bit 0: ADAPTOR_REVISION</td>
<td>50h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>02h</td>
<td>Bit 3: Reserved: but 0 for type 2</td>
<td>2Dh</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>03h</td>
<td>Bit 7:4 1010 = Dual mode defined by dual mode[1] standard</td>
<td>48h</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>04h</td>
<td>Device ID</td>
<td>44h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>05h</td>
<td>Hardware revision</td>
<td>4Dh</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>06h</td>
<td>IEE_OUI first two hex digits</td>
<td>49h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>07h</td>
<td>IEE_OUI second two hex digits</td>
<td>20h</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>08h</td>
<td>IEE_OUI third two hex digits</td>
<td>41h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>09h</td>
<td>00h</td>
<td>44h</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>0Ah</td>
<td>41h</td>
<td>44h</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>0Bh</td>
<td>50h</td>
<td>41h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>0Ch</td>
<td>54h</td>
<td>50h</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>0Dh</td>
<td>4Fh</td>
<td>54h</td>
<td>00h</td>
<td></td>
</tr>
<tr>
<td>0 Eh</td>
<td>52h</td>
<td>4Fh</td>
<td>00h</td>
<td>Read only</td>
</tr>
<tr>
<td>0Fh</td>
<td>04h</td>
<td>52h</td>
<td>00h</td>
<td></td>
</tr>
</tbody>
</table>

表 3. SNx5DP159 DP-HDMI Adaptor ID Buffer and Extended DDC
### Register Maps (接下页)

表 3. SNx5DP159 DP-HDMI Adaptor ID Buffer and Extended DDC (接下页)

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
<th>Value HDMI</th>
<th>Value DVI</th>
<th>Read or Read/Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Dh</td>
<td>Max TMDS clock rate&lt;br&gt;Default value is F0h in HDMI column&lt;br&gt;Note: Value determined by taking clock rate and dividing by 2.5 and converting to HEX. For HDMI2.0 extend as if the clock rate extended instead of its actual method, clock 1/10 DR and not 1/40 DR.</td>
<td>F0h</td>
<td>42h</td>
<td>Read only</td>
</tr>
<tr>
<td>1Eh</td>
<td>If I2C_DR_CTL = 0 the value is 0Fh → If DDC_AUX_DR_SEL = 0 the value is 0Fh&lt;br&gt;If I2C_DR_CTL = 1 the value is 1Fh → If DDC_AUX_DR_SEL = 1 then value is 1Fh&lt;br&gt;If I2C_DR_CTL = 0 the value is 0Fh&lt;br&gt;If I2C_DR_CTL = 1 the value is 1Fh</td>
<td>0Fh</td>
<td>0Fh</td>
<td>Read only</td>
</tr>
<tr>
<td>1Fh</td>
<td>Reserved</td>
<td>00h</td>
<td>00h</td>
<td>Write/Read</td>
</tr>
<tr>
<td>20h</td>
<td>TMDS_OE&lt;br&gt;Bit 0: 0 = TMDS_ENABLED (default)&lt;br&gt;1 = TMDS_DISABLED&lt;br&gt;Bits 7:1 Reserved</td>
<td>00h</td>
<td>00h</td>
<td>Write/Read</td>
</tr>
<tr>
<td>21h</td>
<td>HDMI Pin Control&lt;br&gt;Bit 0 = CEC_EN&lt;br&gt;Enables connection between the HDMI CEC pin connected to the sink and the CONFIG2 pin to the upstream device + 27-kΩ pullup.&lt;br&gt;0 = CEC_DISABLED (default)&lt;br&gt;1 = CEC_ENABLED&lt;br&gt;Bits 7:1 = RESERVED</td>
<td>00h</td>
<td>00h</td>
<td>Write/Read</td>
</tr>
<tr>
<td>22h</td>
<td>Writing a bit pattern to this register that is not defined above may result in an unpredictable I2C speed selection, but the adaptor must continue to otherwise work normally. Only applicable when using I2C-over-AUX transport&lt;br&gt;01h = 1-Kbps&lt;br&gt;02h = 5-Kbps&lt;br&gt;04h = 10-Kbps&lt;br&gt;08h = 100-kbps&lt;br&gt;10h = 400-Kbps (RSVD in Dual Mode STND)&lt;br&gt;On read, the dual-mode cable adaptor returns a value to indicate the speed currently in use. The default I2C speed prior to software writing to this register is 100-Kbps.&lt;br&gt;Illegal write value shall write register default (08h). This register sets the DDC output DR whether I2C-over-AUX or straight DDC</td>
<td>08h</td>
<td>08h</td>
<td>Write/Read</td>
</tr>
<tr>
<td>23h-FFh</td>
<td>Reserved</td>
<td>00h</td>
<td>00h</td>
<td>Read</td>
</tr>
</tbody>
</table>

### 9.5.2 Local I2C Interface Overview

The SCL_CTL and SDA_CTL pins are used for I2C clock and I2C data respectively. The SNx5DP159 I2C interface conforms to the 2-wire serial interface defined by the I2C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400 kbps.

The device address byte is the first byte received following the start condition from the master device. The 7-bit device address for the SNx5DP159 device decides by the combination of EQ_SEL/A0 and HDMI_SEL/A1. 表 4 clarifies the SNx5DP159 device target address.
### I2C Device Address Description

<table>
<thead>
<tr>
<th>A1/A0</th>
<th>SNx5DP159 I2C Device Address</th>
<th>ADD</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1</td>
<td>0/1 BC/BD</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>1/0 BA/BB</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0/0 B8/B9</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>0/1 B6/B7</td>
</tr>
</tbody>
</table>

#### 9.5.3 I2C Control Behavior

Follow this procedure to write to the SNx5DP159 device I2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SNx5DP159 device 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The SNx5DP159 device acknowledges the address cycle by combination of A0 and A1.
3. The master presents the subaddress (I2C register within SNx5DP159 device) to be written, consisting of one byte of data, MSB-first.
4. The SNx5DP159 device acknowledges the subaddress cycle.
5. The master presents the first byte of data to be written to the I2C register.
6. The SNx5DP159 device acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SNx5DP159.
8. The master terminates the write operation by generating a stop condition (P).

Follow this procedure to read the SNx5DP159 I2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SNx5DP159 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The SNx5DP159 device acknowledges the address cycle by combination of A0 and A1.
3. The master presents the subaddress (I2C register within SNx5DP159 device) to be read, consisting of one byte of data, MSB-first.
4. The SNx5DP159 device acknowledges the subaddress cycle.
5. The master initiates a read operation by generating a start condition (S), followed by the SNx5DP159 7-bit address and a one-value W/R bit to indicate a read cycle.
6. The SNx5DP159 device acknowledges the address cycle.
7. The SNx5DP159 device transmit the contents of the memory registers MSB-first starting at the written subaddress.
8. The SNx5DP159 device will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer.
9. If an ACK is received, the SNx5DP159 device transmits the next byte of data.
10. The master terminates the read operation by generating a stop condition (P).

Upon reset, the SNx5DP159 sub-address will always be set to 0x00. When no subaddress is included in a read operation, the SNx5DP159 subaddress increments from previous acknowledged read or write data byte. If it is required to read from a subaddress that is different from the SNx5DP159 internal subaddress, a write operation with only a subaddress specified is needed before performing the read operation.

Refer to 表 6 for the SNx5DP159 device local I2C register descriptions. Reads from reserved fields return 0s and writes are ignored.
9.5.4 I2C Control and Status Registers

Reads from reserved fields return 0, and writes to read-only reserved registers are ignored. Writes to reserved registers, which are marked with ‘W’, produce unexpected behavior. All addresses not defined by this specification are considered reserved. Reads from these addresses return 0 and writes will be ignored.

9.5.4.1 Bit Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are described in 表 5.

### 表 5. Field Access Tags

<table>
<thead>
<tr>
<th>ACCESS TAG</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Read</td>
<td>The field is read by software</td>
</tr>
<tr>
<td>W</td>
<td>Write</td>
<td>The field is written by software</td>
</tr>
<tr>
<td>S</td>
<td>Set</td>
<td>The field is set by a write of one. Writes of 0 to the field have no effect</td>
</tr>
<tr>
<td>C</td>
<td>Clear</td>
<td>The field is cleared by a write of 1. Writes of 0 to the field have no effect</td>
</tr>
<tr>
<td>U</td>
<td>Update</td>
<td>Hardware may autonomously update this field</td>
</tr>
<tr>
<td>NA</td>
<td>No access</td>
<td>Not accessible or not applicable</td>
</tr>
</tbody>
</table>

9.5.4.2 CSR Bit Field Definitions

9.5.4.2.1 ID Registers

### 表 6. ID Registers

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BIT</th>
<th>DESCRIPTION</th>
<th>ACCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h:07h</td>
<td>7:0</td>
<td>DEVICE_ID</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td></td>
<td>These fields return a string of ASCII characters “DP159” followed by three space characters. Address 0x00 – 0x07 = {0x44“D”, 0x50“P”, 0x31“1”, 0x35“5”, 0x39“9”, 0x20, 0x20, 0x20}</td>
<td></td>
</tr>
<tr>
<td>08h</td>
<td>7:0</td>
<td>REV_ID. This field identifies the device revision. 0000001 – DP159 revision 1</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x000001 – DP159 revision 1</td>
<td></td>
</tr>
</tbody>
</table>
### 9.5.4.2.2 Misc Control

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BIT</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
<th>ACCESS</th>
</tr>
</thead>
</table>
| 09h     | 7   | 1'b0    | SWAP_EN: This field enables swapping the input main link lanes  
0 – Disable (default)  
1 – Enable  
Note: field is loaded from SWAP/POL pin; Writes ignored when I2C_EN/PIN = 0 | RWU |
|         | 6   | 1'b0    | LANE_POLARITY: swaps the input data and clock lanes polarity.  
0 – Disabled: No polarity swap  
1 – Swaps the input data and clock lane polarity  
Note: field is loaded from SWAP/POL pin; Writes ignored when I2C_EN/PIN = 0. This feature is only valid when in retimer mode. | RWU |
|         | 5:4 | 2'b00   | Reserved | R |
|         | 3   | 1'b0    | PD_EN  
0 – Normal working (default)  
1 – Forced power-down by I²C, lowest power state | RW |
|         | 2   | 1'b0    | HPD_AUTO_PWRDWN_DISABLE  
0 – Automatically enters power down mode based on HPD_SNK (default)  
1 – Will not automatically enter power mode based upon HPD_SNK | RW |
|         | 1:0 | 2'b10   | I²C_DR_CTL. I²C data rate supported for configuring device  
00 – 5-kbps  
01 – 10-kbps  
10 – 100-kbps (default)  
11 – 400-kbps (Note: HPD_AUTO_PWRDWN_DISABLE must be set before enabling 400 Kbps mode) | RW |
| 0Ah     | 7   | 1'b0    | Application Mode Selection  
0 – Source (default) - Set the adaptive EQ mid point to between 6.5-dB and 7.5-dB  
1 – Sink - Sets the adaptive EQ starting point to between 12-dB and 13-dB | RW |
|         | 6   | 1'b0    | HPDSNK_GATE_EN: This field sets the functional relationship between HPD_SNK and HPD_SRC.  
0 – HPD_SNK passed through to the HPD_SRC (default)  
1 – HPD_SNK will not pass through to the HPD_SRC. | RW |
|         | 5   | 1'b1    | EQ_ADA_EN: this field enables the equalizer working state.  
0 – Fixed EQ  
1 – Adaptive EQ (default)  
 Writes are ignored when I2C_EN/PIN = 0 | RWU |
|         | 4   | 1'b1    | EQ_EN: this field enables the receiver equalizer.  
0 – EQ disabled  
1 – EQ enable (default) | RW |
|         | 3   | 1'b1    | AUX_BRG_EN: this field enable the AUX bridge working. This is only valid for the 48-pin package.  
0 – AUX bridge disable  
1 – AUX bridge enable (default) | RWU |
|         | 2   | 1'b0    | APPLY_RXTX_CHANGES , Self clearing write-only bit. Writing a 1 to this bit will apply new slew, tx_term, twps1, eqen, eqadapt, swing, eqf, eqlev settings to the clock and data lanes. Writes to the respective registers do not take immediate effect. This bit does not need to be written if I²C configuration occurs while OE or hpd_sink are low, I²C power down is active. | W |
|         | 1:0 | 2'b01   | DEV_FUNC_MODE: This field selects the device working function mode.  
00 – Redriver mode across full range 250 Mbps to 6-Gbps  
01 - Automatic redriver to retimer crossover at 1.0 Gbps (default)  
10 - Automatic retimer for HDMI2.0  
11 - Retimer mode across full range 250 Mbps to 6-Gbps  
When changing crossover point, need to toggle PD_EN or toggle external HPD_SNK. | RW |

**Mode Selection Definition:** This bit lets the receiver know where the device is located in a system for the purpose of centering the AEQ point. The SNx5DP159 is targeting the source application, so the default value is 0, which will center the EQ at 6.5 to 7.5-dB depending upon TMDS_CLOCK_RATIO_STATUS value, see 表 9. If the SNx5DP159 is in a dock or sink application, the value should be changed to a value of 1, which will center the EQ at 12 to 13-dB depending upon TMDS_CLOCK_RATIO_STATUS value.
## 9.5.4.2.3 HDMI Control

### 表 8. HDMI Control

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BIT</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
<th>ACCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Bh</td>
<td>7:6</td>
<td>2'b00</td>
<td>SLEW_CTL: Slew rate control. 2'b0 is fastest and 2'b11 is slowest. Writes ignored when I2C_EN/PIN = 0</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>1'b0</td>
<td>HDMI_SEL: Control; Writes ignored when I2C_EN/PIN = 0</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 – HDMI (default)</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 – DVI</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td>4:3</td>
<td>2'b00</td>
<td>TX_TERM_CTL: Controls termination for HDMI TX</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 – No termination</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 – 150 to 300-Ω</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 – Reserved</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 – 75 to 150-Ω</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: Reflects the value of the TX_TERM_CTL pin; Writes ignored when I2C_EN/PIN = 0</td>
<td>RWU</td>
</tr>
<tr>
<td>0Ch</td>
<td>2</td>
<td>1'b0</td>
<td>Reserved</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1'b0</td>
<td>TMDS_CLOCK_RATIO_STATUS: This field is updated from snoop of I²C write to slave address 0xA8 offset 0x20 bit 1 that occurred on the SDA_SRC/SCL_SRC interface. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b1, then this field will be set to a 1'b1. When bit 1 of address 0xA8 offset 0x20 is written to a 1'b0, then this field will be set to a 1'b0. This field is reset to the default value whenever HPD_SNK is de-asserted for greater than 2 ms.</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 – TMDS clock is 1/10 of TMDS bit period (default)</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 – TMDS clock is 1/40 of TMDS bit period</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1'b0</td>
<td>DDC_TRAIN_SET: This field indicates the DDC training block function status. If disabled, the device can only work at the HDMI1.4b[2] or DVI mode</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 – DDC training enable (default)</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 – DDC training disable</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: To force TMDS_CLOCK_RATIO_STATUS to 1, this register bit must be set to 1 which will force the 1/40 mode for HDMI2.0.</td>
<td>RW</td>
</tr>
<tr>
<td>0Ch</td>
<td>7:5</td>
<td>3'b000</td>
<td>VSWING_DATA: Data output swing control</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000 – Vsadj set</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001 – Increase by 7%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010 – Increase by 14%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011 – Increase by 21%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 – Decrease by 30%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101 – Decrease by 21%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110 – Decrease by 14%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111 – Decrease by 7%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td>4:2</td>
<td>3'b000</td>
<td>VSWING_CLK: Clock Output Swing Control</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000 – Vsadj set</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001 – Increase by 7%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010 – Increase by 14%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011 – Increase by 21%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 – Decrease by 30%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101 – Decrease by 21%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110 – Decrease by 14%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111 – Decrease by 7%</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: Default is set by DR, which means standard based swing values but this allows for the swing to be overridden by selecting one of these values</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td>1:0</td>
<td>2'b00</td>
<td>HDMI_TWST1. HDMI de-emphasis FIR post-cursor-1 signed tap weight.</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 – No de-emphasis</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 – 2-dB de-emphasis</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 – Reserved</td>
<td>RWU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 – Reserved</td>
<td>RWU</td>
</tr>
</tbody>
</table>
### 9.5.4.2.4 Equalization Control Register

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BIT</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
<th>ACCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Dh</td>
<td>7:6</td>
<td>2'b00</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td>5:3</td>
<td>1'b000</td>
<td>Data Lane EQ – Sets fixed EQ values</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HDMI1.4b[2] HDMI2.0[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000 – 0-dB 000 – 0-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001 – 4.5-dB 001 – 3-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010 – 6.5-dB 010 – 5-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011 – 8.5-dB 011 – 7.5-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 – 10.5-dB 100 – 9.5-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101 – 12-dB 101 – 11-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110 – 14-dB 110 – 13-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111 – 16.5-dB 111 – 14.5-dB</td>
<td></td>
</tr>
<tr>
<td>2:1</td>
<td>2:1</td>
<td>1'b00</td>
<td>Clock Lane EQ - Sets fixed EQ values</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HDMI1.4b[2] HDMI2.0[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 – 0-dB 00 – 0-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 – 1.5-dB 01 – 1.5-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 – 3-dB 10 – 3-dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 – RSVD 11 – 4.5-dB</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1'b0</td>
<td>0 – Clock VOD is half the set value when TMDS_CLOCK_RATIO_STATUS states in HDMI2.0 mode</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 – Disables TMDS_CLOCK_RATIO_STATUS control of the clock VOD so the output swing is full swing</td>
<td></td>
</tr>
</tbody>
</table>

### 9.5.4.2.5 EyeScan Control Register

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BITS</th>
<th>DEFAULT</th>
<th>DESCRIPTION</th>
<th>ACCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0Eh</td>
<td>7:4</td>
<td>4'b0000</td>
<td>PV_SYNC[3:0]. Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>3:0</td>
<td>4'b0000</td>
<td>PV_LD[3:0]. Load pattern-verifier controls into RX lanes. When asserted high, the PV_TO, PV_SEL, PV_LEN, PV_CP20, and PV_CP values are enabled into the corresponding RX lane. These values are then latched and held when PV_LD[n] is subsequently de-asserted low. 1 bit per lane.</td>
<td>RWU</td>
</tr>
<tr>
<td>0Fh</td>
<td>7:4</td>
<td>4'b0000</td>
<td>PV_FAIL[3:0]. Pattern verification mismatch detected. 1 bit per lane.</td>
<td>RU</td>
</tr>
<tr>
<td></td>
<td>3:0</td>
<td>4'b0000</td>
<td>PV_TIP[3:0]. Pattern search/training in progress. 1 bit per lane.</td>
<td>RU</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>1'b0</td>
<td>PV_CP20. Customer pattern length 20 or 16 bits.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 – 16 bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 – 20 bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>1'b0</td>
<td>Reserved</td>
<td>R</td>
</tr>
<tr>
<td>10h</td>
<td>5:3</td>
<td>3'b000</td>
<td>PV_LEN[2:0]. PRBS pattern length</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000 – PRBS7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>001 – PRBS11</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>010 – PRBS23</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>011 – PRBS31</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 – PRBS15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>101 – PRBS15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>110 – PRBS20</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>111 – PRBS20</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2:0</td>
<td>3'b000</td>
<td>PV_SEL[24:0]. Pattern select control</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000 – Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>001 – PRBS</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>010 – Clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>011 – Custom</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1xx – Timing only mode with sync pulse spacing defined by PV_LEN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11h</td>
<td>7:0</td>
<td>1'h00</td>
<td>PV_CP[7:0]. Custom pattern data.</td>
<td>RW</td>
</tr>
<tr>
<td>12h</td>
<td>7:0</td>
<td>1'h00</td>
<td>PV_CP[15:8]. Custom pattern data.</td>
<td>RW</td>
</tr>
<tr>
<td>ADDRESS</td>
<td>BITS</td>
<td>DEFAULT</td>
<td>DESCRIPTION</td>
<td>ACCESS</td>
</tr>
<tr>
<td>---------</td>
<td>------</td>
<td>---------</td>
<td>-------------</td>
<td>--------</td>
</tr>
<tr>
<td>13h</td>
<td>7:4</td>
<td>4'b0000</td>
<td>Reserved</td>
<td>R</td>
</tr>
<tr>
<td>3:0</td>
<td>4'b0000</td>
<td>PV_CP[19:16]. Custom pattern data. Used when PV_CP20 = 1'b1.</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>14h</td>
<td>7:3</td>
<td>5'b00000</td>
<td>Reserved</td>
<td>R</td>
</tr>
<tr>
<td>2:0</td>
<td>3'b000</td>
<td>PV_THR[2:0]. Pattern-verifier retain threshold.</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>15h</td>
<td>7</td>
<td>1'b0</td>
<td>DESKEW_CMPLT: Indicates TMDS lane deskew has completed when high</td>
<td>R</td>
</tr>
<tr>
<td>6:5</td>
<td>2'b0</td>
<td>Reserved</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1'b0</td>
<td>BERT_CLR. Clear BERT counter (on rising edge).</td>
<td>RSU</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>1'b0</td>
<td>TST_INQ_CLR. Clear latched interrupt flag.</td>
<td>RSU</td>
<td></td>
</tr>
<tr>
<td>2:0</td>
<td>3'b000</td>
<td>TST_SEL[2:0]. Test interrupt source select.</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>16h</td>
<td>7:4</td>
<td>4'b0000</td>
<td>PV_DP_EN[3:0]. Enabled datapath verified based on DP_TST_SEL, 1 bit per lane.</td>
<td>RW</td>
</tr>
<tr>
<td>3</td>
<td>1'b0</td>
<td>Reserved</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>17h</td>
<td>7:4</td>
<td>4'b0000</td>
<td>TST_INQ[3:0]. Latched interrupt flag. 1 bit per lane</td>
<td>RU</td>
</tr>
<tr>
<td>3:0</td>
<td>4'b0000</td>
<td>TST_INT[3:0]. Test interrupt flag. 1 bit per lane.</td>
<td>RU</td>
<td></td>
</tr>
<tr>
<td>18h</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[7:0]. BERT error count. Lane 0</td>
<td>RU</td>
</tr>
<tr>
<td>19h</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[11:8]. BERT error count. Lane 0</td>
<td>RU</td>
</tr>
<tr>
<td>1Ah</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[19:12]. BERT error count. Lane 1</td>
<td>RU</td>
</tr>
<tr>
<td>1Bh</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[23:20]. BERT error count. Lane 1</td>
<td>RU</td>
</tr>
<tr>
<td>1Ch</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[31:24]. BERT error count. Lane 2</td>
<td>RU</td>
</tr>
<tr>
<td>1Dh</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[35:32]. BERT error count. Lane 2</td>
<td>RU</td>
</tr>
<tr>
<td>1 Eh</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[19:12]. BERT error count. Lane 3</td>
<td>RU</td>
</tr>
<tr>
<td>1Fh</td>
<td>7:4</td>
<td>1'h0</td>
<td>BERT_CNT[23:20]. BERT error count. Lane 3</td>
<td>RU</td>
</tr>
<tr>
<td>20h</td>
<td>7:4</td>
<td>1'b1</td>
<td>AUX_TX_SR Slew Rate Control for AUX Output</td>
<td>RW</td>
</tr>
<tr>
<td>2:0</td>
<td>3'b010</td>
<td>AUX_SWING; Swing Control for AUX Output</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>000 – 270 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001 – 355 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>010 – 450 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>011 – 535 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 – 625 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>101 – 710 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>110 – 800 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>111 – Not allowed</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
10 Application and Implementation

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

DP159 is designed to accept AC coupled HDMI input signals. The device provides signal conditioning and level shifting functions to drive a compliant HDMI source connector. DP159 can be used as an DP1.2 retimer, follow application note SLLA358 for required additional configuration. In many major PC or gaming platforms APU/GPU can provide AC coupled HDMI 2.0 signals, DP159 is suitable for such platforms.

10.1 Application Information

The DP159 was defined to work in mainly in source applications such as gaming systems, Blu-Ray DVD player, desktop, notebook or VR. The following sections provide design consideration for various types of applications.

10.1.1 Use Case of SNx5DP159

SNx5DP159 can be used on the motherboard and dongle applications. The following use case diagrams show the connection of AUX and DDC between source side and sink side. The control pin pull up and pull down resistors are shown from reference. If a high is needed only use the pull up. If a low is needed only use the pull down. If mid level is to be selected do not use either resistors and leave the pin floating/No connect. The 6.5-Ω Vsadj resistor value shown is explained further in the compliance section, for the RSB package.

The DP159 was defined to work in mainly in source applications such as gaming systems, Blu-Ray DVD player, Desktop, Notebook or VR. The following sections provide design consideration for various types of applications.

图 30 shows the original connection of SNx5DP159 on motherboard through the DDC channel. The DDC DR default is 100-kHz and is capable to adjust to 400-kHz.
### Application Information (接下页)

#### 40-Pin

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN_D2p</td>
</tr>
<tr>
<td>2</td>
<td>OUT_D2p</td>
</tr>
<tr>
<td>3</td>
<td>IN_D2n</td>
</tr>
<tr>
<td>4</td>
<td>OUT_D2n</td>
</tr>
<tr>
<td>5</td>
<td>IN_D1p</td>
</tr>
<tr>
<td>6</td>
<td>OUT_D1p</td>
</tr>
<tr>
<td>7</td>
<td>IN_D1n</td>
</tr>
<tr>
<td>8</td>
<td>OUT_D1n</td>
</tr>
<tr>
<td>9</td>
<td>IN_D0p</td>
</tr>
<tr>
<td>10</td>
<td>OUT_D0p</td>
</tr>
<tr>
<td>11</td>
<td>IN_D0n</td>
</tr>
<tr>
<td>12</td>
<td>OUT_D0n</td>
</tr>
<tr>
<td>13</td>
<td>IN_CLKp</td>
</tr>
<tr>
<td>14</td>
<td>OUT_CLKp</td>
</tr>
<tr>
<td>15</td>
<td>IN_CLKn</td>
</tr>
<tr>
<td>16</td>
<td>OUT_CLKn</td>
</tr>
</tbody>
</table>

#### HDMI/DVI Receptacle

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TMDS_D2p</td>
</tr>
<tr>
<td>2</td>
<td>TMDS_D2n</td>
</tr>
<tr>
<td>3</td>
<td>GND1</td>
</tr>
<tr>
<td>4</td>
<td>TMDS_D2n</td>
</tr>
<tr>
<td>5</td>
<td>TMDS_D2n</td>
</tr>
<tr>
<td>6</td>
<td>GND2</td>
</tr>
<tr>
<td>7</td>
<td>TMDS_D1p</td>
</tr>
<tr>
<td>8</td>
<td>GND3</td>
</tr>
<tr>
<td>9</td>
<td>TMDS_D1n</td>
</tr>
<tr>
<td>10</td>
<td>GND4</td>
</tr>
<tr>
<td>11</td>
<td>TMDS_D0p</td>
</tr>
<tr>
<td>12</td>
<td>GND5</td>
</tr>
<tr>
<td>13</td>
<td>TMDS_D0n</td>
</tr>
<tr>
<td>14</td>
<td>GND6</td>
</tr>
<tr>
<td>15</td>
<td>TMDS_CLKp</td>
</tr>
<tr>
<td>16</td>
<td>TMDS_CLKn</td>
</tr>
<tr>
<td>17</td>
<td>CEC</td>
</tr>
<tr>
<td>18</td>
<td>CASE_GND1</td>
</tr>
<tr>
<td>19</td>
<td>CASE_GND2</td>
</tr>
<tr>
<td>20</td>
<td>CASE_GND3</td>
</tr>
<tr>
<td>21</td>
<td>CASE_GND4</td>
</tr>
</tbody>
</table>

---

图 30. Implementation for Motherboard 1
Application Information (接下页)

图 31 shows the connection for both DDC and AUX GPU connections with the SNx5DP159RGZ. Only one can be implemented at a time. Only the RGZ package supports the I²C-over-AUX implementation. The control pin pull up and pull down resistors are shown for reference. If a high is needed only use the pull up. If a low is needed only use the pull down. If mid level is to be selected do not use either resistors and leave the pin floating/No connect.

Note 1: For applications where the GPU or Sink does not support clock stretching the DDC lines from the GPU/DP TX should bypass the SCL_SRC and SDA_SRC but still connect to the SCL_SNK and SDA_SNK pins on the DP159. The SCL_SRC and SDA_SRC pins must be pulled to ground. Note that if the GPU/DP TX cannot support the 5V DDC lines from the connector, a level shifter is needed to step down the 5V signals to the voltage level the GPU/DP TX can support.

图 31. Implementation for Motherboard 2
Application Information (接下页)

图 32 shows the SNx5DP159 in the dongle application. It uses the unified structure on DisplayPort connector. SNx5DP159 has to identify if the signal comes from DDC or from AUX in i²C-over-AUX format. Due to the AUX channel needed, use only the RGZ package for this application.

### 10.1.2 DDC Pullup Resistors

This section is for information only and subject to change depending upon system implementation.
Application Information (接下页)

The pullup resistor value is determined by two requirements:

A. The maximum sink current of the I²C buffer:

The maximum sink current is 3-mA or slightly higher for an I²C driver supporting standard-mode I²C[4] operation.

\[ R_{up(min)} = \frac{V_{CC}}{I_{sink}} \]  

(1)

B. The maximum transition time on the bus:

The maximum transition time, T, of an I²C bus is set by an RC time constant, where R is the pullup resistor value, and C is the total load capacitance. The parameter, k, can be calculated from 公式 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. 表 11 summarizes the possible values of k under different threshold combinations.

\[ T = k \times RC \]  

(2)

\[ V(t) = V_{CC} \times \left(1 - e^{-\frac{t}{RC}}\right) \]  

(3)

### 表 11. Value k Upon Different Input Threshold Voltages

<table>
<thead>
<tr>
<th>Vth–</th>
<th>Vth+</th>
<th>0.7 VCC</th>
<th>0.65 VCC</th>
<th>0.6 VCC</th>
<th>0.55 VCC</th>
<th>0.5 VCC</th>
<th>0.45 VCC</th>
<th>0.4 VCC</th>
<th>0.35 VCC</th>
<th>0.3 VCC</th>
</tr>
</thead>
</table>
| 0.1 VCC | 1.0986 | 0.9445  | 0.8109  | 0.6931  | 0.5878  | 0.4925  | 0.4055  | 0.3254  | 0.2513  
| 0.15 VCC | 1.0415 | 0.8873  | 0.7538  | 0.6360  | 0.5306  | 0.4353  | 0.3483  | 0.2683  | 0.1942  
| 0.2 VCC | 0.9808 | 0.8267  | 0.6931  | 0.5754  | 0.4700  | 0.3747  | 0.2877  | 0.2076  | 0.1335  
| 0.25 VCC | 0.9163 | 0.7621  | 0.6286  | 0.5108  | 0.4055  | 0.3102  | 0.2231  | 0.1431  | 0.0690  
| 0.3 VCC | 0.8473 | 0.6931  | 0.5596  | 0.4418  | 0.3365  | 0.2412  | 0.1542  | 0.0741  |

From 公式 1, \( R_{up(min)} = \frac{5.5-V}{3-mA} = 1.83-k\Omega \) to operate the bus under a 5-V pullup voltage and provide less than 3-mA when the I²C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, \( R_{up(min)} \) can be as low as 1.375-kΩ.

If DDC is working at a standard mode of 100-Kbps, the maximum transition time, T, is fixed, 1 μs, and using the k values from 表 11, the recommended maximum total resistance of the pullup resistors on an I²C bus can be calculated for different system setups. If DDC is working in a fast mode of 400-kbps, the transition time should be set at 300 ns, according to I²C[4] specification.

To support the maximum load capacitance specified in the HDMI specification, \( C_{cable(max)} = 700-pF \), \( C_{source} = 50-pF \), \( C_i = 50-pF \), and \( R_{(max)} \) can be calculated as shown in 表 12.

### 表 12. Pullup Resistor Upon Different Threshold Voltages and 800-pF Loads

<table>
<thead>
<tr>
<th>Vth–</th>
<th>0.7 VCC</th>
<th>0.65 VCC</th>
<th>0.6 VCC</th>
<th>0.55 VCC</th>
<th>0.5 VCC</th>
<th>0.45 VCC</th>
<th>0.4 VCC</th>
<th>0.35 VCC</th>
<th>0.3 VCC</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 VCC</td>
<td>1.14</td>
<td>1.32</td>
<td>1.54</td>
<td>1.8</td>
<td>2.13</td>
<td>2.54</td>
<td>3.08</td>
<td>3.84</td>
<td>4.97</td>
<td>kΩ</td>
</tr>
<tr>
<td>0.15 VCC</td>
<td>1.2</td>
<td>1.41</td>
<td>1.66</td>
<td>1.97</td>
<td>2.36</td>
<td>2.87</td>
<td>3.59</td>
<td>4.66</td>
<td>6.44</td>
<td>kΩ</td>
</tr>
<tr>
<td>0.2 VCC</td>
<td>1.27</td>
<td>1.51</td>
<td>1.8</td>
<td>2.17</td>
<td>2.66</td>
<td>3.34</td>
<td>4.35</td>
<td>6.02</td>
<td>9.36</td>
<td>kΩ</td>
</tr>
<tr>
<td>0.25 VCC</td>
<td>1.36</td>
<td>1.64</td>
<td>1.99</td>
<td>2.45</td>
<td>3.08</td>
<td>4.03</td>
<td>5.6</td>
<td>8.74</td>
<td>18.12</td>
<td>kΩ</td>
</tr>
<tr>
<td>0.3 VCC</td>
<td>1.48</td>
<td>1.8</td>
<td>2.23</td>
<td>2.83</td>
<td>3.72</td>
<td>5.18</td>
<td>8.11</td>
<td>16.87</td>
<td>—</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

To accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I²C bus.
10.2 Typical Application

10.2.1 Design Requirements

The SNx5DP159 can be designed into many types of applications. All applications have certain requirements for the system to work properly. Two voltage rails are required to support the lowest possible power consumption. The OE pin must have a 0.1-µF capacitor to ground. This pin can be driven by a processor but the pin needs to change states after voltage rails have stabilized. Configure the device by using I²C. Pin strapping is provided as I²C is not available in all cases. Because sources may have different naming conventions, confirm the link between the source and the SNx5DP159 is correctly mapped. A swap function is provided for the input pins in case signaling is reversed between the source and the device. For the control pins the values provided below are when they are being controlled by a micro-controller. If this is not the case then using the 65-kΩ for a pull up for high, pulled down for low, and left floating for mid level.
表 13. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>3.3 V</td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>1.1 V</td>
</tr>
<tr>
<td>Main link input voltage</td>
<td>( V_{ID} = 75 \text{ mVpp to } 1.2 \text{ Vpp} )</td>
</tr>
<tr>
<td>Control pin Low</td>
<td>65-k( \Omega ) pulled to GND</td>
</tr>
<tr>
<td>Control pin Mid</td>
<td>No Connect</td>
</tr>
<tr>
<td>Control pin High</td>
<td>65-k( \Omega ) pulled to 3.3-V</td>
</tr>
<tr>
<td>Vsadj resistor</td>
<td>7.06-k( \Omega )</td>
</tr>
<tr>
<td>Main link AC decoupling capacitor</td>
<td>75 to 200 nF, recommend 100 nF</td>
</tr>
</tbody>
</table>

10.2.2 Detailed Design Procedure

The SNx5DP159 is a signal conditioner that provides AC coupling to DC coupling level shifting, to support Dual Mode DisplayPort-capable GPUs or GPUs with AC-coupled drive capability to support HDMI or DVI connectors and compliance. Signal conditioning is accomplished using receive equalization, retiming, and output driver configurability. The transmitter drives 2 to 3 inches of board trace and connector.

Designing in the SNx5DP159 requires the following:

- Determine the loss profile between the GPU and the HDMI/DVI connector.
- Based upon the loss profile and signal swing, determine the optimal location for the SNx5DP159, to pass electrical compliance.
- Use the typical application drawings in Use Case of SNx5DP159 for information on using the AC coupling capacitors and control pin resistors.
- The DP159 has a receiver adaptive equalizer by default but can also be configured for fixed value equalization using the \( EQ\_SEL \) control pin.
- Set the \( V_{OD} \), pre-emphasis, termination, and edge rate levels to support compliance by using the appropriate Vsadj resistor value and by setting the \( PRE\_SEL \), SLEW\_CTL, and TX\_TERM\_CTL control pins.
- Adding pre-emphasis will improve performance on bandwidth limited channels and make steeper transitions. \( V_{OD} \) can be increased to compensate for DC losses and have a sheerer slope. SLEW\_CTL handle transition inclination. Making the transition sharper will improve skew performance.
- The thermal pad must be connected to ground.
- See the schematics in Application Information on recommended decouple capacitors from VCC pins to ground.

10.2.3 Application Curve

图 34. 5.94 Gbps Compliance Eye Mask
## 10.3 System Example

### 10.3.1 Compliance Testing

Compliance testing is very system design specific. Properly designing the system and configuring the DP159 can help pass transmitter compliance for the system. The following information is the starting point to help prepare for compliance test. As each system is different there are many features in the DP159 to help tune the circuit. These include $V_{OD}$ adjust by changing the $V_{Sadj}$ resistor value or using I$^2$C. Other knobs to turn are pre/de-emphasis and slew rate control. Passing both HDMI2.0 and HDMI1.4b compliance is easier to accomplish when using I$^2$C as this provides more fine tuning capability.

#### For the SNx5DP159RGZ:

**Pin Strapping**
- HDMI2.0 & HDMI1.4b
  - $V_{Sadj}$ Resistor = 7.06-kΩ
  - PRE_SEL = NC for 0-dB
  - TX_TERM_CTL = NC for Auto Select
  - SLEW_CTL = NC

**I$^2$C Control**
- HDMI2.0 & HDMI1.4b
  - $V_{Sadj}$ Resistor = 7.06 kΩ
  - PRE_SEL = Reg0Ch[1:0] = 00 (labeled HDMI_TWPST)
  - TX_TERM_CTL =
    - Reg0Bh[4:3] = 00 → No term; HDMI1.4b < 2Gbps (This may be best value for all HDMI1.4b)
    - Reg0Bh[4:3] = 01 → 150 to 300 Ω; HDMI1.4b > 2Gbps
    - Reg0Bh[4:3] = 11 → 75 to 150 Ω; HDMI2.0
  - SLEW_CTL = Reg0Bh[7:6] = 10

#### For the SNx5DP159RSB:

**Pin Strapping**
- HDMI2.0 and HDMI1.4b
  - $V_{Sadj}$ Resistor = 6.5 kΩ
  - PRE_SEL = L for –2 dB
  - TX_TERM_CTL = NC for Auto Select
  - SLEW_CTL = NC

**I$^2$C**
- HDMI2.0
  - $V_{Sadj}$ Resistor = 6.5 kΩ
  - PRE_SEL = Reg0Ch[1:0] = 01 (labeled HDMI_TWPST)
  - TX_TERM_CTL = Reg0Bh[4:3] = 11
  - SLEW_CTL = Reg0Bh[7:6] = 10

**HDMI1.4b**
- $V_{Sadj}$ Resistor = 6.5 kΩ
- VSWING_DATA & VSWING_CLK to -7% = Reg0Ch[7:2] = 111111
- PRE_SEL = Reg0Ch[1:0] = 00: (Labeled HDMI_TWPST)
  - TX_TERM_CTL: Reg0Bh[4:3] =
    - <2 Gbps = 00 for no termination (This may be best value for all HDMI1.4b)
    - >2 Gbps and < 3.4 Gbps = 01 for 150 to 300 Ω
  - SLEW_CTL = Reg0Bh[7:6] = 10
11 Power Supply Recommendations

11.1 Power Management
To minimize the power consumption of customer application, SNx5DP159 uses dual power supply. \( V_{CC} \) is 3.3-V with 10% range to support the I/O voltage. The \( V_{DD} \) is 1.00-V to 1.27-V range to supply the internal digital control circuit. \( V \) operates in two different working states. See Table 14 for conditions for each mode. When OE is deasserted and then reasserted the device will rest to its default configurations. If different configurations were programmed using \( I^2C \) then the device will have to be reprogrammed.

- **Power-down mode:**
  - \( OE = \) Low puts the device into its lowest power state by shutting down all function blocks
  - When OE is re-asserted the transitions from \( L \rightarrow H \) will create a reset and if the device is programmed through \( I^2C \) it will have to be reprogrammed.
  - \( OE = \) High, \( HPD_{SNK} = \) Low
  - Writing a 1 to register 09h[3]

- **Normal operation:** Working in redriver or retimer
- **When HPD asserts,** the device CDR and output will enable based on the signal detector circuit result
- **\( HPD_{SRC} = HPD_{SNK} \)** in all conditions. The HPD channel operational when \( V_{CC} \) over 3-V.

注
When the SNx5DP159 is put into a power down state using the OE pin the \( I^2C \) registers are cleared. The TMDS_CLOCK_RATIO_STATUS bit will be cleared in all power down states. If cleared and HDMI2.0 resolutions are to be supported, the SNx5DP159 expects the source to write a 1 to this bit location. If this does not happen the PLL will not be set properly and no video may be evident.

<table>
<thead>
<tr>
<th>INPUTS (1)</th>
<th>STATUS</th>
<th>MODE</th>
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<tbody>
<tr>
<td>HPD_SNK</td>
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<td>HPD_SRC</td>
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<tr>
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<tr>
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<tr>
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<td>H</td>
<td>Redriver</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Retimer</td>
</tr>
</tbody>
</table>

(1) \( L = \) LOW, \( H = \) HIGH

TMDS output termination control impacts the operating power.

<table>
<thead>
<tr>
<th>INPUTS (1)</th>
<th>STATUS</th>
<th>MODE</th>
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<tr>
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</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Retimer</td>
</tr>
</tbody>
</table>

(1) \( L = \) LOW, \( H = \) HIGH
TMDS output termination control impacts the operating power.

12 Layout

12.1 Layout Guidelines

TI recommends to use at a minimum a four layer stack up to accomplish a low-EMI PCB design. TI recommends six layers because the SNx5DP159 is a two voltage rail device.

- Routing the high-speed input DisplayPort traces and TMDS output traces on the top layer avoids the use of vias (and their discontinuities) and allows for clean interconnects from the HDMI connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.
- The control pin pullup and pulldown resistors are shown in application section for reference. If a high is needed only use the pull up. If a low is needed only use the pull down. If mid level is to be selected do not use either resistors and leave the pin floating/No connect.

![Diagram of recommended 4- or 6-Layer Stack for a Receiver PCB Design](image-url)

图 35. Recommended 4- or 6-Layer Stack for a Receiver PCB Design
12.2 Layout Examples

图 36. Layout Example for the DP159RSB
12.3 Thermal Considerations

On a high-K board: TI recommends to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the SNx5DP159 device can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

On a low-K board: For the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\text{JA}} = 100.84\, ^\circ\text{C/W}$ allowing 545-mW power dissipation at 70°C ambient temperature.

A general PCB design guide for PowerPAD packages is provided in *PowerPAD Thermally Enhanced Package, SLMA002.*
13 器件和文档支持

13.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 16. 相关链接

<table>
<thead>
<tr>
<th>器件</th>
<th>产品文件夹</th>
<th>样片与购买</th>
<th>技术文档</th>
<th>工具与软件</th>
<th>支持和社区</th>
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<tr>
<td>SN65DP159</td>
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13.2 文档支持

13.2.1 相关文档

本节标识的文档均在本数据表中引用。为简化文本，数据表中的大多数参考文献均使用方括号 [文档标签] 标识的文档，而不使用完整的文档标题。

(1) [VESA DisplayPort] 双模标准版本 1.1, 2013 年 2 月 8 日
(2) [HDMI1.4b] 高清多媒体接口规范版本 1.4b, 2011 年 10 月
(3) [HDMI2.0] 高清多媒体接口规范版本 2.0a, 2015 年 3 月
(4) [I²C] I²C 总线规范版本 2.1, 2000 年 1 月
(5) [HDMI1.4b CTS] 高清多媒体接口 CTS 版本 1.4b, 2011 年 10 月
(6) [HDMI2.0 CTS] 高清多媒体接口 CTS 版本 2.0k, 2015 年 6 月

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区**

TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持**

TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.

Blu-Ray is a trademark of Blu-ray Disc Accociation.

13.6 静电放电警告

ESD 可能会造成集成电路的永久损坏。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守本手册的预防措施和安装程序，可能会损坏集成电路。

ESD 的损坏可能导致微小的性能降级，甚至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是根据器件的最新数据和数据手册提供的。如需获取产品说明的浏览器版本，请查看左侧的导航栏。
**IMPORTANT NOTICE**

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Copyright © 2018 德州仪器半导体技术（上海）有限公司
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### Reel Dimensions

![Reel Dimensions Diagram]

**Reel Diameter**

### TAPE Dimensions

![Tape Dimensions Diagram]

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### Quadrant Assignments for Pin 1 Orientation in Tape

![Quadrant Assignments Diagram]

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
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<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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### TAPE AND REEL BOX DIMENSIONS

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</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

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NOTES: (continued)

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