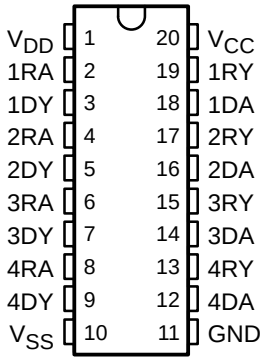
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Very Low Power Consumption . . . 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**

SN65C1154 . . . N PACKAGE
SN75C1154 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

The SN65C1164 and SN75C1154 are low-power BiMOS devices containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices are designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP (N)	Tube of 20	SN65C1154N	SN65C1154N
0°C to 70°C	PDIP (N)	Tube of 20	SN75C1154N	SN75C1154N
	SOIC (DW)	Tube of 25	SN75C1154DW	SN75C1154
		Reel of 2500	SN75C1154DWR	
	SOP (NS)	Reel of 2000	SN75C1154NSR	SN75C1154

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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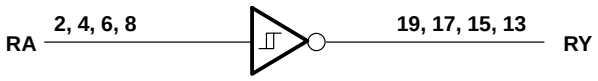
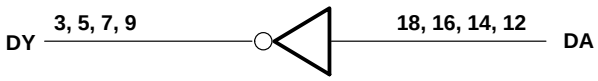
logic diagram (positive logic)

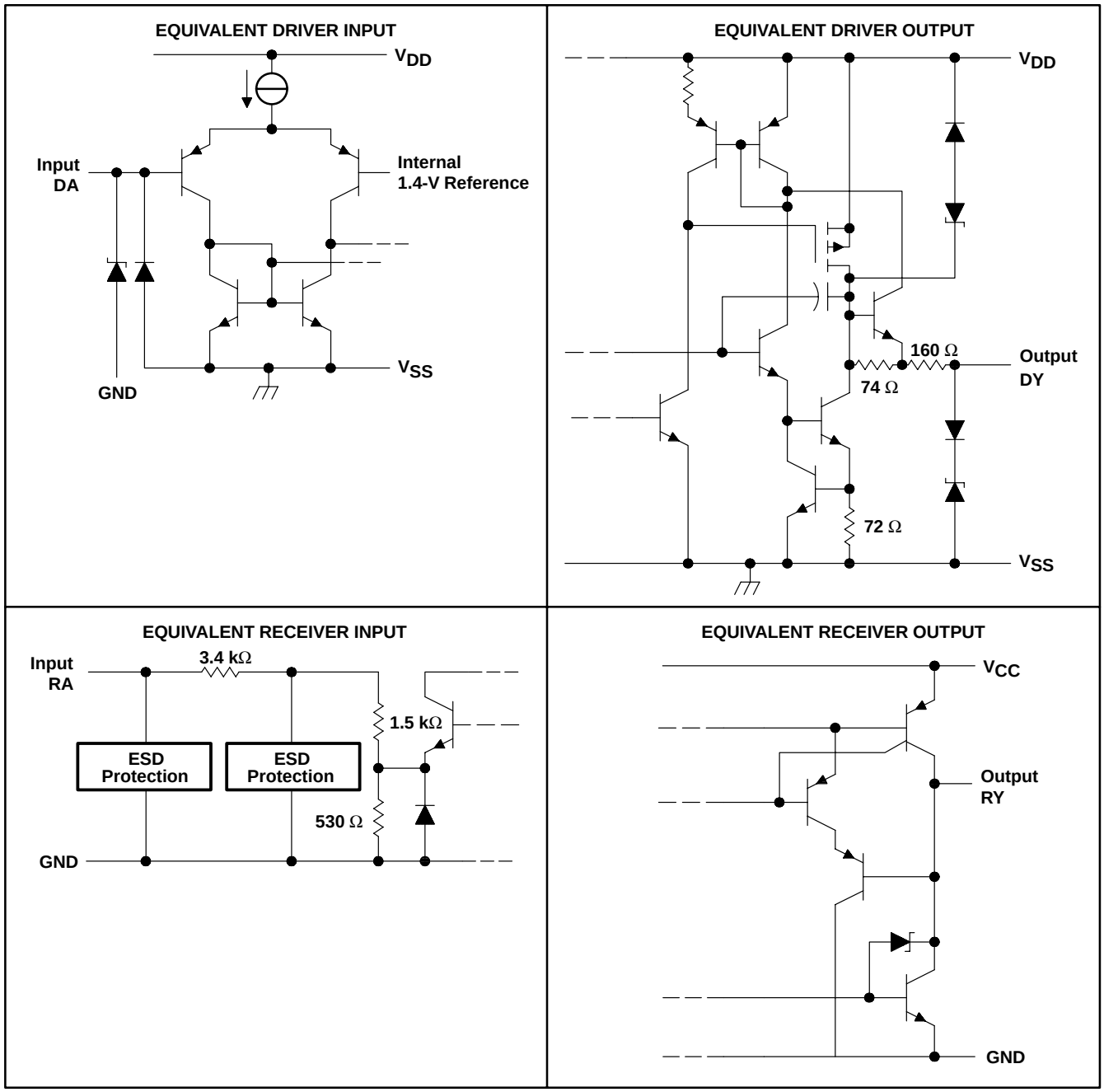
Typical of Each Receiver



Typical of Each Driver



schematics of inputs and outputs



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{DD} (see Note 1) . . . . . 15 V
V_{SS} . . . . . –15 V
V_{CC} . . . . . 7 V
Input voltage range, V_I: Driver . . . . . V_{SS} to V_{DD}
Receiver . . . . . –30 V to 30 V
Output voltage range, V_O: Driver . . . . . (V_{SS} – 6 V) to (V_{DD} + 6 V)
Receiver . . . . . –0.3 V to (V_{CC} + 0.3 V)
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage s are with respect to the network GND terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	12	15	V
V_{SS}	Supply voltage		–4.5	–12	–15	V
V_{CC}	Supply voltage		4.5	5	6	V
V_I	Input voltage	Driver	V_{SS} + 2		V_{DD}	V
		Receiver			±25	
V_{IH}	High-level input voltage	Driver	2			V
V_{IL}	Low-level input voltage	Driver			0.8	V
I_{OH}	High-level output current	Receiver			–1	mA
I_{OL}	High-level output current	Receiver			3.2	mA
T_A	Operating free-air temperature	SN65C1154	–40		85	°C
		SN75C1154	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = –5 V	4	4.5		V
				V_{DD} = 12 V, V_{SS} = –12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 4)	V_{IH} = 2 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = –5 V		–4.4	–4	V
				V_{DD} = 12 V, V_{SS} = –12 V		–10.7	–10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2					1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2					–1	µA
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	–7.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{DD},	See Figure 1	7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = –5 V		115	250	µA
				V_{DD} = 12 V, V_{SS} = –12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = –5 V		–115	–250	µA
				V_{DD} = 12 V, V_{SS} = –12 V		–115	–250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,	V_O = –2 V to 2 V,	See Note 5	300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at one time.
NOTES: 4. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
5. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 to 7 kΩ,	CL = 15 pF		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output§	R_L = 3 to 7 kΩ,	CL = 15 pF		2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output¶	R_L = 3 to 7 kΩ,	CL = 15 pF	0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output¶	R_L = 3 to 7 kΩ,	CL = 15 pF	0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 to 7 kΩ,	C_L = 2500 pF		1	2	µs
t_{THL}	Transition time, high- to low-level output#	R_L = 3 to 7 kΩ,	C_L = 2500 pF		1	2	µs
SR	Output slew rate	R_L = 3 to 7 kΩ,	CL = 15 pF	4	10	30	V/µs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate control and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform
# Measured between 3 V and –3 V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5			1.7	2.1	2.55	V
$V_{IT–}$	Negative-going input threshold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)				600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = –20 μA, See Figure 5 and Note 6			3.5			V
		V_I = 0.75 V, I_{OH} = –1 mA, See Figure 5	V_{CC} = 4.5 V		2.8	4.4		
			V_{CC} = 5 V		3.8	4.9		
			V_{CC} = 5.5 V		4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5				0.17	0.4	V
I_{IH}	High-level input current	V_I = 25 V			3.6	4.6	8.3	mA
		V_I = 3 V			0.43	0.55	1	
I_{IL}	Low-level input current	V_I = –25 V			–3.6	–5	–8.3	mA
		V_I = –3 V			–0.43	–0.55	–1	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4				–8	–15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4				13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V,	V_{SS} = –5 V		400	600	μA
			V_{DD} = 12 V,	V_{SS} = –12 V		400	600	

† All typical values are at T_A = 25°C.

NOTE 6: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ± 10%, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		3	4	μs
t_{TLH}	Transition time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		300	450	ns
t_{THL}	Transition time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ,	See Figure 6		100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise‡	C_L = 50 pF,	R_L = 5 kΩ		1		4	μs

‡ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

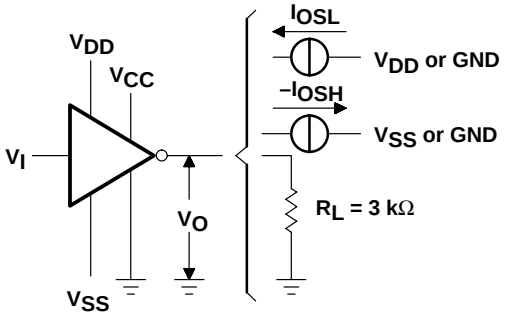


Figure 1. Driver Test Circuit (V_{OH}, V_{OL}, I_{OSL}, I_{OSH})

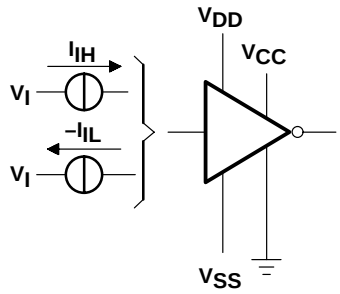
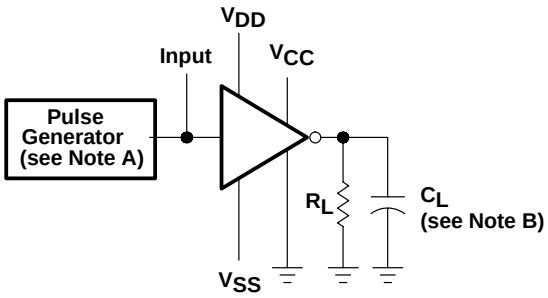
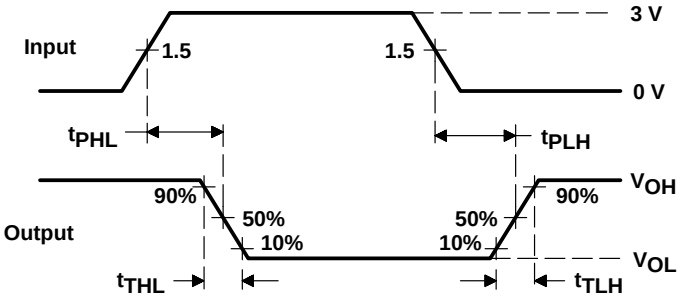


Figure 2. Driver Test Circuit (I_{IL}, I_{IH})



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

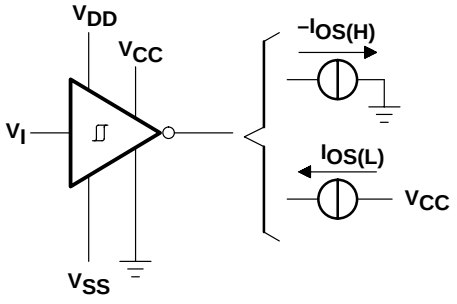


Figure 4. Receiver Test Circuit (I_{OSH}, I_{OSL})

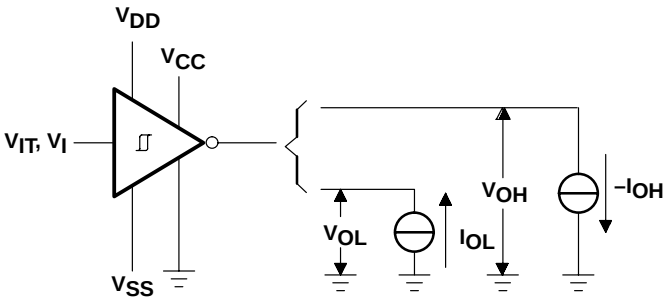
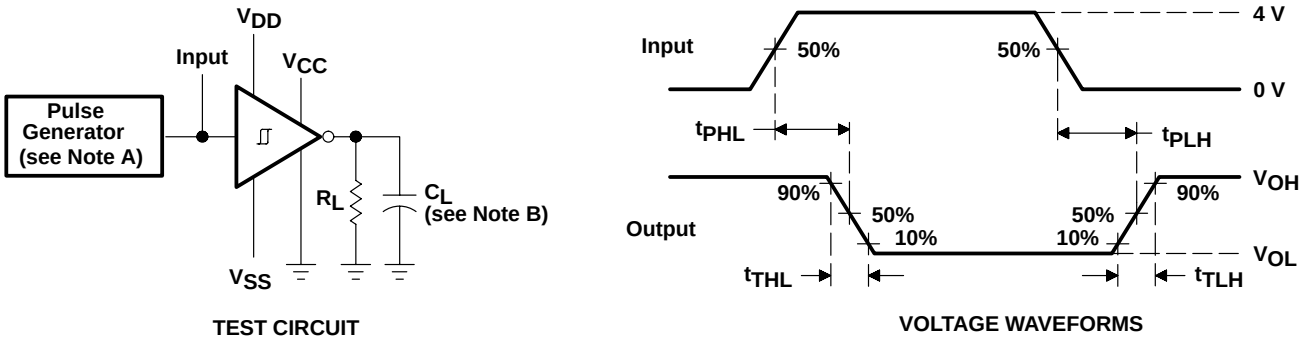


Figure 5. Receiver Test Circuit (V_{IT}, V_{OL}, V_{OH})

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C1154N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65C1154N
SN65C1154N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65C1154N
SN75C1154DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C1154
SN75C1154DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C1154
SN75C1154DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C1154
SN75C1154DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C1154
SN75C1154N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1154N
SN75C1154N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75C1154N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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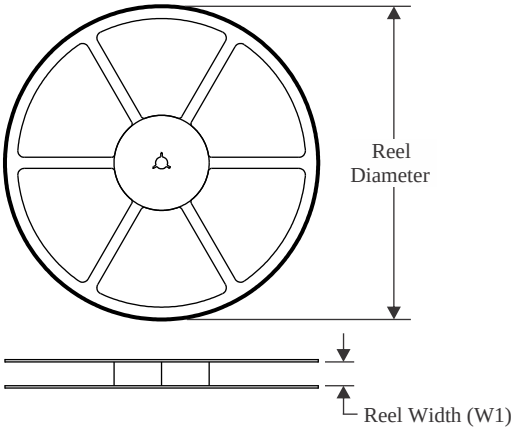
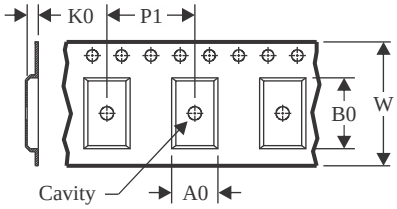
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

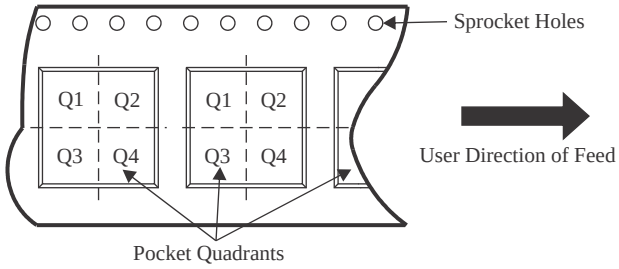


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

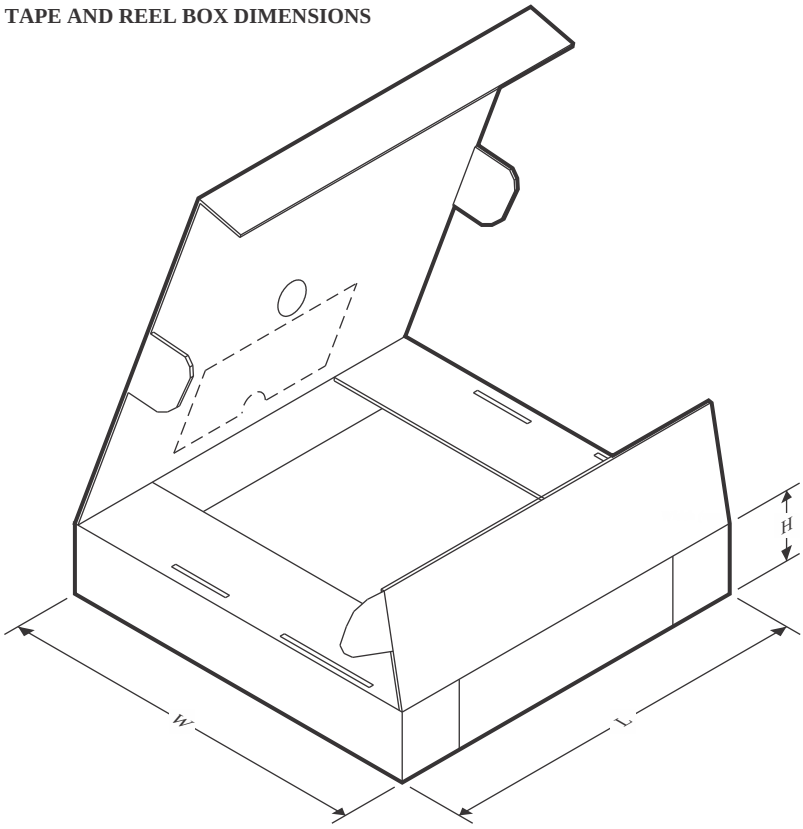
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C1154DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

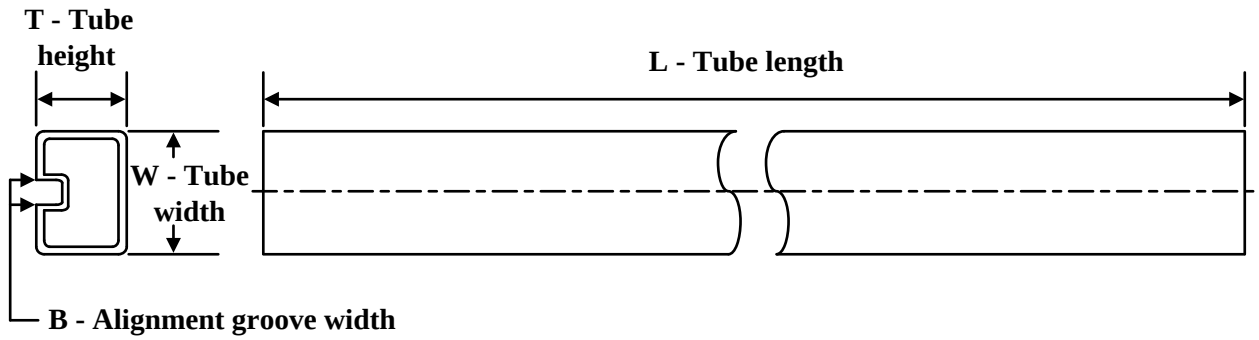
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C1154DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



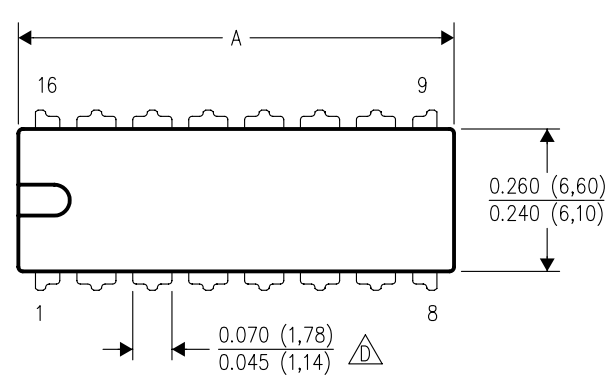
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65C1154N	N	PDIP	20	20	506	13.97	11230	4.32
SN65C1154N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN75C1154DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75C1154DW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75C1154N	N	PDIP	20	20	506	13.97	11230	4.32
SN75C1154N.A	N	PDIP	20	20	506	13.97	11230	4.32

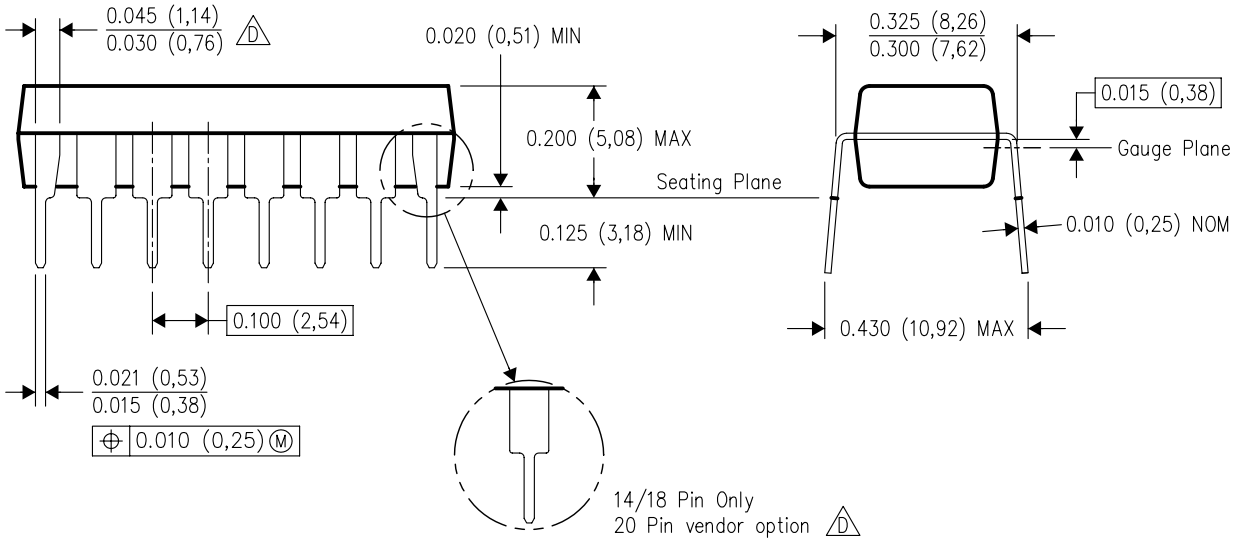
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

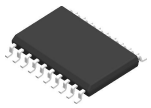


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

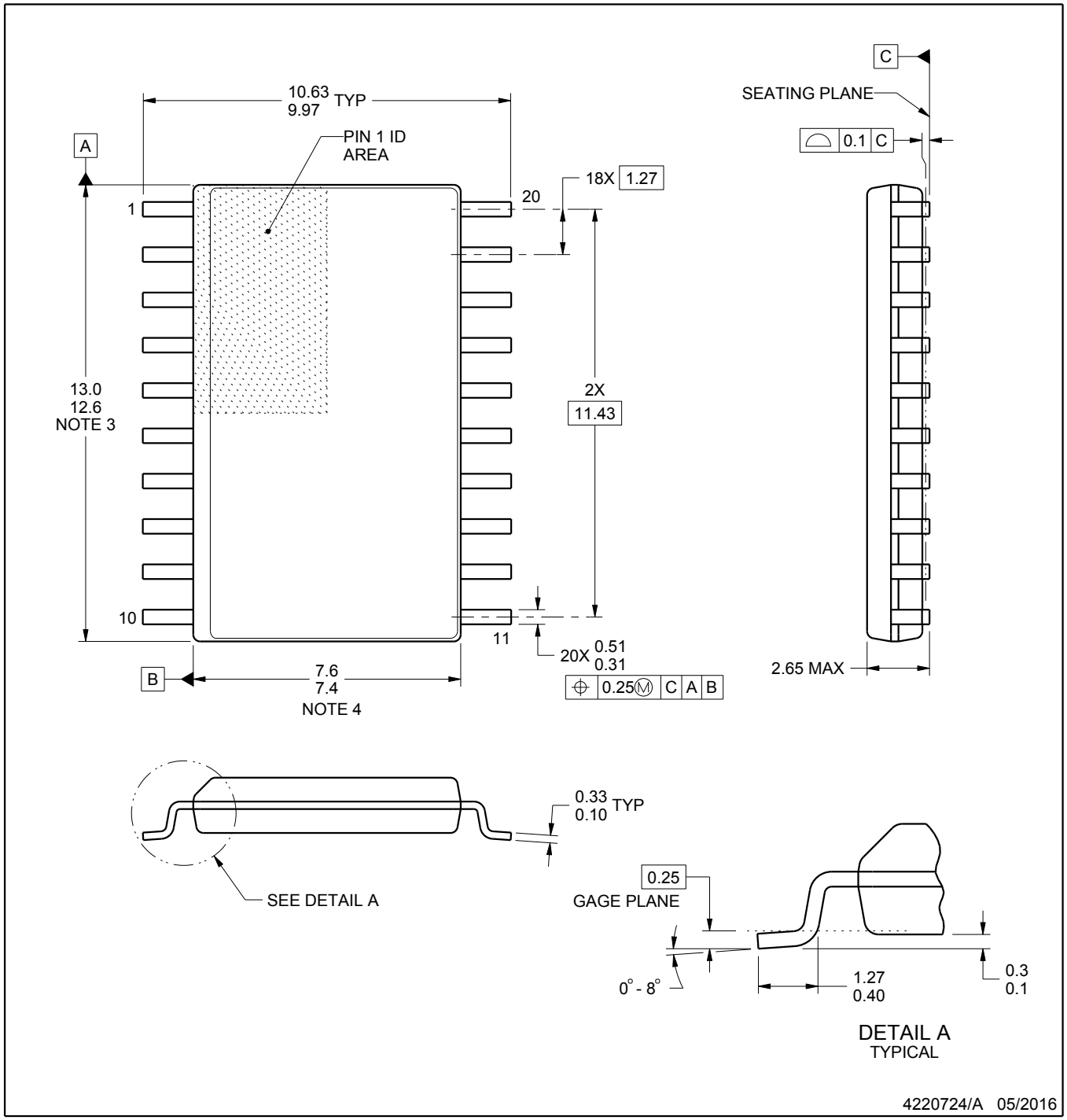


PACKAGE OUTLINE

DW0020A

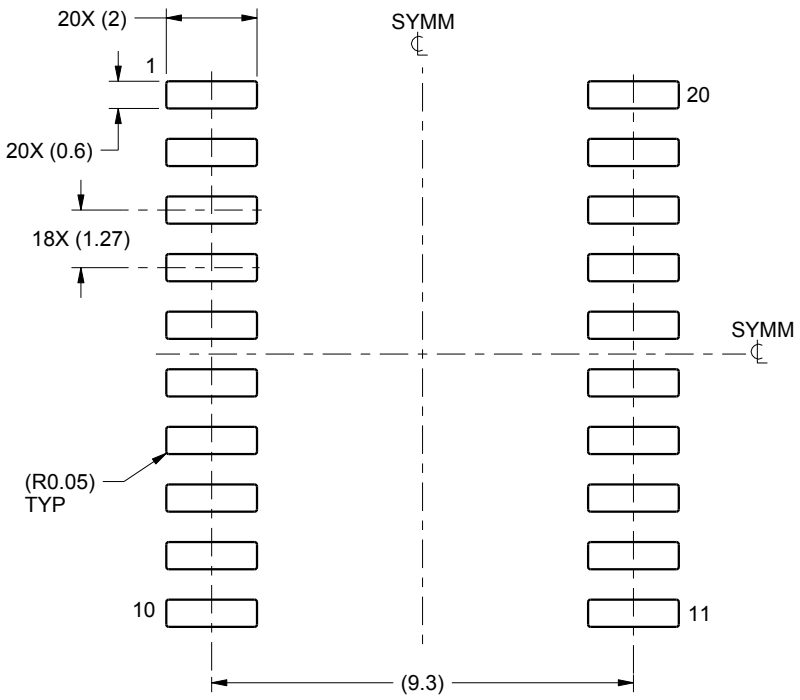
SOIC - 2.65 mm max height

SOIC

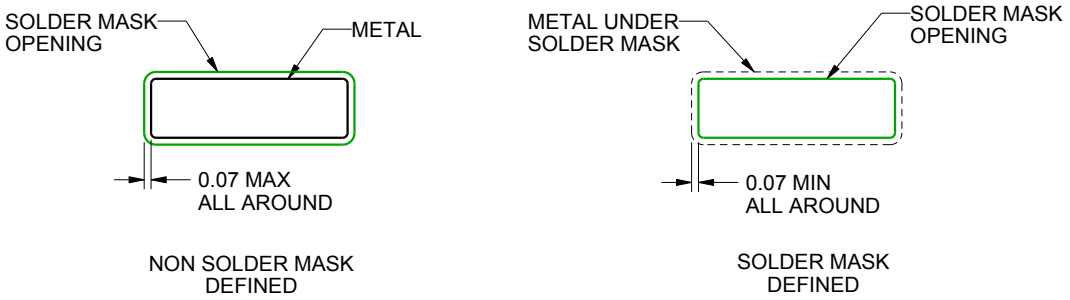


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

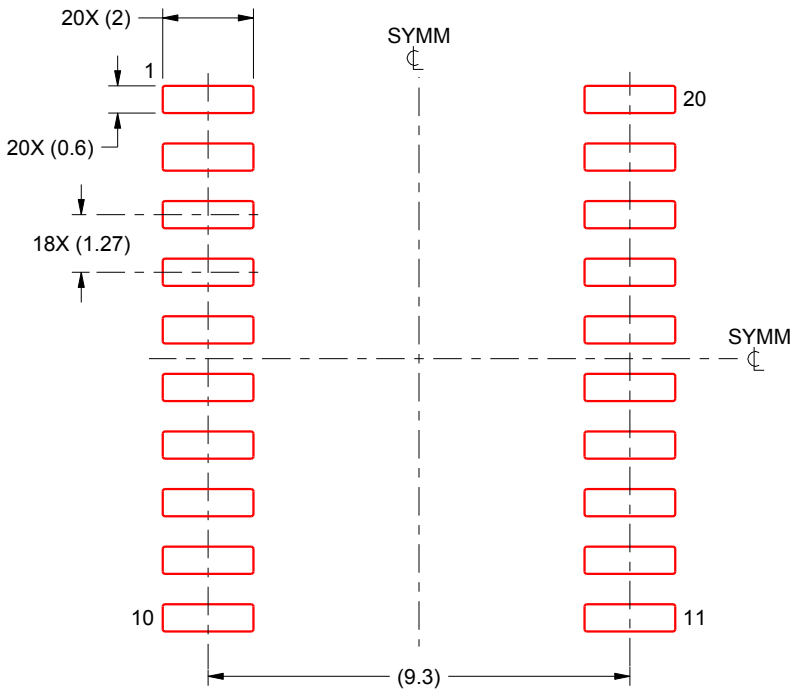


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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