SN75ALS1177、SN75ALS1178 双路差分驱动器和接收器

1 特性

- 达到或超出 TIA/EIA-422-B 和 TIA/EIA-485-A 标准的要求
- 适用于嘈杂环境中长总线上的多点总线传输
- 低电源电流要求（最高 50mA）
- 驱动器正负电流限制
- 驱动器共模输出电压范围为 -7V 至 12V
- 热关断保护驱动器三态输出高电平有效使能
- 接收器共模输入电压范围为 -12V 至 12V
- 接收器输入灵敏度：±200mV
- 接收器迟滞：50mV（典型值）
- 接收器高输入阻抗：12kΩ（最小值）
- 接收器三态输出低电平有效使能（仅限 SN75ALS1177）
- 由 5V 单电源供电

2 应用

- 电机驱动器
- 工厂自动化
- 楼宇自动化

3 说明

SN75ALS1177 和 SN75ALS1178 双路差分驱动器和接收器是专为多点总线传输线路上的双向数据通信而设计的集成电路。这些器件专为平衡传输线路而设计，符合 TIA/EIA-422-B 和 TIA/EIA-485-A 标准。

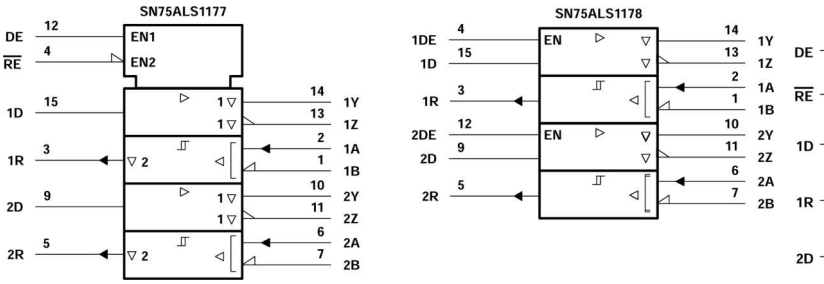
SN75ALS1177 整合了双三态差分线路驱动器和双三态差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起，用作方向控制。每个 SN75ALS1178 驱动器均具有单独的高电平有效使能端。失效防护设计可确保在接收器输入处于开路状态时，接收器输出始终为高电平。

SN75ALS1177 和 SN75ALS1178 的额定工作温度范围是 –0°C 至 70°C。

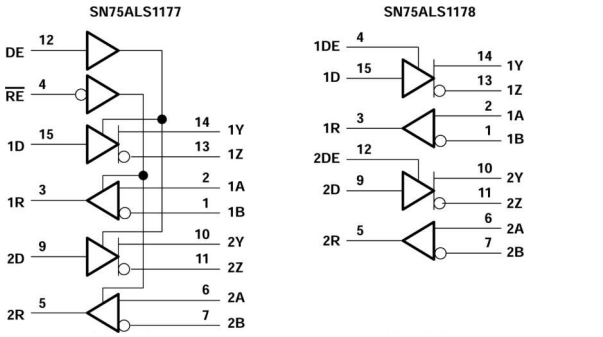
封装选项

器件型号	封装(1)	封装尺寸(2)
SN75ALS1177 SN75ALS1178	SOP（NS，16）	10.2mm × 7.8mm
	PDIP（N，16）	19.3mm x 9.4mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图（正逻辑）

† 这些符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

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4 Pin Configuration and Functions

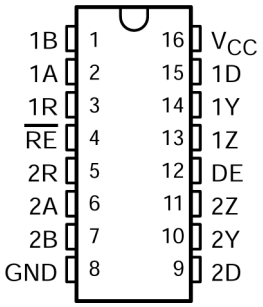

图 4-1. SN75ALS1177: N or NS Package (Top View)

PIN			TYPE	DESCRIPTION
NAME	SO	TSSOP		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
DE	12	12	I	Driver enable (active high)
GND	8	8	—	Device ground pin
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
$\overline{RE}$	4	4	I	Receiver enable pin (active low)
V_{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (inverting) driver output 1
2Z	11	11	O	RS-422 differential (inverting) driver output 2

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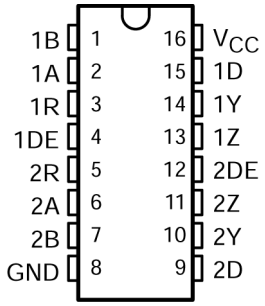

图 4-2. SN75ALS1178: N or NS Package (Top View)

PINT			TYPE	DESCRIPTION
NAME	SO	TSSOP		
1A	2	2	I	RS422 differential input (non-inverting) to receiver 1
2A	6	6	I	RS422 differential input (non-inverting) to receiver 2
1B	1	1	I	RS422 differential input (inverting) to receiver 1
2B	7	7	I	RS422 differential input (inverting) to receiver 2
1D	15	15	I	Logic data input to RS422 driver 1
2D	9	9	I	Logic data input to RS422 driver 2
1DE	4	4	I	Driver 1 enable (active high)
2DE	12	12	I	Driver 2 enable (active high)
GND	8	8	—	Device ground
1R	3	3	O	Logic data output of RS422 receiver 1
2R	5	5	O	Logic data output of RS422 receiver 2
V_{CC}	16	16	—	Power supply
1Y	14	14	O	RS-422 differential (non-inverting) driver output 1
2Y	10	10	O	RS-422 differential (non-inverting) driver output 2
1Z	13	13	O	RS-422 differential (non-inverting) driver output 1
2Z	11	11	O	RS-422 differential (non-inverting) driver output 2

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))		7	V
V_I	Input voltage, (DE, $\overline{RE}$, and D inputs)		7	V
V_O	Output voltage range, drivers	–9	14	V
	Input voltage range, receiver	–14	14	V
	Receiver differential-input voltage range, (see (3))	–14	14	V
	Receiver low-level output current		50	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
(3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{ID}	Differential input voltage	Receiver			±12	V
V_{OC}	Common-mode output voltage	Driver	–7(1)		12	V
V_{IC}	Common-mode input voltage	Receiver			±12	V
V_{IH}	High-level input voltage	DE, $\overline{RE}$, D	2			V
V_{IL}	Low-level input voltage	DE, $\overline{RE}$, D			0.8	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low - level out output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

5.3 Thermal Information

THERMAL METRIC(1)		PDIP (N)	SO (NS)	UNIT
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see (2))	60.6	88.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.1	46.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.6	50.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.5	13.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	40.3	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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5.4 Driver Section

5.4.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA					-1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = - 33mA		3.3		V
V_{OL}	Low-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OL} = 33mA		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5V,	R_L = 100 Ω,	See 图 6-1	$1/2V_{OD1}$ or 2[2]			V
		R_L = 54 Ω,	See 图 6-1		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 4			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 5)	R_L = 54 Ω or 100 Ω,		See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,		See 图 6-1	-1[3]		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 5)	R_L = 54 Ω or 100 Ω,		See 图 6-1			±0.2	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0,	V_O = -7V to 12V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = -7V to 12V					±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7V					100	μA
I_{IL}	Low-level input current	V_{IL} = 0.4V					-100	μA
I_{OS}	Short-circuit output current	V_O = -7V					-250	mA
		V_O = V_{CC}					250	
		V_O = 12V					250	
		V_O = 0V					150	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	50	mA
			Outputs disabled			20	50	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
(4) See TIA/EIA-485-A 图 6-3.5, test termination measurement 2.
(5) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.4.2 Switching Characteristics

at V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high- to low-level output	R_L = 60Ω, C_{L1} = C_{L2} = 100pF, See 图 6-3		9	15	22	ns
t_{PHL}	Propagation delay time, low- to high-level output	R_L = 60Ω , C_{L1} = C_{L2} = 100pF, See 图 6-3		9	15	22	ns
t_{sk}	Output-to-output skew	R_L = 60Ω, C_{L1} = C_{L2} = 100pF, See 图 6-3		0	2	8	ns
t_{PZH}	Output enable time to high level	C_L = 100pF,	See 图 6-4	30	35	50	ns
t_{PZL}	Output enable time to low level	C_L = 100pF,	See 图 6-5	5	15	25	ns
t_{PHZ}	Output disable time from high level	C_L = 15pF,	See 图 6-4	7	15	30	ns

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5.4.2 Switching Characteristics（续）

at V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLZ}	Output disable time from low level	C_L = 15pF,	See 图 6-5	7	15	30	ns

5.5 Receiver Section

5.5.1 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7V,	I_O = -0.4mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5V,	I_O = 8mA	-0.2[2]			V
V_{hys}	Input hysteresis voltage (V_{IT+} - V_{IT-})					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = -18mA				-1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200mV, I_{OH} = -400 μA, See 图 6-2		2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200mV, I_{OL} = 8mA, See 图 6-2				0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4V to 2.4V				±20	μA
I_I	Line input current (see Note 6)		Other input at 0V	V_I = 12V			1	mA
				V_I = -7V			-0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4V				-100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0V,	See Note 7	-15		-85	mA
I_{CC}	Supply current (total package)		No load,	outputs enabled		35	50	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.
(4) Not more than one output should be shorted at a time.

5.5.2 Switching Characteristics

at V_{CC} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		C_L = 15pF,	See 图 6-6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output		C_L = 15pF,	See 图 6-6	15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100pF,	See 图 6-7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100pF,	See 图 6-7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15pF,	See 图 6-7	3.5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15pF,	See 图 6-7	5	12	16	ns

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6 Parameter Measurement Information

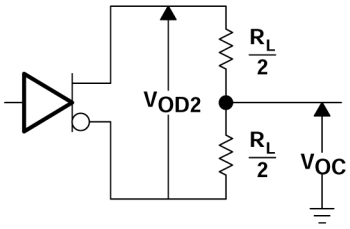


图 6-1. Driver Test Circuit, V_{OD} and V_{OC}

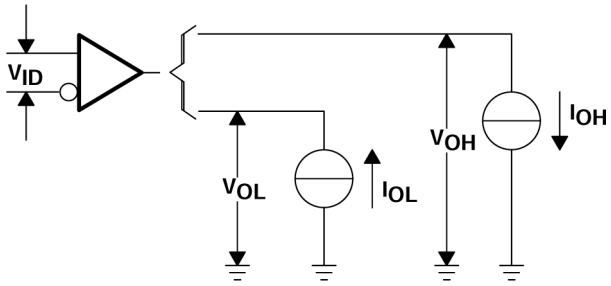
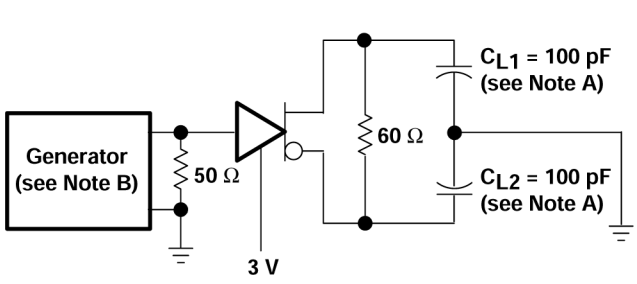
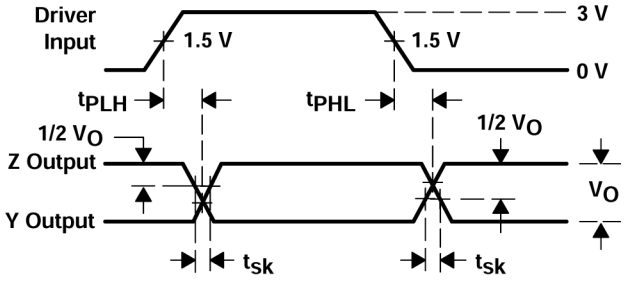


图 6-2. Receiver Test Circuit, V_{OH} and V_{OL}



DRIVER TEST CIRCUIT

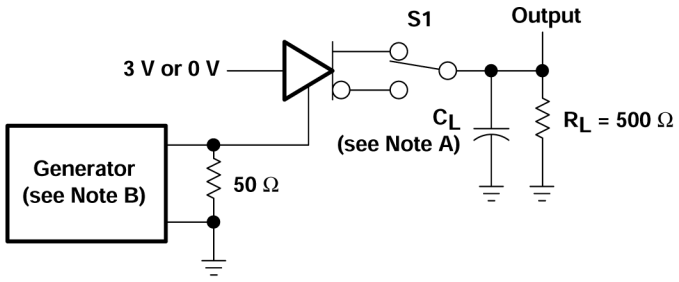


DRIVER VOLTAGE WAVEFORMS

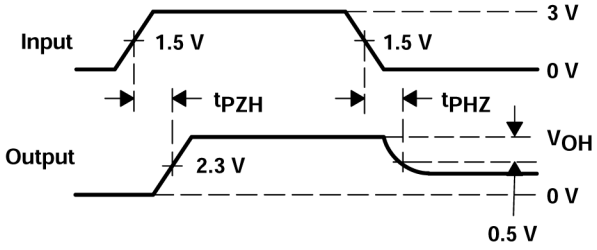
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT



DRIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-4. Driver Enable and Disable Times

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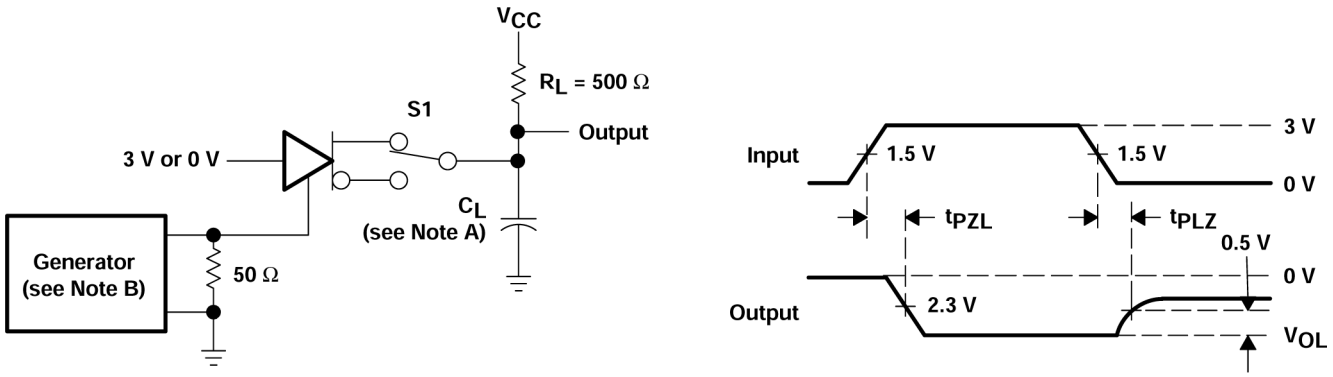


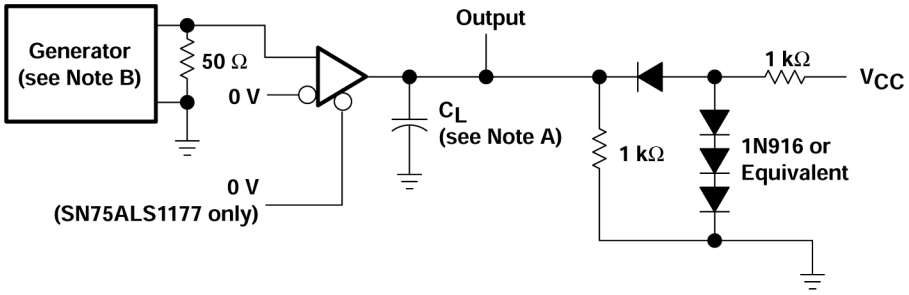
DRIVER TEST CIRCUIT

DRIVER VOLTAGE WAVEFORMS

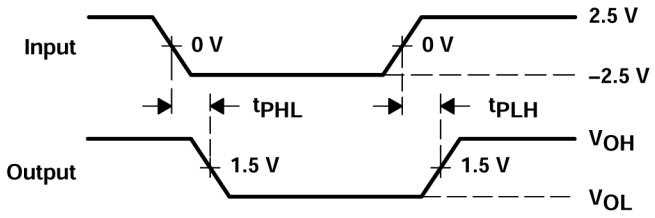
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-5. Driver Enable and Disable Times



RECEIVER TEST CIRCUIT



DRIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-6. Receiver Propagation Delay Times

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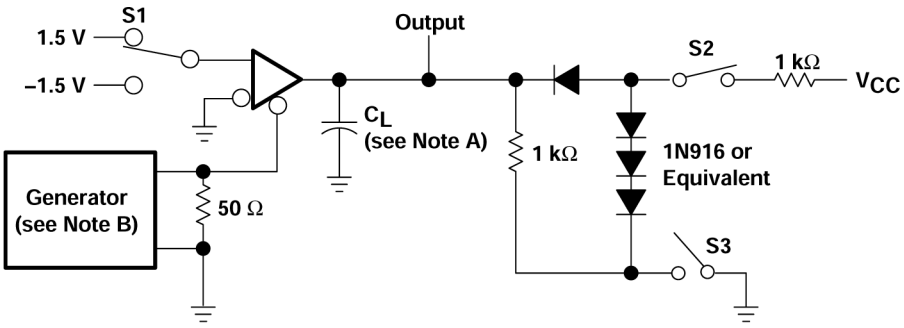
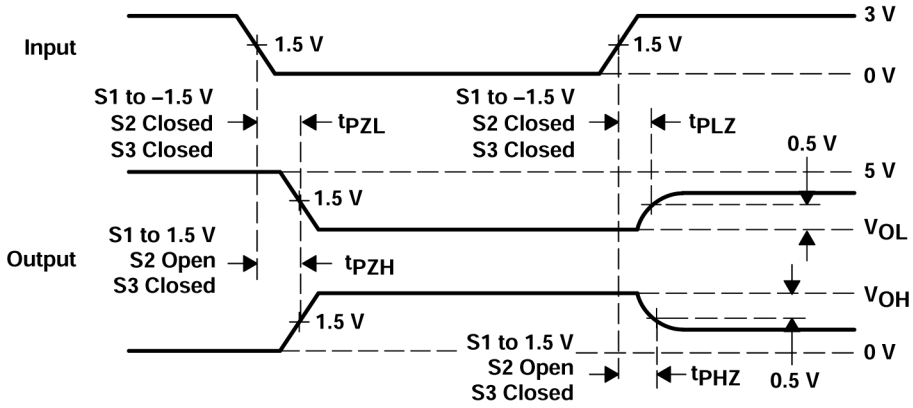


RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ⩽ 1MHz, 50% duty cycle, t_r ⩽ 10ns, t_f ⩽ 10ns.

图 6-7. Receiver Output Enable and Disable Times

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7 Detailed Description

7.1 Device Functional Modes

表 7-1. SN75ALS1177, SN75ALS1178 Functional Table (Each Driver)

INPUT D	ENABLE DE	OUTPUTS(1)	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

表 7-2. SN75ALS1177 Functional Table (Each Receiver)

DIFFERENTIAL A – B	ENABLE $\overline{RE}$ (1)	OUTPUT Y(1)
$V_{ID} \geqslant 0.2V$	L	H
$-0.2\ V < V_{ID} < 0.2V$	L	?
$V_{ID} \leqslant -0.2V$	L	L
X	H	Z
Open	L	H

表 7-3. SN75ALS1178 Functional Table (Each Receiver)

DIFFERENTIAL A – B	OUTPUT Y(1)
$V_{ID} \geqslant 0.2V$	H
$-0.2\ V < V_{ID} < 0.2V$	?
$V_{ID} \leqslant -0.2V$	L
Open	H

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

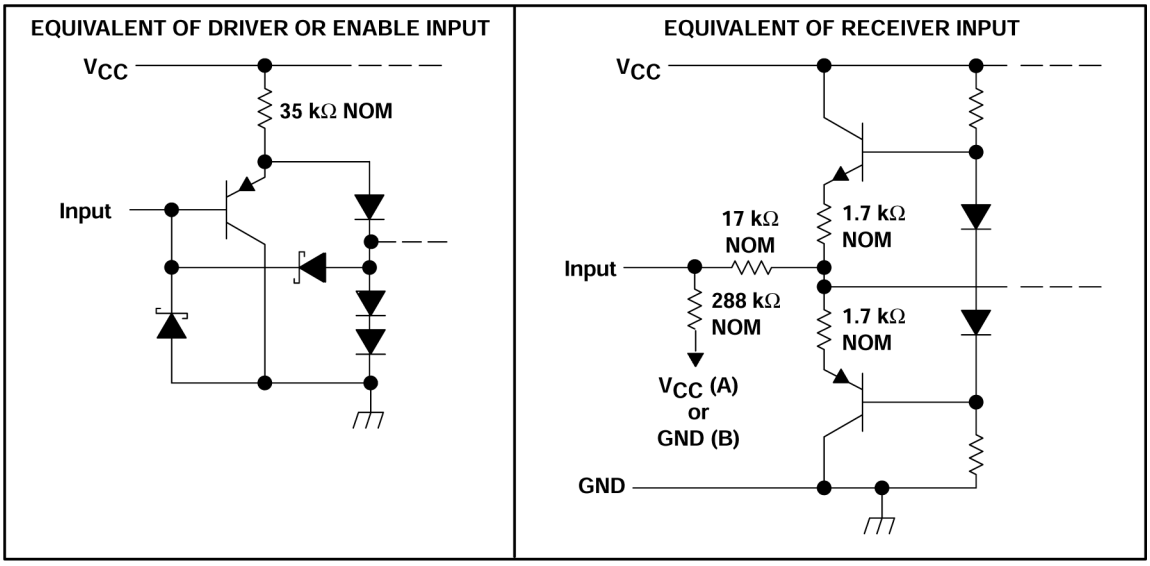

图 7-1. Equivalent Schematics

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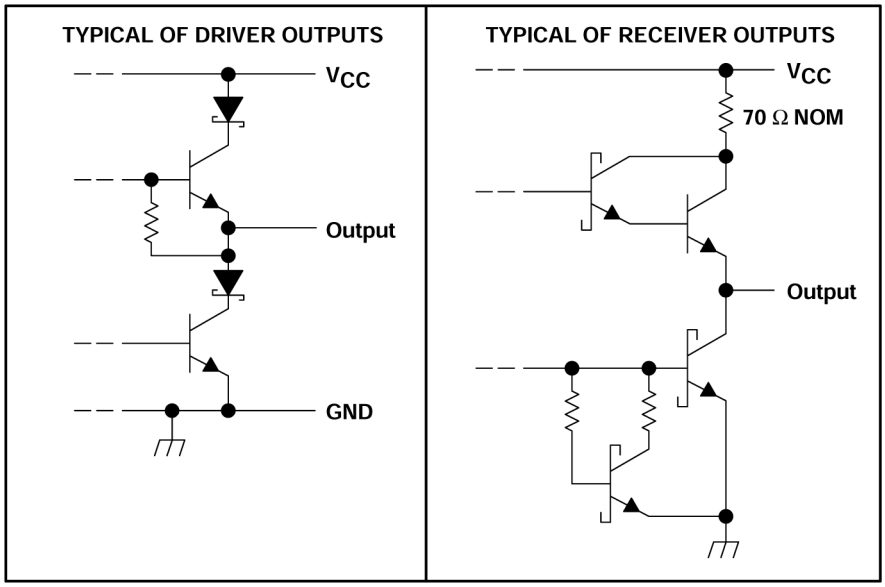

图 7-2. Schematics of Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

E2E™ 支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

Changes from Revision B (February 2001) to Revision C (February 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS1177N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS1177N	Samples
SN75ALS1177NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1177	Samples
SN75ALS1178N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS1178N	Samples
SN75ALS1178NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS1178	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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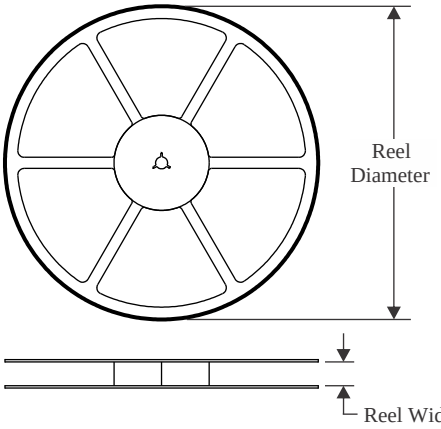
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

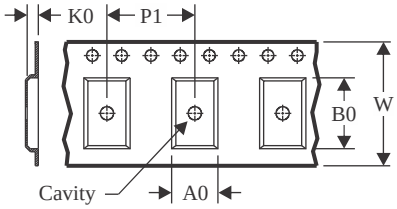
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

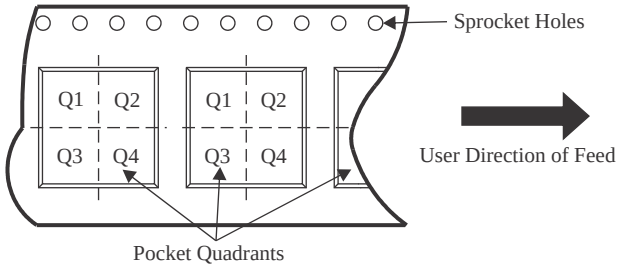


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

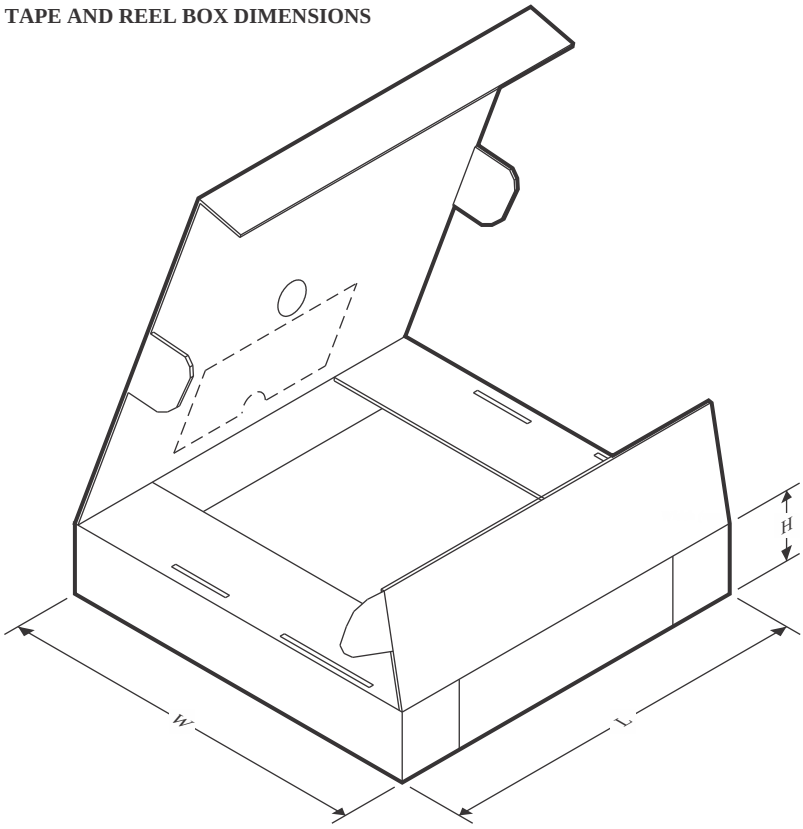
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS1177NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS1177NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS1178NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS1178NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

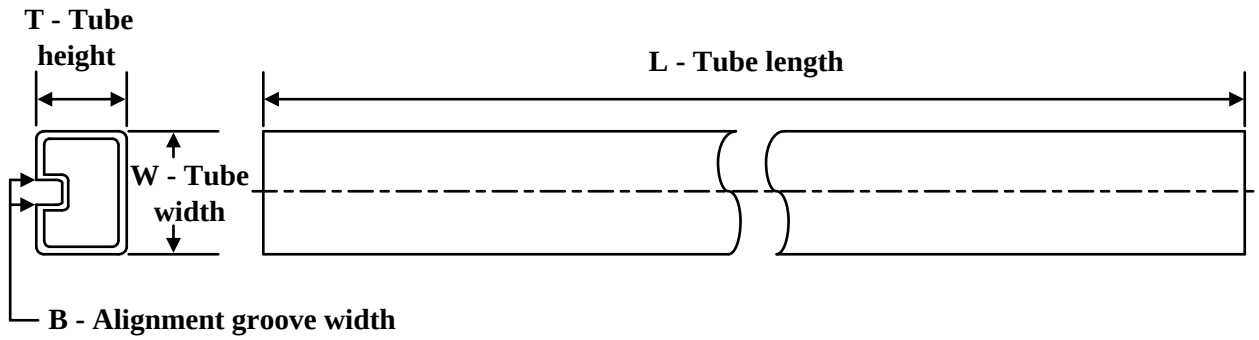
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS1177NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN75ALS1177NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN75ALS1178NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN75ALS1178NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



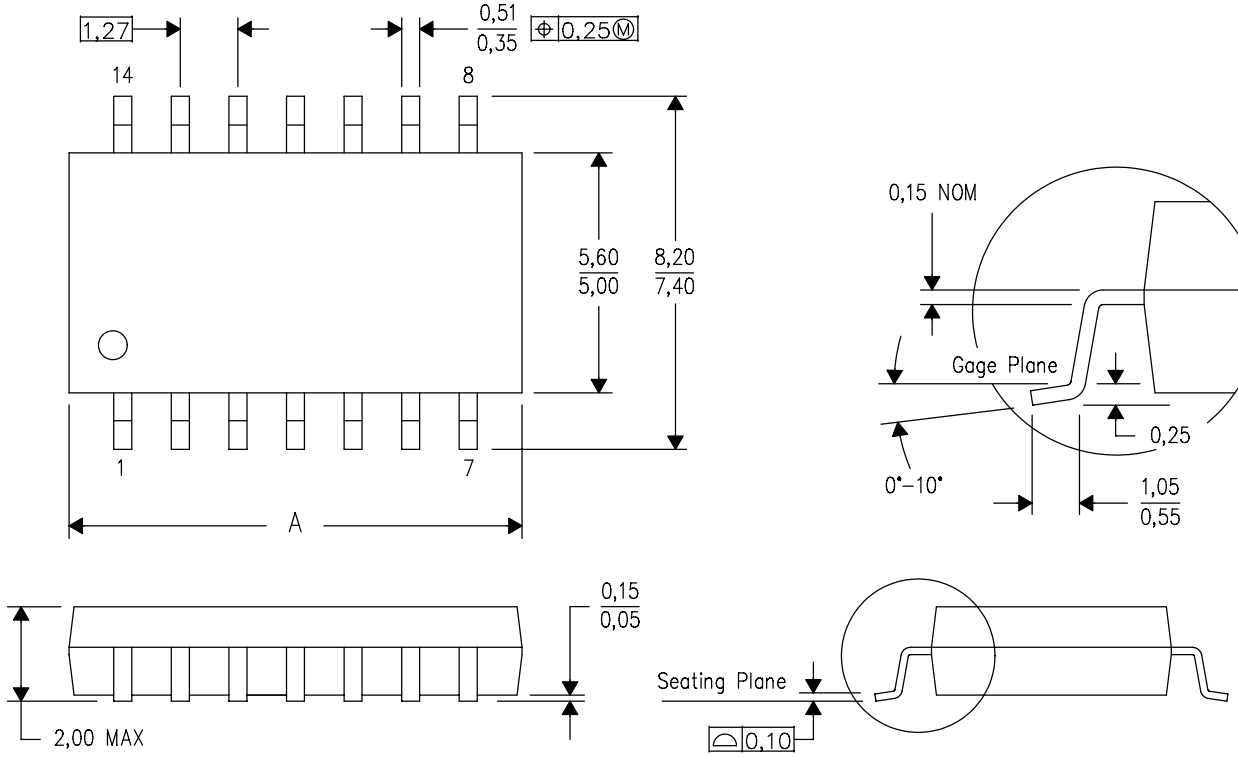
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS1177N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS1178N	N	PDIP	16	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

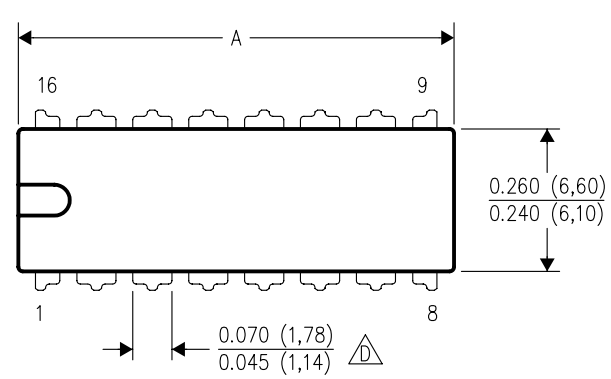
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

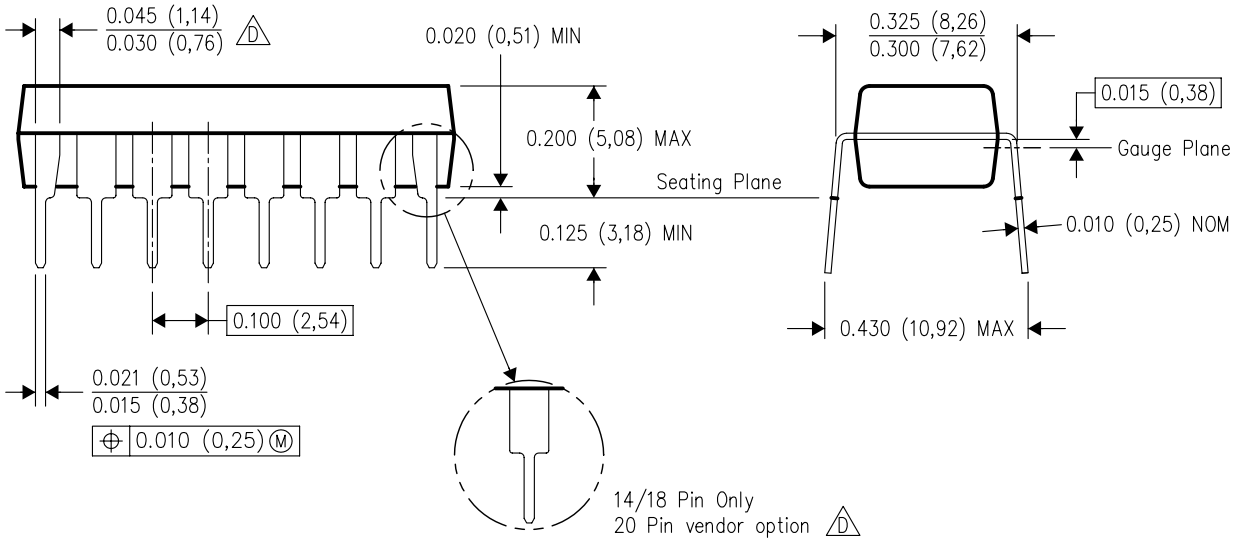
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

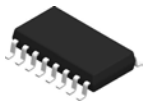


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

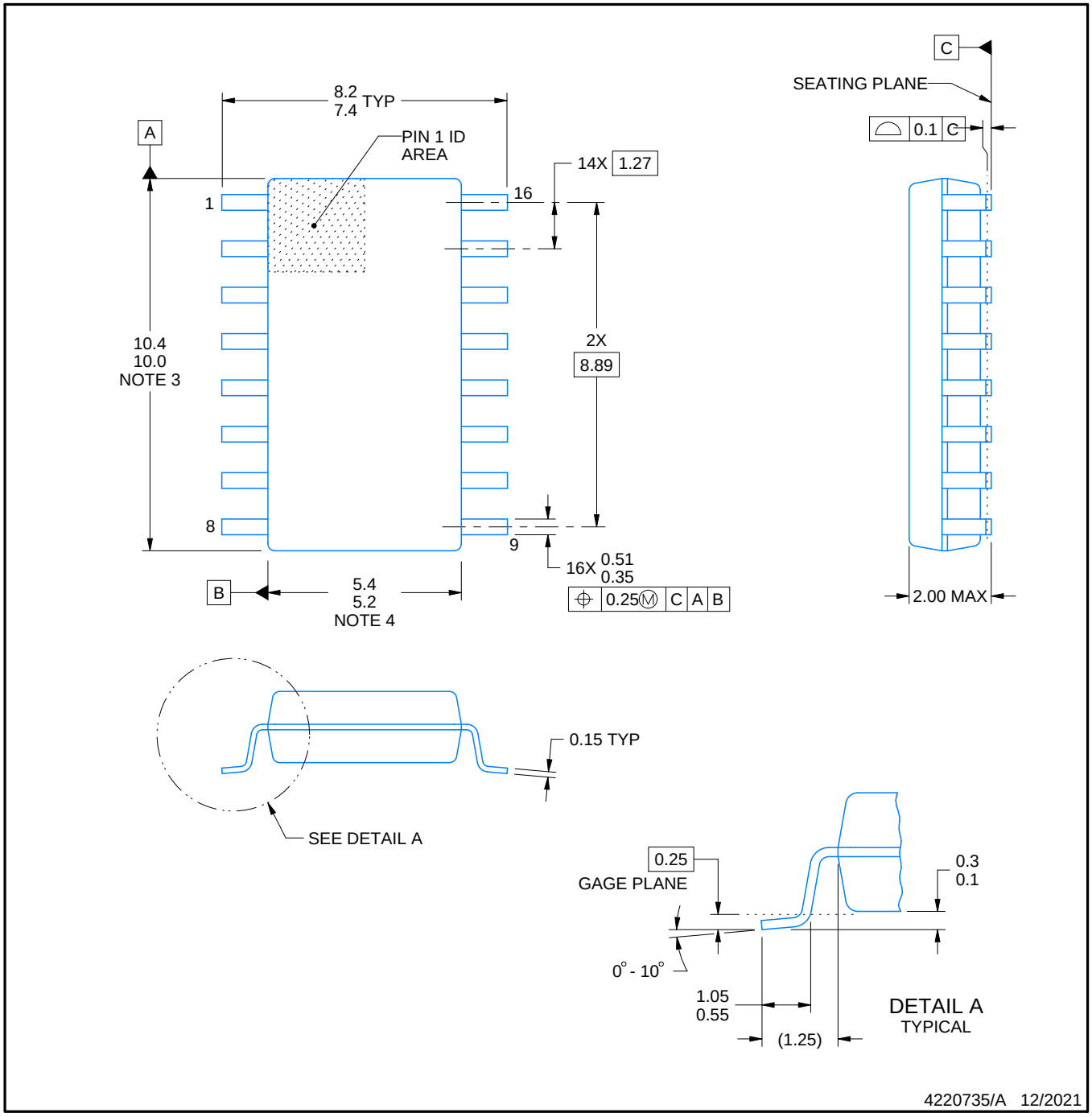


PACKAGE OUTLINE

NS0016A

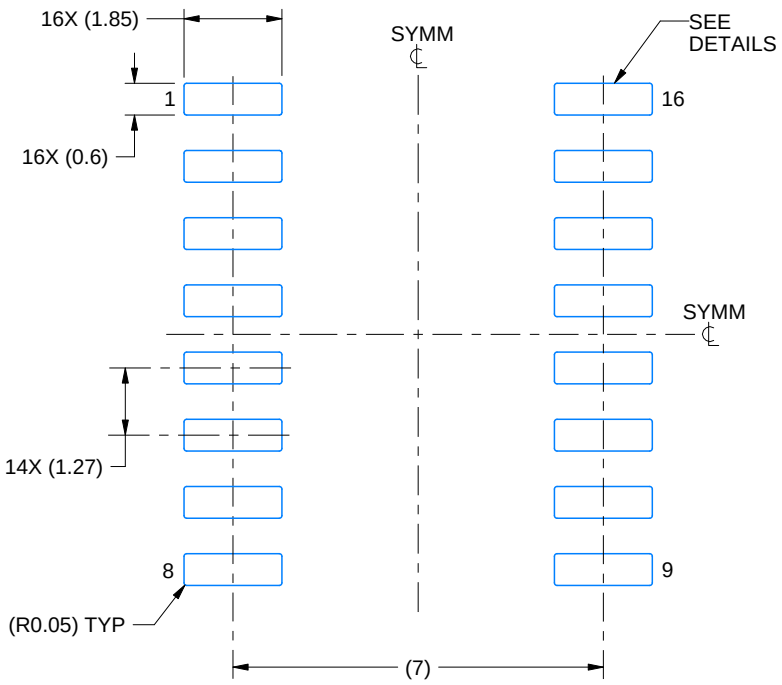
SOP - 2.00 mm max height

SOP

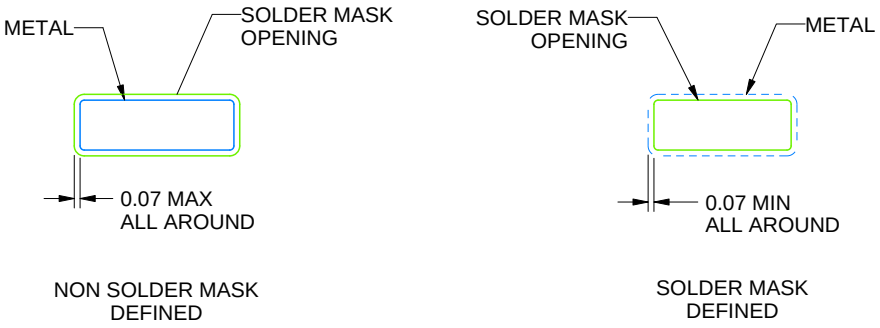


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

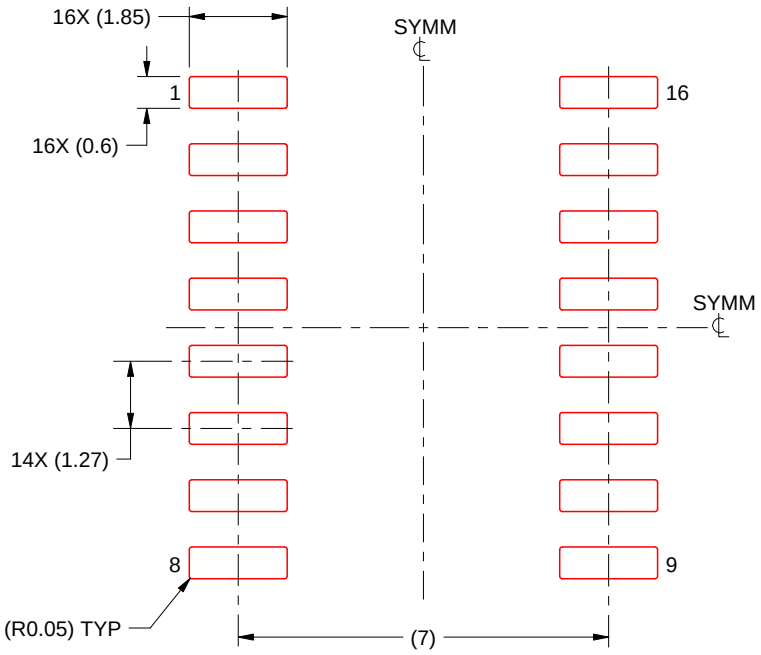
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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