1.5V/1.8V 25-BIT CONFIGURABLE REGISTERED BUFFER WITH ADDRESS-PARITY TEST

FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Pinout Optimizes DDR2 DIMM PCB Layout**
- **Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer**
- **Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption**
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line**
- **Supports 1.5V and 1.8V Supply Voltage Range**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the Control and $\overline{\text{RESET}}$ Inputs**
- **Checks Parity on DIMM-Independent Data Inputs**
- **Able to Cascade With a Second SN74SSTEB32866**
- **Supports Industrial Temperature Range (–40°C to 85°C)**

DESCRIPTION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.425-V to 1.9-V VCC operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the reset ($\overline{\text{RESET}}$) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meets SSTL_18 and SSTL_15 specifications (depending on Supply voltage level), except the open-drain error ($\overline{\text{QERR}}$) output.

The SN74SSTEB32866 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and CLK going low.

The SN74SSTEB32866 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0; D2–D3, D5–D6, D8–D14 when C0 = 0 and C1 = 1; or D1-D6, D8-D13 when C0 = 1 and C1 = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity; i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs, combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR_IN input signal, which arrives one cycle after the input data to which it applies. Two clock cycles after the data are registered, the corresponding partial-parity-out (PPO) and $\overline{\text{QERR}}$ signals are generated.

When used in pairs, the C0 input of the first register is tied low, and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input signal of the first device. Two clock cycles after the data are registered, the corresponding PPO and $\overline{\text{QERR}}$ signals are generated on the second device. The PPO output of the first register is cascaded to the PAR_IN of the second SN74SSTEB32866. The $\overline{\text{QERR}}$ output of the first SN74SSTEB32866 is left floating, and the valid error information is latched on the $\overline{\text{QERR}}$ output of the second SN74SSTEB32866.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA–ZWL	Tape and reel	SN74SSTEB32866ZWLR	SEB866

(1) Package drawings, packing quantities, thermal data, symbolization, PCB design guidelines available at www.ti.com/sc/package.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity-error duration or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE, $\overline{\text{DCS}}$, DODT, and $\overline{\text{CSR}}$) are not included in the parity-check computation.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and are do-not-use (DNU) pins.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared, and the data outputs are driven low quickly, relative to the time required to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SN74SSTEB32866 ensures that the outputs remain low, thus ensuring there will be no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low, except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and Cn inputs always must be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and gates the Qn and PPO outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either DCS or CSR input is low, the Qn and PPO outputs function normally. Also, if the internal low-power signal (LPS1) is high (one cycle after $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ go high), the device gates the $\overline{\text{QERR}}$ output from changing states. If LPS1 is low, the $\overline{\text{QERR}}$ output functions normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and, when driven low, forces the Qn and PPO outputs low and forces the $\overline{\text{QERR}}$ output high. If the $\overline{\text{DCS}}$ control functionality is not desired, the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case the setup-time requirement for $\overline{\text{DCS}}$ is the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS}}$ only, the $\overline{\text{CSR}}$ input should be pulled up to V_{CC} through a pull-up resistor.

The two V_{REF} pins (A3 and T3) are connected together internally by approximately 150Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

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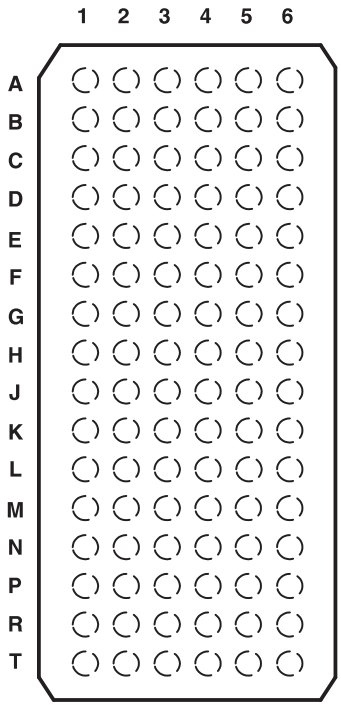
PACKAGE
(TOP VIEW)



Terminal Assignments for 1:1 Register-A (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	D1 (DCKE)	PPO	V_{REF}	V_{CC}	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{CC}	V_{CC}	Q3	Q16
D	D4 (DODT)	$\overline{\text{QERR}}$	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V_{CC}	V_{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7 ($\overline{\text{QCS}}$)	DNU
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{CC}	V_{CC}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{CC}	V_{CC}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{CC}	V_{CC}	Q13	Q24
T	D14	D25	V_{REF}	V_{CC}	Q14	Q25

Each pin name in parentheses indicates the DDR2 DIMM signal name
DNU - Do not use
NC - No internal connection

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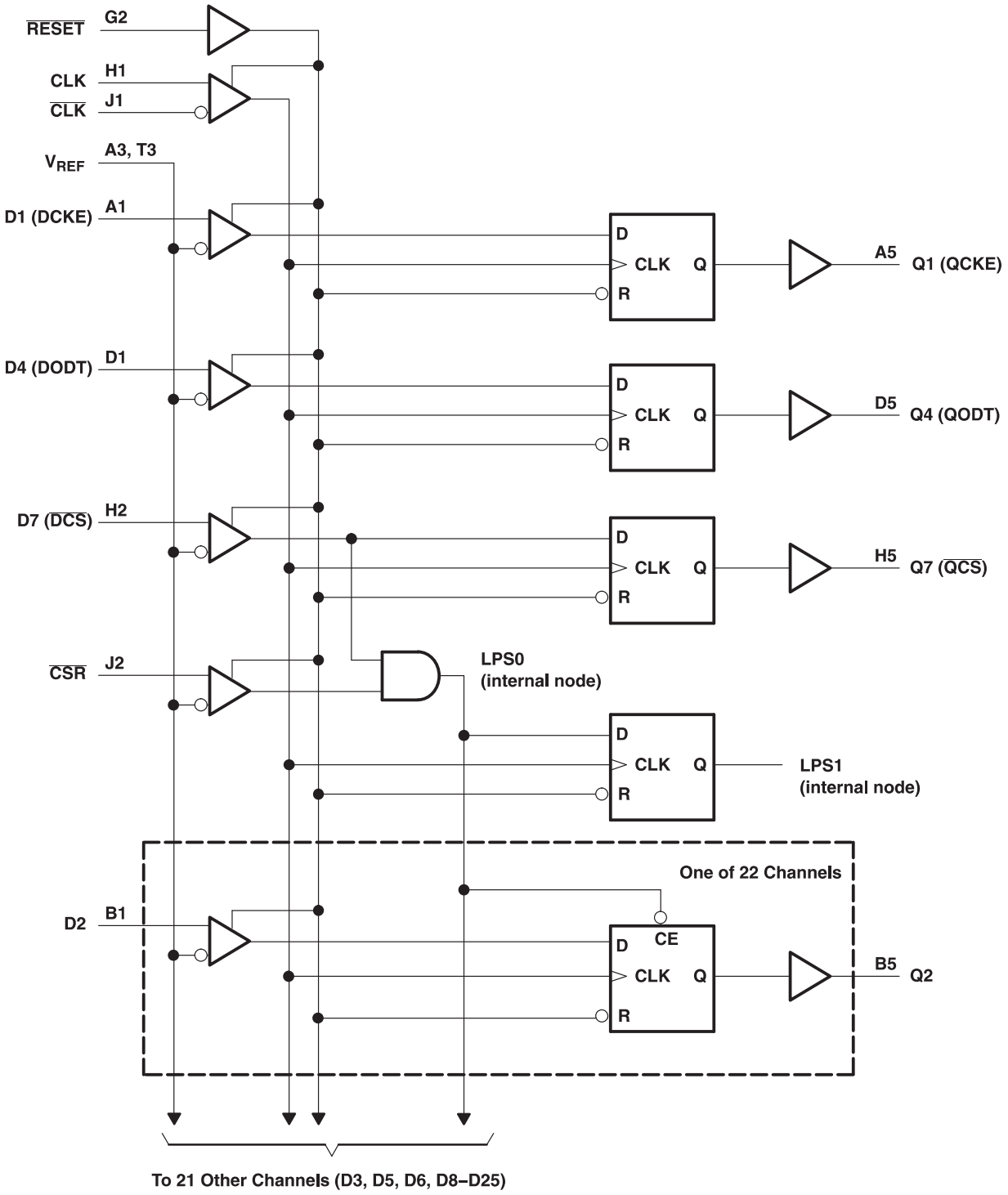
Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0



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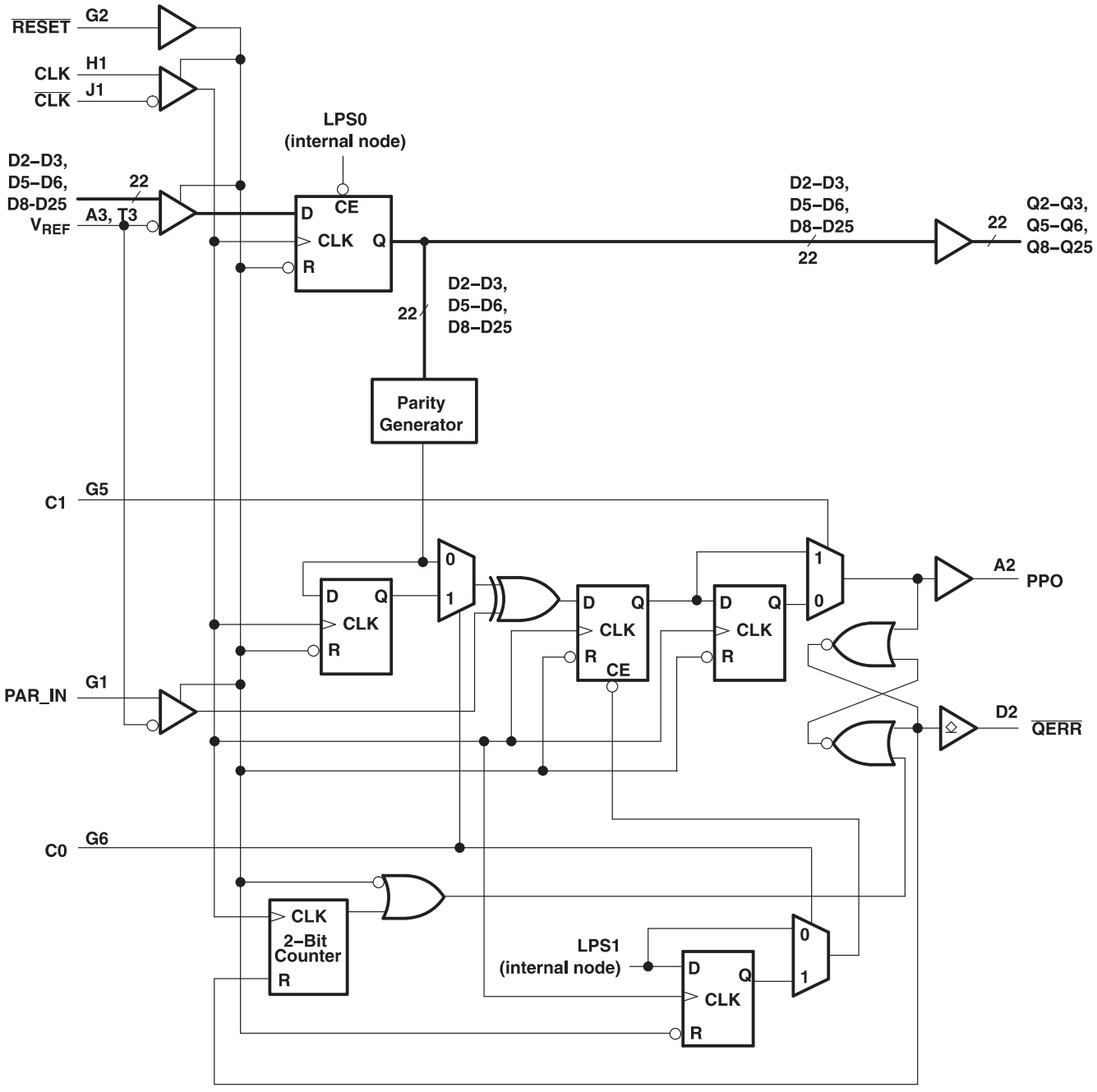
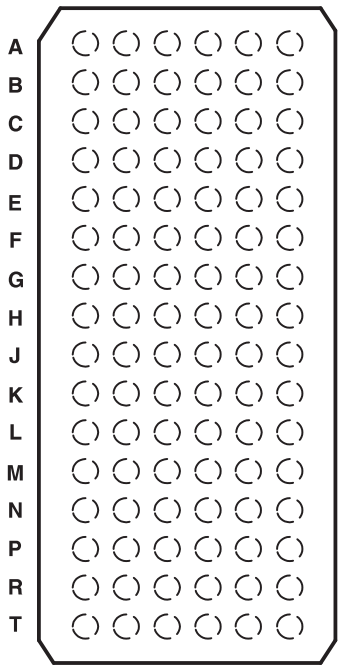
Parity Logic Diagram for 1:1 Register Configuration (Positive Logic); C0 = 0, C1 = 0



PACKAGE
(TOP VIEW)



Terminal Assignments for 1:2 Register-A (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	D1 (DCKE)	PPO	V_{REF}	V_{CC}	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4 (DODT)	$\overline{\text{QERR}}$	GND	GND	Q4A (QODTA)	Q4B(QODTB)
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{CC}	V_{CC}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14	DNU	V_{REF}	V_{CC}	Q14A	Q14B

Each pin name in parentheses indicates the DDR2 DIMM signal name.
DNU - Do not use
NC - No internal connection

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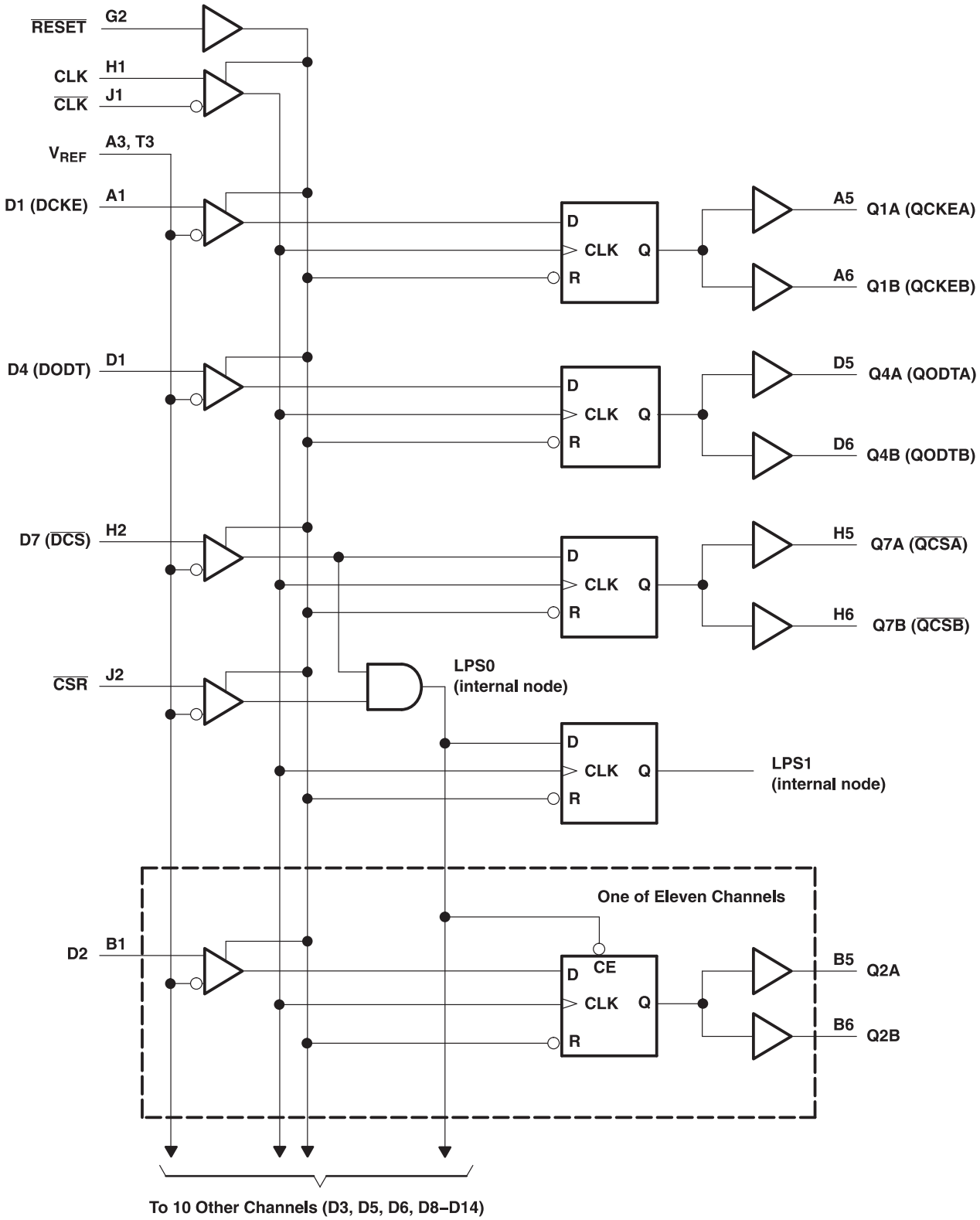
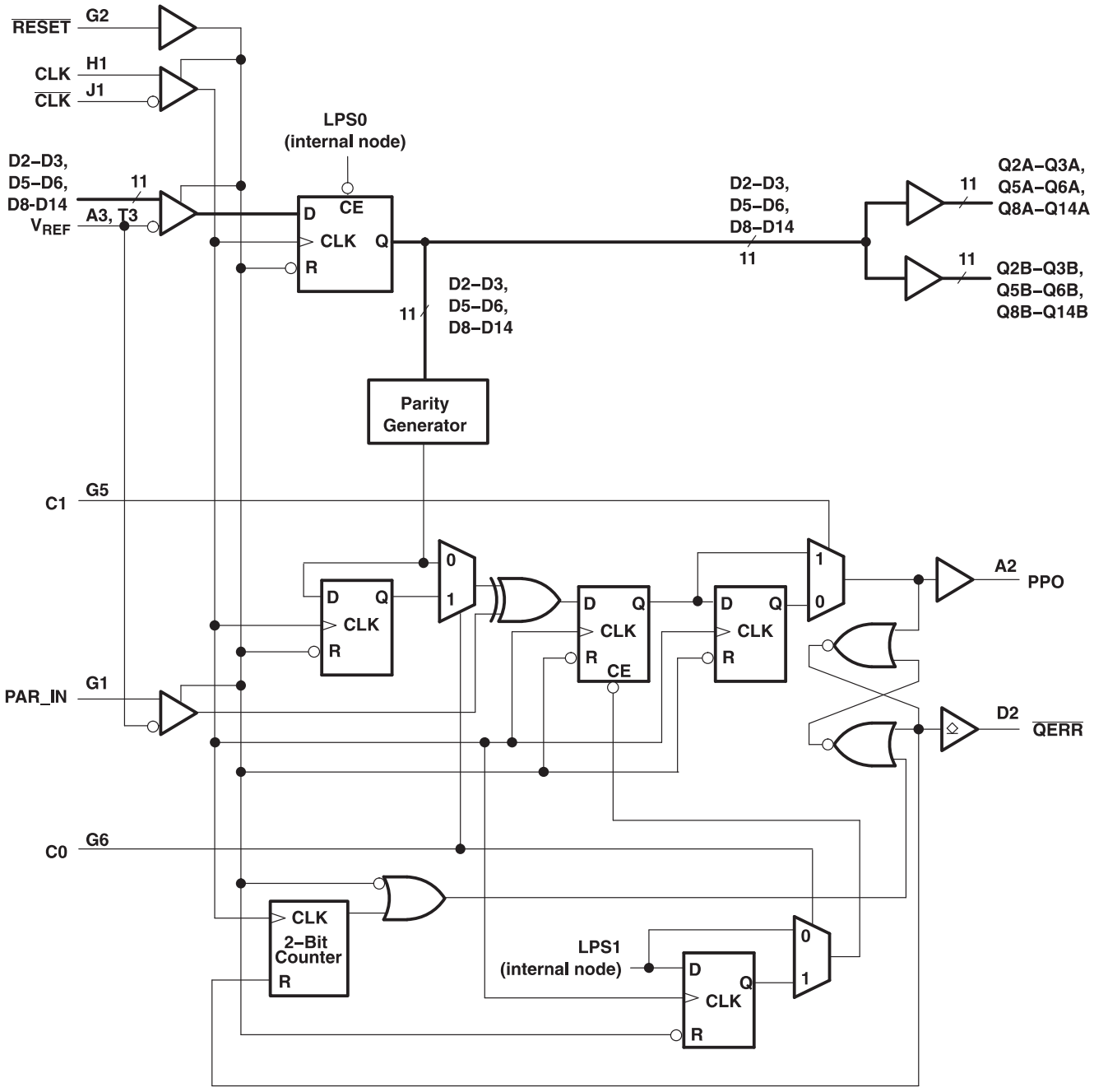
Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1



Parity Logic Diagram for 1:2 Register-A Configuration (Positive Logic); C0 = 0, C1 = 1



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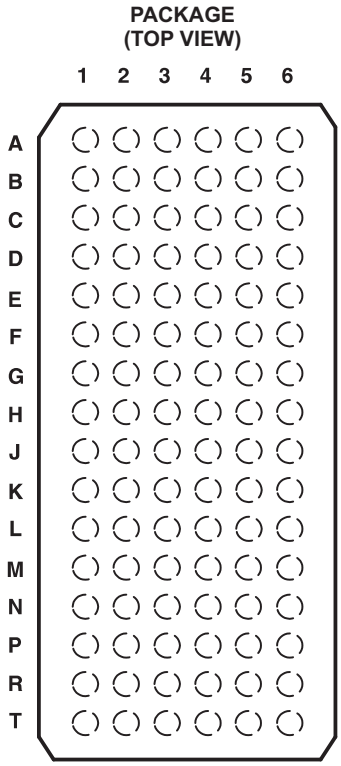

Terminal Assignments for 1:2 Register-B (C0 = 1, C1 = 1)

	1	2	3	4	5	6
A	D1	PPO	V_{REF}	V_{CC}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{CC}	V_{CC}	Q3A	Q3B
D	D4	$\overline{\text{QERR}}$	GND	GND	Q4A	Q4B
E	D5	DNU	V_{CC}	V_{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{\text{RESET}}$	V_{CC}	V_{CC}	C1	C0
H	CLK	D7 ($\overline{\text{DCS}}$)	GND	GND	Q7A ($\overline{\text{QCSA}}$)	Q7B ($\overline{\text{QCSB}}$)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V_{CC}	V_{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{CC}	V_{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V_{CC}	V_{CC}	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{CC}	V_{CC}	Q13A	Q13B
T	D14 (DCKE)	DNU	V_{REF}	V_{CC}	Q14A (QCKEA)	Q14B (QCKEB)

Each pin name in parentheses indicates the DDR2 DIMM signal name.
DNU - Do not use
NC - No internal connection

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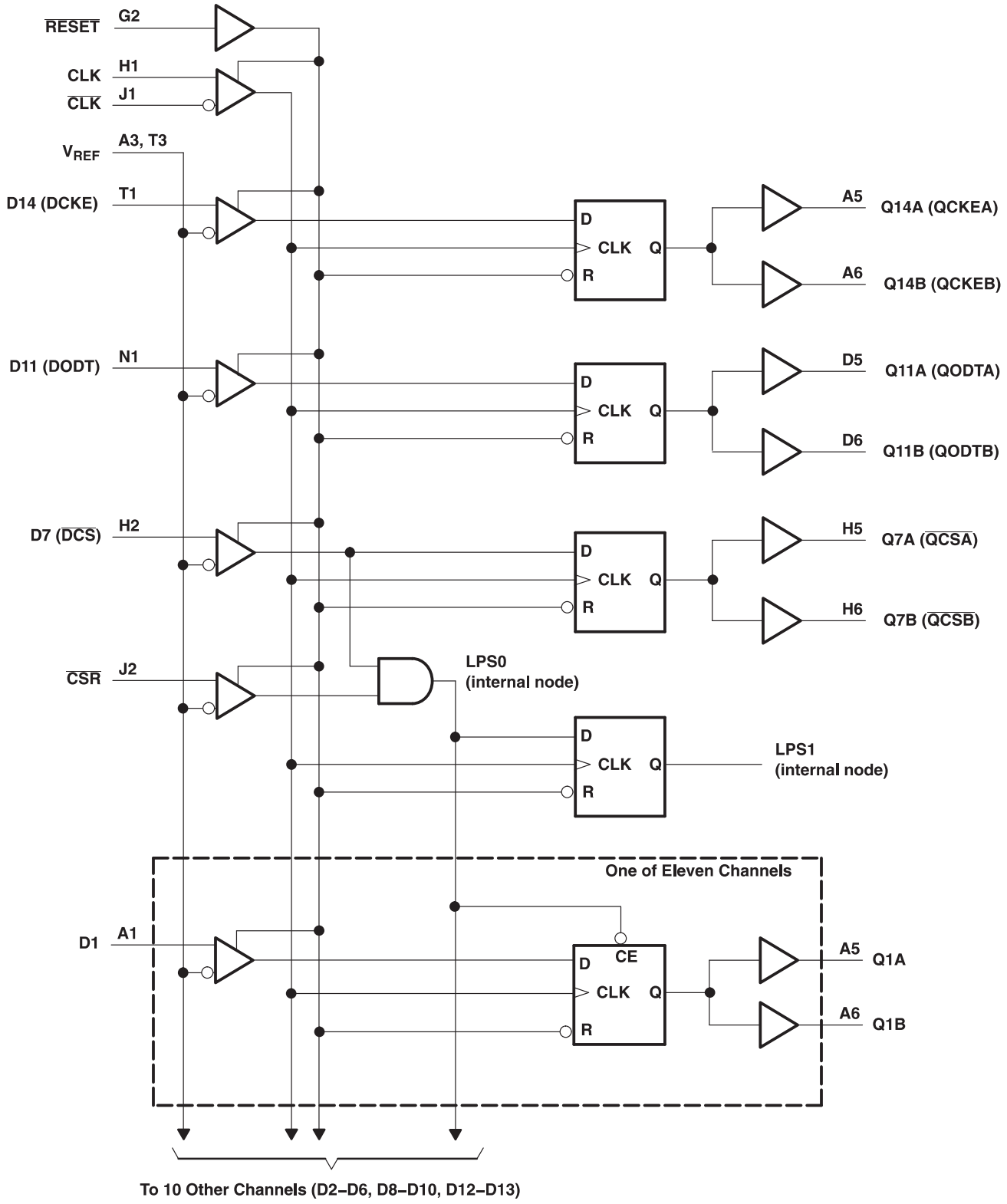
Logic Diagram for 1:2 Register-B Configuration C0 = 1, C1 = 1



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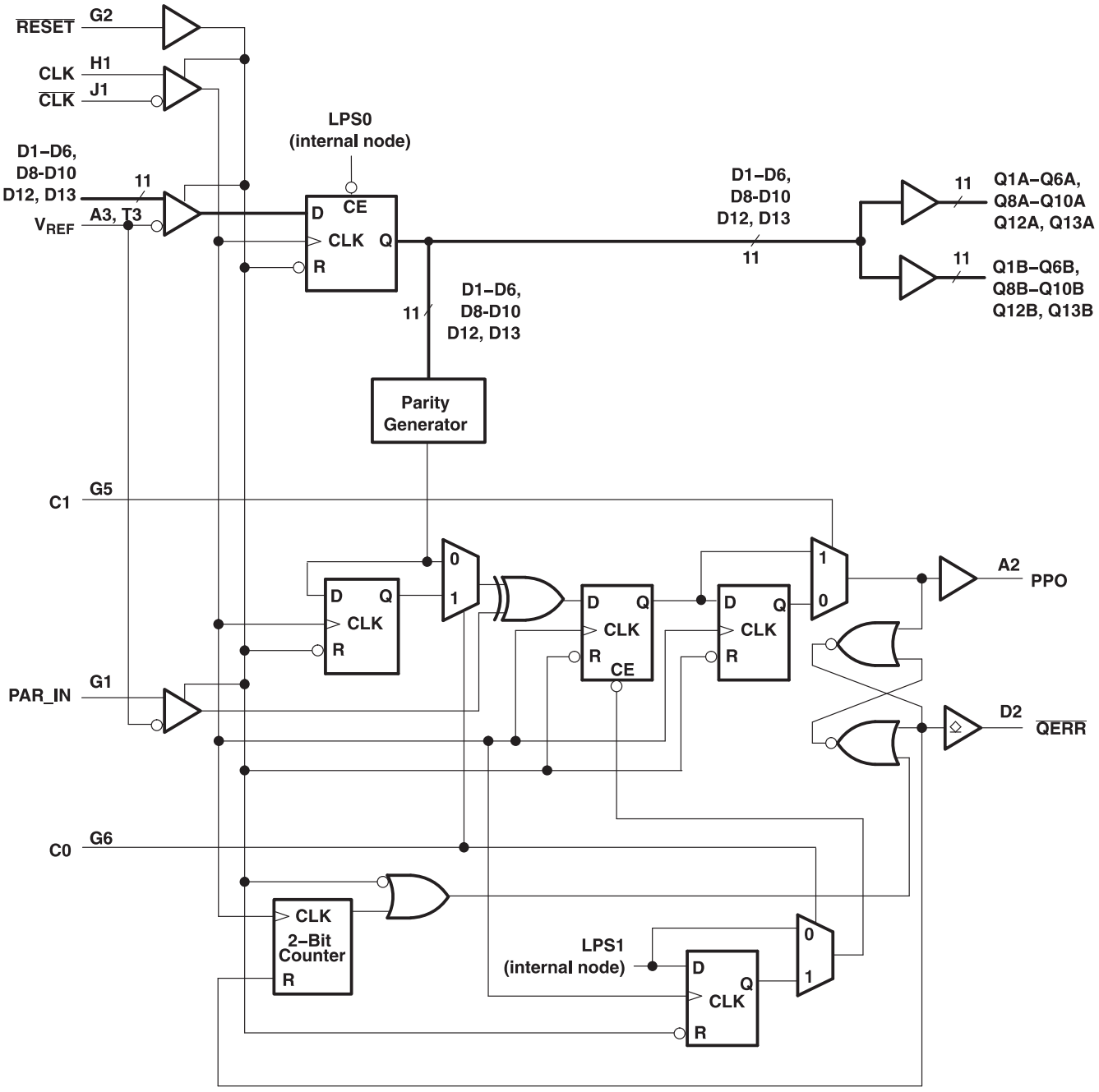
Parity Logic Diagram for 1:2 Register-B Configuration (Positive Logic); C0 = 1, C1 = 1



PIN FUNCTIONS

NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V_{CC}	Power-supply voltage	1.8 V / 1.5 V nominal
V_{REF}	Input reference voltage	0.9 V / 0.75 V nominal
CLK	Positive master clock input	Differential input
$\overline{CLK}$	Negative master clock input	Differential input
C0, C1	Configuration control input. Register A or Register B and 1:1 mode or 1:2 mode select.	LVCMOS inputs
$\overline{RESET}$	Asynchronous reset input. Resets registers and disables V_{REF}, data, and clock differential-input receivers. When $\overline{RESET}$ is low, all Q outputs are forced low and the $\overline{QERR}$ output is forced high.	LVCMOS input
D1-D25	Data input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$.	SSTL_18 inputs / SSTL_15 inputs
$\overline{CSR}$, $\overline{DCS}$	Chip select inputs. Disables D1–D25 (1) outputs switching when both inputs are high	SSTL_18 inputs / SSTL_15 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input / SSTL_15 inputs
DCKE	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	SSTL_18 input / SSTL_15 inputs
PAR_IN	Parity input. Arrives one clock cycle after the corresponding data input. Pull-down resistor of typical 150kΩ to GND.	SSTL_18 input / SSTL_15 inputs, Pull-down
Q1–Q25 (2)	Data outputs that are suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.	1.8 V / 1.5 V CMOS outputs
PPO	Partial parity out. Indicates odd parity of inputs D1–D25. (1)	1.8 V / 1.5 V CMOS output
$\overline{QCS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V / 1.5 V CMOS output
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V / 1.5 V CMOS output
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8 V / 1.5V CMOS output
$\overline{QERR}$	Output error bit. Timing is determined by the device mode.	Open-drain output
NC	No internal connection	
DNU	Do not use. Inputs are in standby-equivalent mode, and outputs are driven low.	

(1) Data inputs = D2, D3, D5, D6, D8-D25 when C0 = 0 and C1 = 0
Data inputs = D2, D3, D5, D6, D8-D14 when C0 = 0 and C1 = 1
Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1.D
(2) Data outputs = Q2, Q3, Q5, Q6, Q8-Q25 when C0 = 0 and C1 = 0
Data outputs = Q2, Q3, Q5, Q6, Q8-Q14 when C0 = 0 and C1 = 1
Data outputs = Q1-Q6, Q8-Q10, Q12, Q13 when C0 = 1 and C1 = 1.

FUNCTION TABLE

INPUTS						OUTPUTS
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dn	Qn
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q_0
H	X	X	L or H	L or H	X	Q_0
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L

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FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	DCKE, $\overline{\text{DCS}}$, $\overline{\text{DODT}}$	QCKE, $\overline{\text{QCS}}$, QODT
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or Floating	X or Floating	X or Floating	L

PARITY AND STANDBY FUNCTION

INPUTS							OUTPUTS	
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	Σ OF INPUTS = H D1–D25 (1)	PAR_IN (2)	PPO	$\overline{\text{QERR}}$ (3)
H	↑	↓	L	X	Even	L	L	H
H	↑	↓	L	X	Odd	L	H	L
H	↑	↓	L	X	Even	H	H	L
H	↑	↓	L	X	Odd	H	L	H
H	↑	↓	H	L	Even	L	L	H
H	↑	↓	H	L	Odd	L	H	L
H	↑	↓	H	L	Even	H	H	L
H	↑	↓	H	L	Odd	H	L	H
H	↑	↓	H	H	X	X	PPO_0	$\overline{\text{QERR}}_0$
H	L or H	L or H	X	X	X	X	PPO_0	$\overline{\text{QERR}}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X	X or Floating	L	H

(1) Data inputs = D2-D3, D5-D6, D8-D25 when C0 = 0 and C1 = 0
Data inputs = D2-D3, D5-D6, D8-D14 when C0 = 0 and C1 = 1
Data inputs = D1-D6, D8-D10, D12, D13 when C0 = 1 and C1 = 1
(2) PAR_IN arrives one clock cycle (C0 = 0) or two clock cycles (C0 = 1) after the data to which it applies.
(3) This transition assumes that $\overline{\text{QERR}}$ is high at the crossing of CLK going high and $\overline{\text{CLK}}$ going low. If $\overline{\text{QERR}}$ goes low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity duration or until $\overline{\text{RESET}}$ is driven low.

PARITY ERROR DETECT IN LOW-POWER MODE (1)

INPUT-DATA ERROR OCCURRENCE (2)	1:1 MODE (C0 = 0, C1 = 0)		1:2 REGISTER-A MODE (C0 = 0, C1 = 1)		1:2 REGISTER-B MODE (C0 = 1, C1 = 1)		CASCADED MODE (Registers A and B)	
	PPO DURATION (3)	$\overline{\text{QERR}}$ DURATION (3)	PPO DURATION (3)	$\overline{\text{QERR}}$ DURATION (3)	PPO DURATION (3)	$\overline{\text{QERR}}$ DURATION (3)	PPO DURATION (3)	$\overline{\text{QERR}}$ DURATION (3)
n – 4	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 3	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 2	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 1	LPM + 2 Cycles	LPM + 2 Cycles	LPM + 1 Cycle	LPM + 1 Cycle	LPM + 2 Cycles	LPM + 2 Cycles	LPM + 2 Cycles	LPM + 2 Cycles
n	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected

(1) If a parity error occurs before the device enters the low-power mode (LPM), the behavior of PPO and $\overline{\text{QERR}}$ is dependent on the mode of the device and the position of the parity error occurrence. This table illustrates the low-power-mode effect on parity detect. The low-power mode is activated on the n clock cycle when $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ go high.
(2) The clock-edge position of a one cycle data-input error relative to the clock-edge (n) which initiates LPM at the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs.
(3) If an error occurs, then $\overline{\text{QERR}}$ output may be driven low and the PPO output driven high. These columns show the clock duration for which the PPO signal will be high.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
V_{CC}	Supply voltage range		–0.5 to 2.5	V
V_I	Input voltage range(2) (3)		–0.5 to V_{CC} + 0.5	V
V_O	Output voltage range(2) (3)		–0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current, (V_I < 0 or V_I > V_{CC})		±50	mA
I_{OK}	Output clamp current, (V_O < 0 or V_O > V_{CC})		±50	mA
I_O	Continuous output current (V_O = 0 to V_{CC})		±50	mA
I_{CC}	Continuous current through each V_{CC} or GND		±100	mA
$R_{\theta JA}$	Thermal impedance, junction-to-ambient(4)	No airflow	39.8	K/W
		Airflow 150 ft/min	34.1	
		Airflow 250 ft/min	33.6	
		Airflow 500 ft/min	32.5	
$R_{\theta JC}$	Thermal resistance, junction-to-case(4)	No airflow	14.5	
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.8 V Range	1.7	1.8	1.9	V
		1.5 V Range	1.425	1.5	1.575	
V_{REF}	Reference voltage		0.49 × V_{CC}	0.5 × V_{CC}	0.51 × V_{CC}	V
V_{TT}	Termination voltage		V_{REF}–40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		VCC	V
V_{IH}	AC high-level input voltage	Data inputs, $\overline{CSR}$, PAR_IN	V_{REF} + 250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, $\overline{CSR}$, PAR_IN			V_{REF}–250 mV	V
V_{IH}	DC high-level input voltage	Data inputs, $\overline{CSR}$, PAR_IN	V_{REF} + 125 mV			V
V_{IL}	DC low-level input voltage	Data inputs, $\overline{CSR}$, PAR_IN			V_{REF}–125 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$, C_n	0.65 × V_{CC}			V
V_{IL}	Low-level input voltage	$\overline{RESET}$, C_n			0.35 × V_{CC}	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	V_{REF}-0.175		V_{REF}+0.175	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	600			mV
I_{OH}	High-level output current	Q outputs, PPO			–8	mA
I_{OL}	Low-level output current	Q outputs, PPO			8	mA
		$\overline{QERR}$ output	30			
T_A	Operating free-air temperature		-40		85	°C

(1) The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	Q outputs, PPO	I_{OH} = –100 µA		1.7V to 1.9V	V_{CC}–0.2			V
		I_{OH} = –6 mA		1.7V	1.3			
		I_{OH} = –100 µA		1.425V to 1.575V	V_{CC}–0.2			
		I_{OH} = –6 mA		1.425V	1.0			
V_{OL}	Q outputs, PPO	I_{OL} = 100 µA		1.7V to 1.9V			0.2	V
		I_{OL} = 6 mA		1.7V			0.4	
		I_{OL} = 100 µA		1.425V to 1.575V			0.2	
		I_{OL} = 6 mA		1.425V			0.4	
	$\overline{QERR}$ output	I_{OL} = 25 mA		1.7V			0.5	
		I_{OL} = 25 mA		1.425V			0.5	
I_I	PAR_IN	V_I = GND		1.9V			-5	µA
		V_I = V_{CC}					25	
	All other inputs(2)	V_I = V_{CC} or GND					±5	
I_{OZ}	$\overline{QERR}$ output	VO = V_{CC} or GND		1.9V			±10	µA
I_{CC}	Static standby	$\overline{RESET}$ = GND	I_O = 0	1.9V			200	µA
	Static operating	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$					40	mA
I_{CCD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8V		45		µA/MHz
	Dynamic operating – per each data input, 1:1 configuration	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				43		µA clock MHz/D input
	Dynamic operating – per each data input, 1:2 configuration					60		
I_{CCDLP}	Chip-select-enabled low-power active mode – clock only	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle	I_O = 0	1.8V		45		µA/MHz
	Chip-select-enabled low-power active mode - 1:1 configuration	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				2		µA clock MHz/D input
	Chip-select-enabled low-power active mode – 1:2 configuration					3		
C_I	Data inputs, $\overline{CSR}$, PAR_IN	V_I = V_{REF} ± 250 mV		1.8V	2.5	3	3.5	pF
	CLK, $\overline{CLK}$	V_{ICR} = 0.9 V, $V_{I(PP)}$ = 600 mV			2		3	
	$\overline{RESET}$	V_I = V_{CC} or GND				4		

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.
(2) Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open.

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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and [1])

			MIN	MAX	UNIT
fclock	Clock frequency			410	MHz
tw	Pulse duration, CLK, $\overline{CLK}$ high or low		1		ns
tact	Differential inputs active time[2] 1.8 V Range			10	ns
tinact	Differential inputs inactive time[3] 1.8 V Range			15	ns
t_{su}	Setup time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ high; $\overline{CSR}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS}$ high	600		ps
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ low	500		
		DODT, DCKE, and Data before CLK↑, $\overline{CLK}$↓	500		
		PAR_IN before CLK↑, $\overline{CLK}$↓	500		
t_h	Hold time	$\overline{DCS}$, DODT, DCKE, and Data after CLK↑, $\overline{CLK}$↓	400		ps
		PAR_IN after CLK↑, $\overline{CLK}$↓	400		

(1) All inputs slew rate is 1 V/ns ± 20%.
(2) V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{RESET}$ is taken high.
(3) V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	See Figure 1	1.8 V Range			410		MHz
		1.5 V Range					
t_{pd}	See Figure 4	1.8 V Range	CLK and $\overline{CLK}$	PPO	0.5	1.7	ns
		1.5 V Range					
t_{PLH}[1]	See Figure 3	1.8 V Range	CLK and $\overline{CLK}$	$\overline{QERR}$	1.2	3	ns
		1.5 V Range					
t_{PHL}[1]	See Figure 3	1.8 V Range			1	2.4	ns
		1.5 V Range					
t_{RPHL}[2]	See Figure 1	1.8 V Range	$\overline{RESET}$	Q		3	ns
		1.5 V Range					
t_{RPHL}	See Figure 4	1.8 V Range		PPO		3	
		1.5 V Range					
t_{RPLH}	See Figure 4	1.8 V Range	RESET	$\overline{QERR}$		3	ns
		1.5 V Range					

(1) This parameter is not included in production test and has to be considered as design goal only.
(2) Includes 350-ps test-load transmission-line delay.

OUTPUT SLEW RATES

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V_{CC} = 1.8 ± 0.1 V		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1	4	V/ns
dV/dt_f	80%	20%	1	4	V/ns
dV/dt_Δ[1]	20% or 80%	80% or 20%		1	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

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PARAMETER MEASUREMENT INFORMATION

PROPAGATION DELAY (Design Goal)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pdm} (1)	1.8 V Range	CLK and $\overline{CLK}$	Q	1.1	1.5	ns
	1.5 V Range			1.3	1.7	
t_{pdmss} (1)	1.8 V Range	CLK and $\overline{CLK}$	Q		1.6	ns
	1.5 V Range				1.8	

(1) Includes 350 psi test-load transmission delay line

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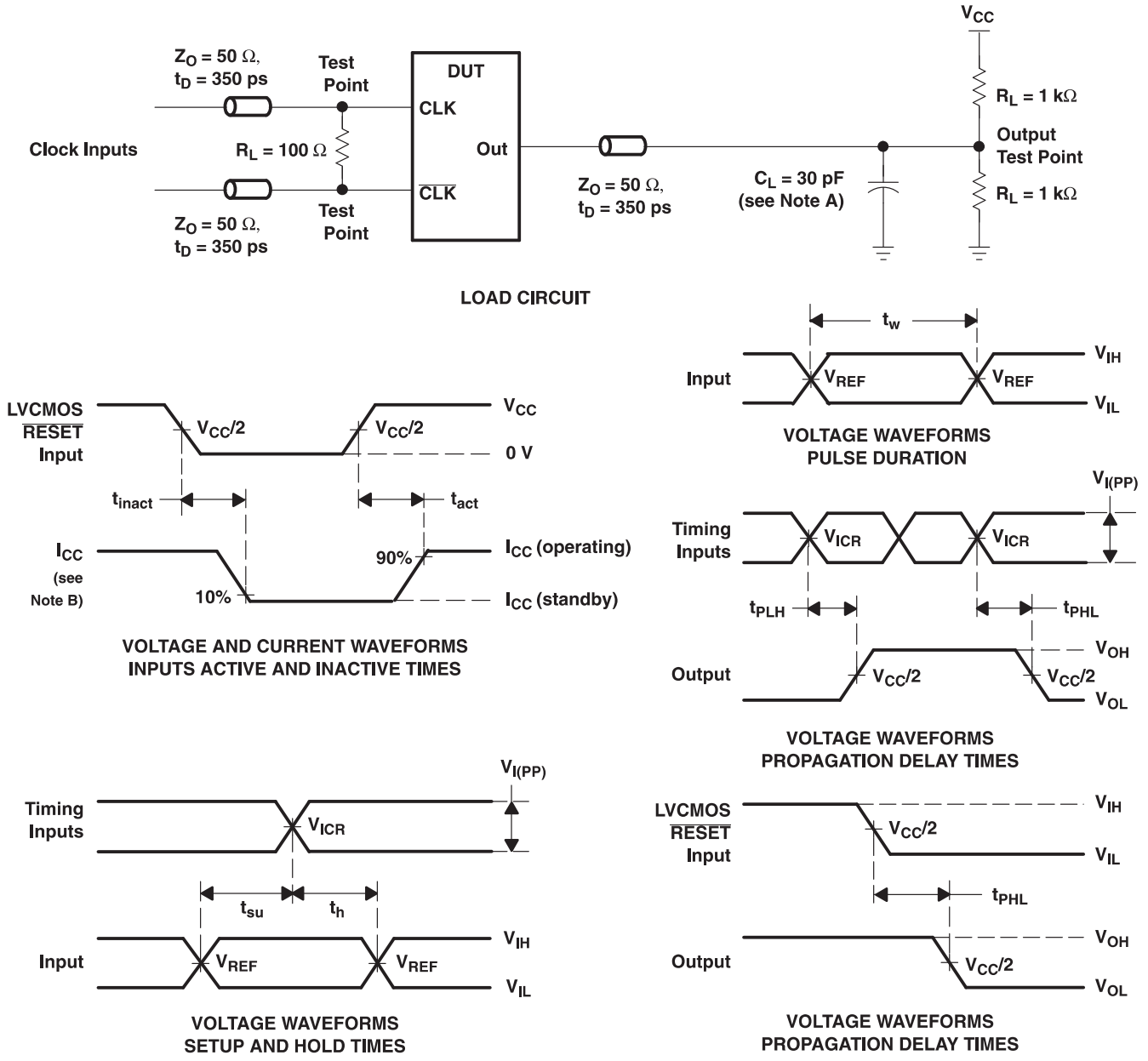

NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time, with one transition per measurement.
E. $V_{REF} = V_{TT} = V_{CC}/2$
F. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. $V_{I(PP)}$ = 600 mV
I. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Data Output Load Circuit and Voltage Waveforms

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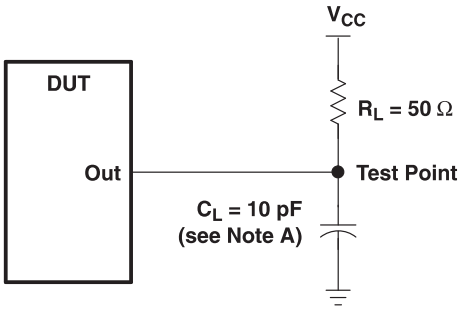
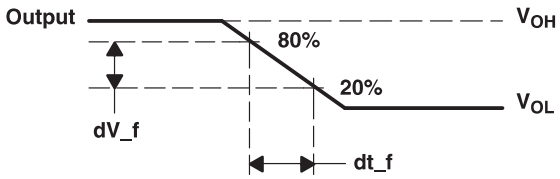
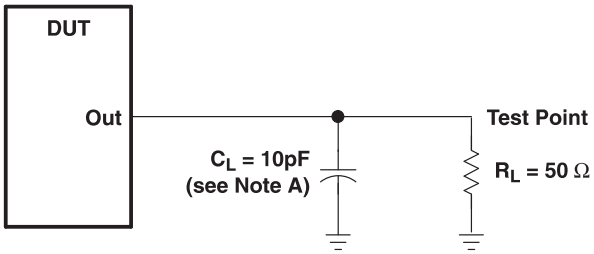


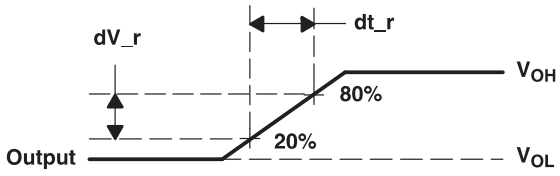
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



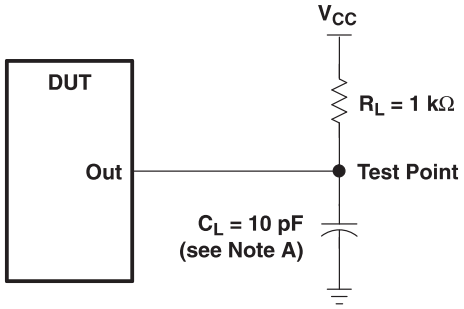
LOAD CIRCUIT
LOW-TO-HIGH SLEW-RATE MEASUREMENT



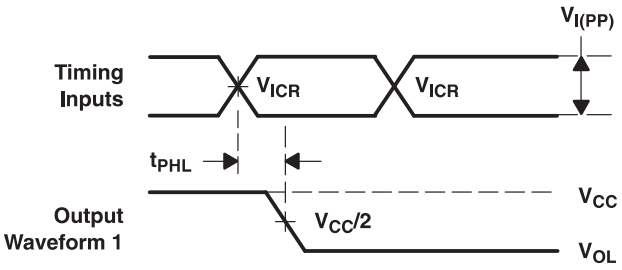
VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

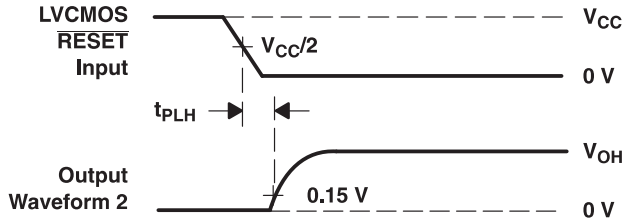
Figure 2. Data Output Slew-Rate Measurement Information



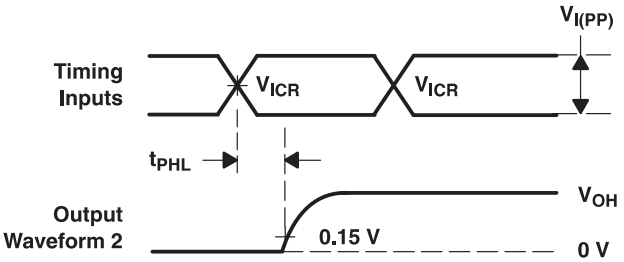
LOAD CIRCUIT



VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(HIGH-TO-LOW)



VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(LOW-TO-HIGH)



VOLTAGE WAVEFORMS
OPEN-DRAIN OUTPUT TRANSITION TIME
(LOW-TO-HIGH)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
C. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Error Output Load Circuit and Voltage Waveforms

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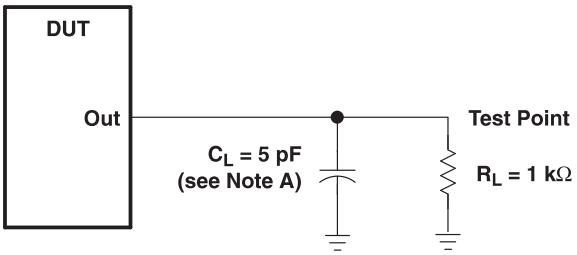
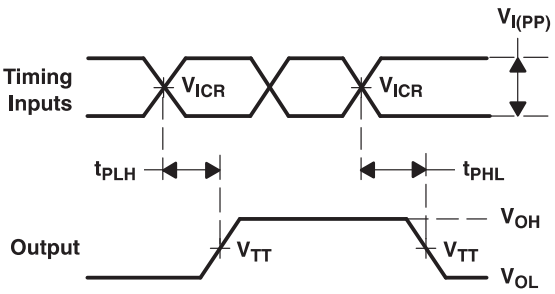
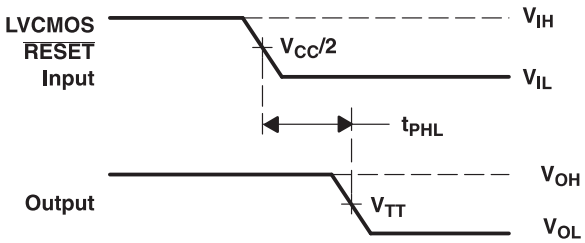


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
C. $V_{REF} = V_{TT} = V_{CC}/2$
D. $V_{IH} = V_{REF} + 250$ mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
E. $V_{IL} = V_{REF} – 250$ mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
F. $V_{I(PP)}$ = 600 mV
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Partial-Parity-Out Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

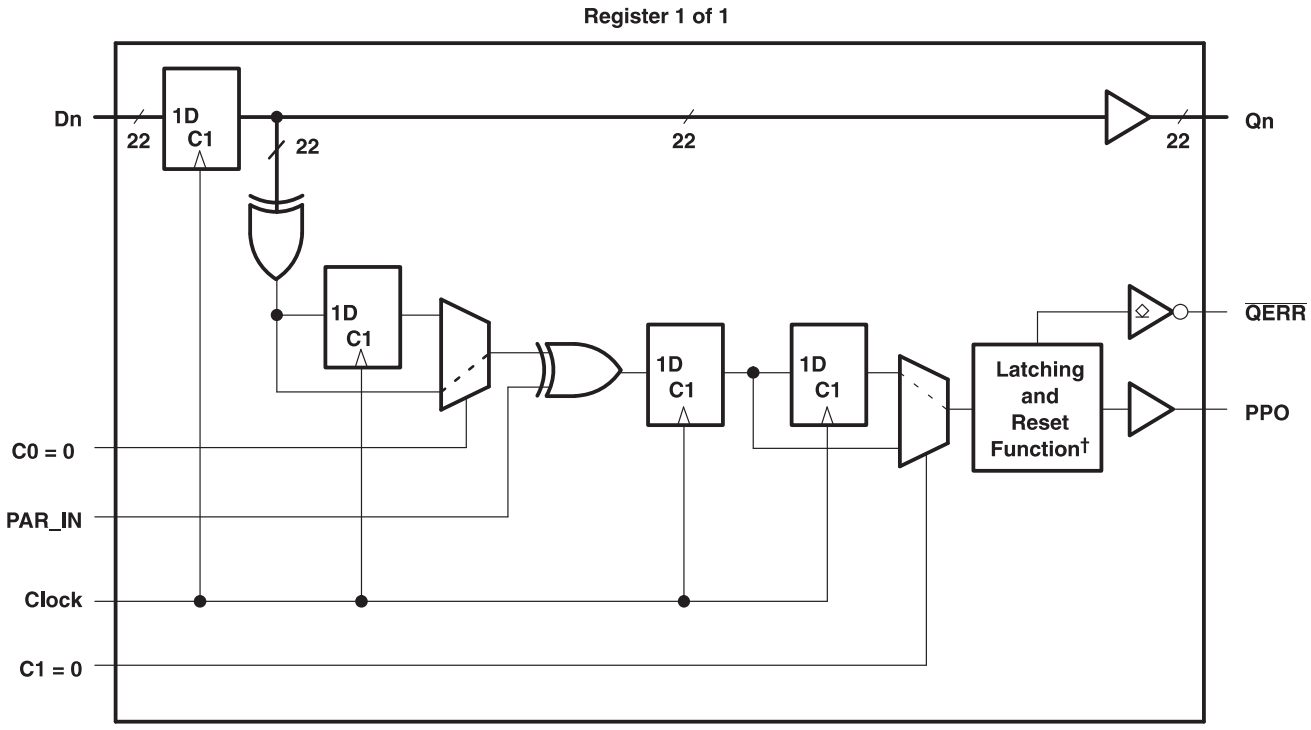
The typical values below are for standard raw cards. Test equipment used was the JEDEC register validation board using pattern 0x43, 0x4F, and 0x5A.

Table 1. Raw Card Values (1) (2)

RAW CARD	t_{pdmss}		OVERSHOOT
	MIN	MAX	
A/F	1.2 ns	1.6 ns	140 mV
B/G	1.3 ns	2.0 ns	430 mV
C/H	1.3 ns	2.0 ns	430 mV

(1) All values are valid under nominal conditions (1.8V) and minimum/maximum of typical signals on one typical DIMM.
(2) Measurements include all jitter and ISI effects.

SN74SSTEB32866 Used as a Single Device in the 1:1 Register Configuration; C0 = 0, C1 = 0



† This function holds the error for two cycles. For details, see the parity logic diagram.

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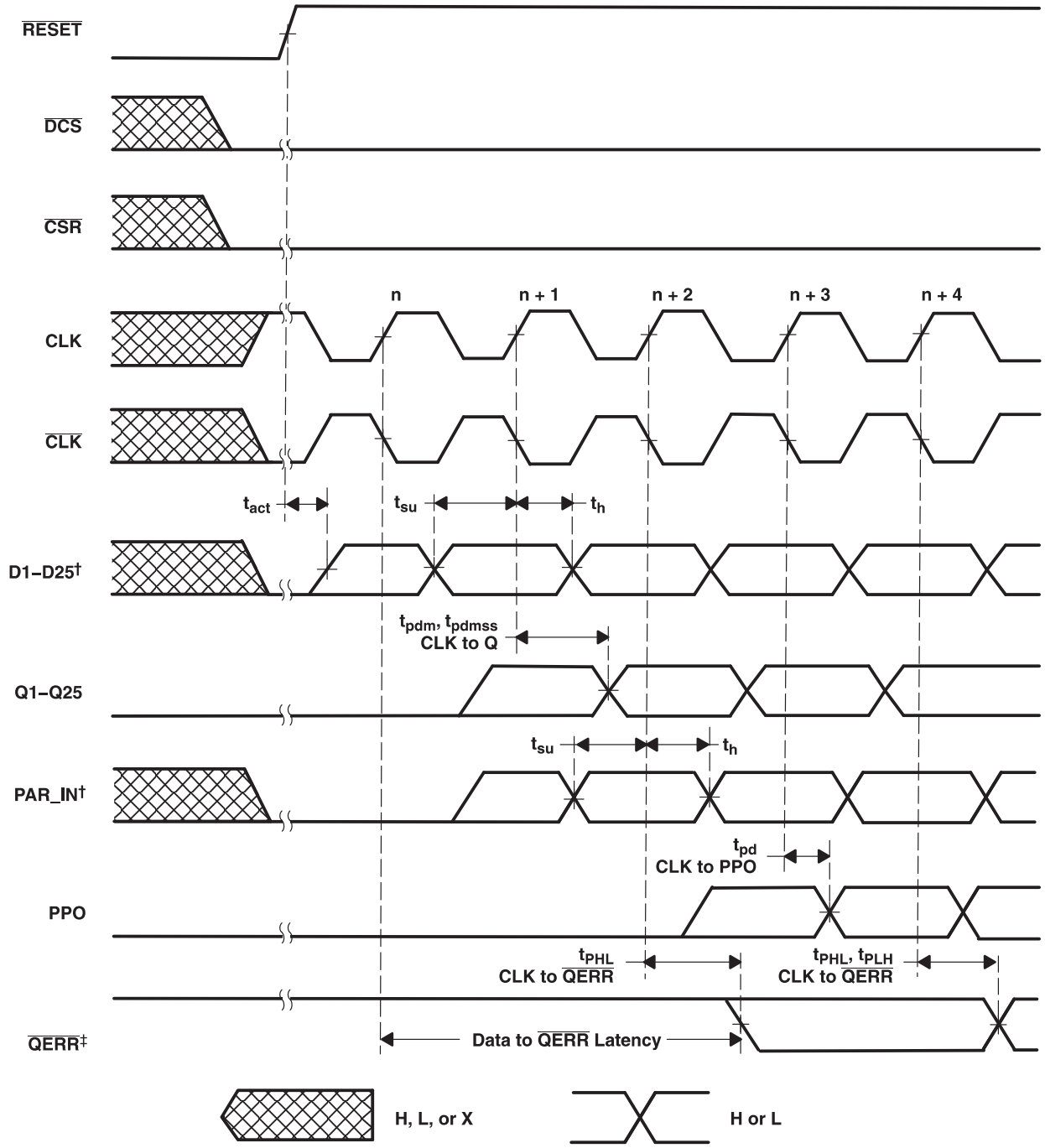
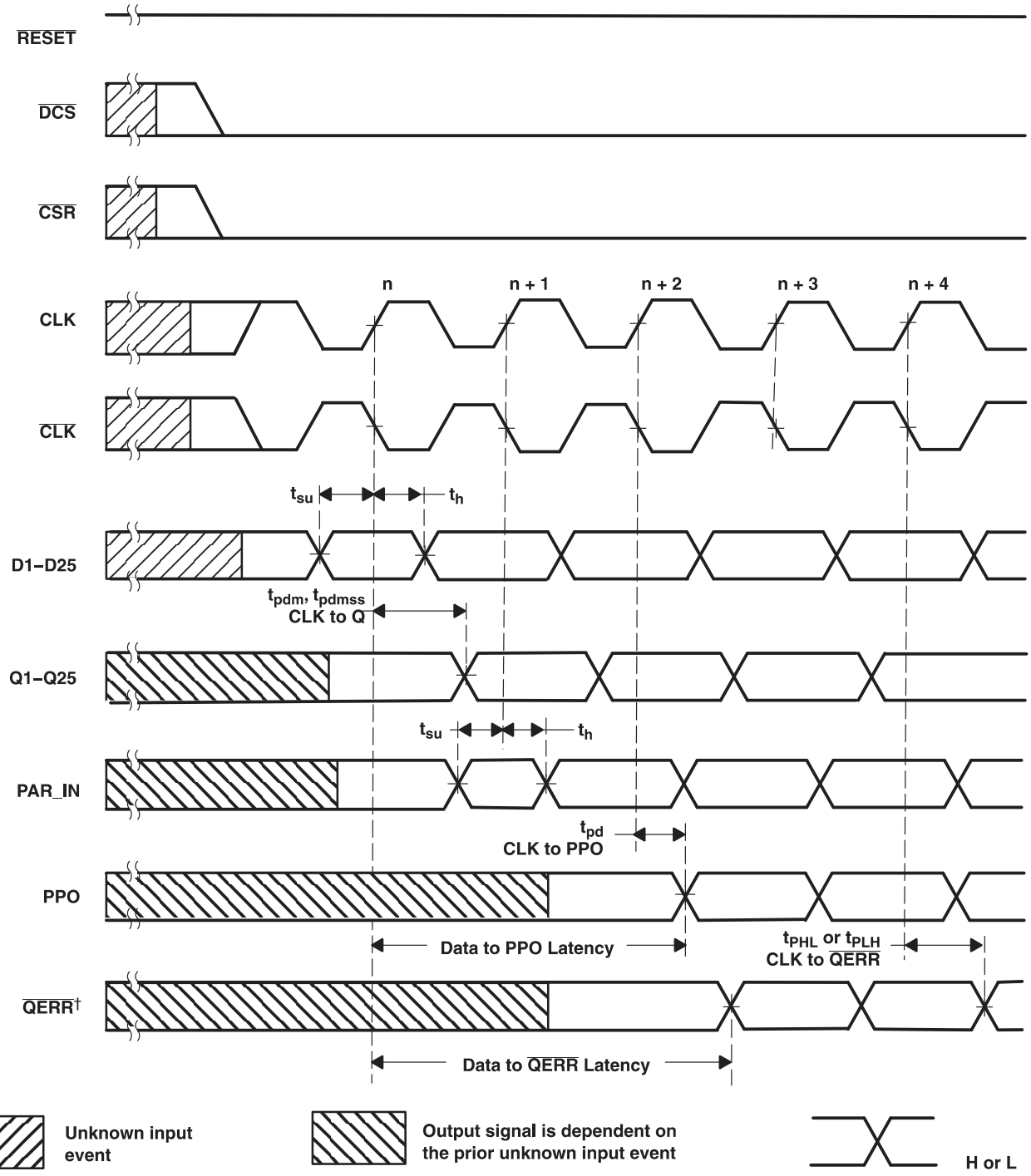
Timing Diagram for SN74SSTEB32866 Used as a Single Device; C0 = 0, C1 = 0 ($\overline{\text{RESET}}$ Switches From L to H)



† After $\overline{\text{RESET}}$ is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

‡If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

Timing Diagram for SN74SSTEB32866 Used as a Single Device; C0 = 0, C1 = 0 ($\overline{\text{RESET}}$ = H)



† If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

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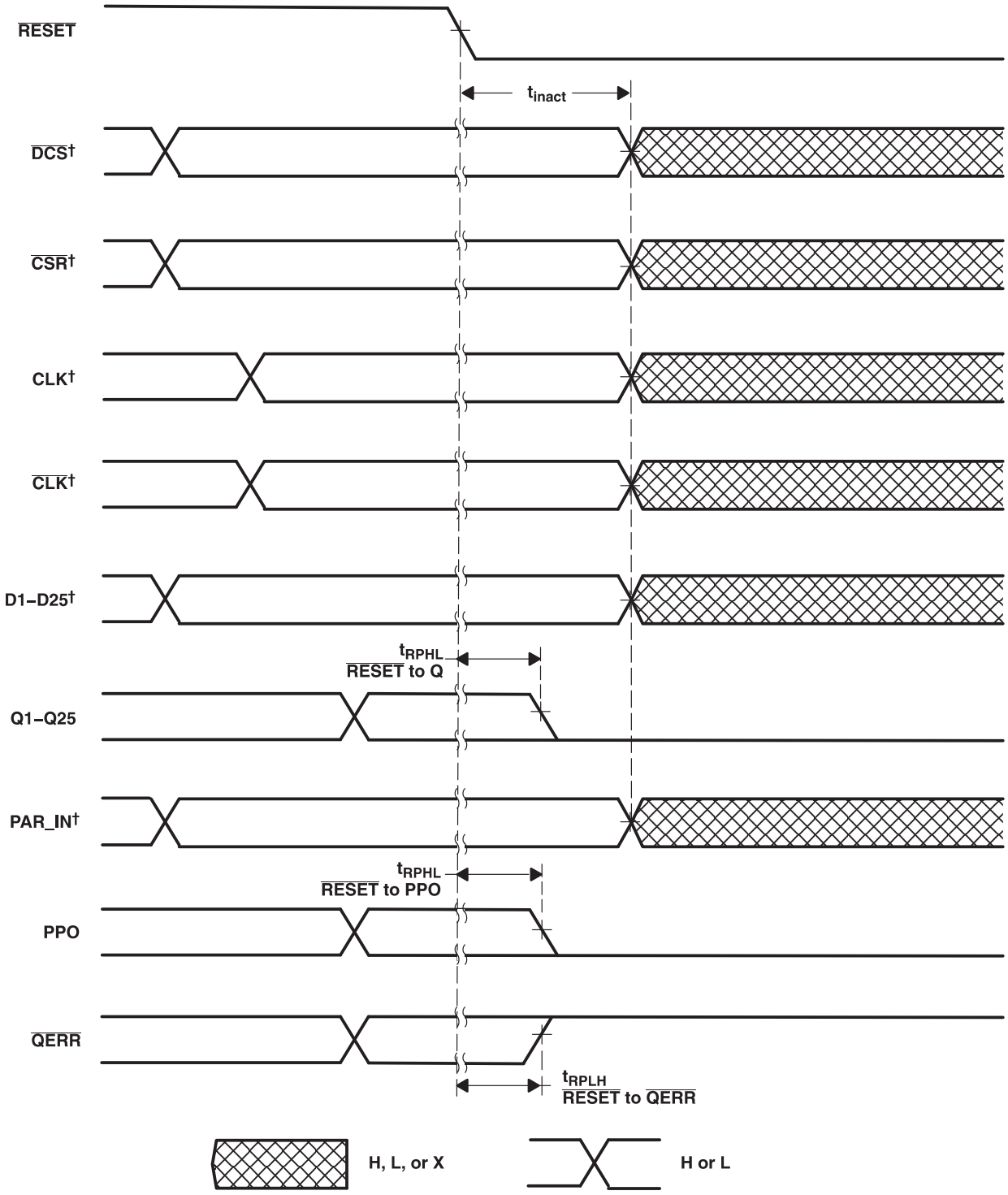
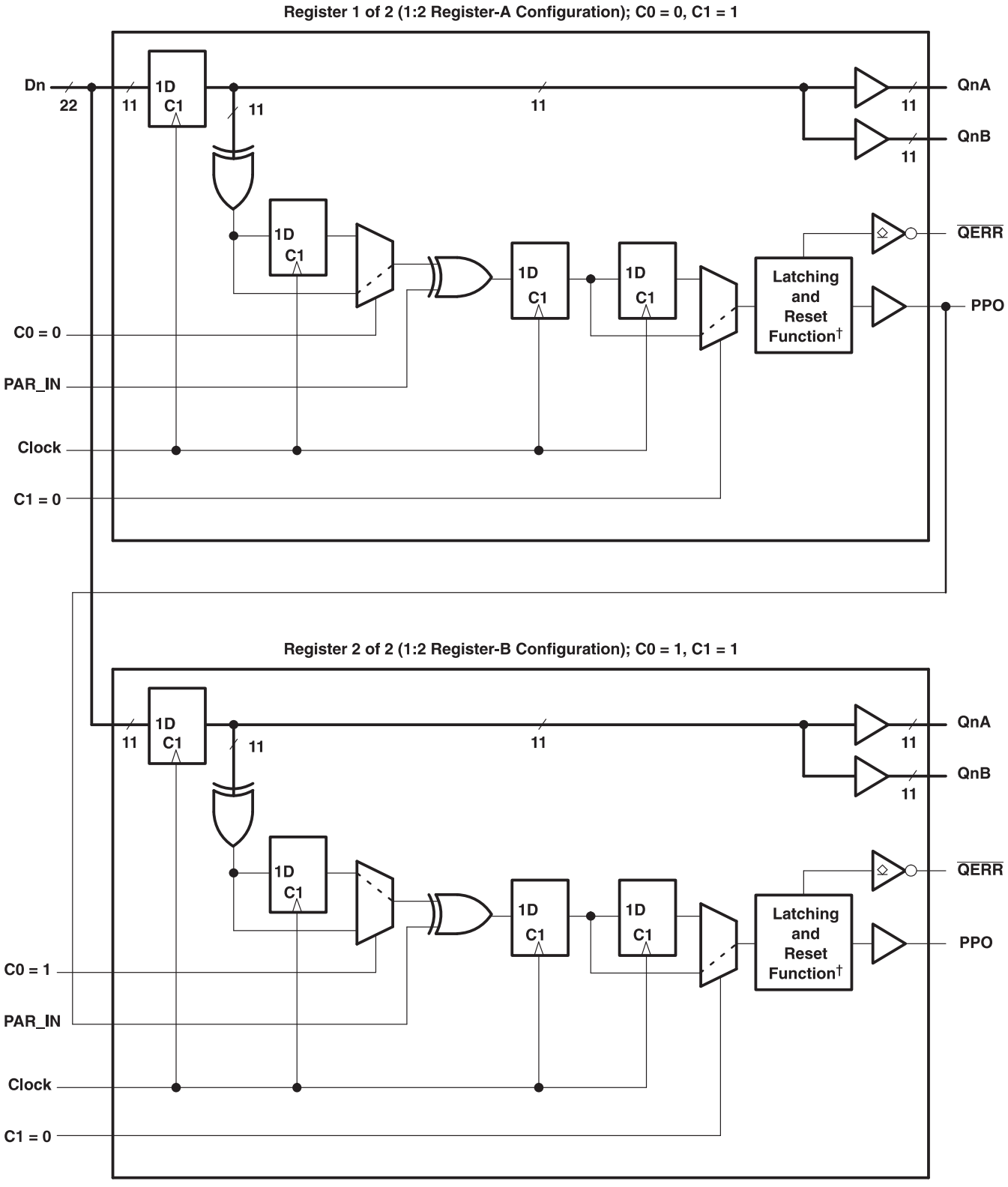
Timing Diagram for SN74SSTEB32866 Used as a Single Device; C0 = 0, C1 = 0 ($\overline{\text{RESET}}$ Switches From = H to L)



† After $\overline{\text{RESET}}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

SN74SSTEB32866 Used in Pair in the 1:2 Register Configuration



† This function holds the error for two cycles. For details, see the parity logic diagram.

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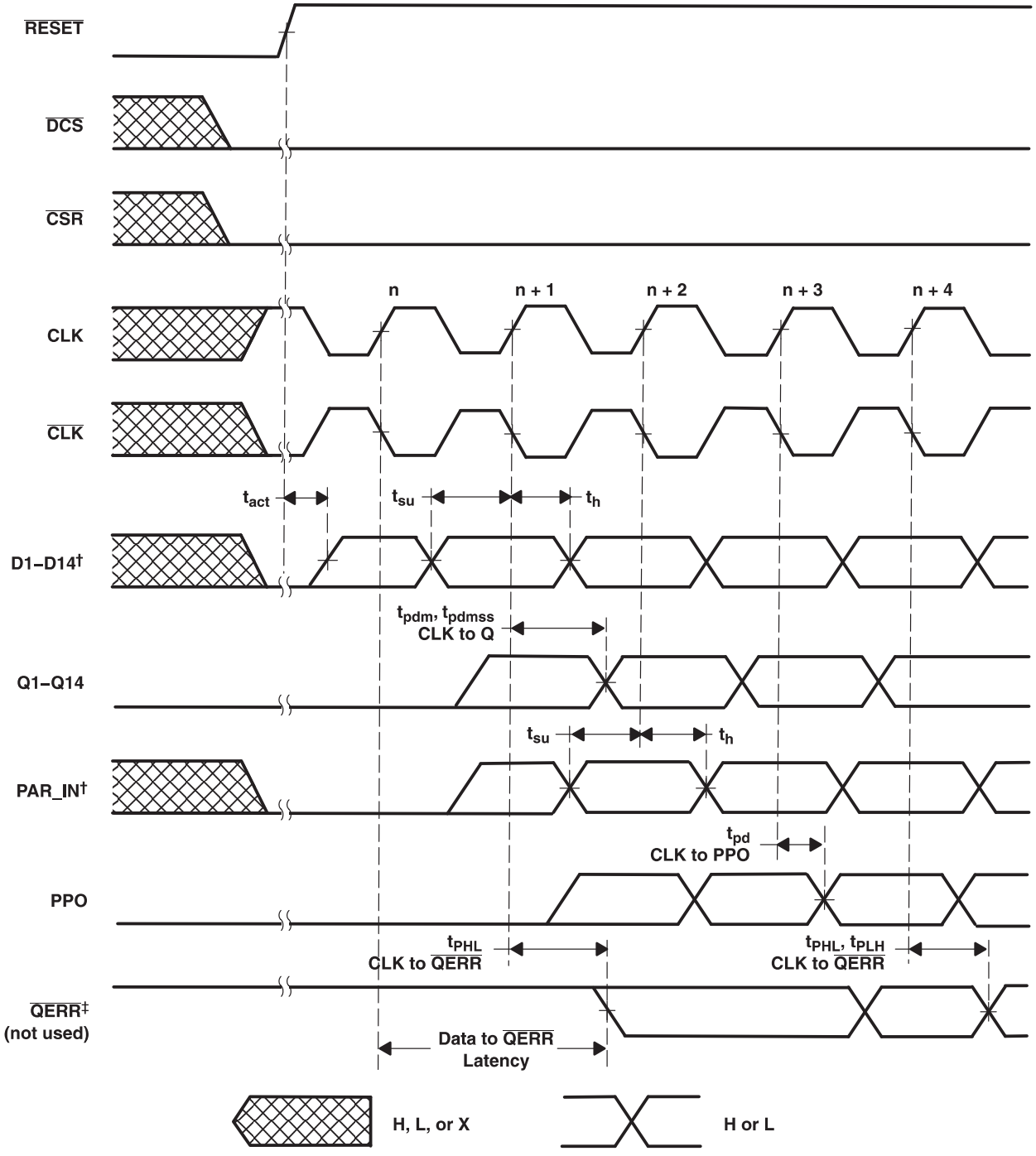
Timing Diagram for the First SN74SSTEB32866 (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 ($\overline{\text{RESET}}$ Switches From L to H)



† After $\overline{\text{RESET}}$ is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

‡ If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n + 1 clock pulse, and it will be valid on the n + 2 clock pulse.

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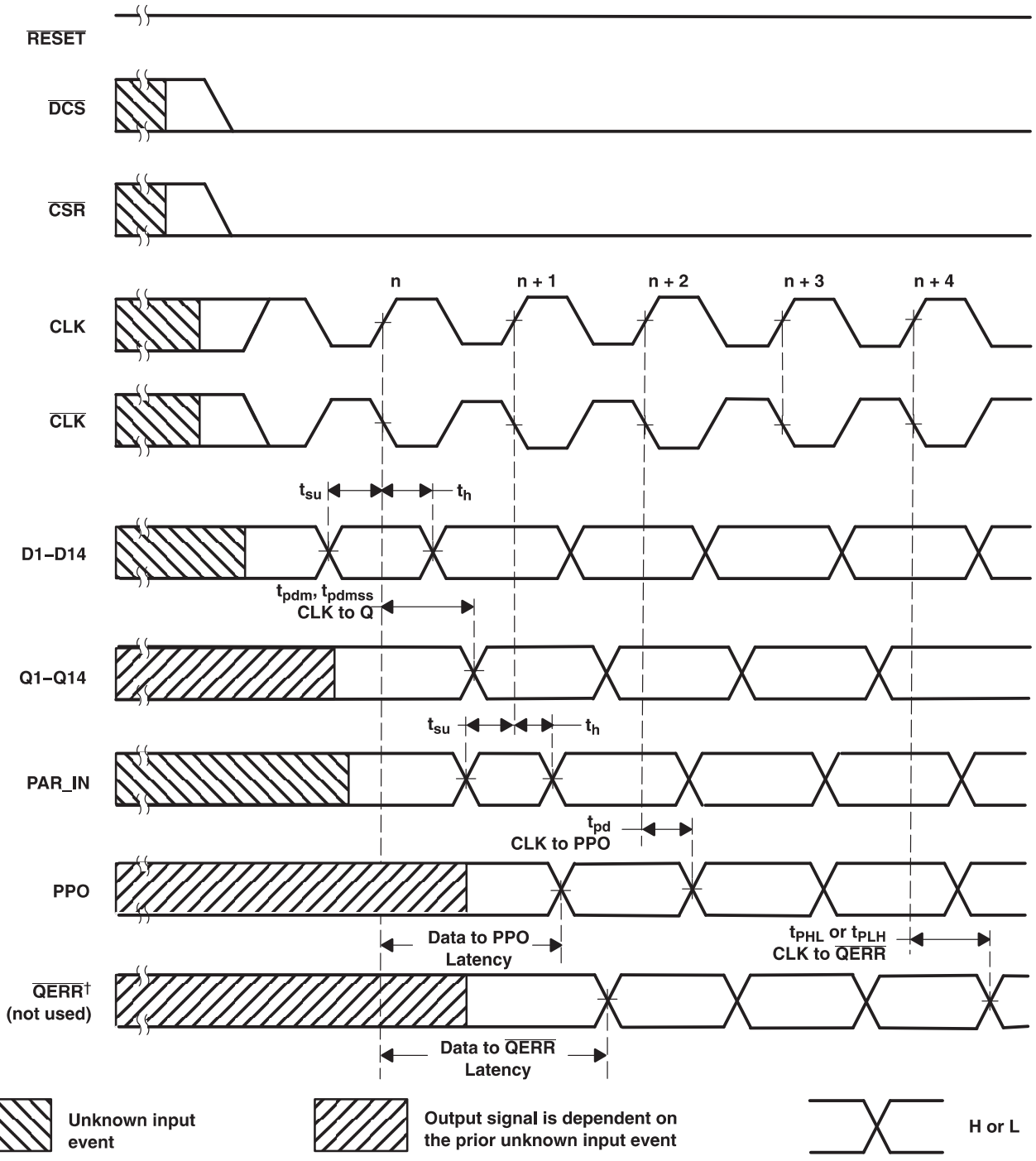
Timing Diagram for the First SN74SSTEB32866 (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 ($\overline{RESET}$ = H)



† If the data is clocked in on the n clock pulse, the $\overline{QERR}$ output signal will be generated on the n + 1 clock pulse, and it will be valid on n + 2 clock pulse. If an error occurs and the $\overline{QERR}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{RESET}$ is driven low.

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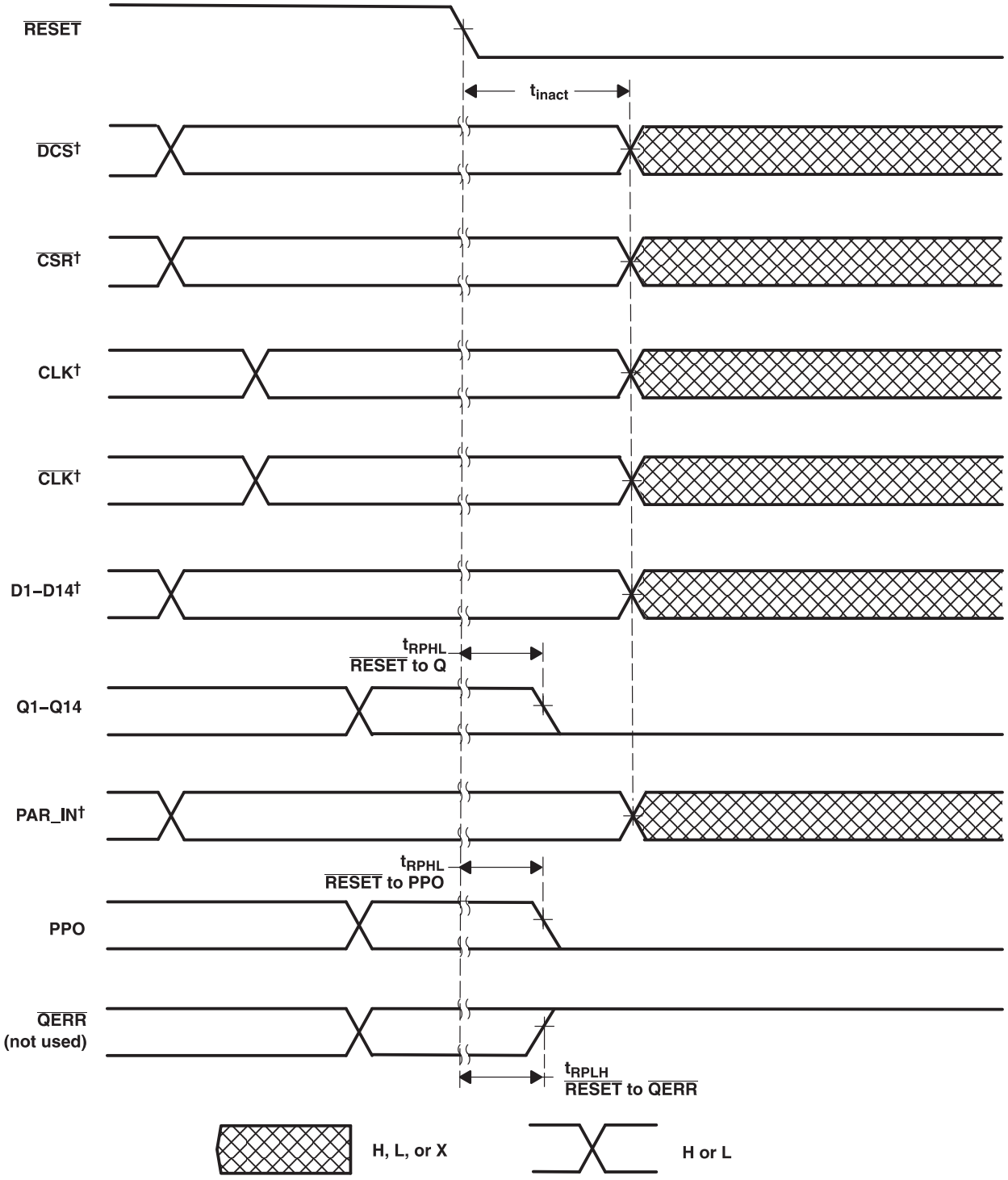
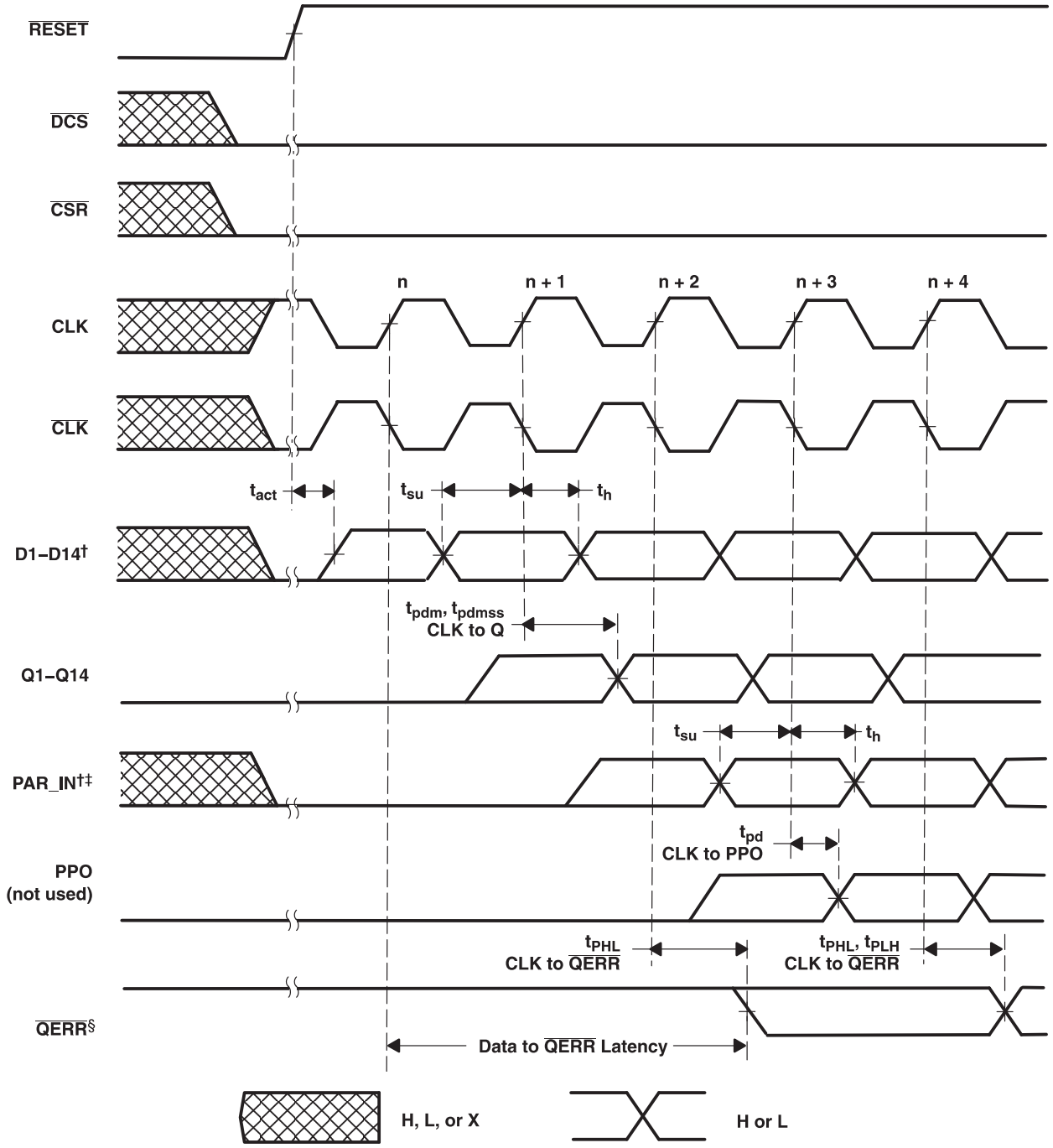
Timing Diagram for the First SN74SSTEB32866 (1:2 Register-A Configuration) Device Used in Pair; C0 = 0, C1 = 1 ($\overline{RESET}$ = Switches From H to L)



† After $\overline{RESET}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

Timing Diagram for the Second SN74SSTEB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 (RESET = Switches From L to H)



† After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid false error.

‡PAR_IN is driven from PPO of the first SN74SSTUB32866 device.

§ If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

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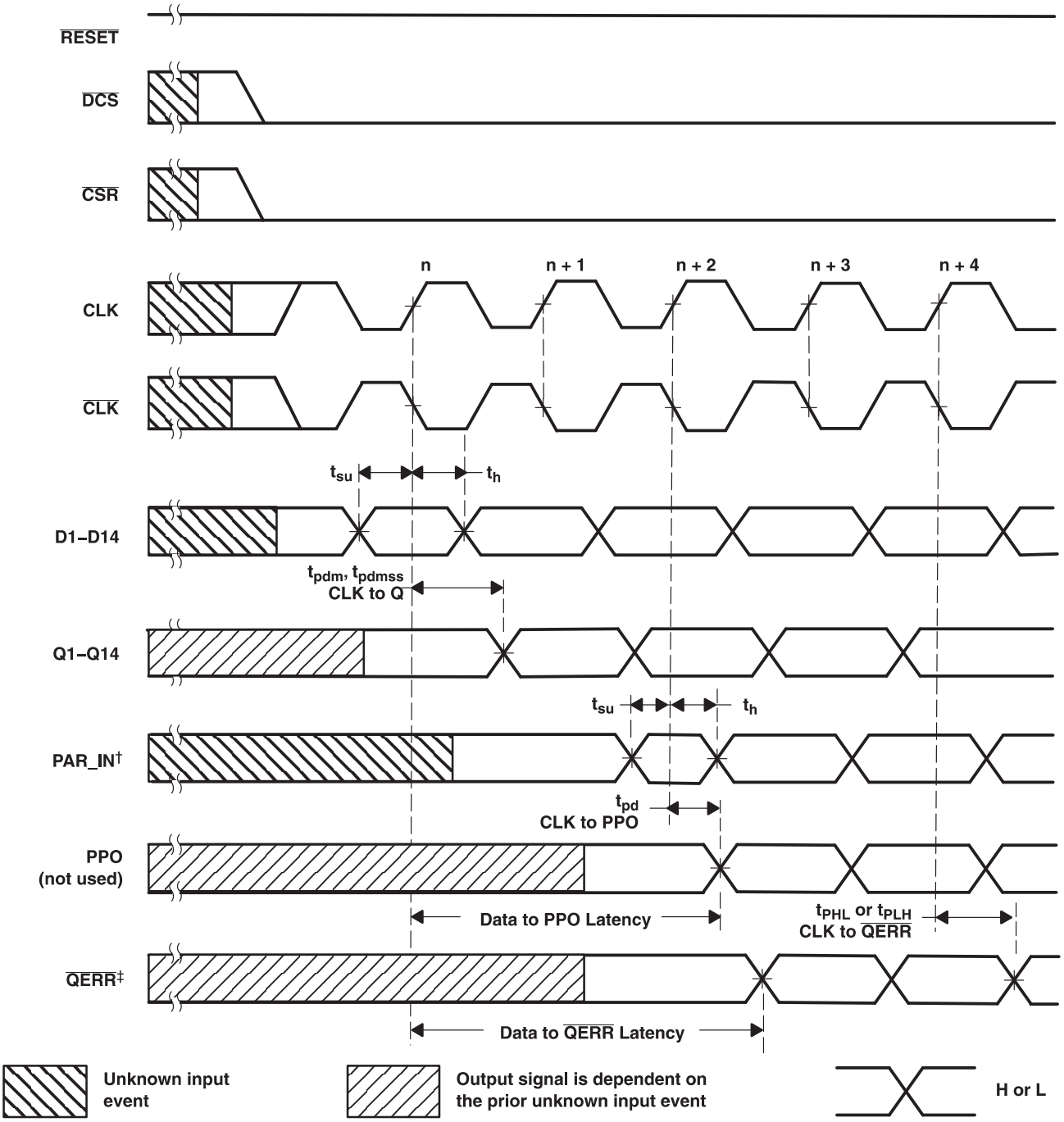
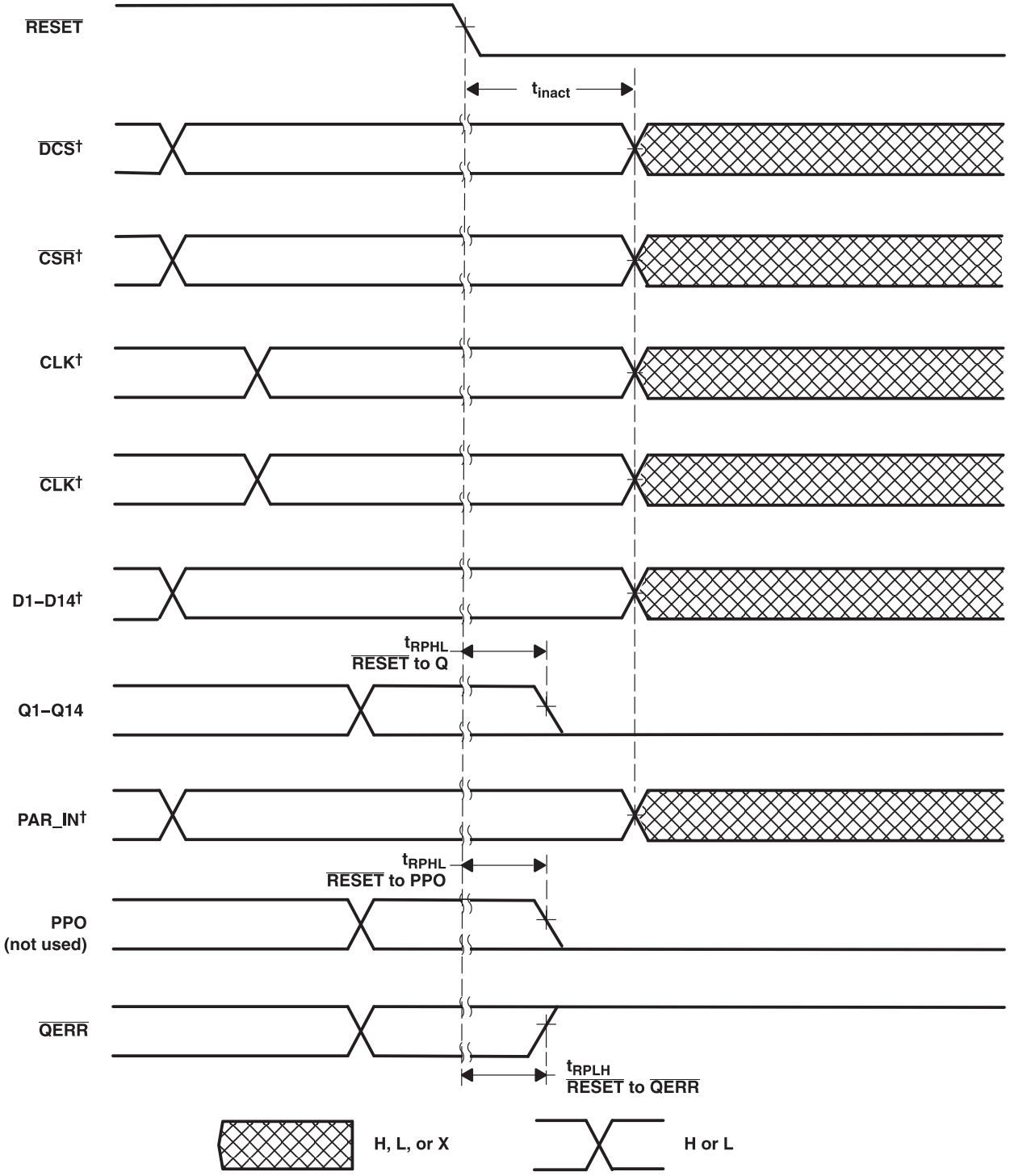
Timing Diagram for the Second SN74SSTEB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 (RESET = H)



† PAR_IN is driven from PPO of the first SN74SSTUB32866 device.

‡ If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

Timing Diagram for the Second SN74SSTEB32866 (1:2 Register-B Configuration) Device Used in Pair; C0 = 1, C1 = 1 ($\overline{RESET}$ = Switches From H to L)



† After $\overline{RESET}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74SSTEB32866ZWLR	Active	Production	BGA (ZWL) | 96	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	SEB866
SN74SSTEB32866ZWLR.B	Active	Production	BGA (ZWL) | 96	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	SEB866

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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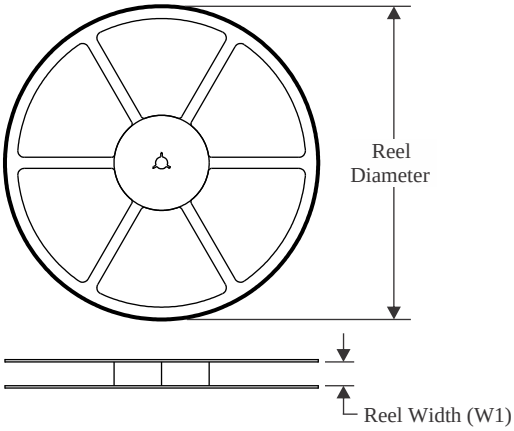
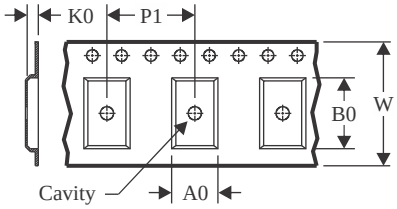
TAPE AND REEL INFORMATION

REEL DIMENSIONS

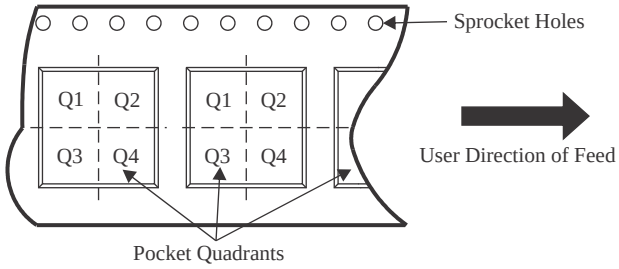


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

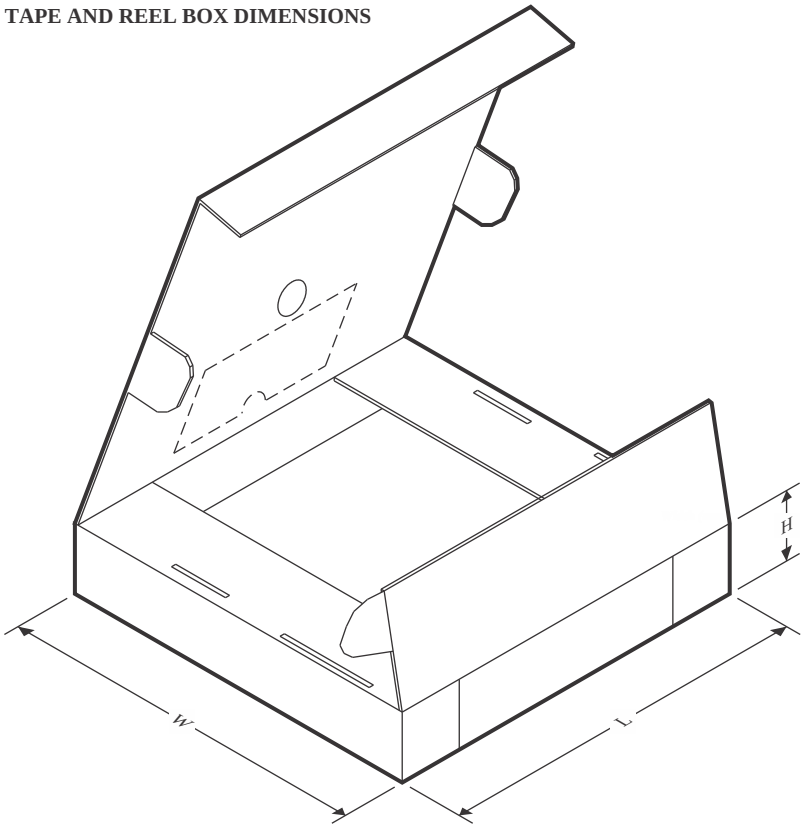
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

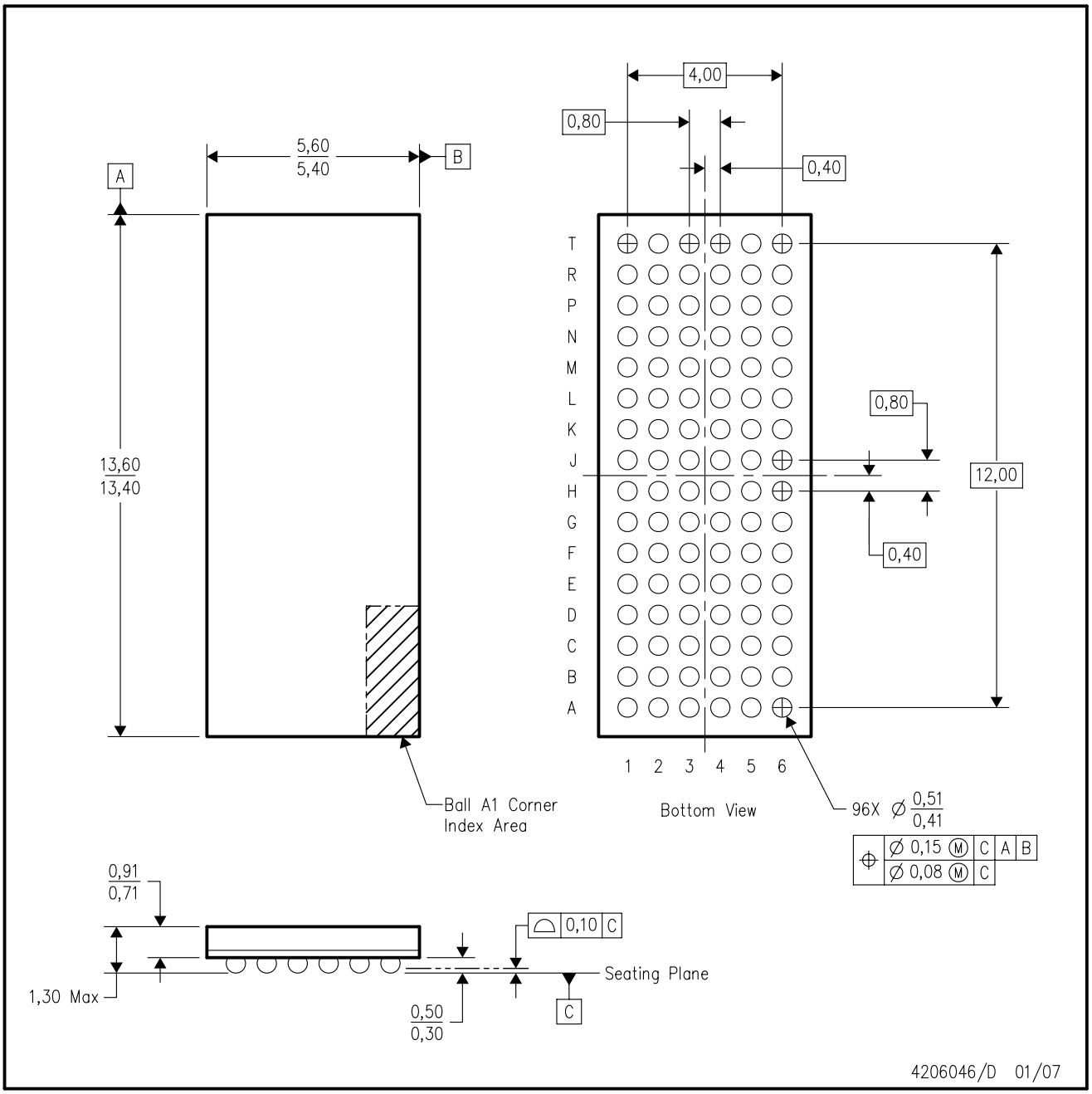
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTEB32866ZWLR	BGA	ZWL	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTEB32866ZWLR	BGA	ZWL	96	1000	350.0	350.0	43.0



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is lead–free. Refer to the 96 GWL package (drawing 4206045) for tin–lead (SnPb).

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