SNx4AHC138 3 线路至 8 线路解码器/多路信号分离器

1 特性

- 工作范围为 2V 至 5.5V V_{CC}
- 专门为高速存储器解码器和数据传输系统设计
- 包含三个使能输入以简化级联和/或数据接收
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求：
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

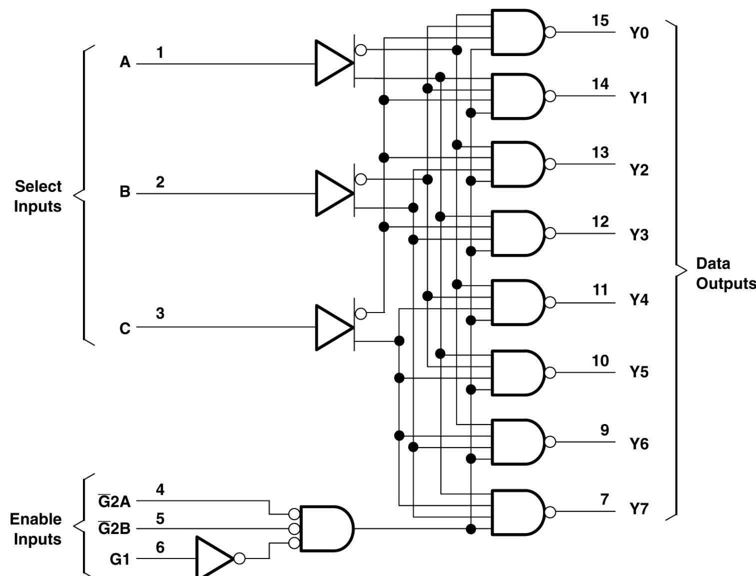
2 说明

SNx4AHC138 解码器/多路信号分离器设计用于需要极短传播延迟时间的高性能存储器解码和数据路由应用。在高性能存储器系统中，可使用此类解码器来尽可能地消除系统解码的影响。与使用高速使能电路的高速存储器一同使用时，这些解码器的延迟时间和存储器的使能时间通常小于存储器的典型存取时间。这意味着解码器引起的有效系统延迟可以忽略不计。

器件信息

器件型号	封装 (1)	封装尺寸 (2)	本体尺寸(3)
SN74AHC138	RGY（VQFN，16）	4mm x 3.5mm	4mm x 3.5mm
	N（PDIP，16）	19.3mm × 9.4mm	19.32mm x 6.35mm
	D（SOIC，16）	9.9mm × 6mm	9.90mm x 3.90mm
	NS（SOP，16）	10.2mm x 7.8mm	10.20mm x 5.30mm
	DB（SSOP，16）	6.2mm × 7.8mm	6.20mm x 5.30mm
	PW（TSSOP，16）	5mm × 6.4mm	5.00mm x 4.40mm
	DGV（TVSOP，16）	3.6mm x 6.4mm	3.6mm x 4.4mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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3 引脚配置和功能

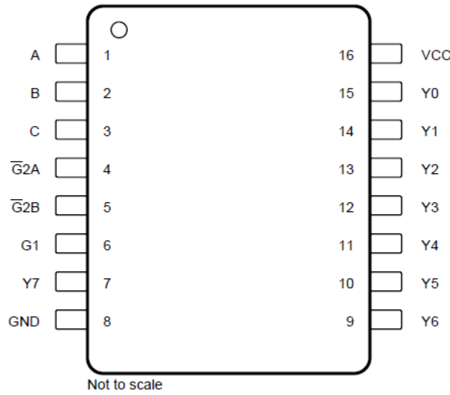


图 3-1. D、DB、DGV、N、NS 或 PW 封装，16 引脚 SOIC、SSOP、TVSOP、PDIP、SOP 或 TSSOP（顶视图）

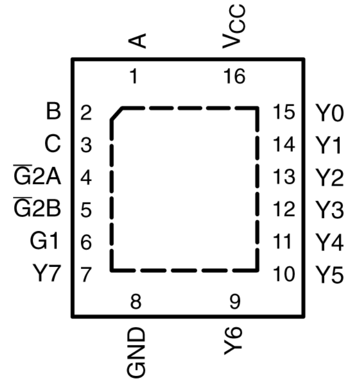
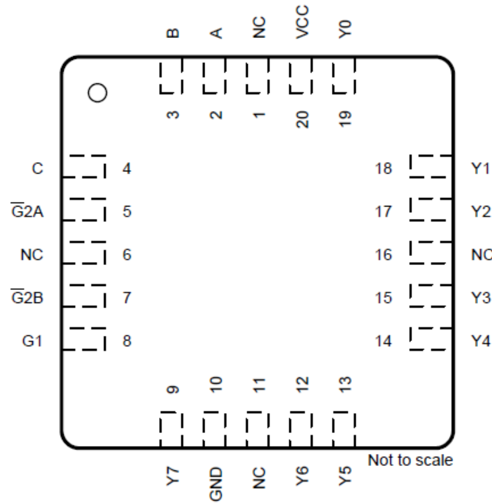


图 3-2. RGY 封装，16 引脚 VQFN（顶视图）



NC：无内部连接

图 3-3. FK 封装，20 引脚 LCCC（顶视图）

表 **3-1.** 引脚功能

引脚		类型(1)	说明
名称	编号		
A_0	1	I	地址选择 0
A_1	2	I	地址选择 1
A_2	3	I	地址选择 2
$\overline{G}_0$	4	I	输出选通 0，低电平有效
$\overline{G}_1$	5	I	输出选通 1，低电平有效
G_2	6	I	输出选通 2
Y_7	7	O	输出 7
GND	8	G	接地
Y_6	9	O	输出 6
Y_5	10	O	输出 5
Y_4	11	O	输出 4
Y_3	12	O	输出 3
Y_2	13	O	输出 2
Y_1	14	O	输出 1
Y_0	15	O	输出 0
V_{CC}	16	P	正电源
散热焊盘(2)			散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源。

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出，P = 电源，G = 接地。
(2) 仅限 WBQB 封装。

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4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I (2)	输入电压范围		-0.5	7	V
V_O (2)	输出电压范围		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	(V_I < 0)		-20	mA
I_{OK}	输出钳位电流	（V_O < 0 或 V_O > V_{CC}）		±20	mA
I_O	持续输出电流	（V_O = 0 至 V_{CC}）		±25	mA
	通过 V_{CC} 或 GND 的持续电流			±75	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 应力超出“绝对最大额定值”下所列的值可能会对器件造成永久损坏。这些仅为在应力额定值下的工作情况，对于额定值下的器件的功能性操作或者在超出“推荐的操作条件”下的任何其它情况，在此并未说明。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

4.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54AHC138		SN74AHC138		单位
			最小值	最大值	最小值	最大值	
V_{CC}	电源电压		2	5.5	2	5.5	V
V_{IH}	高电平输入电压	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	低电平输入电压	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	输入电压			0 5.5		0 5.5	V
V_O	输出电压		0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2 V		-50		-50	mA
		V_{CC} = 3.3 V ± 0.3 V		-4		-4	mA
		V_{CC} = 5 V ± 0.5 V		-8		-8	
I_{OL}	低电平输出电流	V_{CC} = 2 V		50		50	mA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	输入转换上升或下降速率	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	自然通风条件下的工作温度范围		-55	125	-40	85	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢变化或悬空的影响*，文献编号 SCBA004。

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4.3 热性能信息

热性能指标[(1)]		SN74AHC138							单位
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16							
$R_{\theta JA}$	结至环境热阻	93.8	82	120	67	64	135.9	39	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *半导体和 IC 封装热指标* 应用报告。

4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54AHC138		SN74AHC138		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = −50 μA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I_{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I=5.5 V 或 GND	0 V 至 5.5 V			±0.1		±1[(1)]		±1	μA
I_{CC}	V_I = V_{CC} 或 GND， I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} 或 GND	5 V		2	10				10	pF

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试（在 V_{CC} = 0V 时）。

4.5 开关特性： V_{CC} = 3.3V ± 0.3V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 3.3V ± 0.3V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	到（输出）	负载电容	T_A = 25°C			SN54AHC138		SN74AHC138		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A、B、C	任一 Y	C_L = 15pF		8.2[(1)]	11.4[(1)]	1[(1)]	13[(1)]	1	13	ns
t_{PHL}					8.2[(1)]	11.4[(1)]	1[(1)]	13[(1)]	1	13	
t_{PLH}	G1	任一 Y	C_L = 15pF		8.1[(1)]	12.8[(1)]	1[(1)]	15[(1)]	1	15	ns
t_{PHL}					8.1[(1)]	12.8[(1)]	1[(1)]	15[(1)]	1	15	
t_{PLH}	$\overline{G2A}$，$\overline{G2B}$	任一 Y	C_L = 15pF		8.2[(1)]	11.4[(1)]	1[(1)]	13.5[(1)]	1	13.5	ns
t_{PHL}					8.2[(1)]	11.4[(1)]	1[(1)]	13.5[(1)]	1	13.5	
t_{PLH}	A、B、C	任一 Y	C_L = 50pF		10	15.8	1	18	1	18	ns
t_{PHL}					10	15.8	1	18	1	18	
t_{PLH}	G1	任一 Y	C_L = 50pF		10.6	16.3	1	18.5	1	18.5	ns
t_{PHL}					10.6	16.3	1	18.5	1	18.5	
t_{PLH}	$\overline{G2A}$，$\overline{G2B}$	任一 Y	C_L = 50pF		10.7	14.9	1	17	1	17	ns
t_{PHL}					10.7	14.9	1	17	1	17	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

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4.6 开关特性： V_{CC} = 5V ± 0.5V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	到（输出）	负载电容	T_A = 25°C			SN54AHC138		SN74AHC138		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A、B、C	任一 Y	C_L = 15pF		5.7[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	ns
t_{PHL}					5.7[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	
t_{PLH}	G1	任一 Y	C_L = 15pF		5.6[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	ns
t_{PHL}					5.6[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	
t_{PLH}	$\overline{G2A}$，$\overline{G2B}$	任一 Y	C_L = 15pF		5.8[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	ns
t_{PHL}					5.8[(1)]	8.1[(1)]	1[(1)]	9.5[(1)]	1	9.5	
t_{PLH}	A、B、C	任一 Y	C_L = 50pF		7.2	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.2	10.1	1	11.5	1	11.5	
t_{PLH}	G1	任一 Y	C_L = 50pF		7.1	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	1	11.5	
t_{PLH}	$\overline{G2A}$，$\overline{G2B}$	任一 Y	C_L = 50pF		7.3	10.1	1	11.5	1	11.5	ns
t_{PHL}					7.3	10.1	1	11.5	1	11.5	

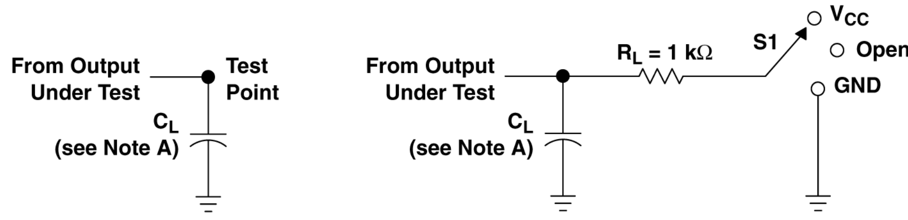
(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

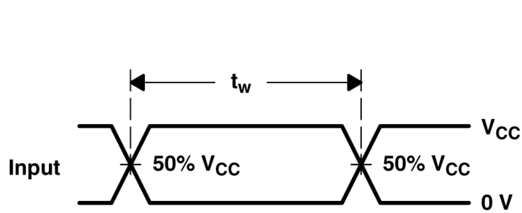
4.7 工作特性

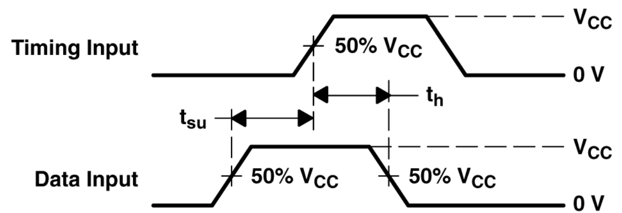
V_{CC} = 5V，T_A = 25°C

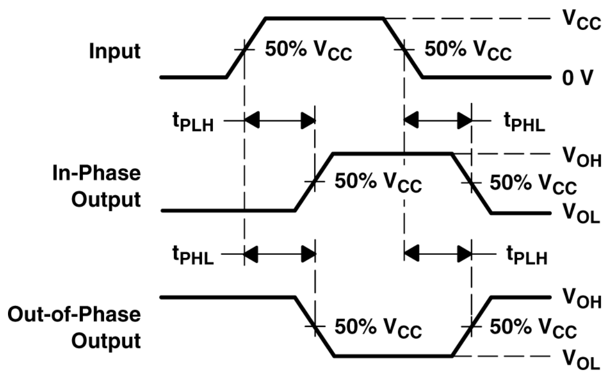
参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	无负载，	f = 1 MHz	13	pF

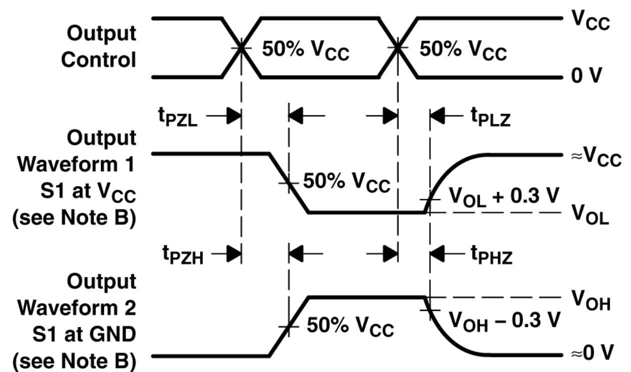
5 参数测量信息











A. C_L 包括探头和夹具电容。
B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。
C. 所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50 Ω，t_r ≤ 3 ns，t_f ≤ 3 ns。
D. 一次测量一个输出，每次测量一个输入转换。
E. 并非所有参数和波形都适用于所有器件。

图 5-1. 负载电路和电压波形

测试	S1
t_{PLH}/t_{PHL}	开路
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
漏极开路	V_{CC}

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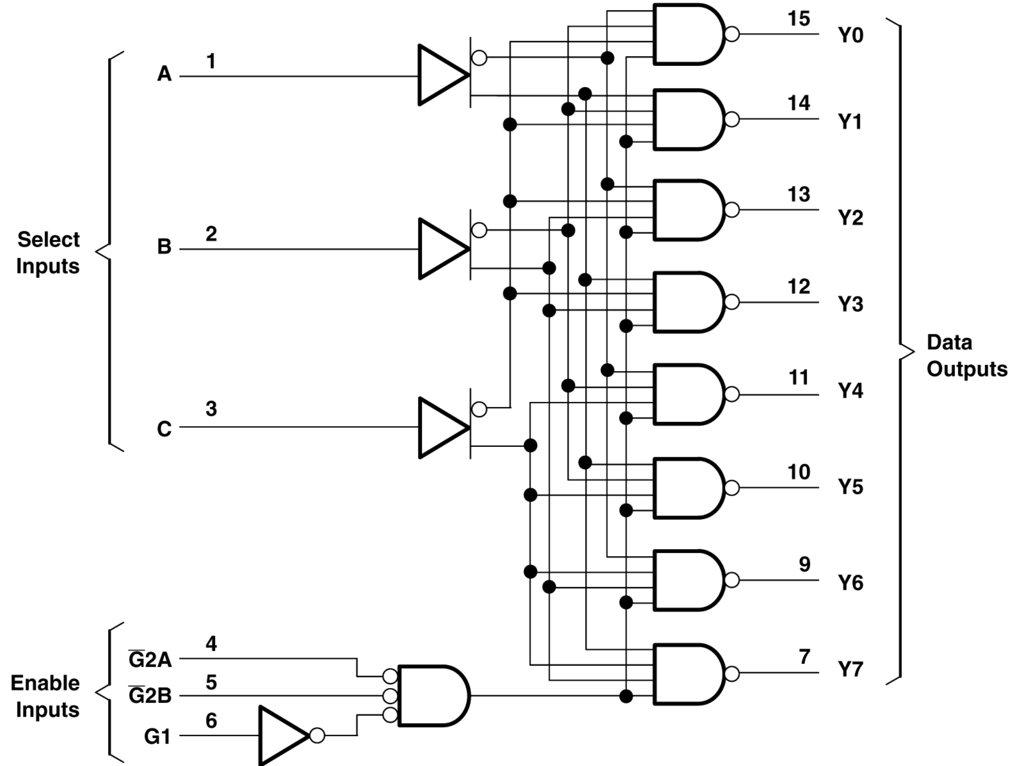
6 详细说明

6.1 概述

二进制选择输入和三个使能输入条件可从八条输出线路中选择其中一条。两个低电平有效使能输入和一个高电平有效使能输入可在扩展时减少对外部门电路或反相器的需要。无需外部反相器即可实现 24 线解码器，并且 32 线解码器只需要一个反相器。使能输入可用作多路信号分离应用的数据输入。

6.2 功能方框图



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

6.3 功能表

使能输入			选择输入			输出							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 应用信息

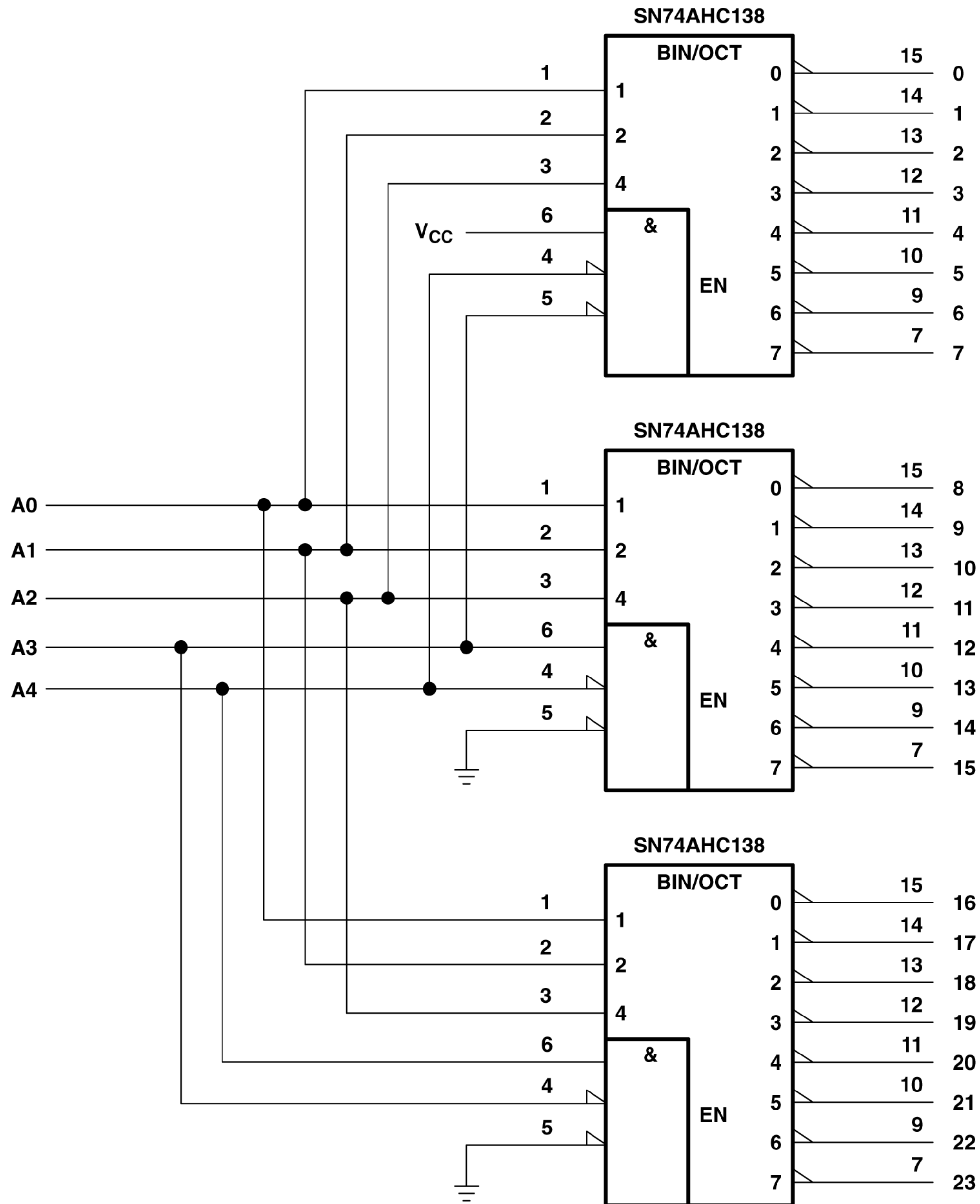


图 7-1. 24 位解码方案

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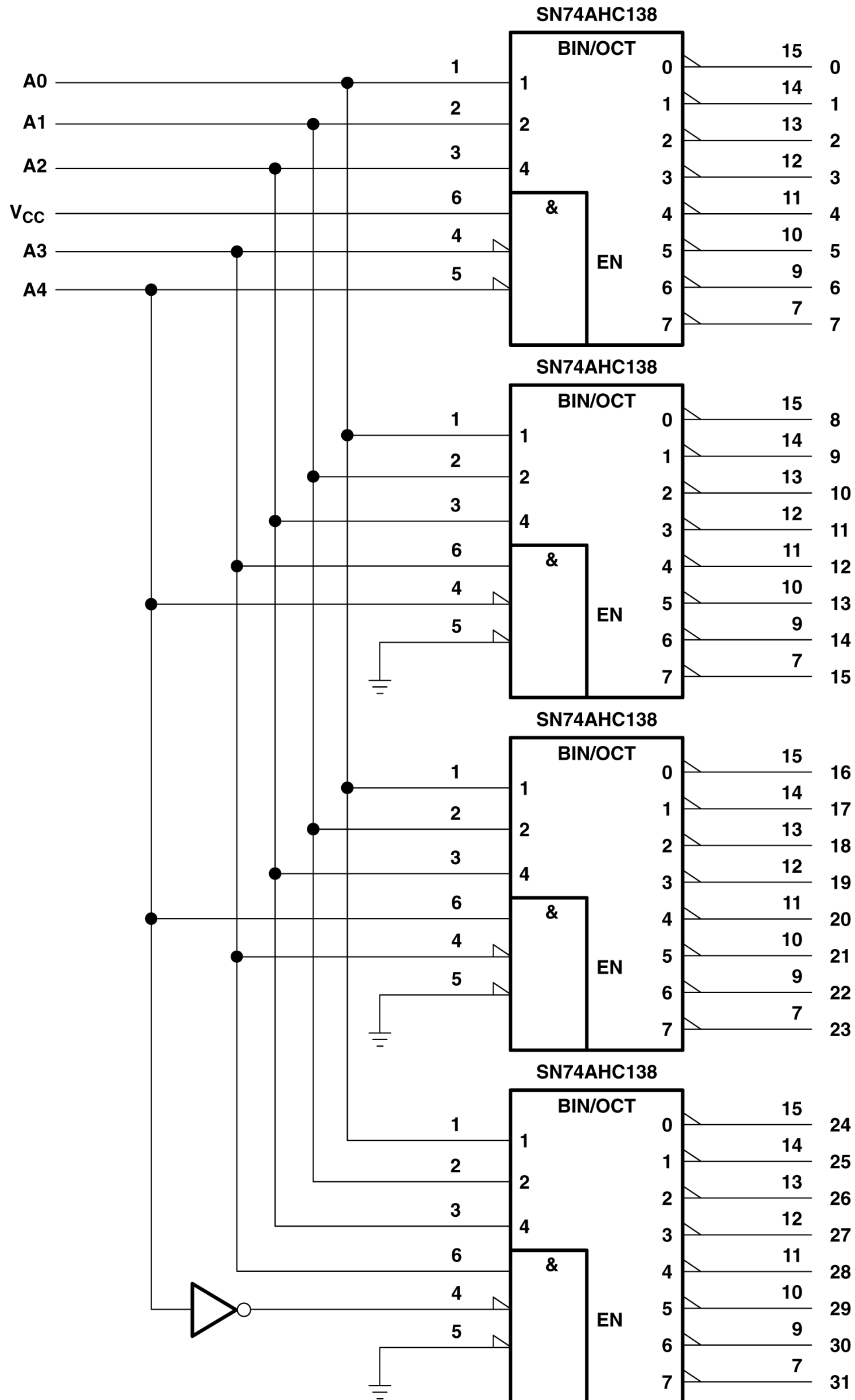

图 **7-2. 32** 位解码方案

7.2 电源相关建议

7.3 布局

7.3.1 布局指南

使用多输入和多通道逻辑器件时，输入不得悬空。在许多情况下，数字逻辑器件的功能或部分功能未被使用；例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时。此类未使用的输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的操作状态。数字逻辑器件的所有未使用输入必须连接到由输入电压规范定义的逻辑高电平电压或逻辑低电平电压，以防止其悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，输入连接到 GND 或 V_{CC}，以对逻辑功能更有意义或更方便者为准。

7.3.2 布局示例

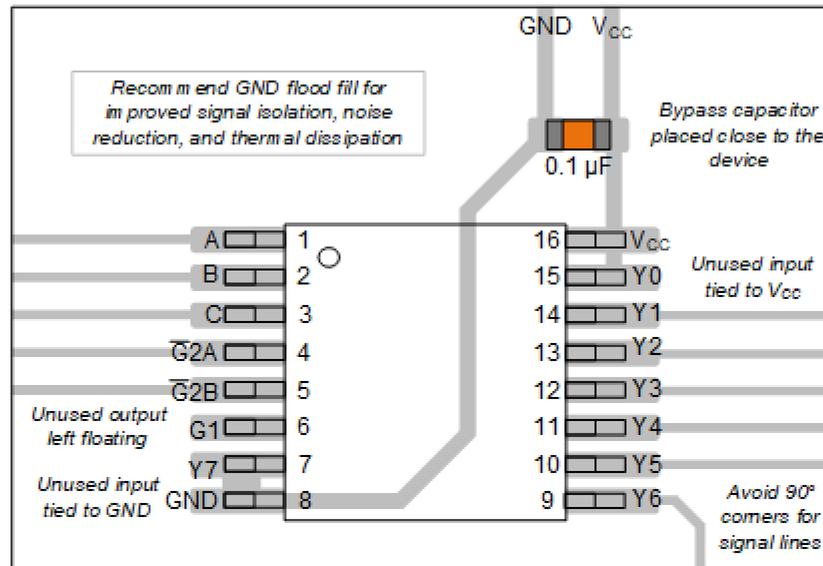

图 7-3. SN74AHC138 的示例布局

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8 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持(模拟)

8.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件,以及申请样片或购买产品的快速链接。

表 8-1. 相关链接

器件	产品文件夹	样片 & 购买	技术文档	工具 & 软件	支持 & 社区
SN54AHC138	点击此处	点击此处	点击此处	点击此处	点击此处
SN74AHC138	点击此处	点击此处	点击此处	点击此处	点击此处

8.2 接收文档更新通知

要接收文档更新通知,请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料,可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题,获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范,并且不一定反映 TI 的观点;请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序,可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注:以前版本的页码可能与当前版本的页码不同

Changes from Revision M (April 2024) to Revision N (July 2024) **Page**

- 将 D 封装的热性能指标 RθJA 的值从 73 更新为 93.8,所有值均以 °C/W 为单位..6

Changes from Revision L (July 2003) to Revision M (April 2024) **Page**

- 添加了*封装信息*表、*引脚功能*表、*ESD 等级*表、*热性能信息*表、*器件功能模式*、“应用和实施”部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分..1
- 删除了对机器放电模型的引用..1

- 将 PW 封装的热性能指标 RθJA 的值从 108 更新为 135.9，所有值均以 °C/W 为单位.................................... 6

10 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9851601Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601Q2A SNJ54AHC 138FK	Samples
5962-9851601QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QE A SNJ54AHC138J	Samples
5962-9851601QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QF A SNJ54AHC138W	Samples
SN74AHC138D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AHC138	
SN74AHC138DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC138	Samples
SN74AHC138N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC138N	Samples
SN74AHC138NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC138	Samples
SN74AHC138PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	HA138	
SN74AHC138PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HA138	Samples
SN74AHC138RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA138	Samples
SNJ54AHC138FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601Q2A SNJ54AHC 138FK	Samples
SNJ54AHC138J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QE A SNJ54AHC138J	Samples
SNJ54AHC138W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9851601QF A SNJ54AHC138W	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

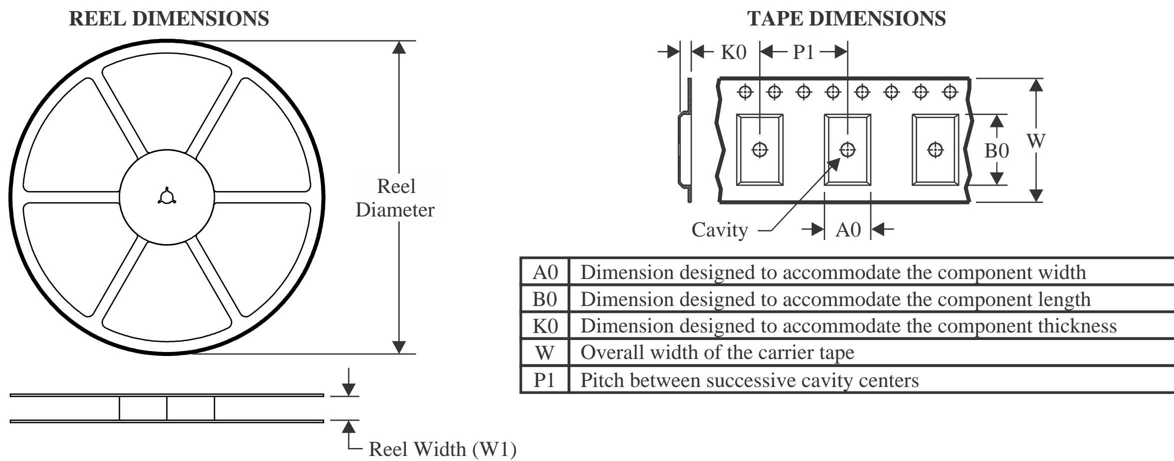
OTHER QUALIFIED VERSIONS OF SN54AHC138, SN74AHC138 :

- Catalog : SN74AHC138
- Automotive : SN74AHC138-Q1, SN74AHC138-Q1
- Military : SN54AHC138

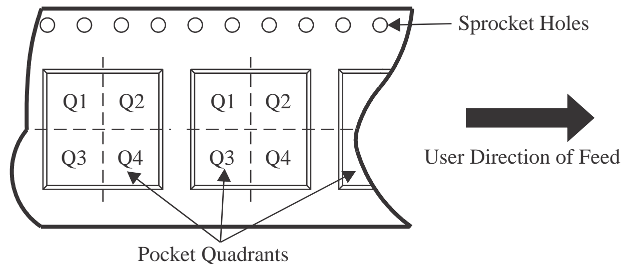
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



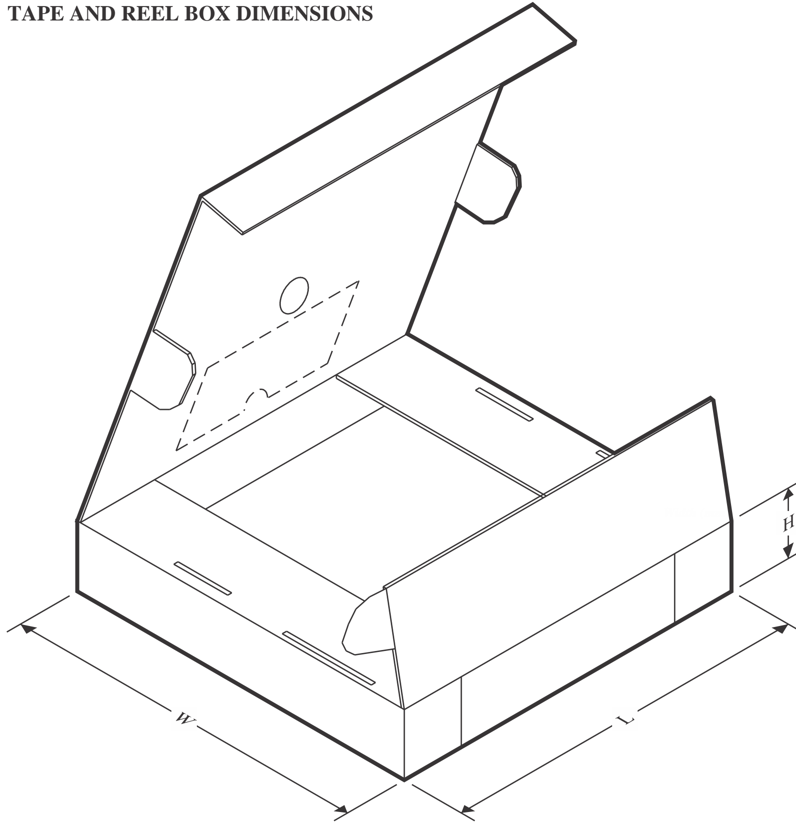
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC138DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC138DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC138DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC138NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC138PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC138PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC138RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

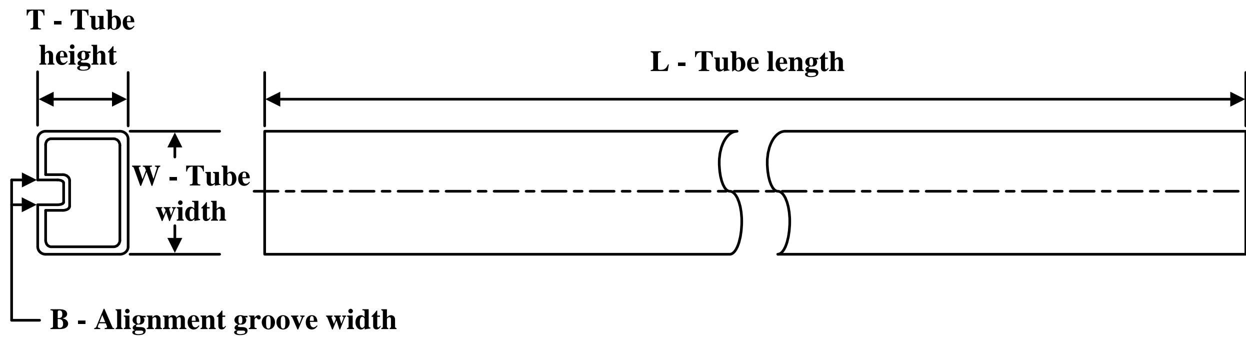
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC138DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHC138DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AHC138DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC138DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC138DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC138NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74AHC138PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC138PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHC138RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

TUBE

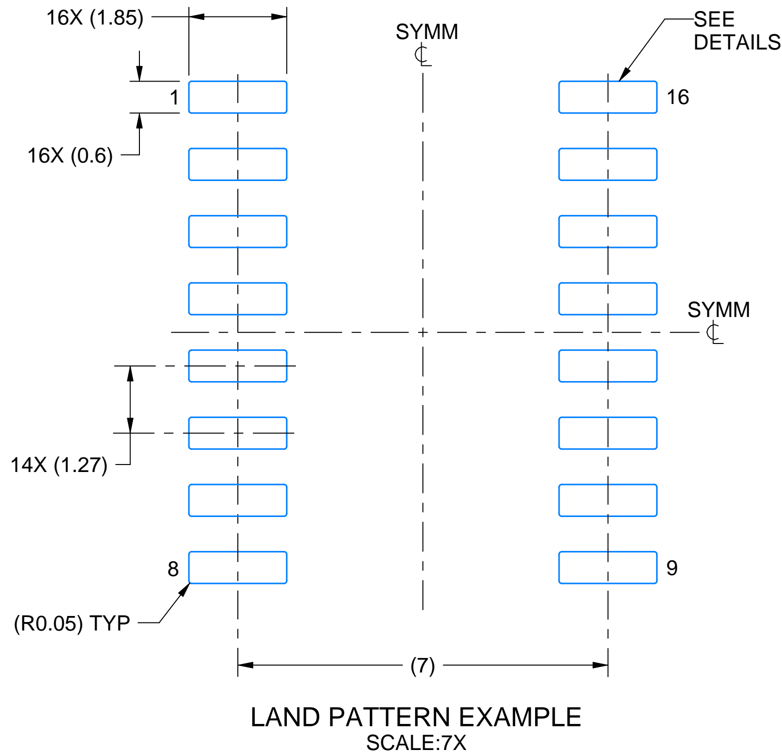


*All dimensions are nominal

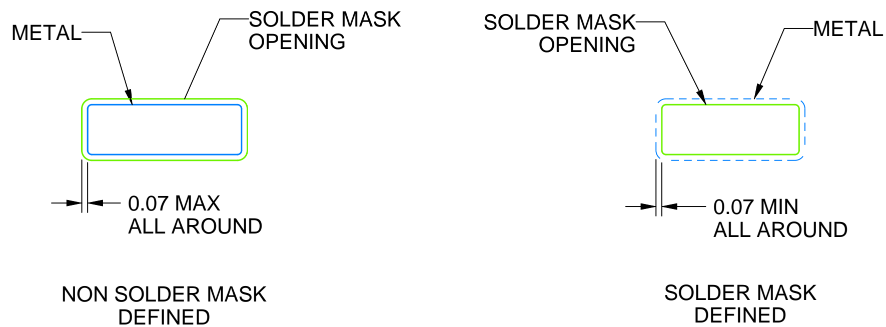
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9851601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9851601QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74AHC138N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC138N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54AHC138FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC138W	W	CFP	16	25	506.98	26.16	6220	NA

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

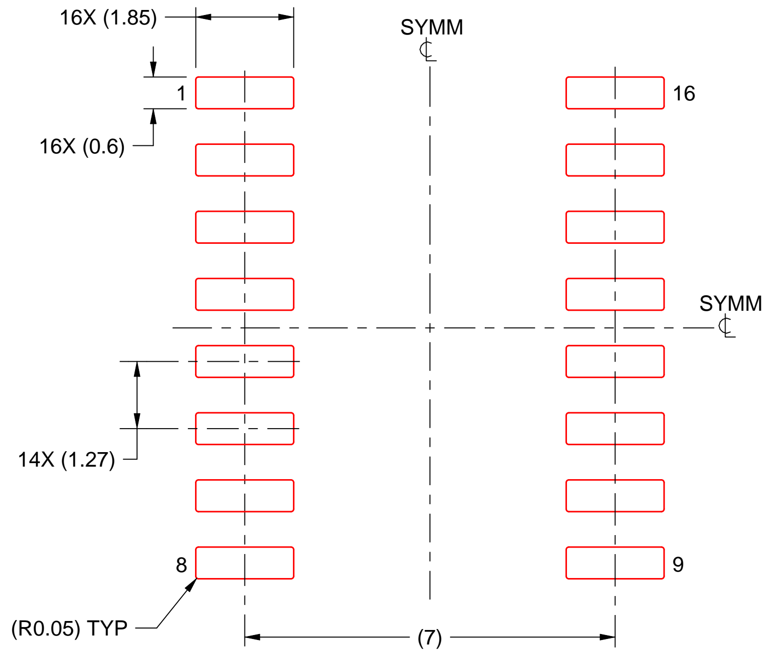
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



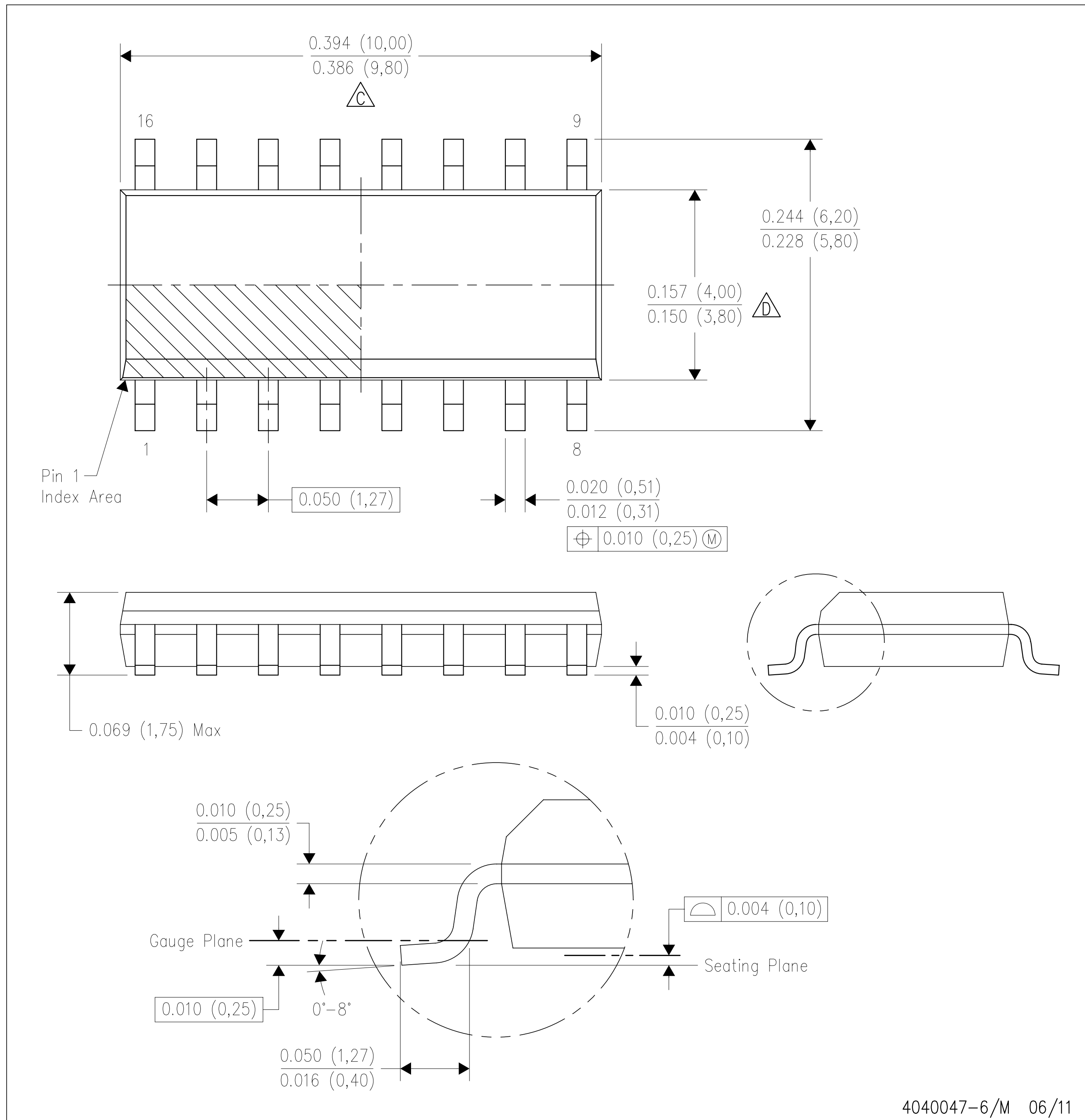
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE

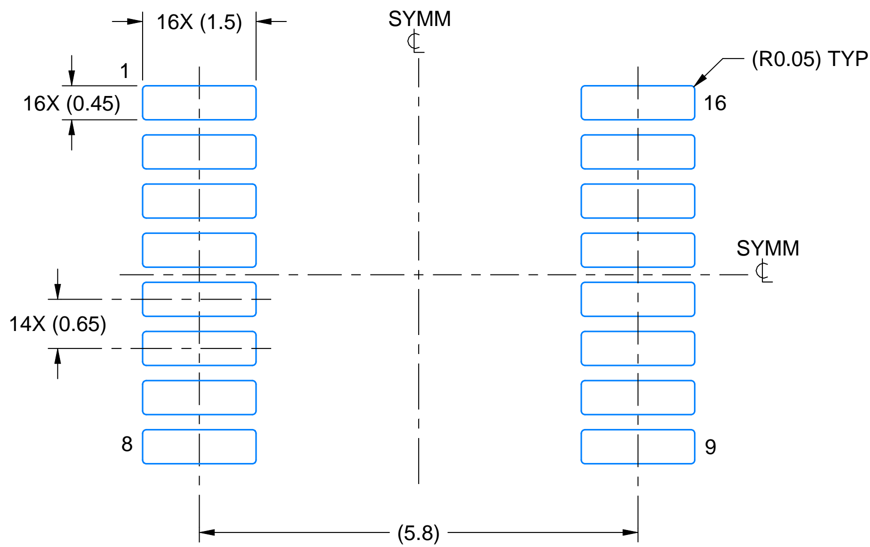


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

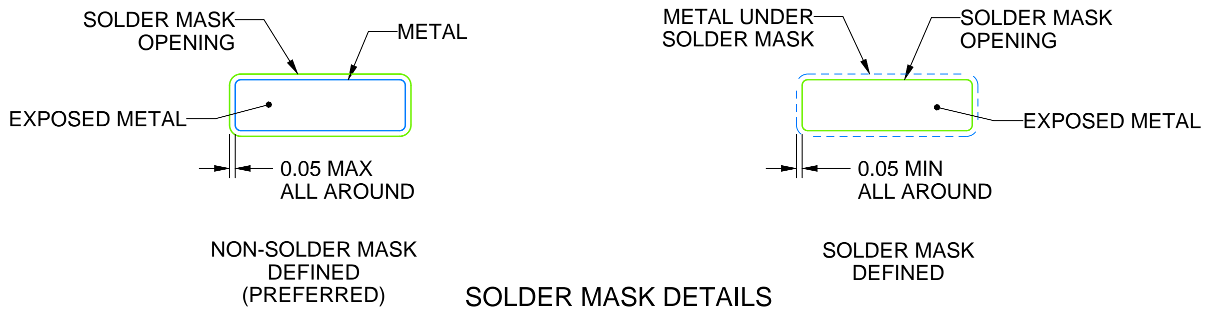
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

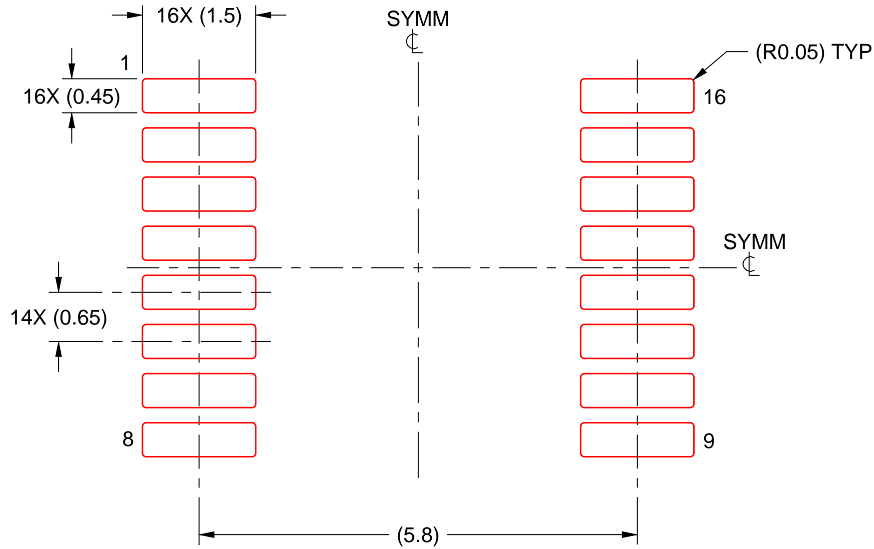


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

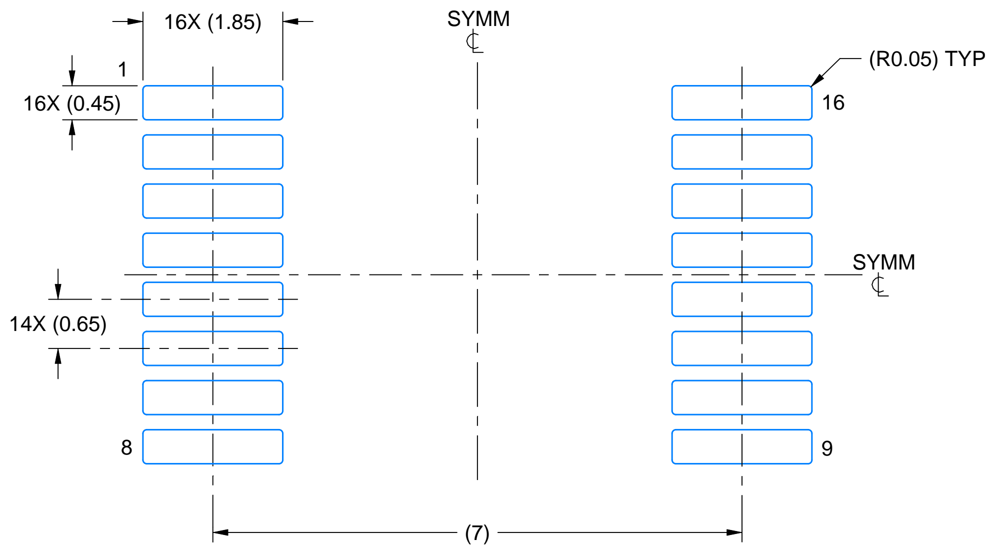
4220204/A 02/2017

NOTES: (continued)

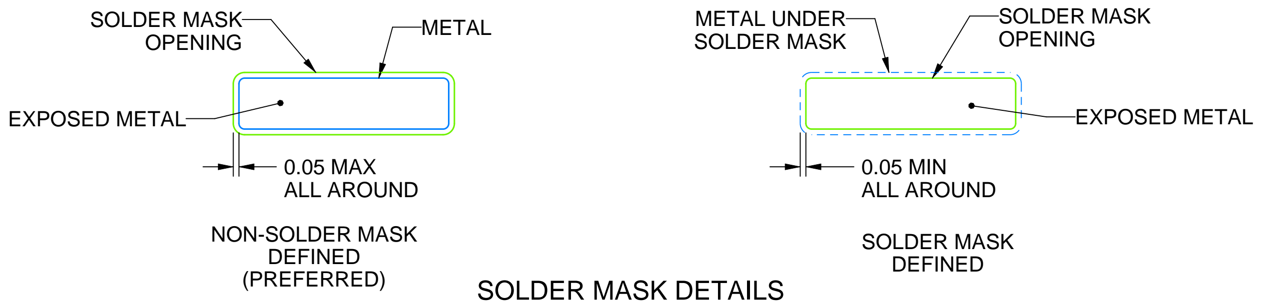
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

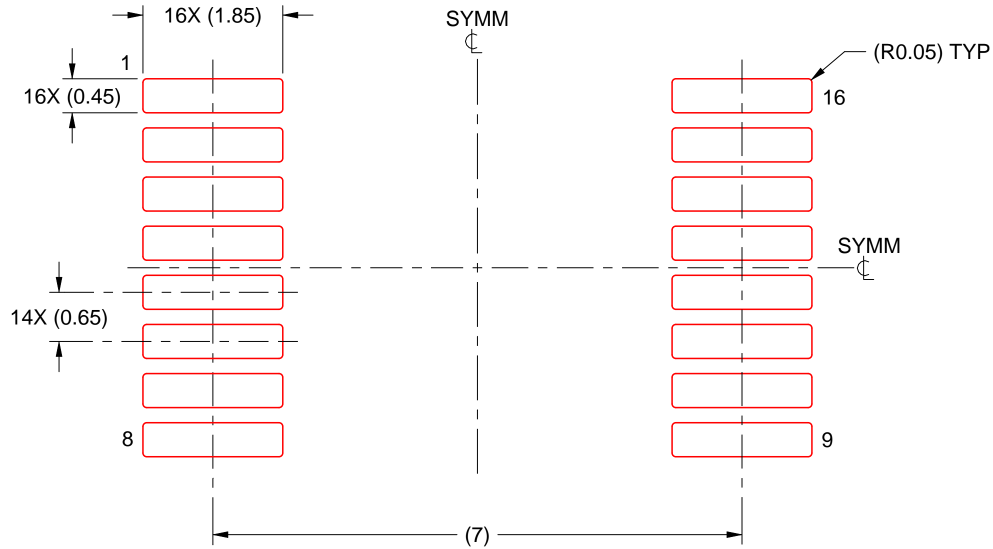


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

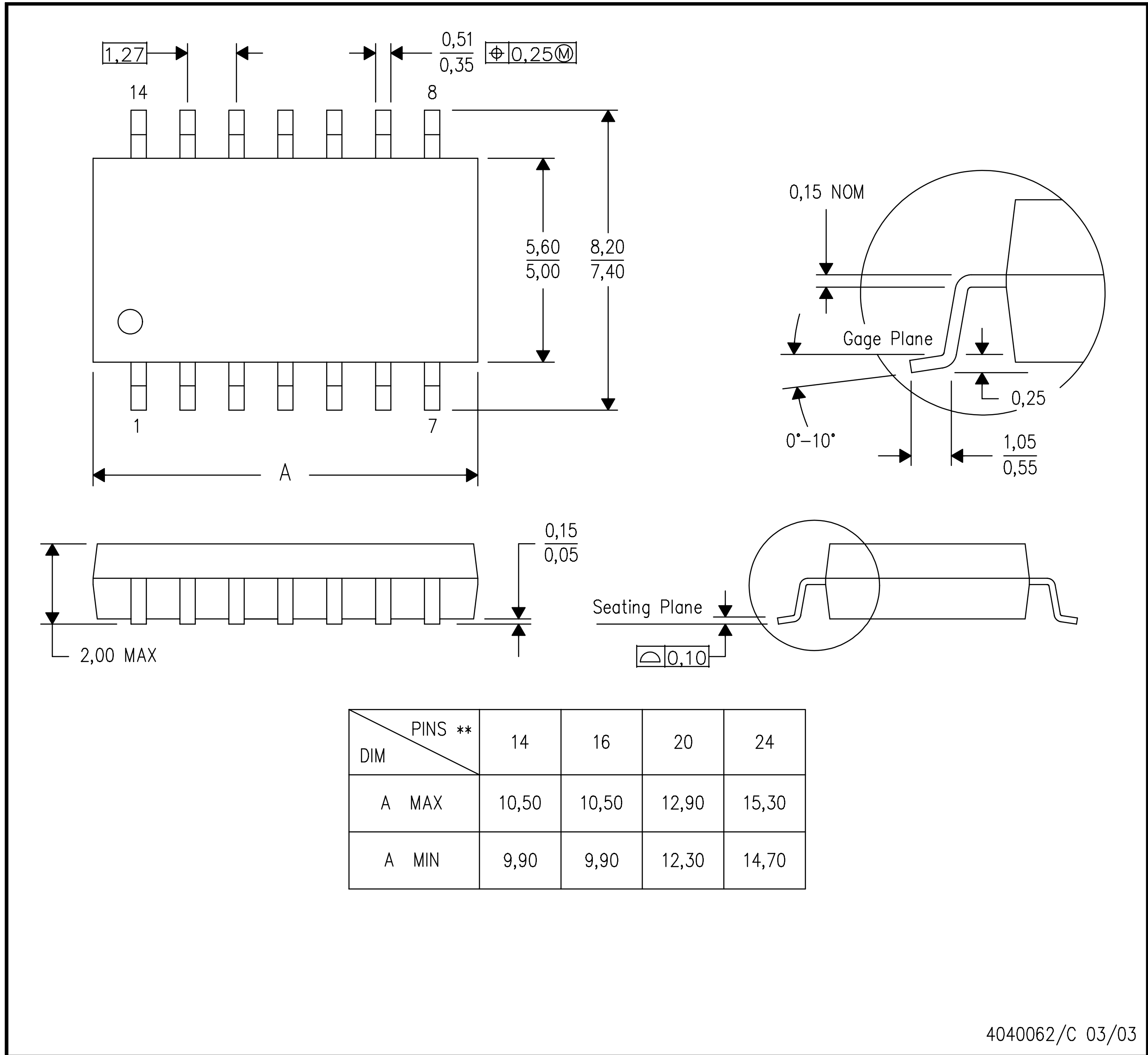
4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

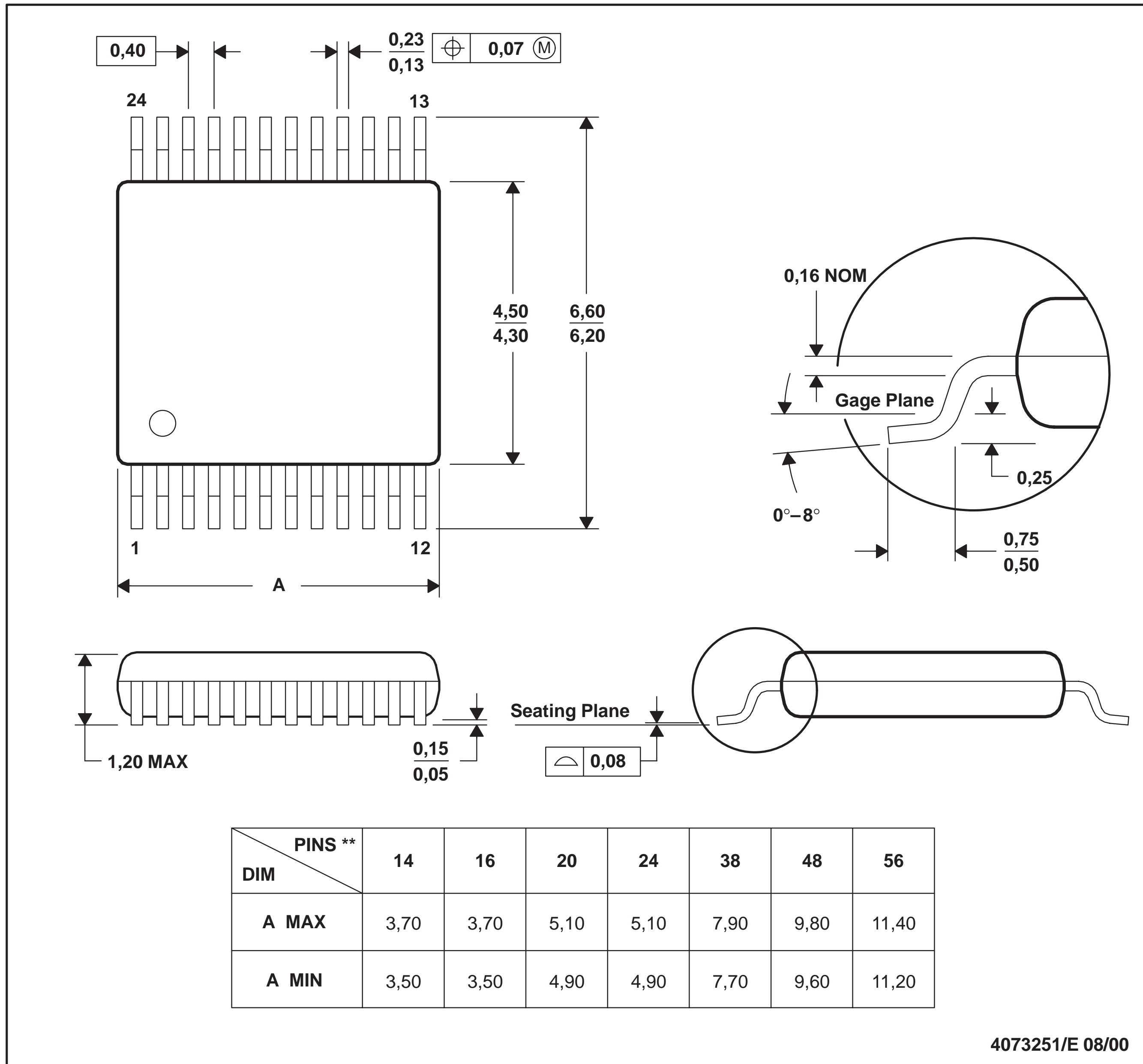


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

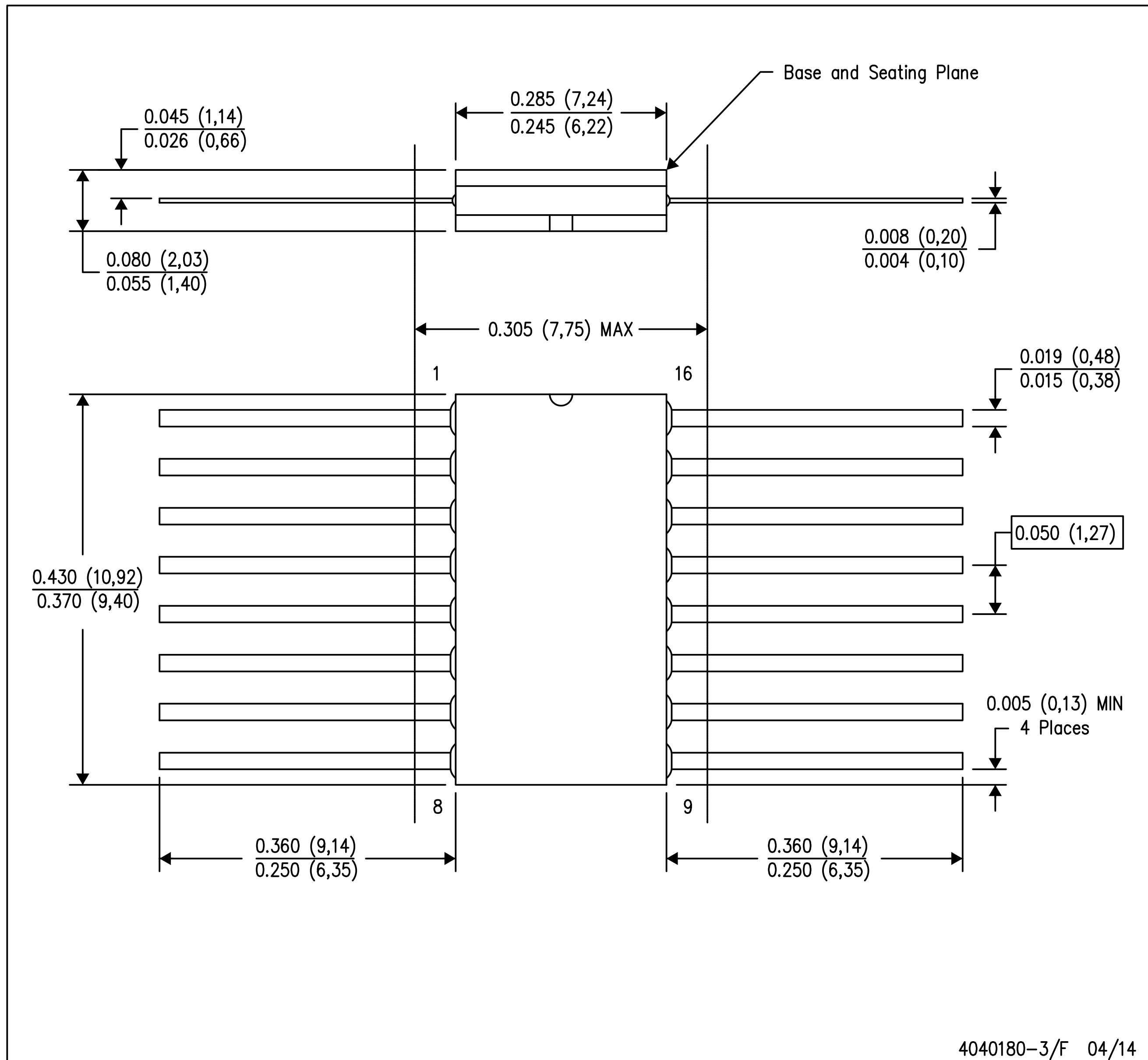
24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

W (R-GDFP-F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

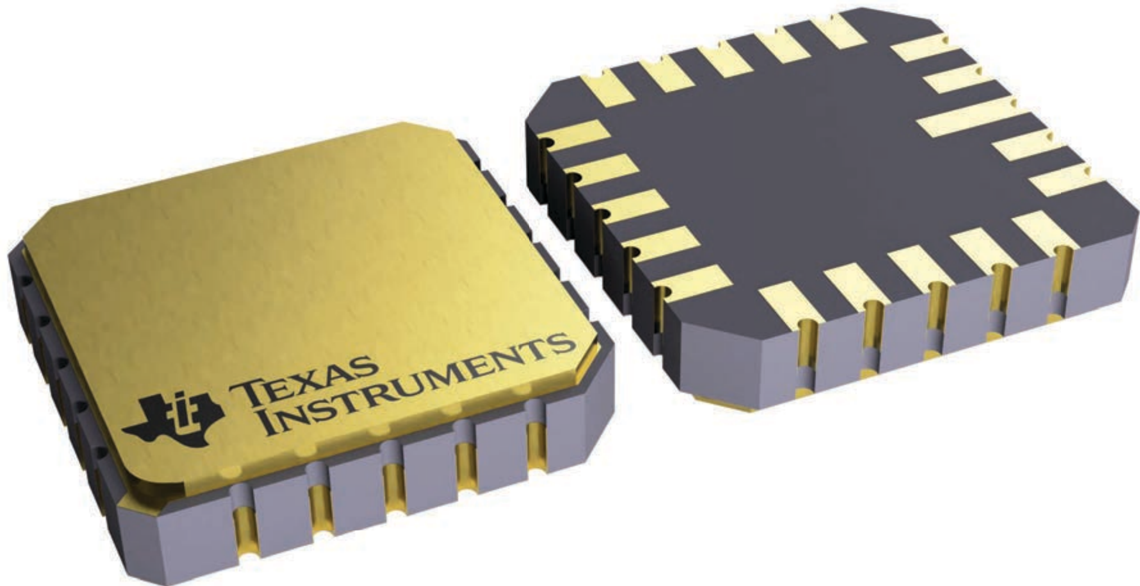
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

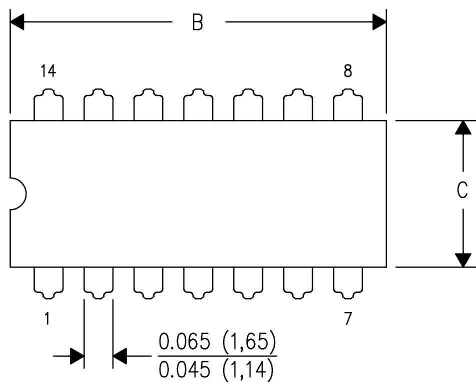
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



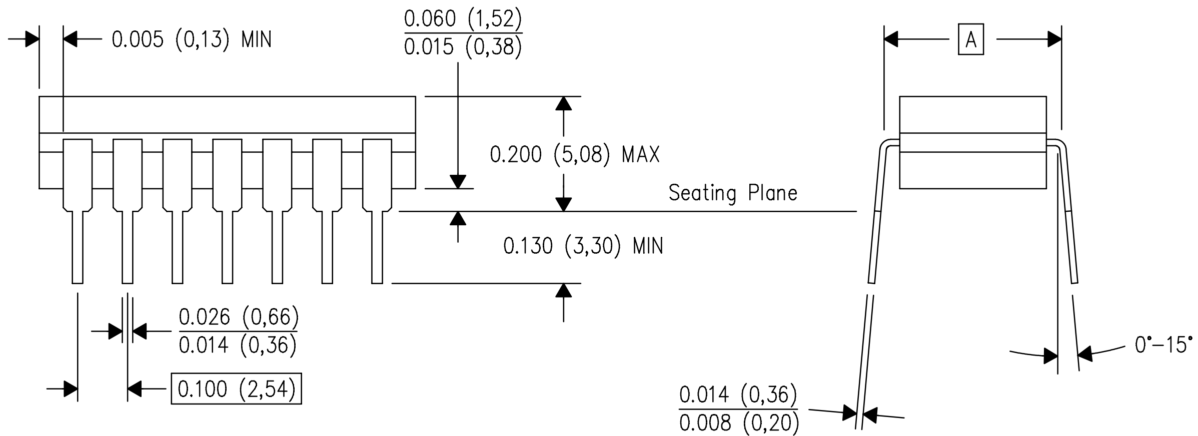
4229370\A\

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

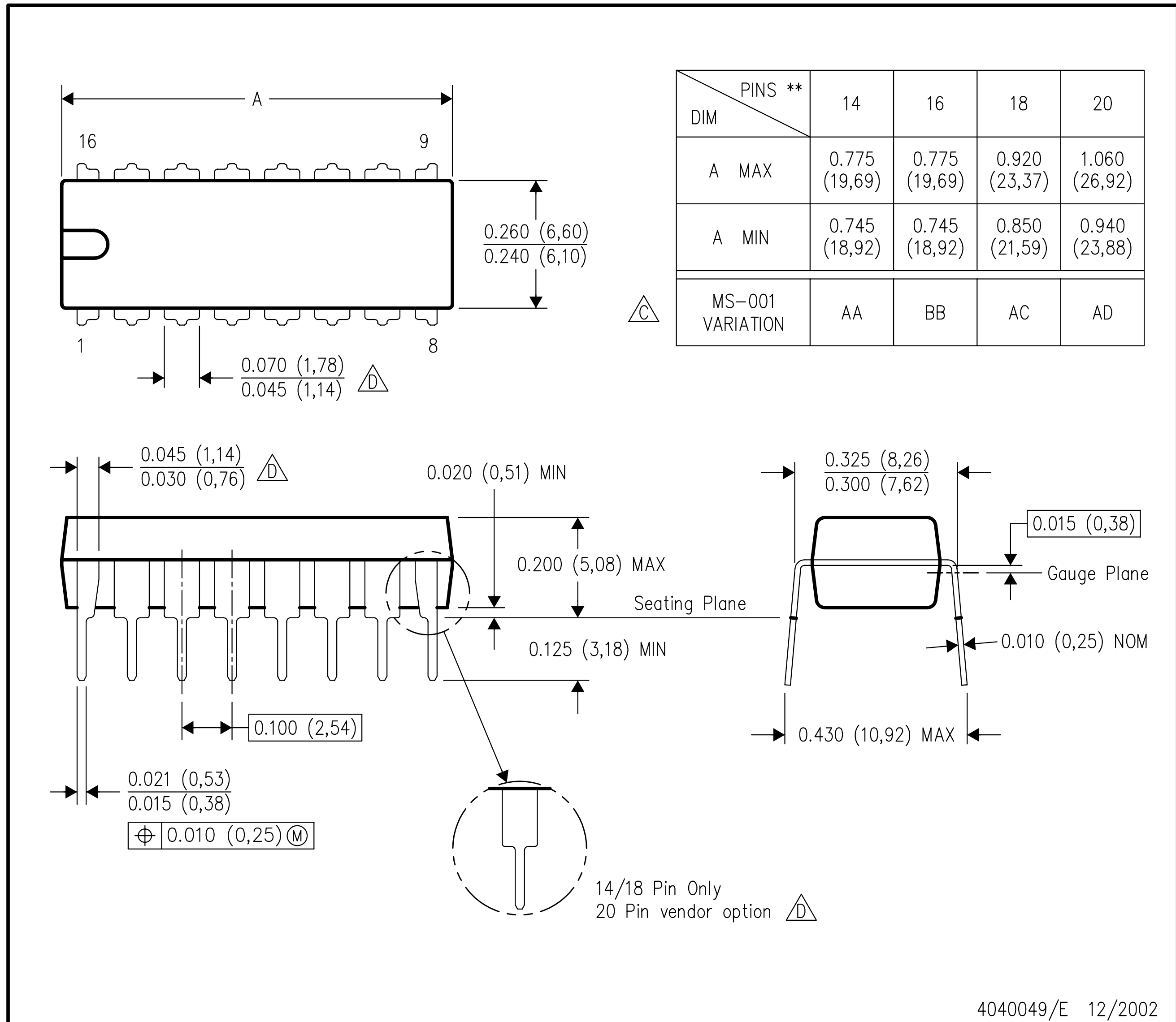


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

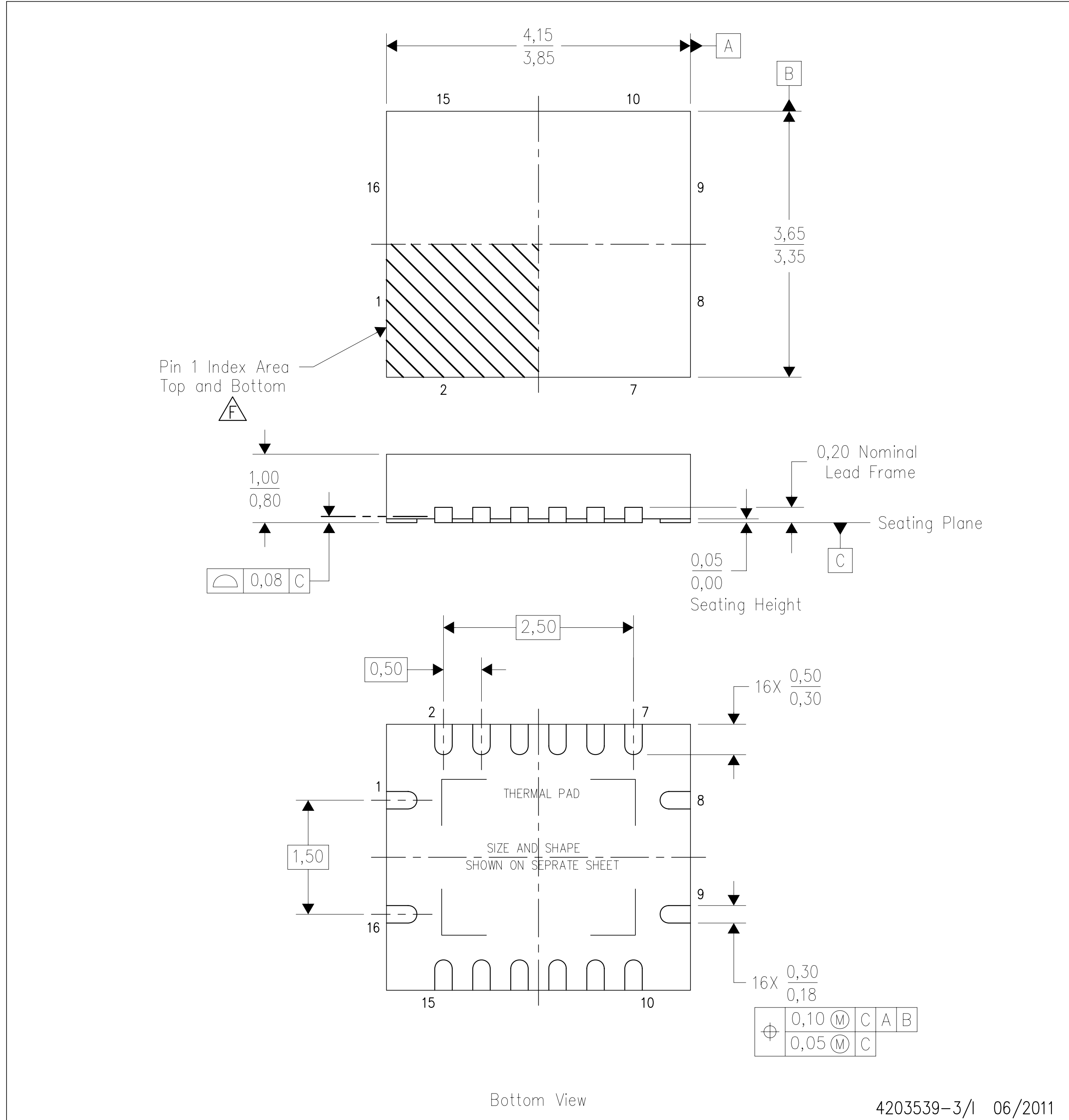
16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS-001 VARIATION	AA	BB	AC	AD

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

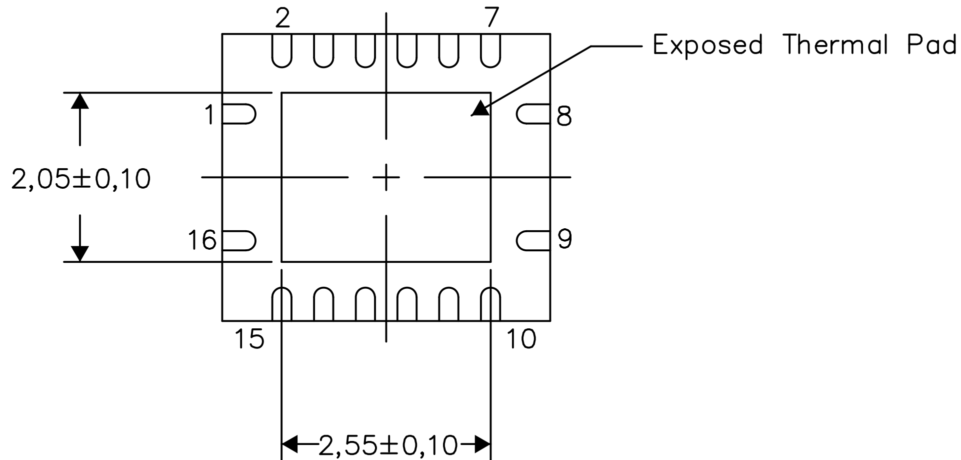
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

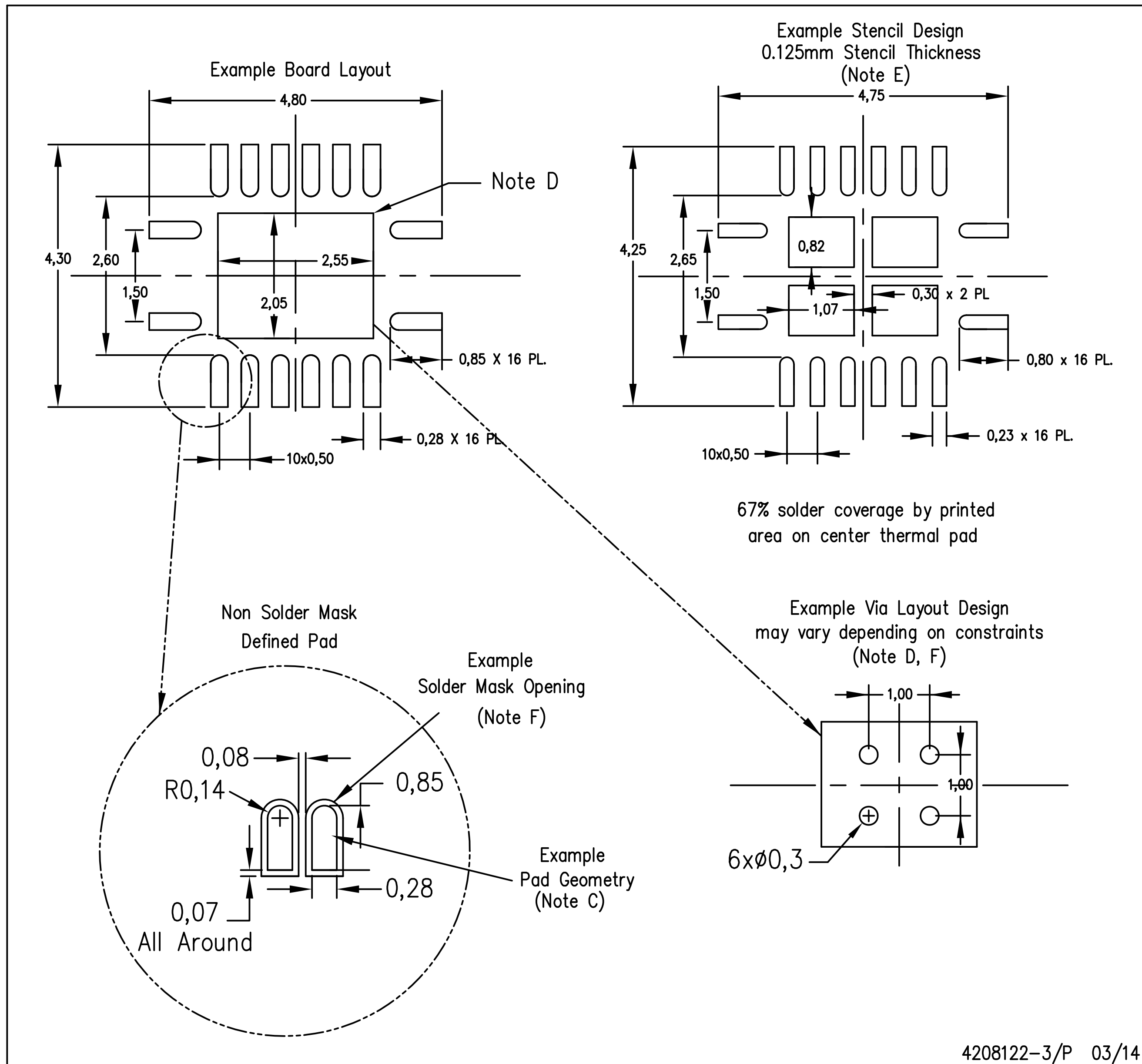
The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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