SN54HC195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SCLS124A–DECEMBER 1992–REVISED NOVEMBER 2007

FEATURES

- **Synchronous Parallel Load**
- **Positive-Edge-Triggered Clocking**
- **J and $\overline{K}$ Inputs to First Stage**
- **Complementary Outputs From Last Stage**
- **Package Options: Plastic and Ceramic DIPS and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DESCRIPTION/ORDERING INFORMATION

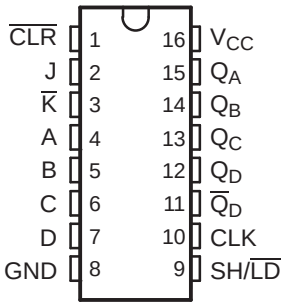
These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction Q_A and Q_D).

Parallel loading is accomplished by applying the 4-bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

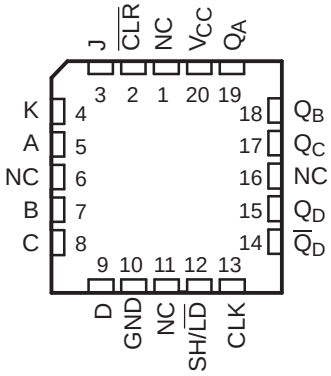
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of –55°C to 125°C.

SN54HC195 . . . J PACKAGE
(TOP VIEW)

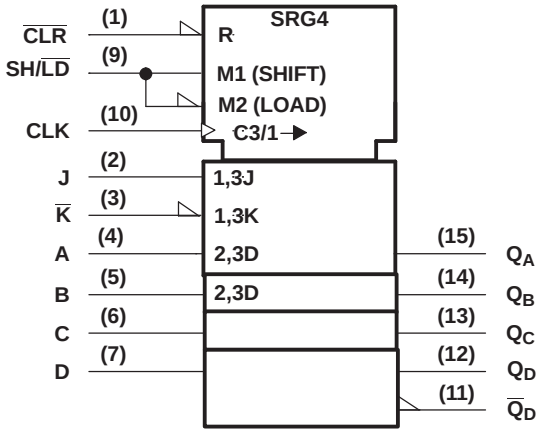


SN54HC195 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

LOGIC SYMBOL†



† This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617−12.

Pin numbers shown are for J package.

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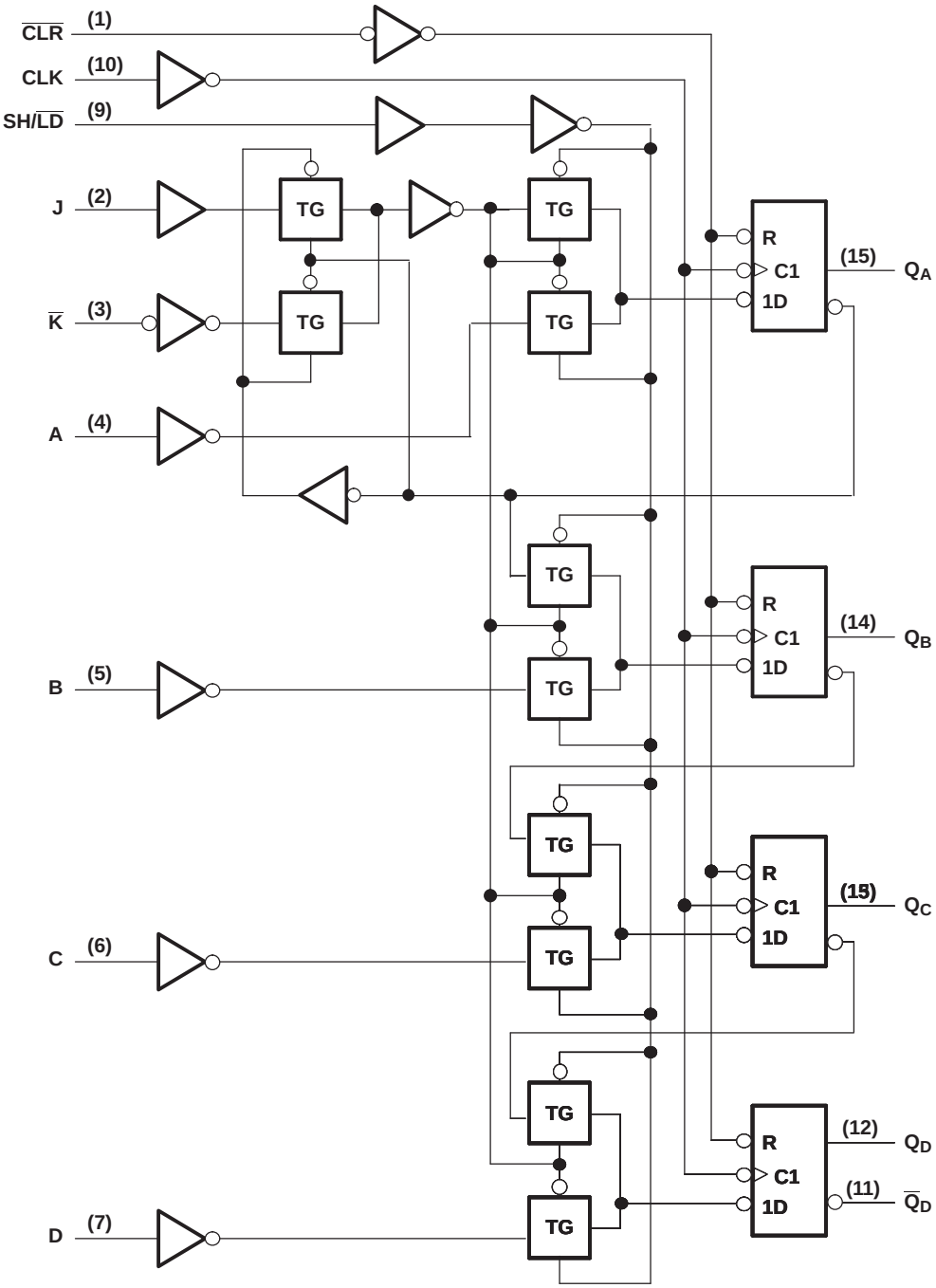
LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for J package.

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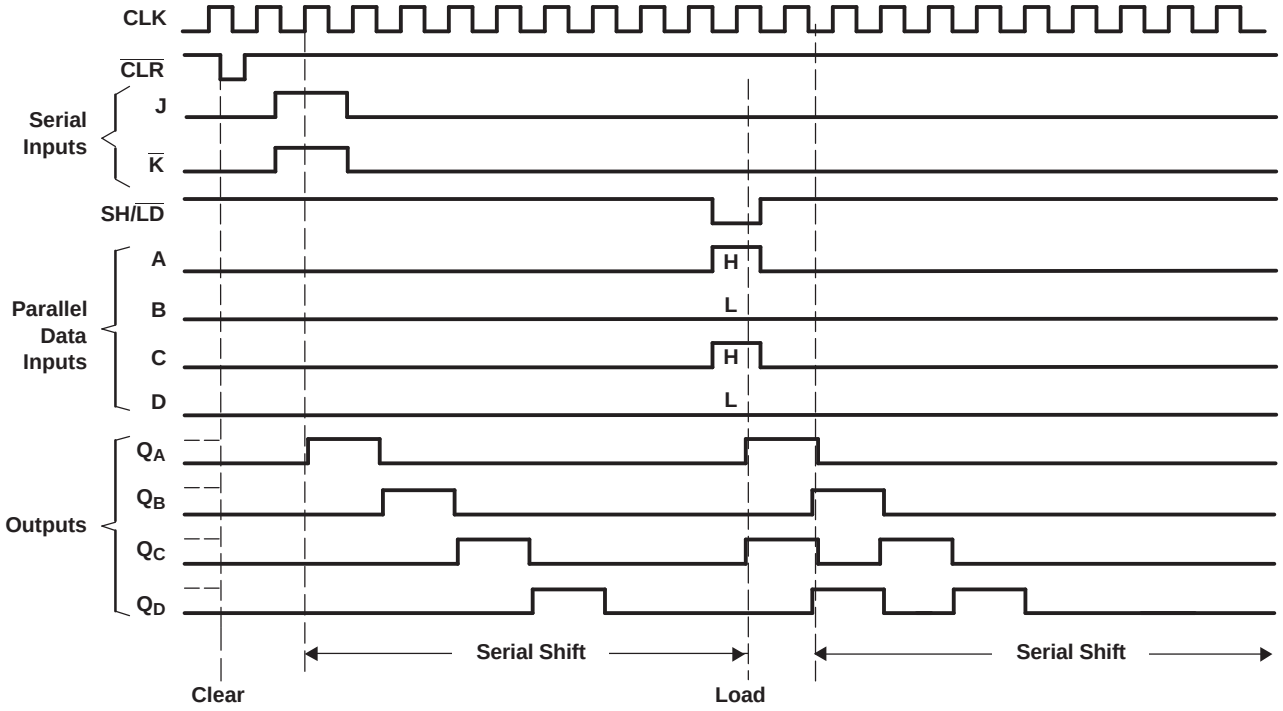
FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{CLR}$	SH/$\overline{LD}$	CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		25	mA
	Continuous current through V_{CC} or GND pins			50	mA
	Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package			300	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package			260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	
		V_{CC} = 6 V	0		1.2	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	ns
		V_{CC} = 4.5 V	0		500	
		V_{CC} = 6 V	0		400	
T_A	Operating free-air temperature		–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL},	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
	$V_I = V_{IH}$ or V_{IL},	I_{OH} = –4 mA	4.5 V	3.98	4.30		3.7		
	$V_I = V_{IH}$ or V_{IL},	I_{OH} = –5.2 mA	6 V	5.48	5.80		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL},	I_{OL} = 20 μA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
	$V_I = V_{IH}$ or V_{IL},	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4	
	$V_I = V_{IH}$ or V_{IL},	I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160	μA
C_I	$V_I = V_{CC}$ or GND		2 V to 6 V		3	10		10	pF

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TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC195		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	MHz
			4.5 V	0	31	0	21	
			6 V	0	36	0	25	
t_w	Pulse duration	CLK high or low	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		$\overline{CLR}$ low	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t_{su}	Setup time, before CLK↑	SH/$\overline{LD}$, or serial and parallel data, or CLR inactive	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		26		
t_h	Hold time, after CLK↑	SH/$\overline{LD}$, or serial and parallel data, or CLR inactive	2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF(1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		MHz
			4.5 V	31	50		21		
			6 V	36	60		25		
t_{pd}	CLK	Q_A thru Q_D or $\overline{Q}_D$	2 V		67	145		220	ns
			4.5 V		17	29		44	
			6 V		14	25		37	
t_{pd}	$\overline{CLR}$	Q_A thru Q_D or $\overline{Q}_D$	2 V		67	150		225	ns
			4.5 V		17	30		45	
			6 V		13	26		38	
t_t		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	
C_{pd}	Power dissipation capacitance		No load, T_A = 25°C						65 pF typ

(1) Load circuit and voltage waveforms are shown in previous pages.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8682701EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682701EA SNJ54HC195J
SN54HC195J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC195J
SN54HC195J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC195J
SNJ54HC195J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682701EA SNJ54HC195J
SNJ54HC195J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682701EA SNJ54HC195J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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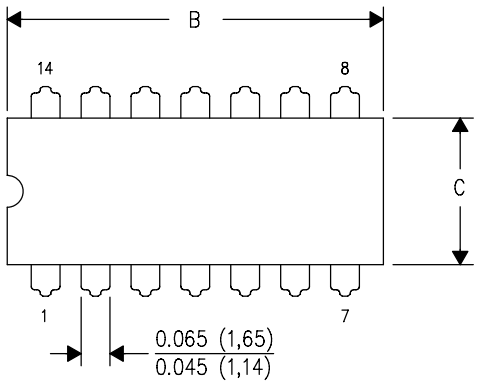
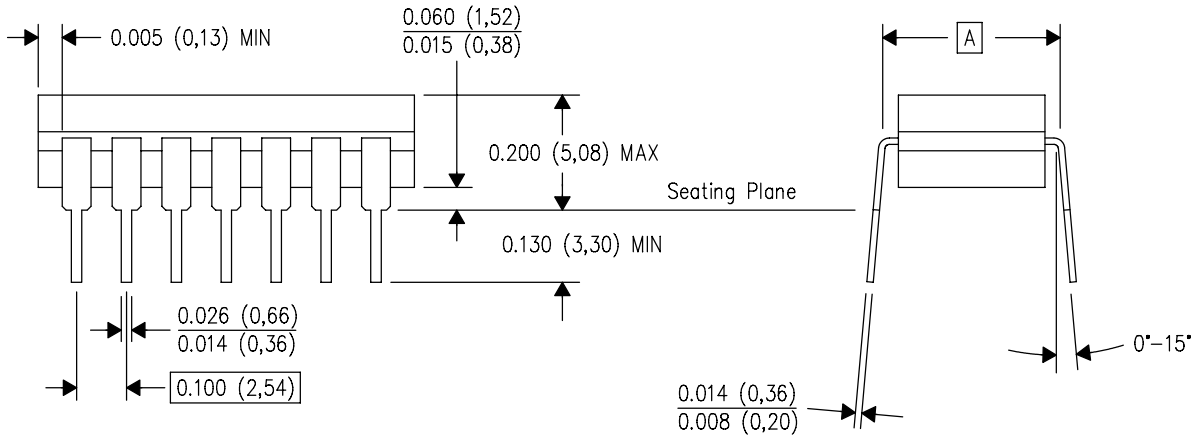
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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