



## FULL DIFFERENTIAL ANALOG INPUT 24-BIT, 192-kHz STEREO A/D CONVERTER

### FEATURES

- 24-Bit Delta-Sigma Stereo A/D Converter
- High Performance:
  - Dynamic Range: 112 dB (Typical)
  - SNR: 111 dB (Typical)
  - THD+N: –102 dB (Typical)
- High-Performance Linear Phase Antialias Digital Filter:
  - Pass-Band Ripple:  $\pm 0.005$  dB
  - Stop-Band Attenuation: –100 dB
- Fully Differential Analog Input:  $\pm 2.5$  V
- Audio Interface: Master- or Slave-Mode Selectable
- Data Formats: Left-Justified, I<sup>2</sup>S, Standard 24-Bit, and DSD
- Function:
  - Peak Detection
  - High-Pass Filter (HPF): –3 dB at 1 Hz,  $f_s = 48$  kHz
- Sampling Rate up to 192 kHz
- System Clock: 128  $f_s$ , 256  $f_s$ , 384  $f_s$ , 512  $f_s$ , or 768  $f_s$
- Dual Power Supplies:
  - 5 V for Analog
  - 3.3 V for Digital
- Power Dissipation: 225 mW
- Small 28-Pin SSOP
- DSD Output: 1 Bit, 64  $f_s$

### APPLICATIONS

- AV Amplifier
- MD Player
- Digital VTR
- Digital Mixer
- Digital Recorder

### DESCRIPTION

The PCM1804 is a high-performance, single-chip stereo A/D converter with fully differential analog voltage input. The PCM1804 uses a precision delta-sigma modulator and includes a linear phase antialias digital filter and high-pass filter (HPF) that removes dc offset from the input signal. The PCM1804 is suitable for a wide variety of mid- to high-grade consumer and professional applications, where excellent performance and 5-V analog supply and 3.3-V digital power-supply operation are required. The PCM1804 can achieve both PCM audio and DSD format due to the precision delta-sigma modulator. The PCM1804 is fabricated using an advanced CMOS process and is available in a small 28-pin SSOP package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

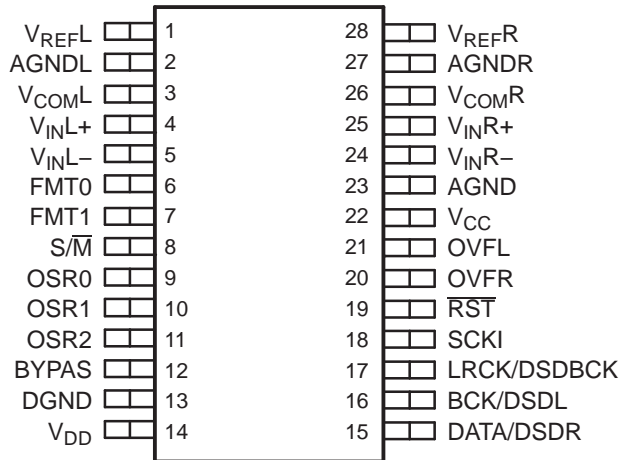
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All other trademarks are the property of their respective owners.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground. Specific guidelines for handling devices of this type are contained in the publication *Electrostatic Discharge (ESD) (SSYA008)*, available from Texas Instruments.

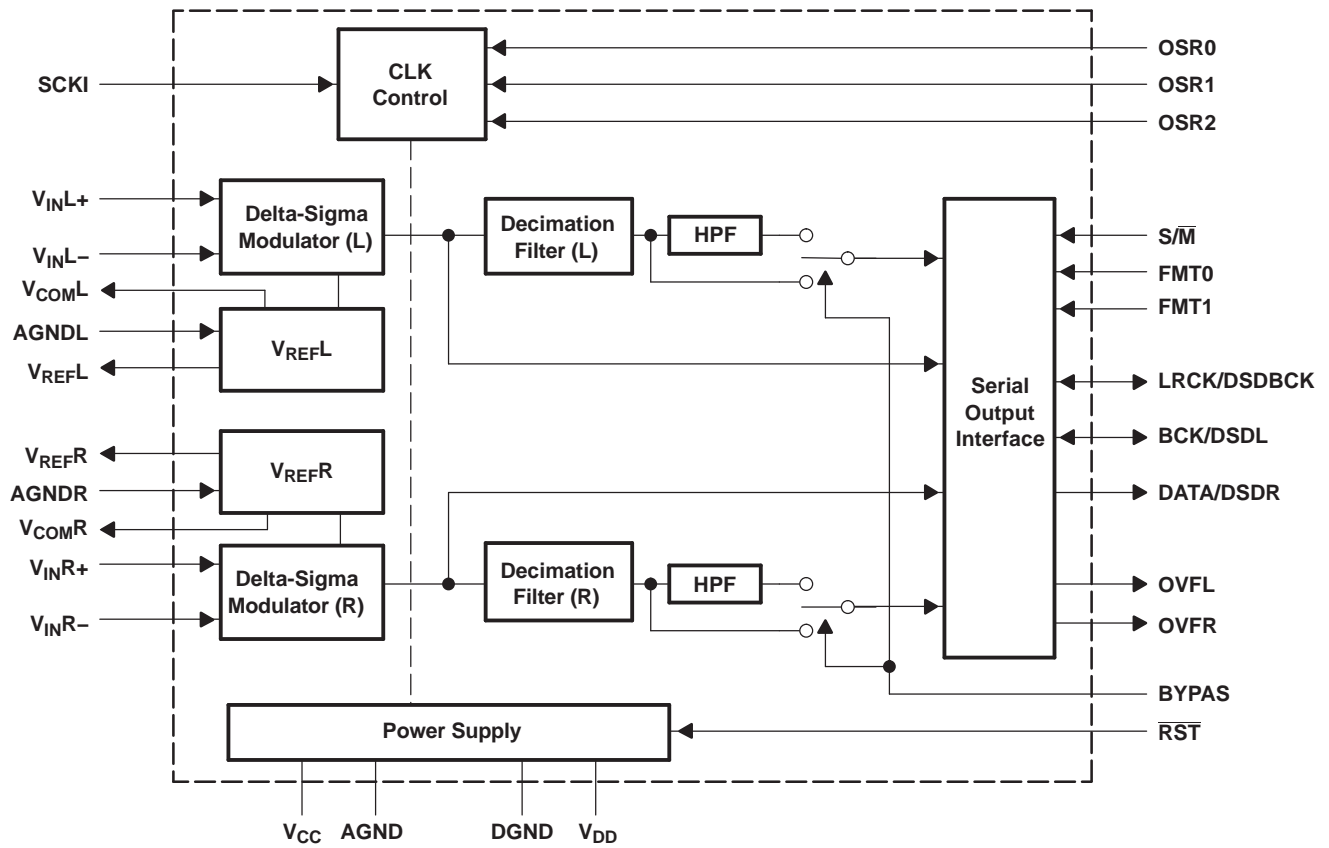
### PIN ASSIGNMENTS

PCM1804 PACKAGE  
(TOP VIEW)



P0007-02

**FUNCTIONAL BLOCK DIAGRAM**



B0029-01

## Terminal Functions

TERMINAL		I/O	DESCRIPTIONS
NAME	PIN		
AGND	23	–	Analog ground
AGNDL	2	–	Analog ground for $V_{REFL}$
AGNDR	27	–	Analog ground for $V_{REFR}$
BCK/DSDL	16	I/O	Bit clock input/output in PCM mode. L-channel audio data output in DSD mode. <sup>(1)</sup>
BYPAS	12	I	HPF bypass control. High: HPF disabled, Low: HPF enabled <sup>(1)</sup>
DATA/DSDR	15	O	L-channel and R-channel audio data output in PCM mode. R-channel audio data output in DSD mode. (DSD output, when in DSD mode)
DGND	13	–	Digital ground
FMT0	6	I	Audio data format 0. See <a href="#">Table 5</a> . <sup>(2)</sup>
FMT1	7	I	Audio data format 1. See <a href="#">Table 5</a> . <sup>(2)</sup>
LRCK/DSDBCK	17	I/O	Sampling clock input/output in PCM and DSD modes. <sup>(1)</sup>
OSR0	9	I	Oversampling ratio 0. See <a href="#">Table 1</a> and <a href="#">Table 2</a> . <sup>(2)</sup>
OSR1	10	I	Oversampling ratio 1. See <a href="#">Table 1</a> and <a href="#">Table 2</a> . <sup>(2)</sup>
OSR2	11	I	Oversampling ratio 2. See <a href="#">Table 1</a> and <a href="#">Table 2</a> . <sup>(2)</sup>
OVFL	21	O	Overflow signal of L-channel in PCM mode. This is available in PCM mode only.
OVFR	20	O	Overflow signal of R-channel in PCM mode. This is available in PCM mode only.
$\overline{RST}$	19	I	Reset, power-down input, active-low <sup>(2)</sup>
SCKI	18	I	System clock input; 128 $f_S$ , 256 $f_S$ , 384 $f_S$ , 512 $f_S$ , or 768 $f_S$ . <sup>(3)</sup>
$S/\overline{M}$	8	I	Slave/master mode selection. See <a href="#">Table 4</a> . <sup>(2)</sup>
$V_{CC}$	22	–	Analog power supply
$V_{COML}$	3	–	L-channel analog common-mode voltage (2.5 V)
$V_{COMR}$	26	–	R-channel analog common-mode voltage (2.5 V)
$V_{DD}$	14	–	Digital power supply
$V_{INL-}$	5	I	L-channel analog input, negative pin
$V_{INL+}$	4	I	L-channel analog input, positive pin
$V_{INR-}$	24	I	R-channel analog input, negative pin
$V_{INR+}$	25	I	R-channel analog input, positive pin
$V_{REFL}$	1	–	L-channel voltage reference output, requires capacitors for decoupling to AGND
$V_{REFR}$	28	–	R-channel voltage reference output, requires capacitors for decoupling to AGND

(1) Schmitt-trigger input

(2) Schmitt-trigger input with internal pulldown (51 k $\Omega$  typically), 5-V tolerant.

(3) Schmitt-trigger input, 5-V tolerant.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Supply voltage	$V_{CC}$	–0.3 V to 6.5 V
	$V_{DD}$	–0.3 V to 4 V
Ground voltage differences	AGND, AGNDL, AGNDR, DGND	±0.1 V
Supply voltage difference	$V_{CC}, V_{DD}$	$V_{CC} - V_{DD} < 3$ V
Digital input voltage	FMT0, FMT1, S/M, OSR0, OSR1, OSR2, SCKI, RST	–0.3 V to 6.5 V
	BYPAS, DATA/DSDR, BCK/DSDL, LRCK/DSDBCK, OVFL, OVFR	–0.3 V to ( $V_{DD} + 0.3$ V)
Analog input voltage	$V_{REFL}, V_{REFR}, V_{COML}, V_{COMR}, V_{INL+}, V_{INR+}, V_{INL-}, V_{INR-}$	–0.3 V to ( $V_{CC} + 0.3$ V)
Input current (any pins except supplies)		±10 mA
$T_A$	Ambient temperature under bias	–40°C to 125°C
$T_{stg}$	Storage temperature	–55°C to 150°C
$T_J$	Junction temperature	150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

	MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC}$	4.75	5	5.25	V
Digital supply voltage, $V_{DD}$	3	3.3	3.6	V
Analog input voltage, full-scale (–0 dB), differential input	5			Vp-p
Digital input logic family	TTL compatible			
Digital input clock frequency	System clock		36.864	MHz
	Sampling clock		192	kHz
Digital output load capacitance	10			pF
Operating free-air temperature, $T_A$	–10	70		°C

**ELECTRICAL CHARACTERISTICS**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ , master mode, single-speed mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PCM1804DB			UNIT
		MIN	TYP	MAX	
Resolution			24		Bits
<b>DATA FORMAT</b>					
Audio data interface format		Standard, I <sup>2</sup> S, left-justified			
Audio data bit length			24		Bits
Audio data format		MSB first, 2s complement, DSD			
<b>DIGITAL INPUT/OUTPUT</b>					
Logic family		TTL compatible			
$V_{IH}$	High-level input voltage	(1) (2)	2	5.5	Vdc
		(3)	2	$V_{DD}$	
$V_{IL}$	Low-level input voltage	(1) (2) (3)		0.8	Vdc
$I_{IH}$	High-level input current	$V_{IN} = V_{DD}$ (1)	65	100	$\mu\text{A}$
		$V_{IN} = V_{DD}$ (2)		$\pm 10$	
		$V_{IN} = V_{DD}$ (3)		$\pm 100$	
$I_{IL}$	Low-level input current	$V_{IN} = 0\text{ V}$ (1) (2)		$\pm 10$	$\mu\text{A}$
		$V_{IN} = 0\text{ V}$ (3)		$\pm 50$	
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{ mA}$ (4)	2.4		Vdc
$V_{OL}$	Low-level output voltage	$I_{OL} = 1\text{ mA}$ (4)		0.4	Vdc
<b>CLOCK FREQUENCY</b>					
$f_S$	Sampling frequency		32	192	kHz
	System clock frequency	256 $f_S$ , single rate (5)	12.288		MHz
		384 $f_S$ , single rate (5)	18.432		
		512 $f_S$ , single rate (5)	24.576		
		768 $f_S$ , single rate (5)	36.864		
		256 $f_S$ , dual rate (6)	24.576		
		384 $f_S$ , dual rate (6)	36.864		
		128 $f_S$ , quad rate (7)	24.576		
		192 $f_S$ , quad rate (7)	36.864		
<b>DC ACCURACY</b>					
	Gain mismatch, channel-to-channel			$\pm 3$	% of FSR
	Gain error ( $V_{IN} = -0.5\text{ dB}$ )			$\pm 4$	% of FSR
	Bipolar zero error	HPF bypass		$\pm 0.2$	% of FSR

(1) Pins 6–11, 19: FMT0, FMT1, S/M, OSR0, OSR1, OSR2,  $\overline{\text{RST}}$  [Schmitt-trigger input with internal pulldown (51 k $\Omega$  typically), 5-V tolerant]

(2) Pin 18: SCK1 (Schmitt-trigger input, 5-V tolerant)

(3) Pins 12, 16–17: BYPAS, BCK/DSDL, LRCK/DSDBCK (in slave mode, Schmitt-trigger input)

(4) Pins 15–17, 20, and 21: DATA/DSDR, BCK/DSDL, LRCK/DSDBCK (in master mode), OVFR, OVFL

(5) Single rate,  $f_S = 48\text{ kHz}$

(6) Dual rate,  $f_S = 96\text{ kHz}$

(7) Quad rate,  $f_S = 192\text{ kHz}$

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ , master mode, single-speed mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PCM1804DB			UNIT
		MIN	TYP	MAX	
<b>DYNAMIC PERFORMANCE <sup>(8)</sup></b>					
THD+N Total harmonic distortion plus noise	$V_{IN} = -0.5\text{ dB}$	$f_S = 48\text{ kHz}$ , system clock = $256 f_S$	-102	-95	dB
	$V_{IN} = -60\text{ dB}$		-49		
	$V_{IN} = -0.5\text{ dB}$	$f_S = 96\text{ kHz}$ , system clock = $256 f_S$	-101		
	$V_{IN} = -60\text{ dB}$		-47		
	$V_{IN} = -0.5\text{ dB}$	$f_S = 192\text{ kHz}$ , system clock = $128 f_S$	-101		
	$V_{IN} = -60\text{ dB}$		-47		
	$V_{IN} = -0.5\text{ dB}$	DSD mode	-100		
Dynamic range (A-weighted)	$V_{IN} = -60\text{ dB}$	$f_S = 48\text{ kHz}$ , system clock = $256 f_S$	106	112	dB
		$f_S = 96\text{ kHz}$ , system clock = $256 f_S$		112	
		$f_S = 192\text{ kHz}$ , system clock = $128 f_S$		112	
	DSD mode		112		
SNR (A-weighted)		$f_S = 48\text{ kHz}$ , system clock = $256 f_S$	105	111	dB
		$f_S = 96\text{ kHz}$ , system clock = $256 f_S$		111	
		$f_S = 192\text{ kHz}$ , system clock = $128 f_S$		111	
		DSD mode		111	
Channel separation		$f_S = 48\text{ kHz}$ , system clock = $256 f_S$	97	109	dB
		$f_S = 96\text{ kHz}$ , system clock = $256 f_S$		107	
		$f_S = 192\text{ kHz}$ , system clock = $128 f_S$		107	
<b>ANALOG INPUT</b>					
Input voltage	Differential input		$\pm 2.5$		V
Center voltage			2.5		V <sub>dc</sub>
Input impedance	Single-ended		10		k $\mu$
<b>DIGITAL FILTER PERFORMANCE</b>					
Pass-band edge	Single rate, dual rate			$0.453 f_S$	Hz
Stop-band edge	Single rate, dual rate			$0.547 f_S$	Hz
Pass-band ripple	Single rate, dual rate			$\pm 0.005$	dB
Stop-band attenuation	Single rate, dual rate		-100		dB
Pass-band edge (-0.005 dB)	Quad rate			$0.375 f_S$	Hz
Pass-band edge (-3 dB)	Quad rate			$0.49 f_S$	Hz
Stop-band edge	Quad rate			$0.77 f_S$	Hz
Pass-band ripple	Quad rate			$\pm 0.005$	dB
Stop-band attenuation	Quad rate		-135		dB
Group delay	Single rate, dual rate			$37/f_S$	s
Group delay	Quad rate			$9.5/f_S$	s
HPF frequency response	-3 dB			$f_S/48000$	Hz

(8)  $f_{IN} = 1\text{ kHz}$ , using System Two™ audio measurement system by Audio Precision™ in RMS mode, with 20-kHz LPF and 400-Hz HPF in calculation for single rate, or with 40-kHz LPF in calculation for dual and quad rates.

**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ , master mode, single-speed mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM1804DB			UNIT
			MIN	TYP	MAX	
<b>POWER SUPPLY REQUIREMENTS</b>						
$V_{CC}$	Supply voltage range		4.75	5	5.25	Vdc
$V_{DD}$			3	3.3	3.6	
$I_{CC}$	Supply current	$V_{CC} = 5\text{ V}$ <sup>(9)</sup> <sup>(10)</sup> <sup>(11)</sup>		35	45	mA
$I_{DD}$		$V_{DD} = 3.3\text{ V}$ <sup>(9)</sup> <sup>(12)</sup>		15	20	
		$V_{DD} = 3.3\text{ V}$ <sup>(10)</sup> <sup>(12)</sup>		27		
		$V_{DD} = 3.3\text{ V}$ <sup>(11)</sup> <sup>(12)</sup>		18		
$P_D$	Power dissipation	Operation, $V_{CC} = 5\text{ V}$ , $V_{DD} = 3.3\text{ V}$ <sup>(9)</sup> <sup>(12)</sup>		225	290	mW
		Operation, $V_{CC} = 5\text{ V}$ , $V_{DD} = 3.3\text{ V}$ <sup>(10)</sup> <sup>(12)</sup>		265		
		Operation, $V_{CC} = 5\text{ V}$ , $V_{DD} = 3.3\text{ V}$ <sup>(11)</sup> <sup>(12)</sup>		235		
		Power down, $V_{CC} = 5\text{ V}$ , $V_{DD} = 3.3\text{ V}$		5		
<b>TEMPERATURE RANGE</b>						
	Operation temperature		-10		70	$^\circ\text{C}$
$\theta_{JA}$	Thermal resistance			100		$^\circ\text{C/W}$

(9) Single rate,  $f_S = 48\text{ kHz}$

(10) Dual rate,  $f_S = 96\text{ kHz}$

(11) Quad rate,  $f_S = 192\text{ kHz}$

(12) Minimum load on DATA/DSDR (pin 15)



### TYPICAL PERFORMANCE CURVES - SINGLE RATE

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

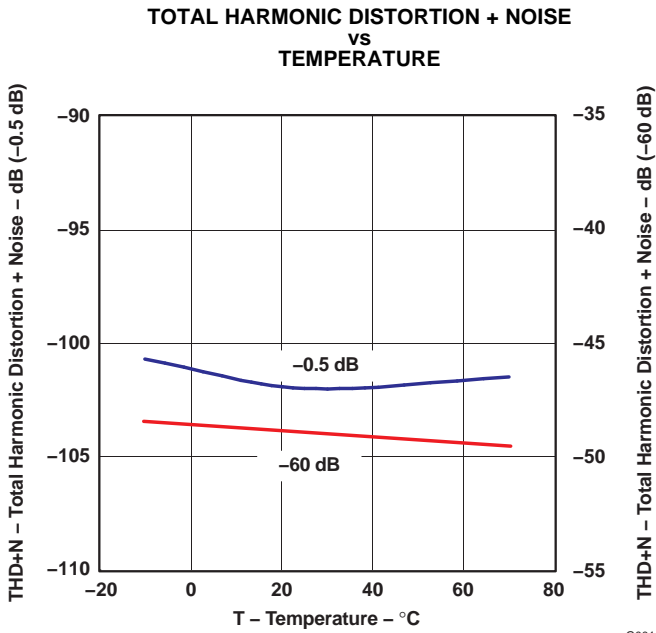


Figure 1.

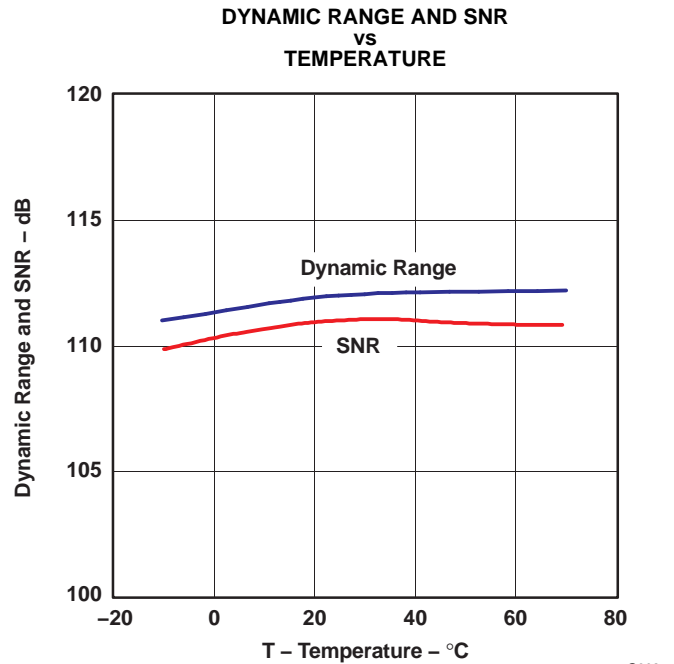


Figure 2.

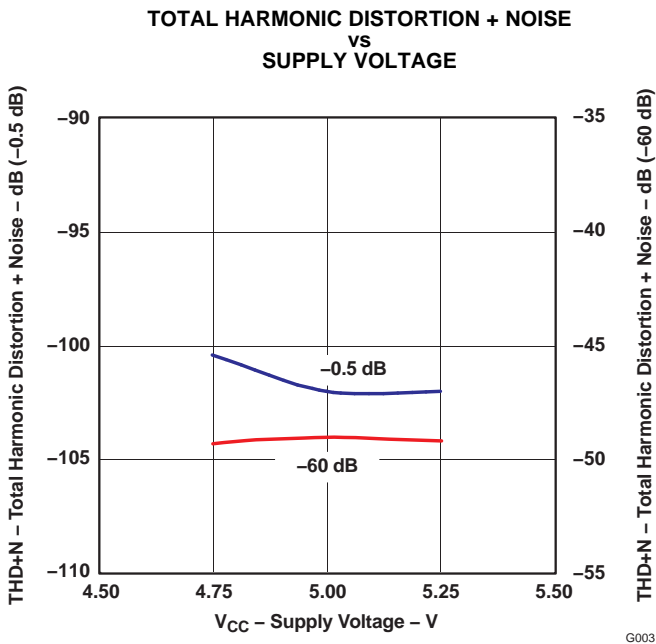


Figure 3.

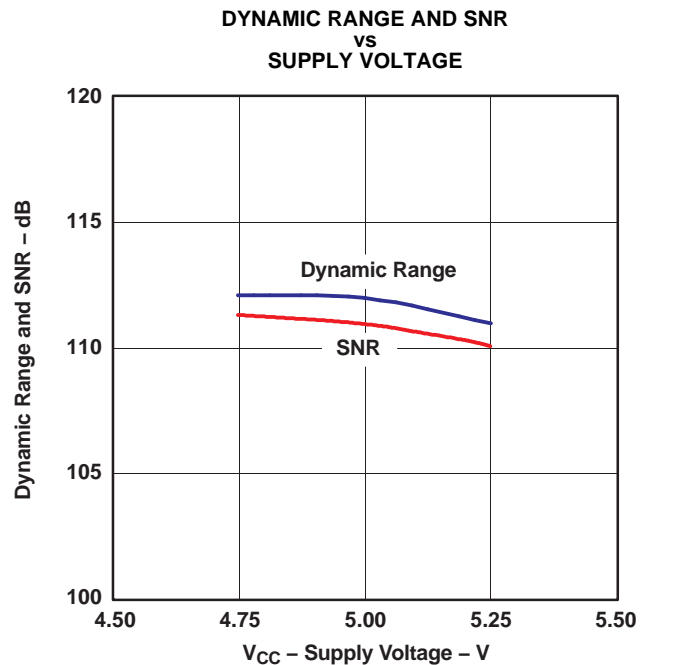


Figure 4.

**TYPICAL PERFORMANCE CURVES - SINGLE RATE (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

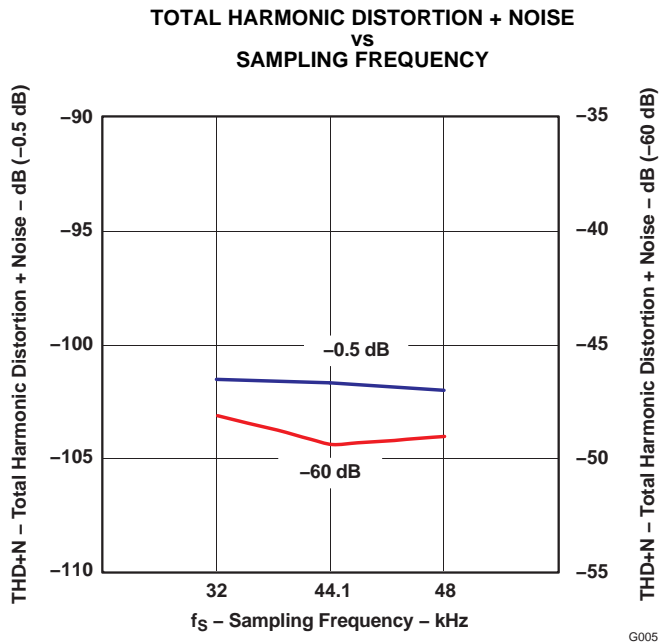


Figure 5.

G005

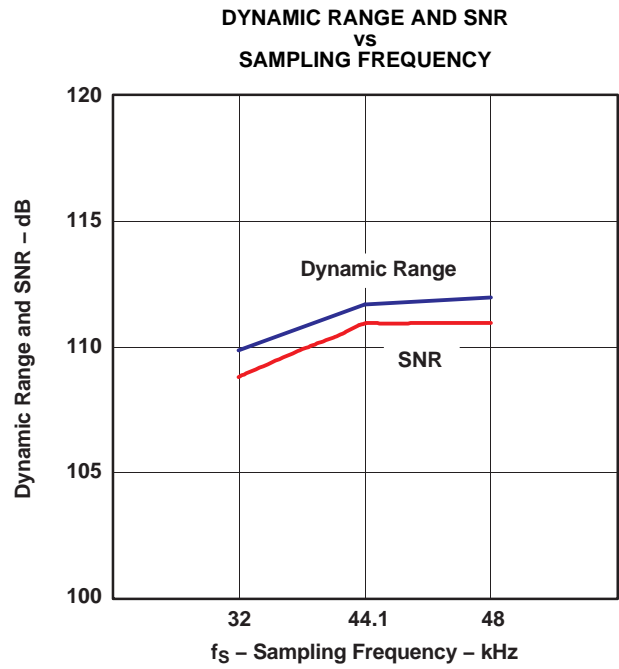


Figure 6.

G006

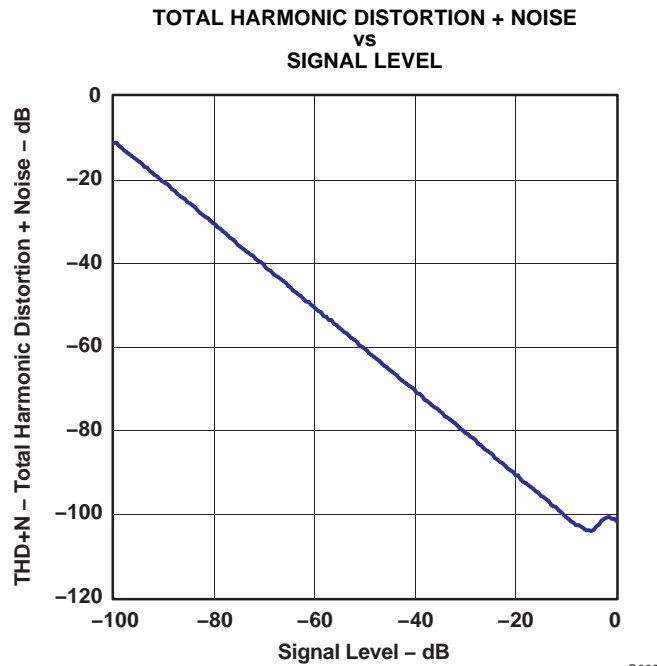


Figure 7.

G009

**TYPICAL PERFORMANCE CURVES - SINGLE RATE (continued)**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode,  $f_S = 48\text{ kHz}$ , system clock =  $256 f_S$ , 24-bit data, unless otherwise noted.

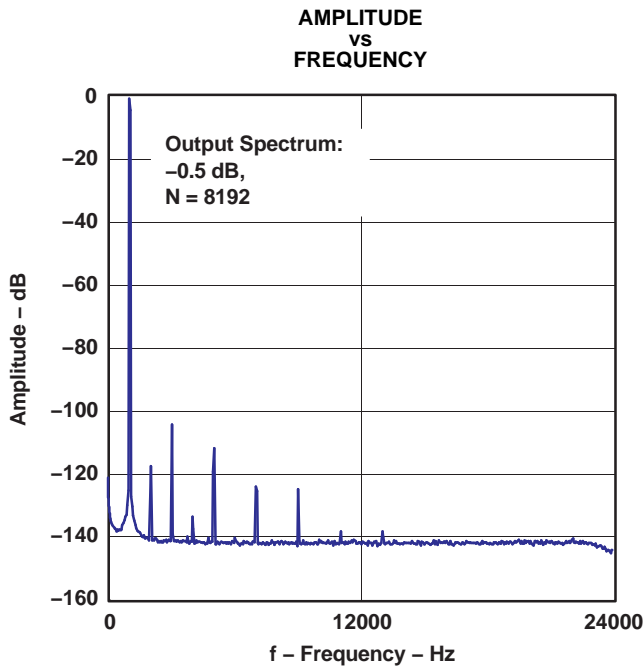


Figure 8.

G007

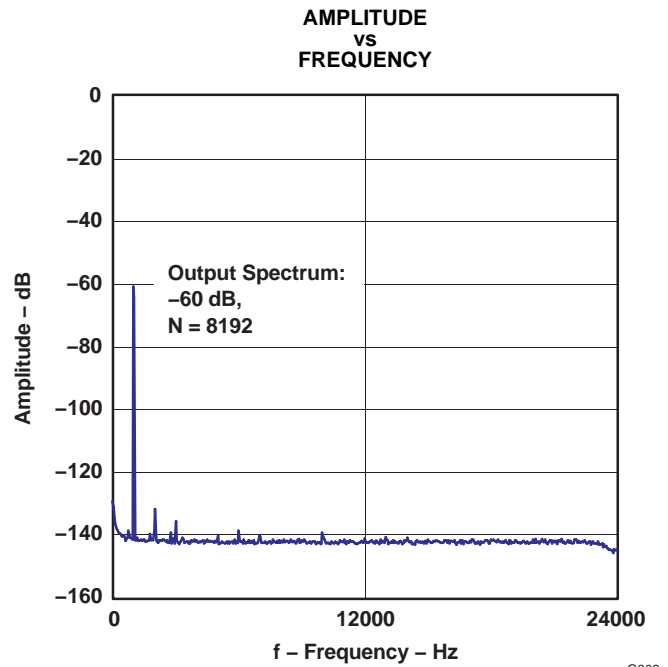


Figure 9.

G008

**TYPICAL PERFORMANCE CURVES - DUAL RATE**

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode, and 24-bit data, unless otherwise noted.

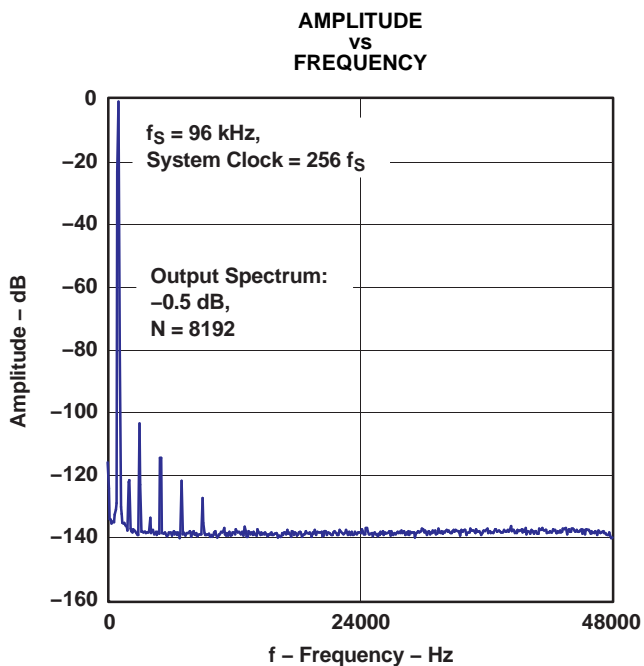


Figure 10.

G010

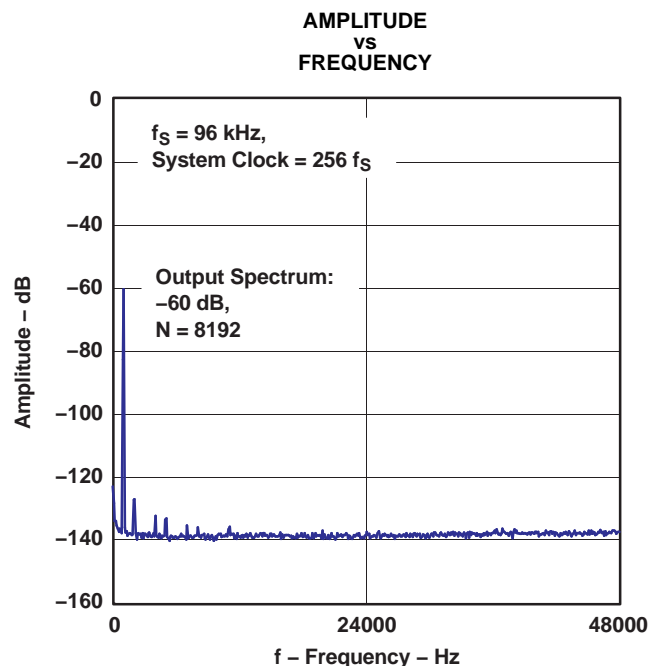


Figure 11.

G011

### TYPICAL PERFORMANCE CURVES - QUAD RATE

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode, 24-bit data, unless otherwise noted.

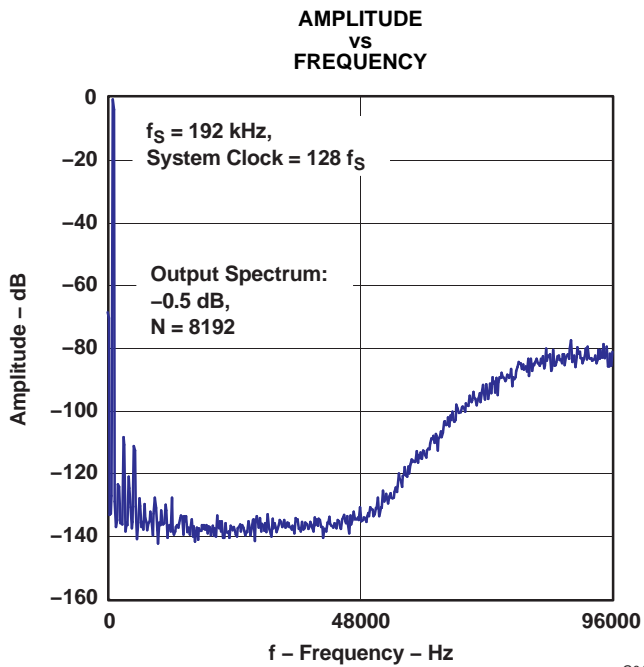


Figure 12.

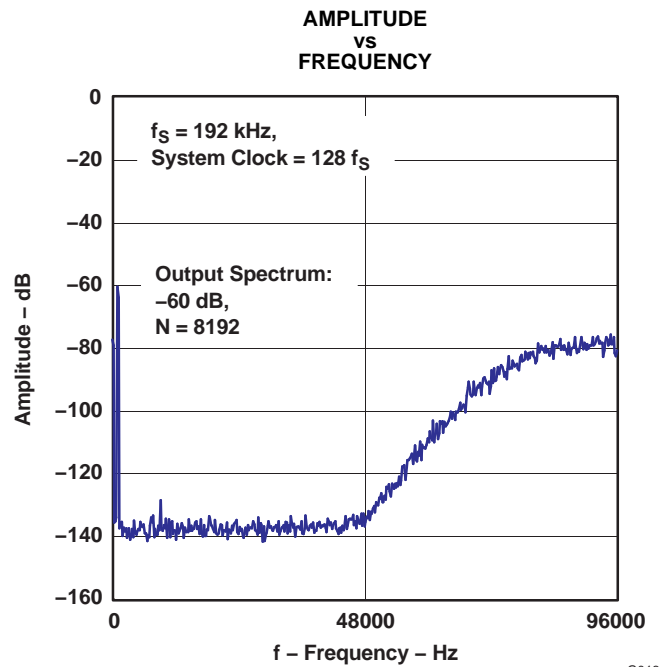


Figure 13.

### TYPICAL PERFORMANCE CURVES - DSD MODE

All specifications at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ , master mode,  $f_S = 44.1\text{ kHz}$ , system clock = 16.9344 MHz, unless otherwise noted.

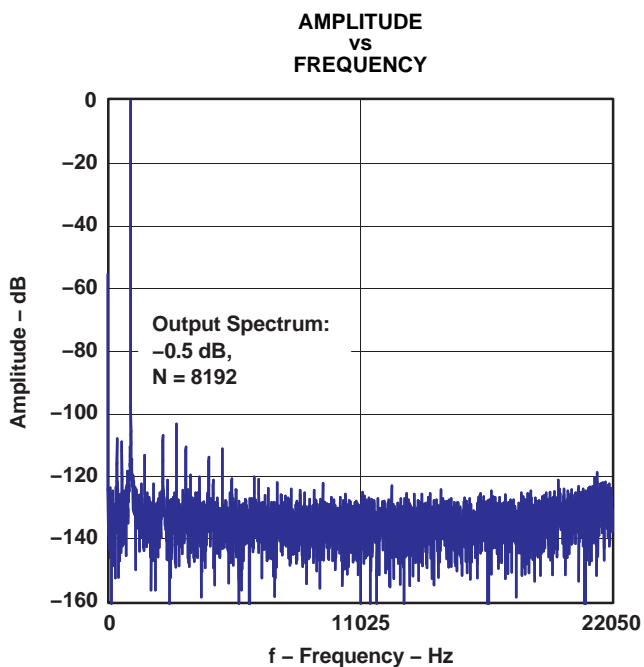


Figure 14.

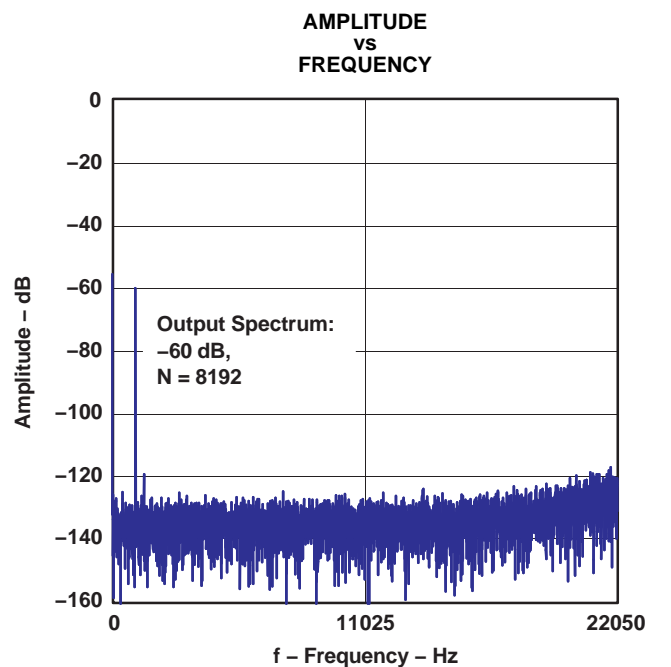
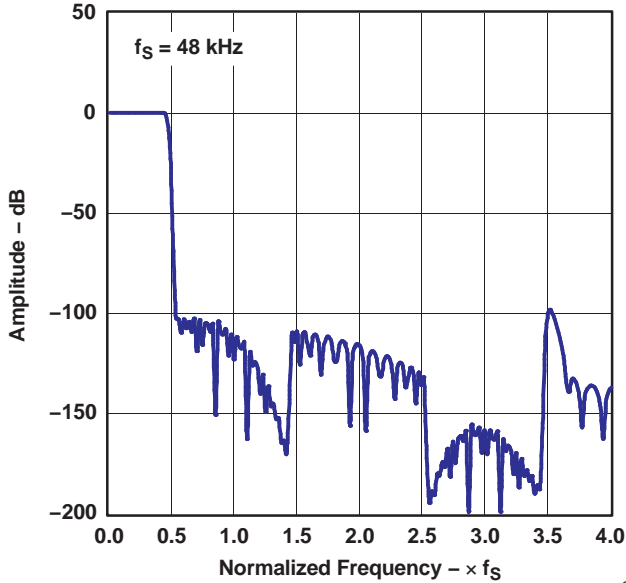


Figure 15.

**TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER**

**LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Single-Rate**

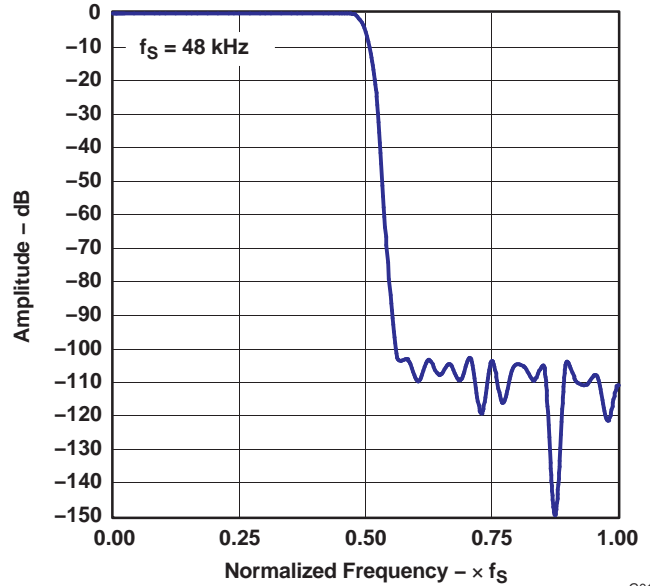
**OVERALL CHARACTERISTICS  
FOR SINGLE-RATE FILTER**



G016

Figure 16.

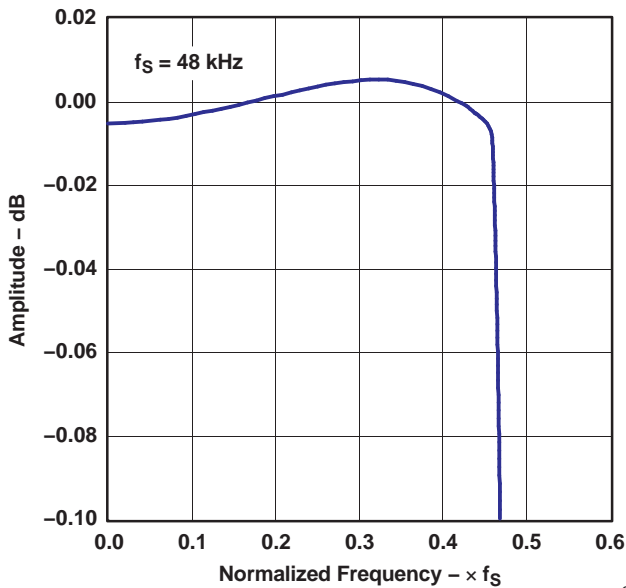
**STOP-BAND ATTENUATION CHARACTERISTICS  
FOR SINGLE-RATE FILTER**



G017

Figure 17.

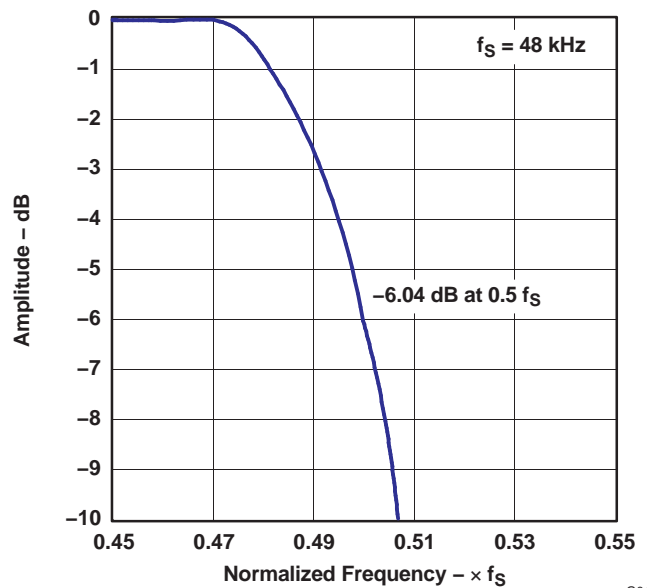
**PASS-BAND RIPPLE CHARACTERISTICS  
FOR SINGLE-RATE FILTER**



G018

Figure 18.

**TRANSIENT BAND CHARACTERISTICS  
FOR SINGLE-RATE FILTER**



G019

Figure 19.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)  
 LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Dual-Rate

OVERALL CHARACTERISTICS  
FOR DUAL-RATE FILTER

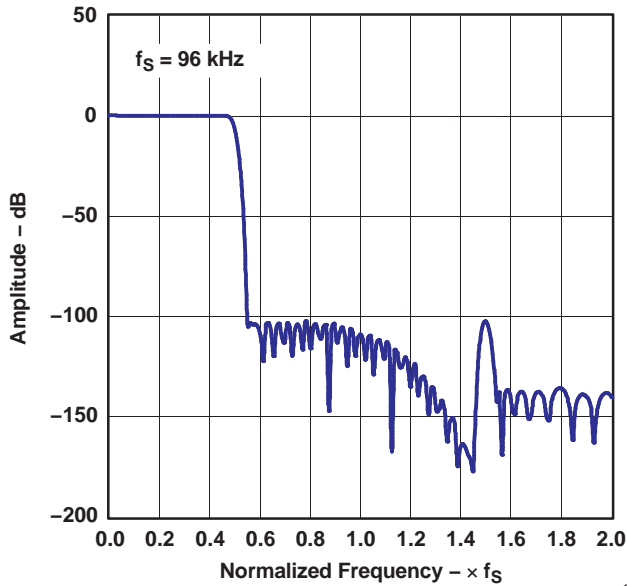


Figure 20.

STOP-BAND ATTENUATION CHARACTERISTICS  
FOR DUAL-RATE FILTER

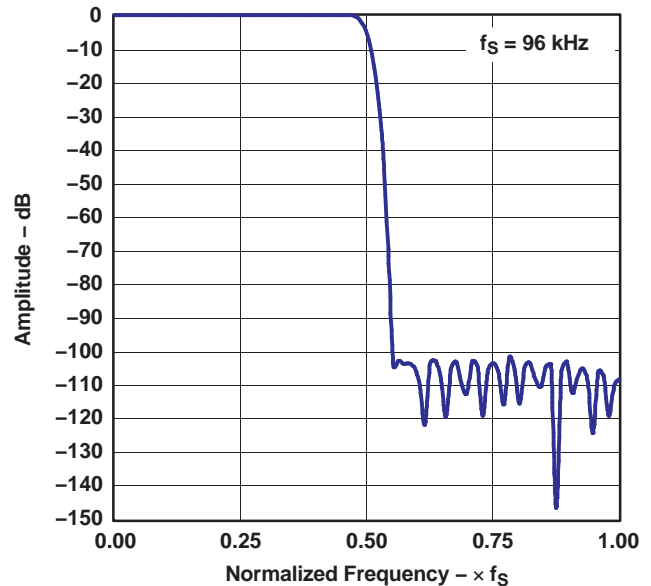


Figure 21.

PASS-BAND RIPPLE CHARACTERISTICS  
FOR DUAL-RATE FILTER

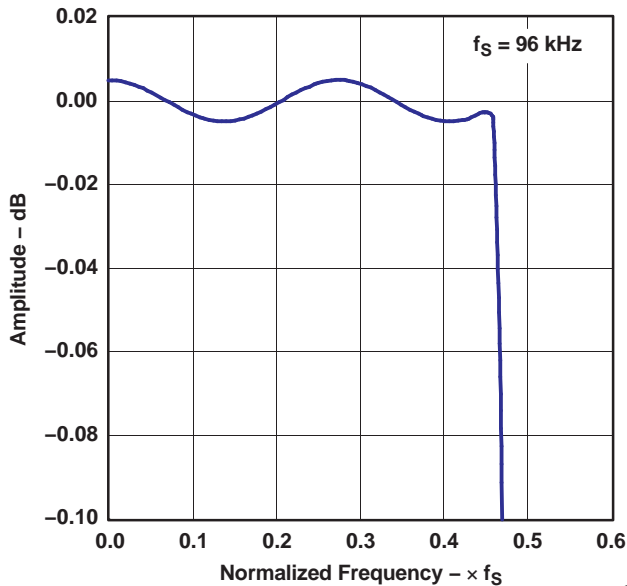


Figure 22.

TRANSIENT BAND CHARACTERISTICS  
FOR DUAL-RATE FILTER

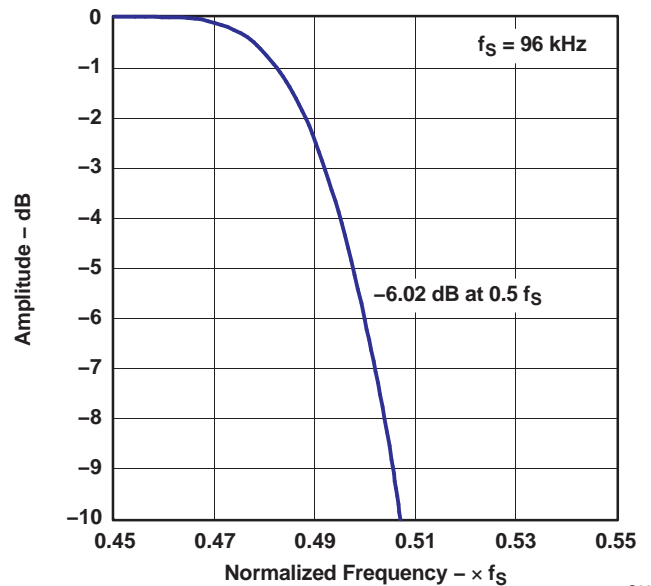


Figure 23.

**TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)**  
**LINEAR PHASE ANTIALIAS DIGITAL FILTER FREQUENCY RESPONSE - Quad-Rate**

**OVERALL CHARACTERISTICS FOR QUAD-RATE FILTER**

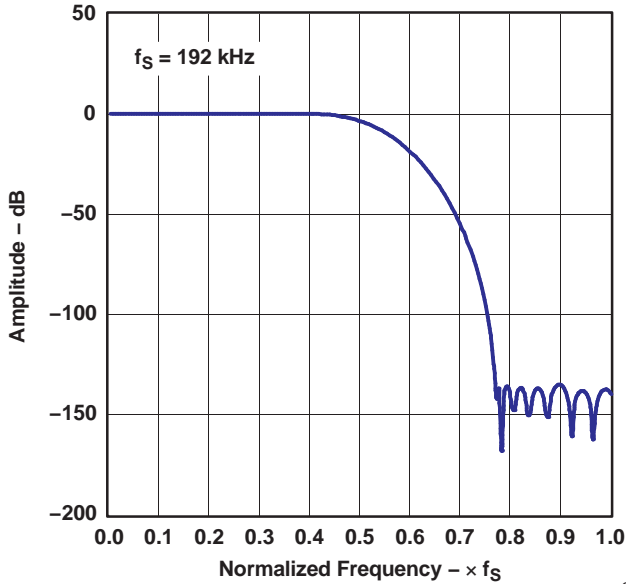


Figure 24.

G024

**STOP-BAND ATTENUATION CHARACTERISTICS FOR QUAD-RATE FILTER**

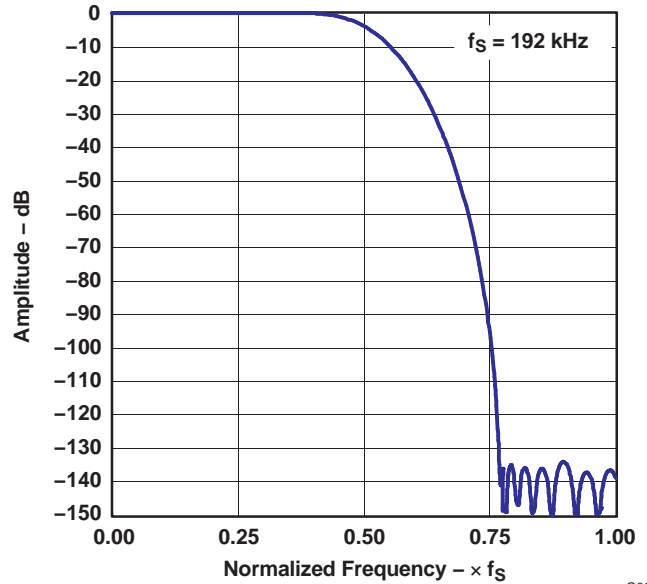


Figure 25.

G025

**PASS-BAND RIPPLE CHARACTERISTICS FOR QUAD-RATE FILTER**

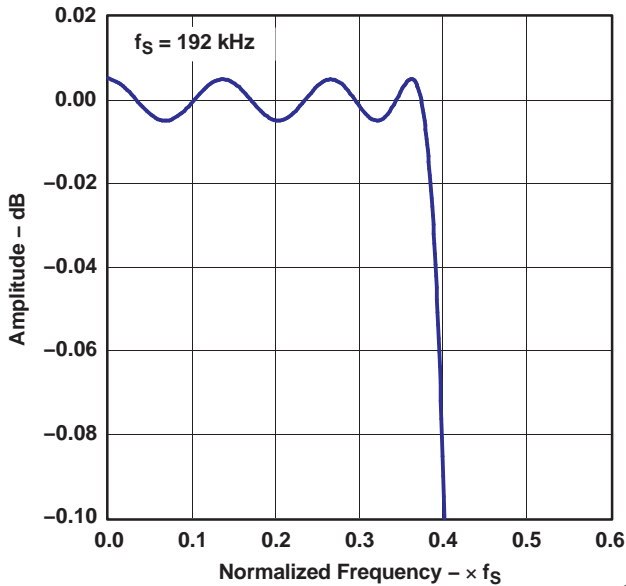


Figure 26.

G026

**TRANSIENT BAND CHARACTERISTICS FOR QUAD-RATE FILTER**

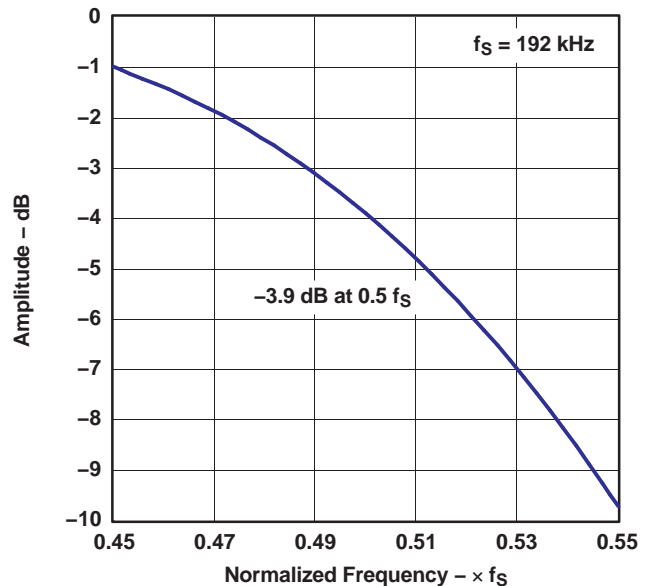


Figure 27.

G027

## TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued) HIGH-PASS FILTER (HPF) FREQUENCY RESPONSE

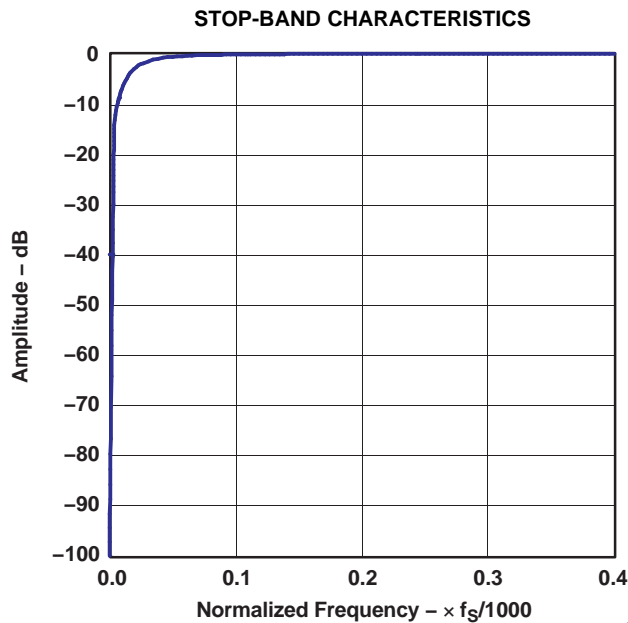


Figure 28.

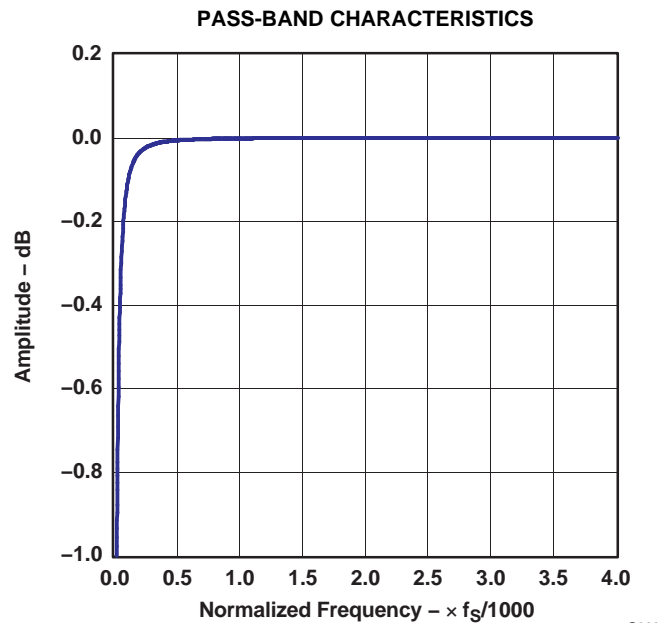


Figure 29.

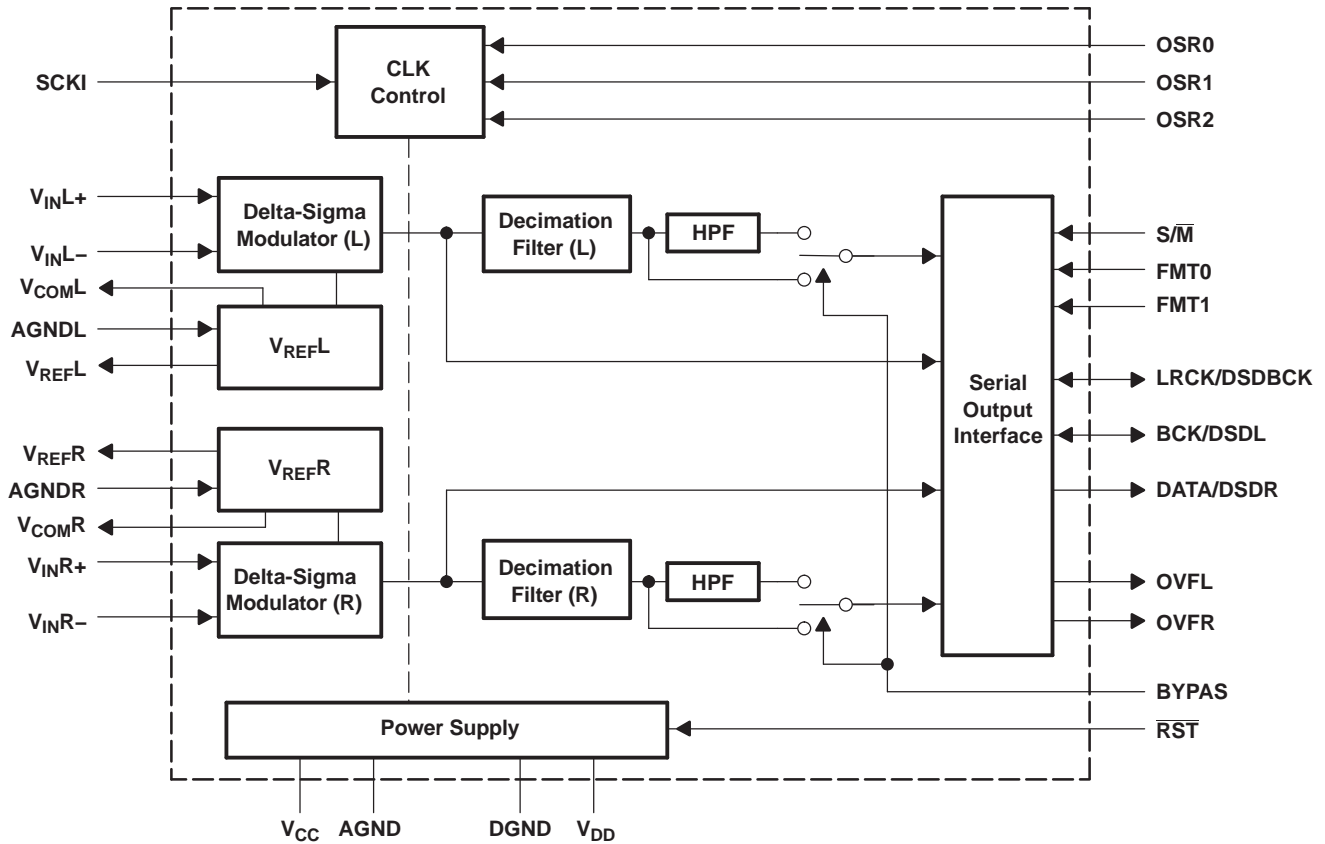
## PRINCIPLES OF OPERATION

### THEORY OF OPERATION

The PCM1804 consists of a band-gap reference, a delta-sigma modulator with full-differential architecture for L-channel and R-channel, a decimation filter with a high-pass filter, and a serial interface circuit. [Figure 30](#) illustrates the total architecture of the PCM1804. An on-chip, high-precision reference with 10- $\mu$ F external capacitor(s) provides all the reference voltage needed in the PCM1804, and it defines the full-scale voltage range of both channels. Full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance. The input signal is sampled at  $\times 128$ ,  $\times 64$ , and  $\times 32$  oversampling rates according to the oversampling ratio control, OSR[0:2]. The single rate, dual rate, and quad rate eliminate the external sample-and-hold amplifier. [Figure 31](#) illustrates how for each oversampling ratio the PCM1804 decimates the modulator output down to PCM data when the modulator is running at 6.144 MHz. The delta-sigma modulation randomizes the modulator outputs and reduces the idle tone level. The oversampled data stream from the delta-sigma modulator is converted to a  $1-f_s$ , 24-bit digital signal, while removing high-frequency noise components using a decimation filter. The dc components of the signal are removed by the HPF, and the HPF output is converted to a time-multiplexed serial signal through the serial interface, which provides flexible serial formats and master/slave modes. The PCM1804 also has a DSD output mode. The PCM1804 can output the signal directly from the modulators to DSDL (pin 16) and DSDR (pin 15).

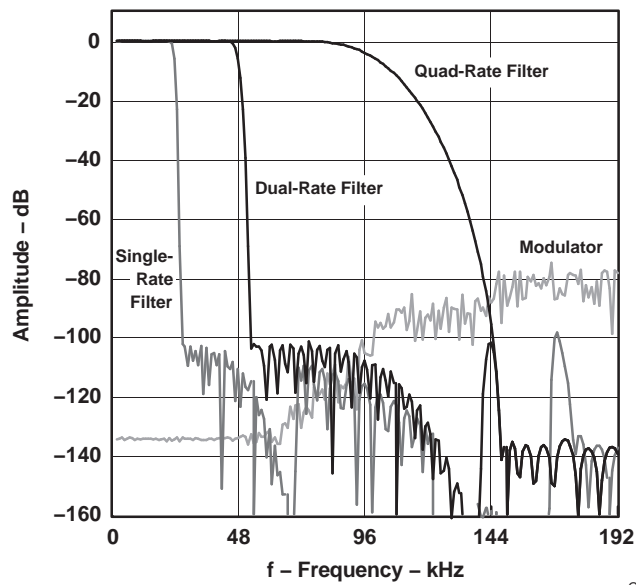


PRINCIPLES OF OPERATION (continued)



B0029-01

Figure 30. Total Block Diagram of PCM1804



G030

Figure 31. Spectrum of Modulator Output and Decimation Filter

## PRINCIPLES OF OPERATION (continued)

### SYSTEM CLOCK INPUT

The PCM1804 supports  $128 f_s$ ,  $192 f_s$  (only in master mode at quad rate),  $256 f_s$ ,  $384 f_s$ ,  $512 f_s$ , and  $768 f_s$  as a system clock, where  $f_s$  is the audio sampling frequency. The system clock must be supplied on SCKI (pin 18). [Table 3](#) shows the relationship of typical sampling frequency and the system clock frequency, and [Figure 32](#) shows system clock timing. In master mode, the system clock rate is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in [Table 1](#). In slave mode, the system clock rate is automatically detected. In DSD mode, OSR2 (pin 11), OSR1 (pin 10), OSR0 (pin 9), and the system clock frequency are fixed as shown in [Table 1](#) and [Table 3](#).

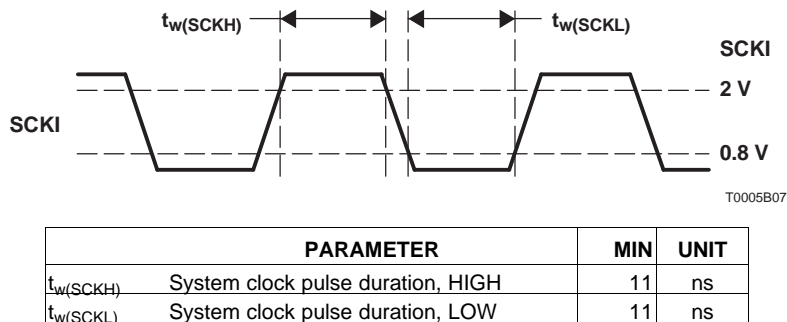


Figure 32. System Clock Input Timing

### POWER-ON AND RESET FUNCTIONS

The PCM1804 has both an internal power-on-reset circuit and  $\overline{RST}$  (pin 19). For internal power-on reset, initialization (reset) is performed automatically at the time when the power supply  $V_{DD}$  exceeds 2 V (typical) and  $V_{CC}$  exceeds 4 V (typical).  $\overline{RST}$  accepts external forced reset, and a low level on  $\overline{RST}$  initiates the reset sequence. Because an internal pulldown resistor terminates  $\overline{RST}$ , no connection of  $\overline{RST}$  is equivalent to a low-level input. Because the system clock is used as a clock signal for the reset circuit, the system clock must be supplied as soon as power is supplied; more specifically, at least three system clocks are required prior to  $V_{DD} > 2$  V,  $V_{CC} > 4$  V, and  $\overline{RST} = \text{high}$ . While  $V_{DD} < 2$  V (typical),  $V_{CC} < 4$  V (typical), or  $\overline{RST} = \text{low}$ , and  $1/f_s$  (maximum) count after  $V_{DD} > 2$  V (typical),  $V_{CC} > 4$  V (typical) and  $\overline{RST} = \text{high}$ , the PCM1804 stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of  $1116/f_s$  has passed. [Figure 33](#) and [Figure 34](#) illustrate the internal power-on-reset and external-reset timing, respectively. [Figure 35](#) illustrates the digital output for power-on reset and  $\overline{RST}$  control. The PCM1804 needs  $\overline{RST} = \text{low}$  when control pins are changed or in slave mode when SCKI, LRCK, and BCK are changed.

### POWER-DOWN FUNCTION

The PCM1804 has a power-down feature that is controlled by  $\overline{RST}$  (pin 19). Entering the power-down mode is done by keeping the  $\overline{RST}$  input level low for more than  $65536/f_s$ . In the master mode, the SCKI (pin 18) is used as the clock signal for the power-down counter. While in the slave mode, SCKI (pin 18) and LRCK (pin 17) are used as the clock signal. The clock(s) must be supplied until the power-down sequence completes. As soon as  $\overline{RST}$  goes high, the PCM1804 starts the reset-release sequence described in the *Power-On and Reset Functions* section.

### OVERSAMPLING RATIO

The oversampling ratio is selected by OSR2 (pin 11), OSR1 (pin 10), and OSR0 (pin 9) as shown in [Table 1](#) and [Table 2](#). The PCM1804 needs  $\overline{RST} = \text{low}$  when logic levels on the OSR2, OSR1, and OSR0 pins are changed.

**Table 1. Oversampling Ratio in Master Mode**

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate ( $\times 128 f_s$ )	$768 f_s$
Low	Low	High	Single rate ( $\times 128 f_s$ )	$512 f_s$
Low	High	Low	Single rate ( $\times 128 f_s$ )	$384 f_s$
Low	High	High	Single rate ( $\times 128 f_s$ )	$256 f_s$
High	Low	Low	Dual rate ( $\times 64 f_s$ )	$384 f_s$
High	Low	High	Dual rate ( $\times 64 f_s$ )	$256 f_s$
High	High	Low	Quad rate ( $\times 32 f_s$ )	$192 f_s$
High	High	High	Quad rate ( $\times 32 f_s$ )	$128 f_s$
High	Low	Low	DSD mode ( $\times 64 f_s$ )	$384 f_s$
High	Low	High	DSD mode ( $\times 64 f_s$ )	$256 f_s$

**Table 2. Oversampling Ratio in Slave Mode**

OSR2	OSR1	OSR0	OVERSAMPLING RATIO	SYSTEM CLOCK RATE
Low	Low	Low	Single rate ( $\times 128 f_s$ )	Automatically detected
Low	Low	High	Dual rate ( $\times 64 f_s$ )	Automatically detected
Low	High	Low	Quad rate ( $\times 32 f_s$ ) <sup>(1)</sup>	Automatically detected
Low	High	High	Reserved	–
High	Low	Low	Reserved	–
High	Low	High	Reserved	–
High	High	Low	Reserved	–
High	High	High	Reserved	–

(1) Only at the  $128\text{-}f_s$  system clock rate

**Table 3. Sampling Frequency and System Clock Frequency**

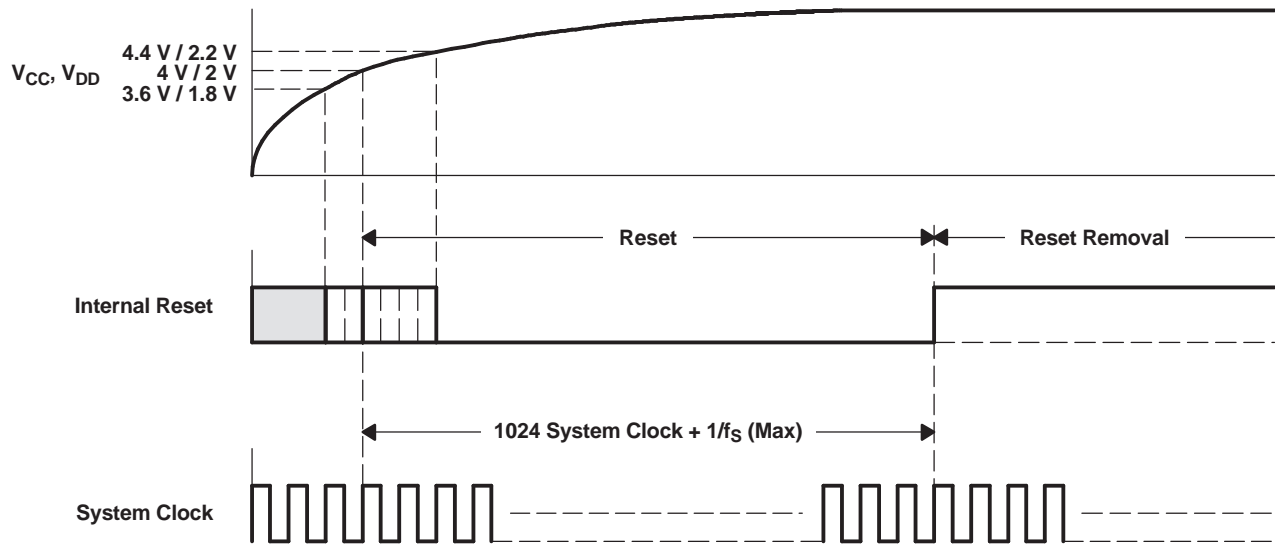
OVERSAMPLING RATIO	SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)					
		$128 f_s$	$192 f_s$ <sup>(1)</sup>	$256 f_s$	$384 f_s$	$512 f_s$	$768 f_s$
Single rate <sup>(2)</sup>	32	–	–	8.192	12.288	16.384	24.576
	44.1	–	–	11.2896	16.9344	22.5792	33.8688
	48	–	–	12.288	18.432	24.576	36.864
Dual rate <sup>(3)</sup>	88.2	–	–	22.5792	33.8688	–	–
	96	–	–	24.576	36.864	–	–
Quad rate <sup>(4)</sup>	176.4	22.5792	33.8688	–	–	–	–
	192	24.576	36.864	–	–	–	–
DSD mode <sup>(3)</sup>	44.1	–	–	11.2896	16.9344	–	–

(1) Only available in master mode at the quad rate

(2) Modulator is running at  $128 f_s$ .

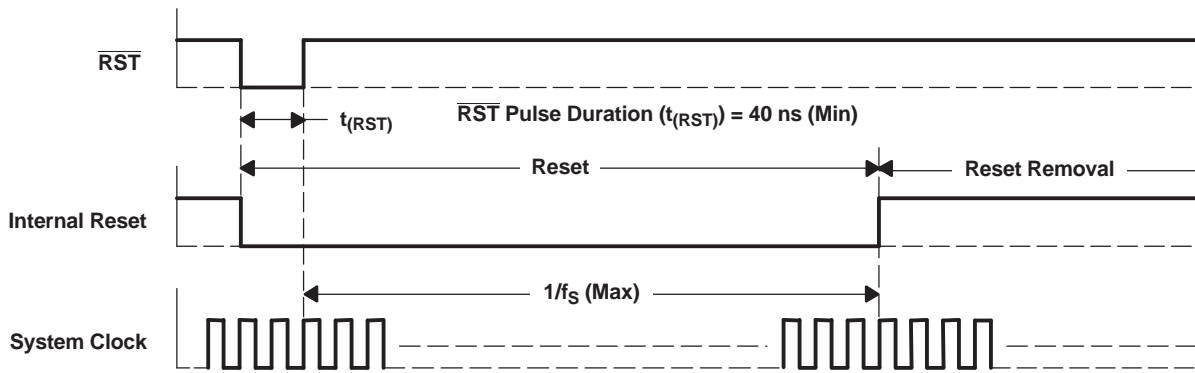
(3) Modulator is running at  $64 f_s$ .

(4) Modulator is running at  $32 f_s$ .



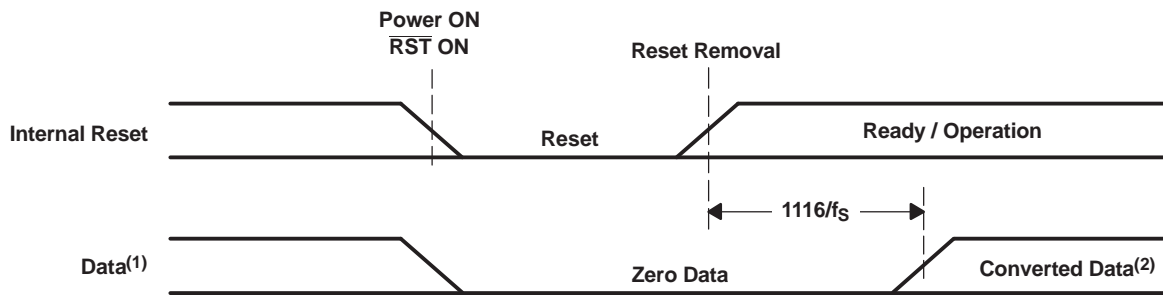
T0014-07

Figure 33. Internal Power-On-Reset Timing



T0015-05

Figure 34. External Reset Timing



T0051-01

- (1) In the DSD mode, DSDL is also controlled like DSDR.
- (2) The HPF transient response appears initially.

Figure 35. ADC Digital Output for Power-On Reset and  $\overline{RST}$  Control

## AUDIO DATA INTERFACE

The PCM1804 interfaces the audio system through BCK/DSDL (pin 16), LRCK/DSDBCK (pin 17), and DATA/DSDR (pin 15). The PCM1804 needs  $\overline{RST}$  = low when in the interface mode and/or the data format are changed.

## INTERFACE MODE

The PCM1804 supports master mode and slave mode as interface modes, which are selected by  $S/\overline{M}$  (pin 8) as shown in [Table 4](#). In master mode, the PCM1804 provides the timing of the serial audio data communications between the PCM1804 and the digital audio processor or external circuit. While in slave mode, the PCM1804 receives the timing for data transfer from an external controller. Slave mode is not available for DSD.

**Table 4. Interface Mode**

$S/\overline{M}$	MODE
Low	Master mode
High	Slave mode

## DATA FORMAT

The PCM1804 supports four audio data formats in both master and slave modes, and these data formats are selected by FMT0 (pin 6) and FMT1 (pin 7) as shown in [Table 5](#).

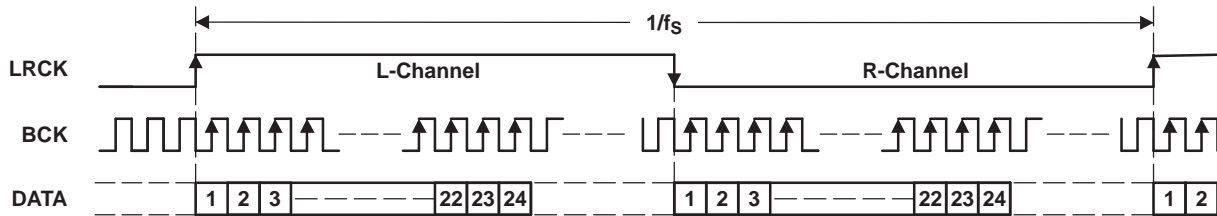
**Table 5. Data Format**

FMT1	FMT0	FORMAT	MASTER	SLAVE
Low	Low	PCM, left-justified, 24-bit	Yes	Yes
Low	High	PCM, I <sup>2</sup> S, 24-bit	Yes	Yes
High	Low	PCM, standard, 24-bit	Yes	Yes
High	High	DSD	Yes	–

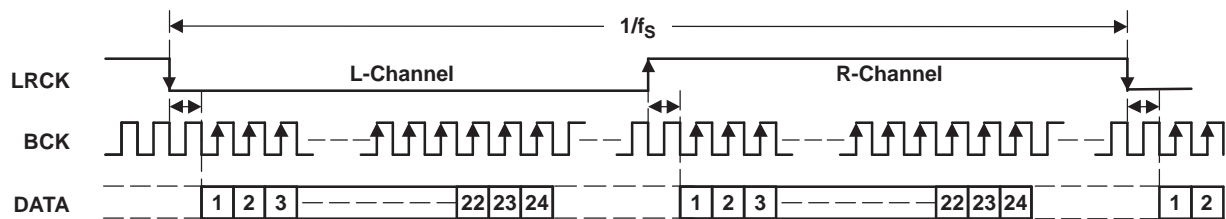
### INTERFACE TIMING FOR PCM

Figure 36 through Figure 38 illustrate the interface timing for PCM.

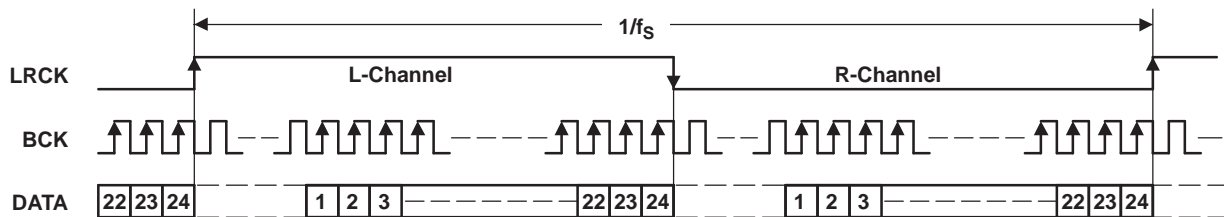
(1) Left-Justified Data Format; L-Channel = High, R-Channel = Low



(2) I<sup>2</sup>S Data Format; L-Channel = Low, R-Channel = High



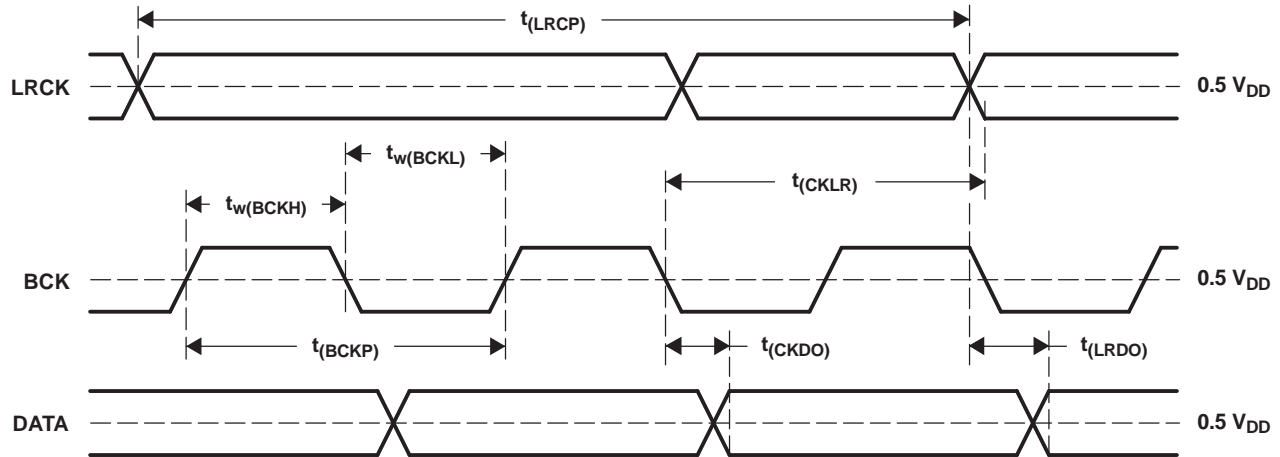
(3) Standard Data Format; L-Channel = High, R-Channel = Low



T0009-03

NOTE: LRCK and BCK work as outputs in master mode and as inputs in slave mode.

**Figure 36. Audio Data Format for PCM**

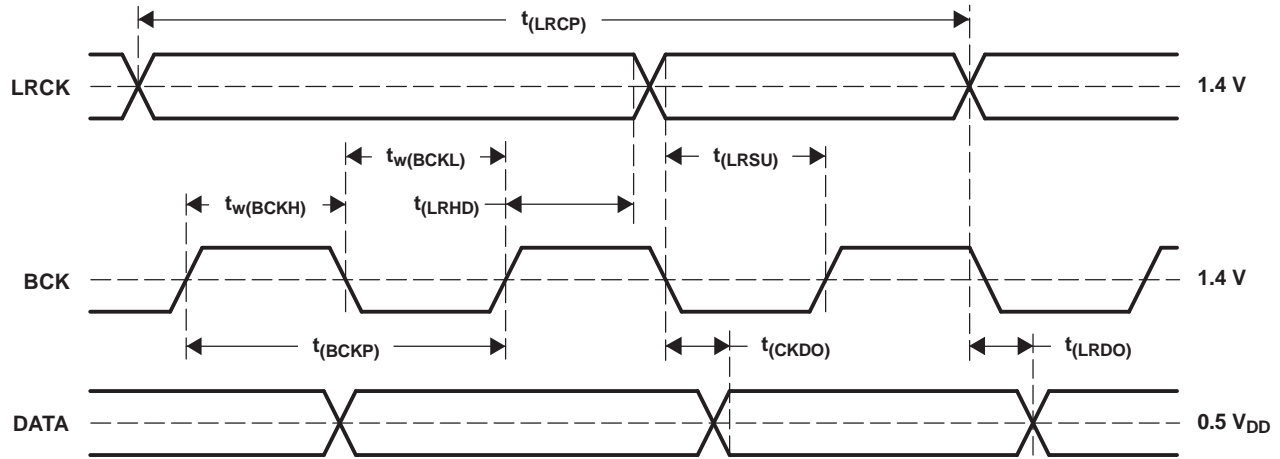


T0018-03

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period		$1/(64 f_S)^{(3)}$		
$t_{w(BCKH)}$	BCK pulse duration, HIGH	32			ns
$t_{w(BCKL)}$	BCK pulse duration, LOW	32			ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	-5		15	ns
$t_{(LRCP)}$	LRCK period		$1/f_S$		
$t_{(CKDO)}$	Delay time, BCK falling edge to DATA valid	-5		15	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DATA valid	-5		15	ns
$t_r$	Rising time of all signals <sup>(1)(2)</sup>			10	ns
$t_f$	Falling time of all signals <sup>(1)(2)</sup>			10	ns

- (1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.
- (2) Load capacitance of all signals is 10 pF.
- (3)  $t_{(BCKP)}$  is fixed at  $1/(64 f_S)$  in case of master mode.

**Figure 37. Audio Data Interface Timing for PCM (Master Mode: LRCK and BCK Work as Outputs)**



T0017-03

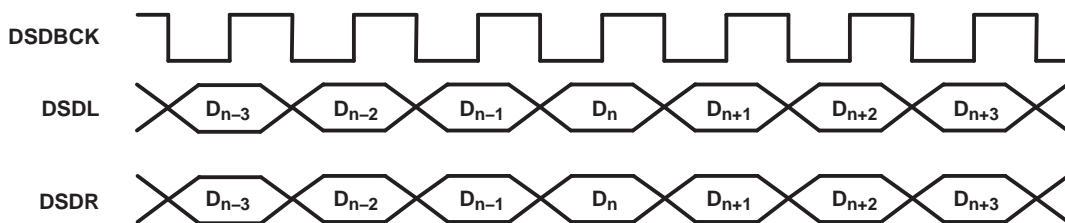
PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	$1/(64 f_S)$		$1/(48 f_S)$	
$t_{w(BCKH)}$	BCK pulse duration, HIGH	32			ns
$t_{w(BCKL)}$	BCK pulse duration, LOW	32			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	12			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	12			ns
$t_{(LRCP)}$	LRCK period		$1/f_S$		
$t_{(CKDO)}$	Delay time, BCK falling edge to DATA valid	5		25	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DATA valid	5		25	ns
$t_r$	Rising time of all signals <sup>(1)(2)</sup>			10	ns
$t_f$	Falling time of all signals <sup>(1)(2)</sup>			10	ns

- (1) Rising and falling times are measured from 10% to 90% of IN/OUT signals swing.
- (2) Load capacitance of DATA/DSDR signal is 10 pF.

**Figure 38. Audio Data Interface Timing for PCM (Slave Mode: LRCK and BCK Work as Inputs)**

### INTERFACE TIMING FOR DSD

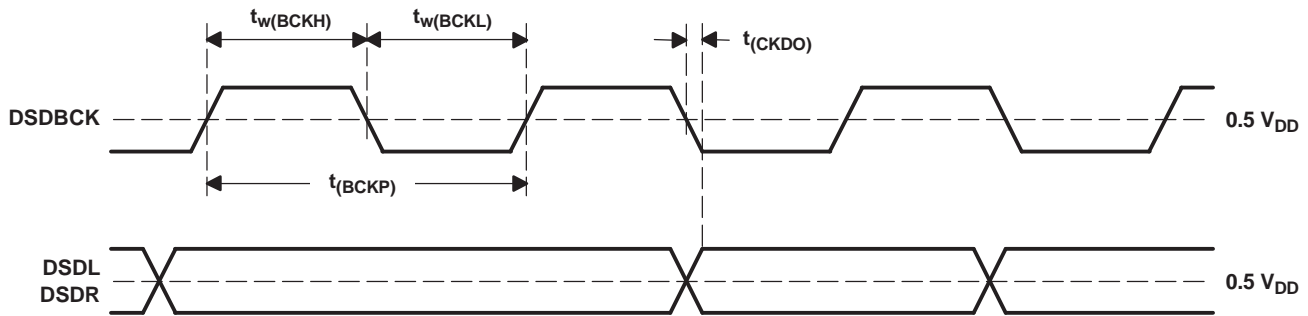
Figure 39 and Figure 40 illustrate the interface timing for DSD.



T0052-01

**Figure 39. Audio Data Format**





T0053-01

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	DSD BCK period		354		ns
$t_{w(BCKH)}$	DSD BCK pulse duration, HIGH		177		ns
$t_{w(BCKL)}$	DSD BCK pulse duration, LOW		177		ns
$t_{(CKDO)}$	Delay time DSD BCK falling edge to DSDL, DSDR valid	-5		15	ns
$t_r$	Rising time of all signals <sup>(1)(2)</sup>			10	ns
$t_f$	Falling time of all signals <sup>(1)(2)</sup>			10	ns

(1) Rising and falling times are measured from 10% to 90% of IN/OUT signal swing.

(2) Load capacitance of DSD BCK/DSDL/DSDR signal is 10 pF.

**Figure 40. Audio Data Interface Timing for DSD (Master Mode Only)**

## SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM FOR PCM

In slave mode, the PCM1804 operates under LRCK synchronized with the system clock SCKI. The PCM1804 does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than  $\pm 6$  BCK during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within  $1/f_s$  and digital output is forced into BPZ code until resynchronization between LRCK and SCKI is completed.

In case of changes less than  $\pm 5$  BCK, resynchronization does not occur and the previously described digital output control and discontinuity do not occur.

Figure 41 illustrates ADC digital output for loss of synchronization and resynchronization. During undefined data, the PCM1804 may generate some noise in the audio signal. Also, the transitions of normal to undefined data and undefined or zero data to normal cause a discontinuity of data on the digital output. This can generate noise in the audio signal. In master mode, synchronization loss never occurs.

## HIGH-PASS FILTER (HPF) BYPASS CONTROL FOR PCM

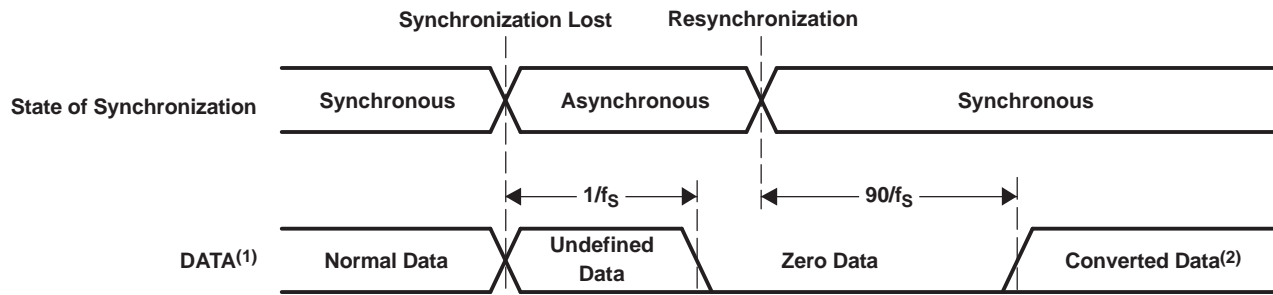
The built-in function for dc component rejection can be bypassed by BYPAS (pin 12) control. In bypass mode, the dc component of the input analog signal and the internal dc offset are also converted and output in the digital output data.

### HPF Bypass Control

BY PAS PIN	HPF MODE
Low	Normal (high-pass) mode
High	Bypass (through) mode

**OVERFLOW FLAG FOR PCM**

The PCM1804 has two overflow flag pins, OVFR (pin 20) and OVFL (pin 21). The pins go to high as soon as the analog input goes across the full-scale range. The high level is held for 1.016 s at maximum, and returns to low if the analog input does not go across the full-scale range for the period.



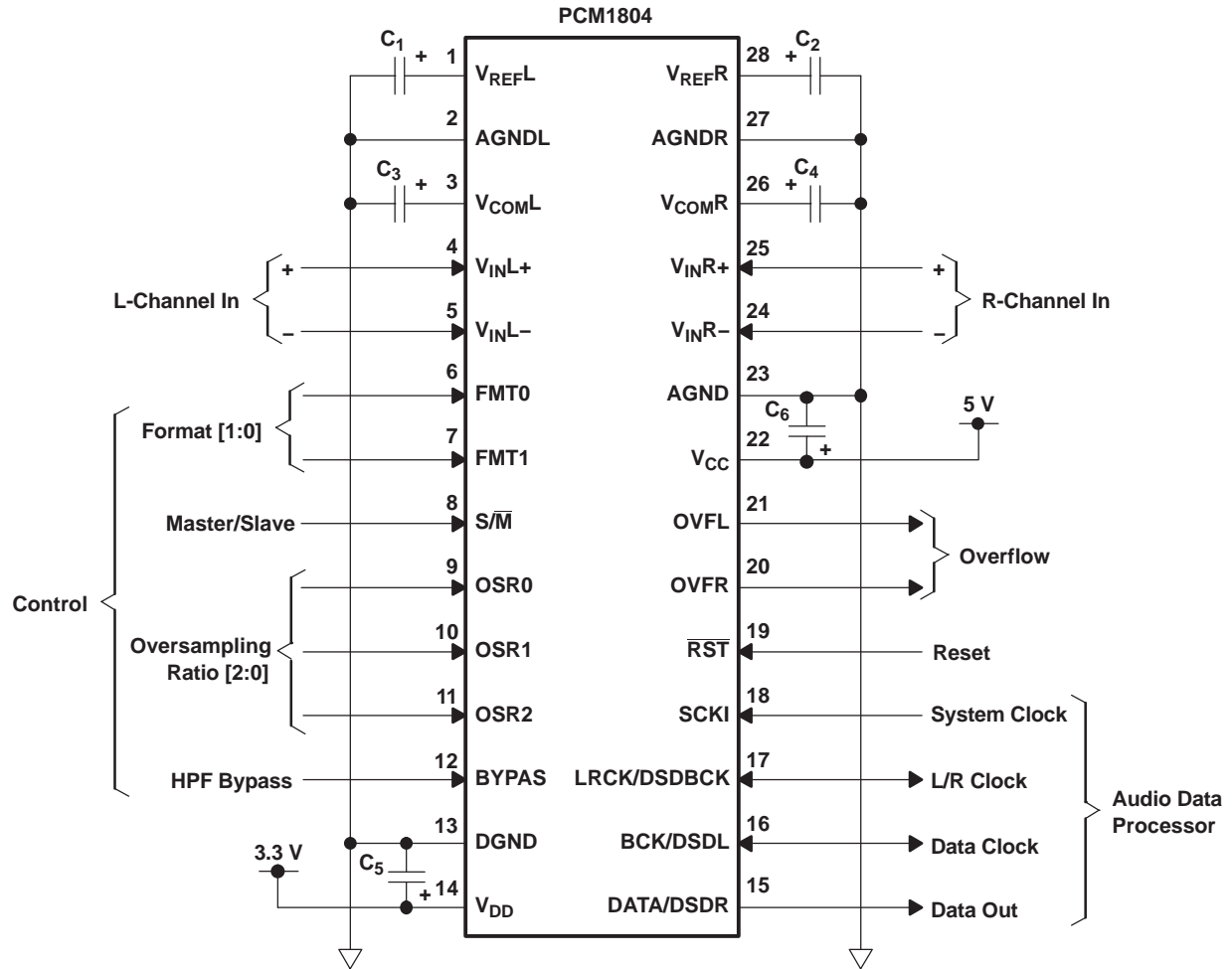
T0020-06

- (1) Applies only for slave mode; the loss of synchronization never occurs in master mode.
- (2) The HPF transient response appears initially.

**Figure 41. ADC Digital Output for Loss of Synchronization and Resynchronization**

## TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 42 illustrates a typical circuit connection diagram in the PCM data format operation.

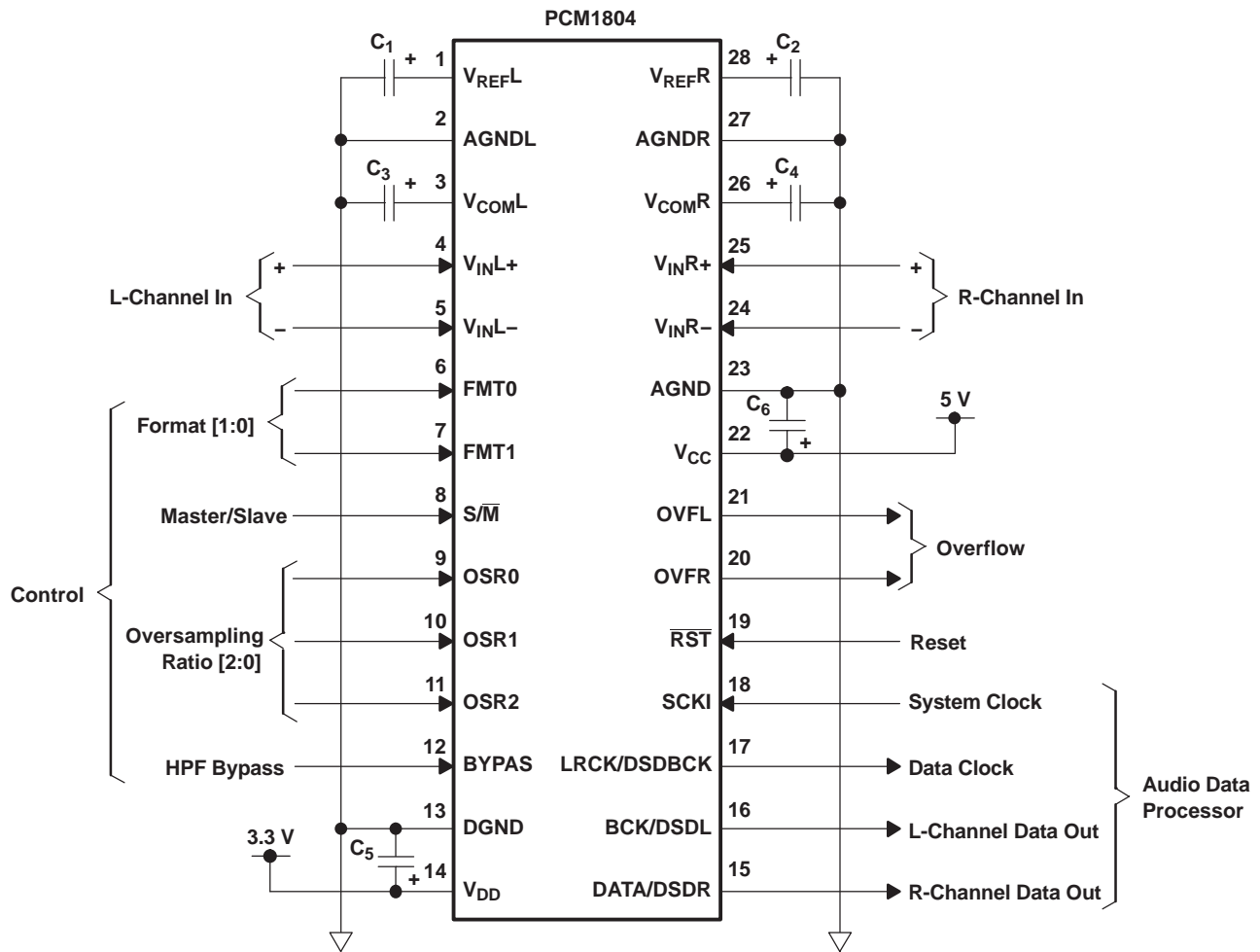


S0058-01

- A. C1, C2, C5, and C6: Bypass capacitors, 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum, depending on layout and power supply
- B. C3, C4: Bypass capacitor, 0.1- $\mu$ F tantalum, depending on layout and power supply

**Figure 42. Typical Circuit Connection Diagram for PCM**

Figure 43 illustrates a typical circuit connection diagram in the DSD data format operation.



S0058-02

- A. C1, C2, C5, and C6: Bypass capacitors, 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum, depending on layout and power supply
- B. C3 and C4: Bypass capacitors, 0.1- $\mu$ F tantalum, depending on layout and power supply

**Figure 43. Typical Circuit Connection Diagram for DSD**

## APPLICATION INFORMATION

### BOARD DESIGN AND LAYOUT CONSIDERATIONS

#### $V_{CC}$ , $V_{DD}$ Pins

The digital and analog power supply lines to the PCM1804 should be bypassed to the corresponding ground pins with 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum capacitors placed as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1804 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power-supply trouble like latch-up or power-supply sequence.

#### $V_{IN}$ Pins

Use of 0.01- $\mu$ F film capacitors between  $V_{INL+}$  and  $V_{INL-}$  and between  $V_{INR+}$  and  $V_{INR-}$  is strongly recommended to remove higher-frequency noise from the delta-sigma input section.

#### $V_{REFX}$ , $V_{COMX}$ Inputs

Use 0.1- $\mu$ F ceramic and 10- $\mu$ F tantalum capacitors between  $V_{REFL}$ ,  $V_{REFR}$ , and corresponding AGNDx, to ensure low-source impedance at ADC references. Use 0.1- $\mu$ F tantalum capacitors between  $V_{COML}$ ,  $V_{COMR}$  and corresponding AGNDx to ensure low source impedance of common voltage. These capacitors should be located as close as possible to the  $V_{REFL}$ ,  $V_{REFR}$ ,  $V_{COML}$ , and  $V_{COMR}$  pins to reduce dynamic errors on references and common voltage. The dc voltage level of these pins is 2.5 V.

#### DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK Pins

The DATA/DSDR, BCK/DSDL, and LRCK/DSDBCK pins in master mode have large load drive capability. Locating the buffer near the PCM1804 and minimizing the load capacitance, minimizes the digital-analog crosstalk and maximizes the dynamic performance of the ADC.

#### System Clock

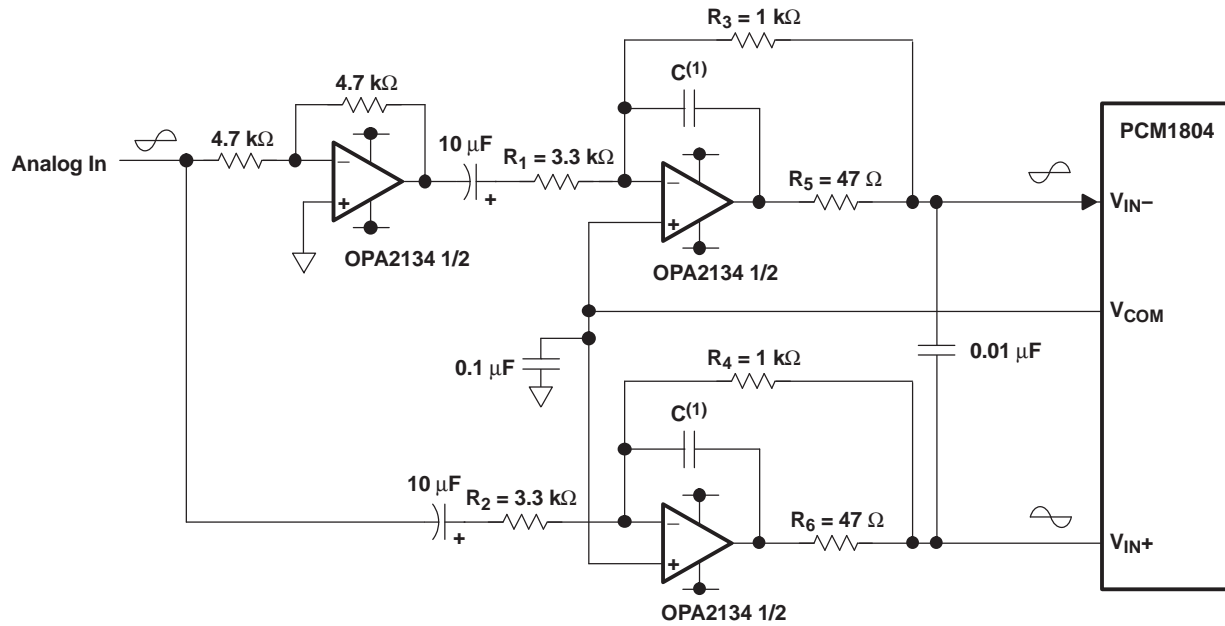
The quality of the system clock can influence dynamic performance, as the PCM1804 operates based on a system clock. Therefore, it might be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK/DSDL or LRCK/DSDBCK transition in slave mode.

#### Reset Control

If capacitors larger than 10  $\mu$ F are used on  $V_{REFL}$  and  $V_{REFR}$ , an external reset control with a delay time corresponding to the  $V_{REFL}$  and  $V_{REFR}$  response is required. Also, it works as a power-down control.

### APPLICATION CIRCUIT FOR SINGLE-ENDED INPUT

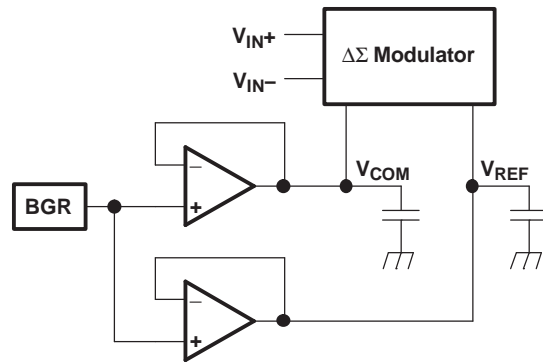
An application diagram for a single-ended input circuit is shown in [Figure 44](#). The maximum signal input voltage and differential gain of this circuit is designed as  $V_{inmax} = 8.28 V_{pp}$ ,  $A_d = 0.3$ . Differential gain ( $A_d$ ) is given by  $R3/R1(R4/R2)$  in a circuit configured as a normal inverted-gain amplifier. Resistor  $R5(R6)$  in the feedback loop gives low-impedance drive operation and noise filtering for the analog input of the PCM1804. The circuit technique using  $R5(R6)$  is recommended.



S0059-01

- (1) A capacitor value of 1800 pF is recommended, unless an input signal greater than -6 dBFS at 100 kHz or higher is applied in the DSD mode. In that case, 3300 pF is recommended.

**Figure 44. Application Circuit for Single-Ended Input Circuit (PCM)**



S0060-01

**Figure 45. Equivalent Circuit of Internal Reference ( $V_{COM}$ ,  $V_{REF}$ )**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1804DB	ACTIVE	SSOP	DB	28	47	RoHS & Green	Call TI   NIPDAU	Level-1-260C-UNLIM	-10 to 70	PCM1804	Samples
PCM1804DBG4	ACTIVE	SSOP	DB	28	47	RoHS & Green	Call TI	Level-1-260C-UNLIM	-10 to 70	PCM1804	Samples
PCM1804DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	Call TI   NIPDAU	Level-1-260C-UNLIM	-10 to 70	PCM1804	Samples
PCM1804DBRG4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-10 to 70	PCM1804	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF PCM1804 :**

- Automotive : [PCM1804-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1804DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

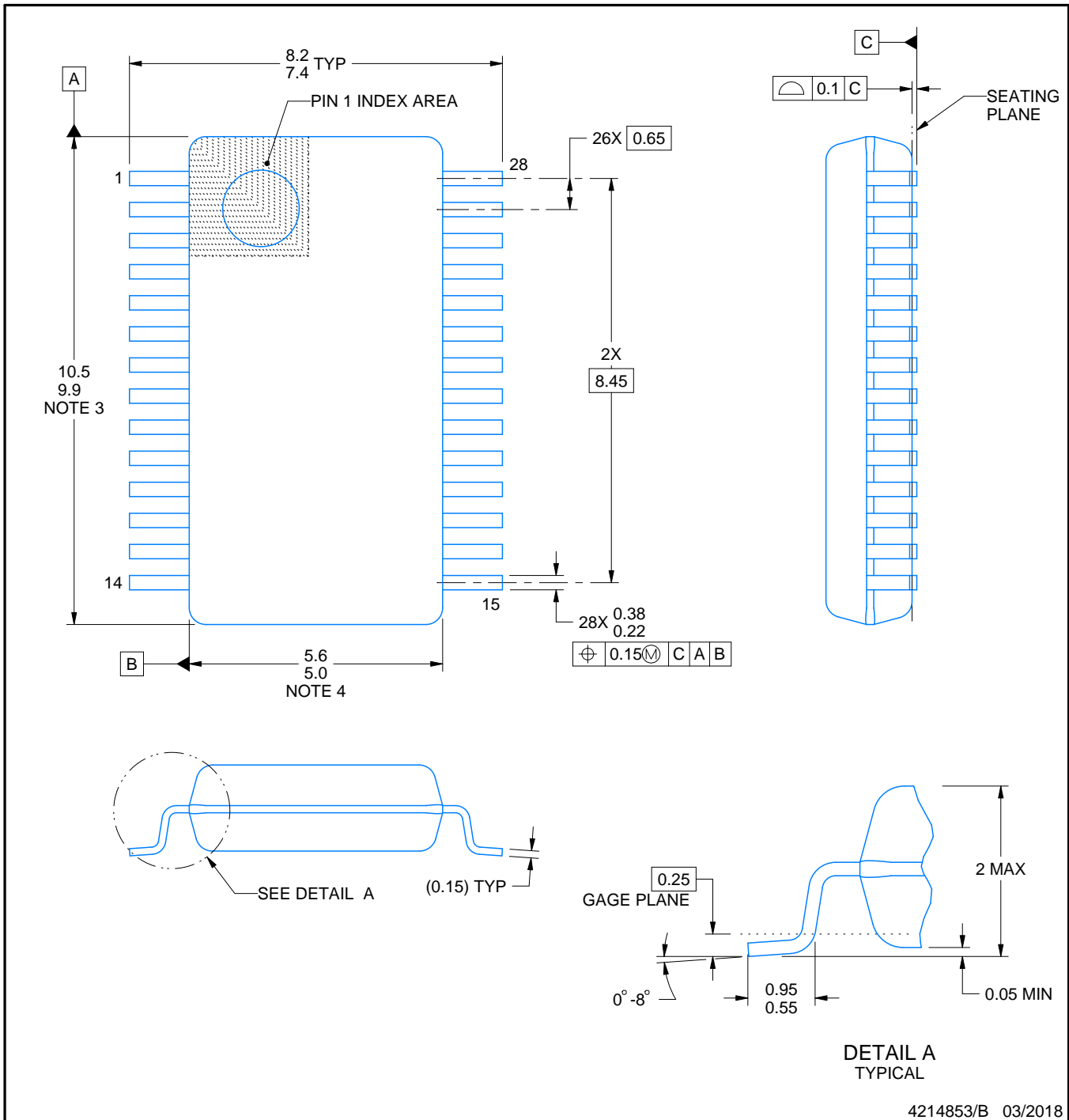
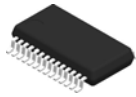

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1804DBR	SSOP	DB	28	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCM1804DB	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DB	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DB	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DBG4	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DBG4	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DBG4	DB	SSOP	28	47	530	10.5	4000	4.1
PCM1804DBR	DB	SSOP	28	2000	530	10.5	4000	4.1
PCM1804DBRG4	DB	SSOP	28	2000	530	10.5	4000	4.1



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NOTES:

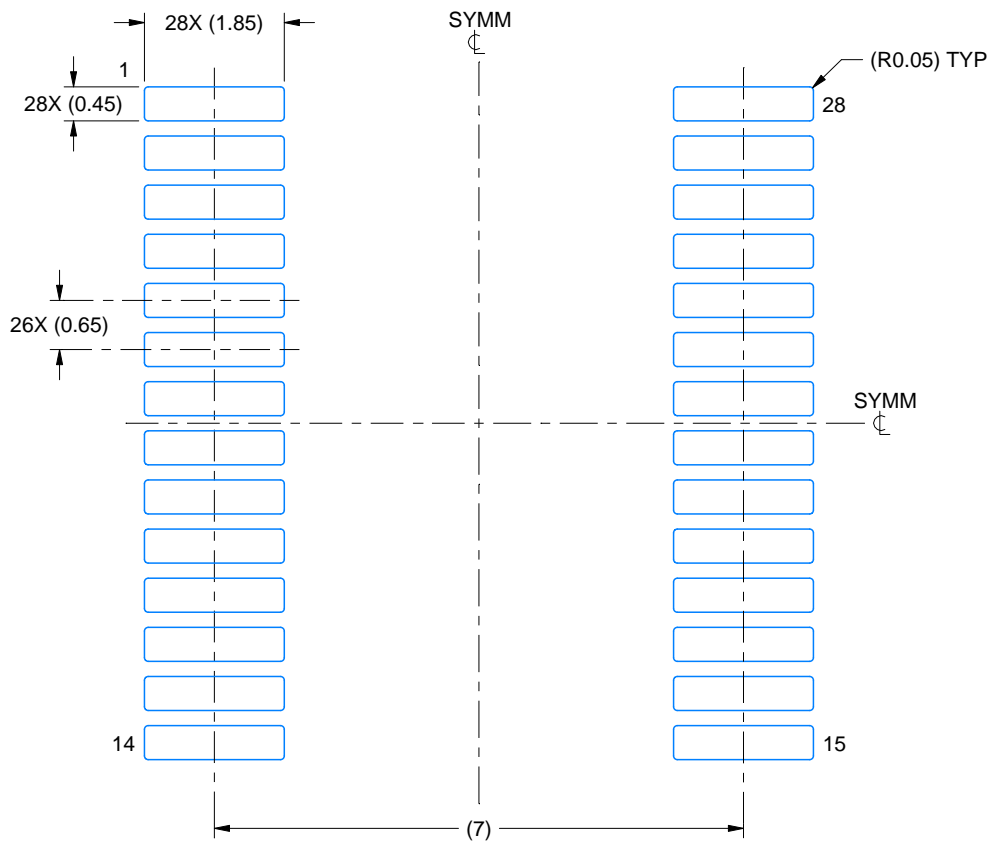
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

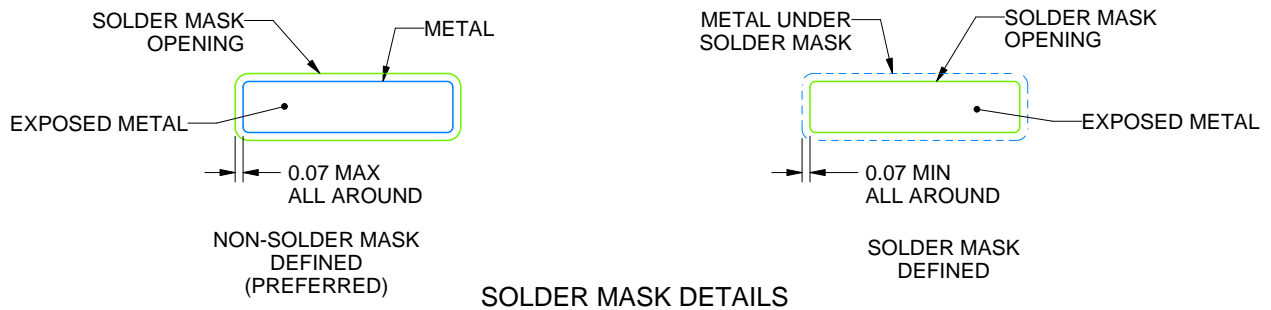
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

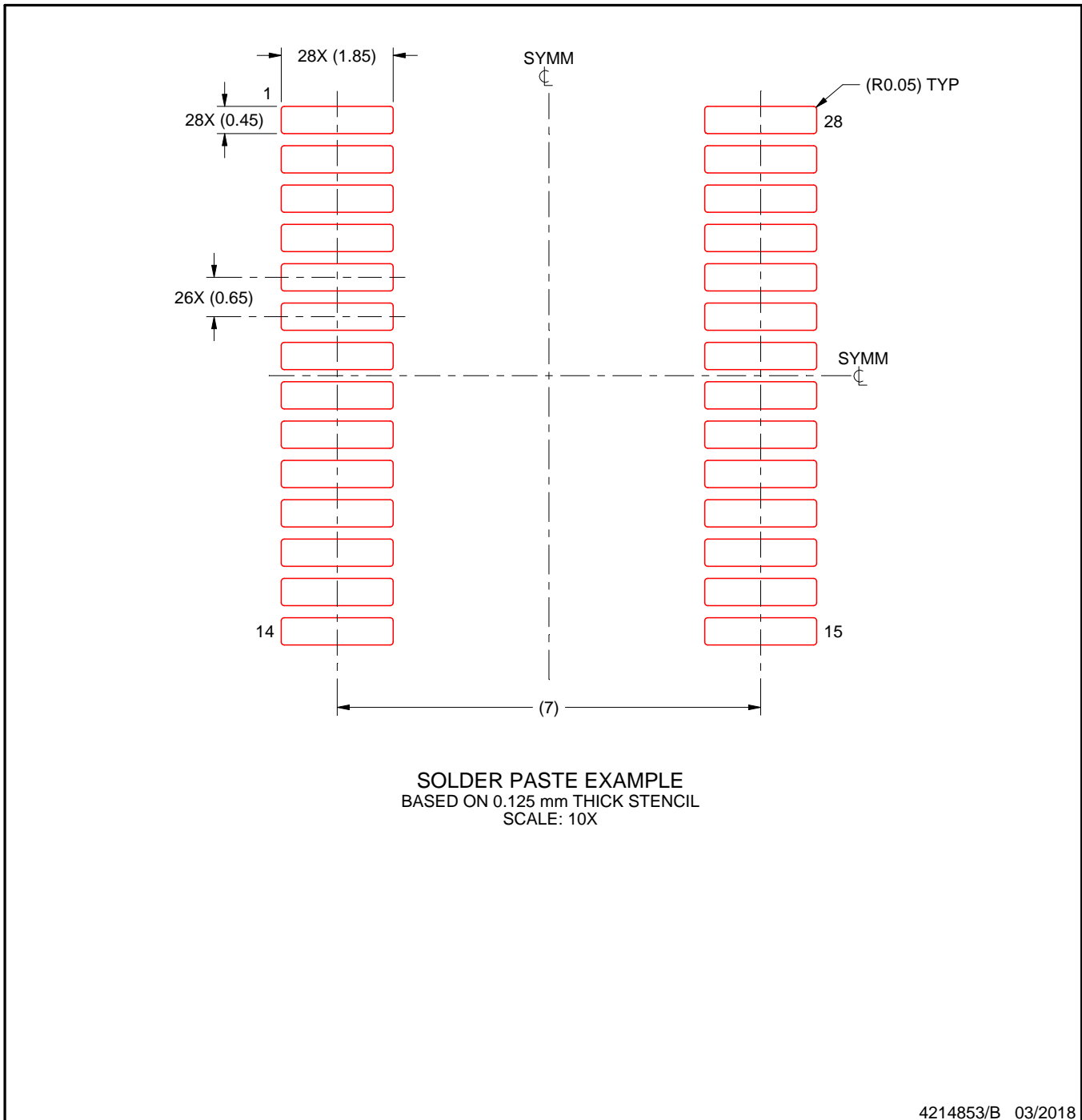
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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