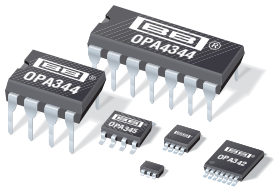


www.ti.com

SBOS107A – APRIL 2000 – REVISED AUGUST 2008

# LOW POWER, SINGLE-SUPPLY, RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

## *Micro*Amplifier™ Series

## FEATURES

- RAIL-TO-RAIL INPUT
- RAIL-TO-RAIL OUTPUT (within 1mV)
- LOW QUIESCENT CURRENT: 150μA typ
- *Micro*SIZE PACKAGES
  - SOT23-5
  - MSOP-8
  - TSSOP-14
- GAIN-BANDWIDTH
  - OPA344: 1MHz, G ≥ 1
  - OPA345: 3MHz, G ≥ 5
- SLEW RATE
  - OPA344: 0.8V/μs
  - OPA345: 2V/μs
- THD + NOISE: 0.006%

## APPLICATIONS

- PCMCIA CARDS
- DATA ACQUISITION
- PROCESS CONTROL
- AUDIO PROCESSING
- COMMUNICATIONS
- ACTIVE FILTERS
- TEST EQUIPMENT

## DESCRIPTION

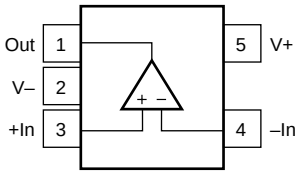
The OPA344 and OPA345 series rail-to-rail CMOS operational amplifiers are designed for precision, low-power, miniature applications. The OPA344 is unity gain stable, while the OPA345 is optimized for gains greater than or equal to five, and has a gain-bandwidth product of 3MHz.

The OPA344 and OPA345 are optimized to operate on a single supply from 2.5V and up to 5.5V with an input common-mode voltage range that extends 300mV beyond the supplies. Quiescent current is only 250μA (max).

Rail-to-rail input and output make them ideal for driving sampling analog-to-digital converters. They are also well suited for general purpose and audio applications and providing I/V conversion at the output of D/A converters. Single, dual and quad versions have identical specs for design flexibility.

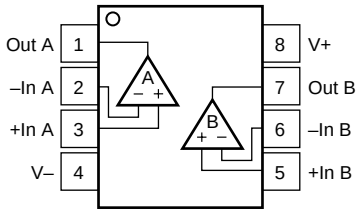
A variety of packages are available. All are specified for operation from –40ºC to 85ºC. A SPICE macromodel for design analysis is available for download from www.ti.com.

OPA344, OPA345



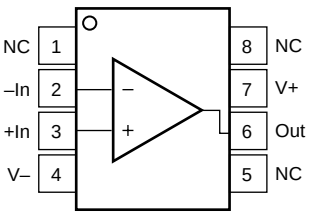

SOT23-5

OPA2344, OPA2345



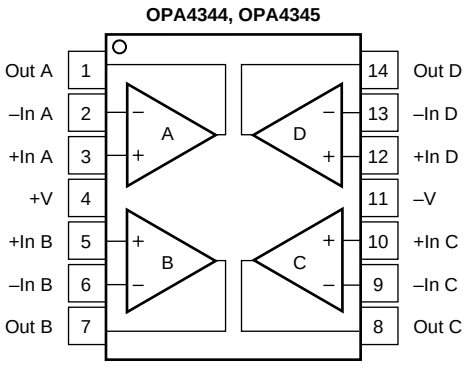

SO-8, MSOP-8, 8-Pin DIP (OPA2344 Only)

OPA344, OPA345




SO-8, 8-Pin DIP (OPA344 Only)

OPA4344, OPA4345




TSSOP-14, SO-14, 14-PIn DIP (OPA4344 Only)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

# SPECIFICATIONS: $V_S$ = 2.7V to 5.5V

At $T_A$ = +25°C, $R_L$ = 10kΩ connected to $V_S/2$ and $V_{OUT}$ = $V_S/2$, unless otherwise noted.
**Boldface** limits apply over the temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITION | OPA344NA, UA, PA<br>OPA2344EA, UA, PA<br>OPA4344EA, UA, PA<br>MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = +5.5V, $V_{CM}$ = $V_S/2$ | | ±0.2 | ±1 | mV |
| **Over Temperature** | | | | **±0.8** | **±1.2** | mV |
| **vs Temperature** | **$dV_{OS}/dT$** | | | **±3** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.7V to 5.5V, $V_{CM}$ < (V+) -1.8V | | 30 | 200 | µV/V |
| **Over Temperature** | | **$V_S$ = 2.7V to 5.5V, $V_{CM}$ < (V+) -1.8V** | | | **250** | µV/V |
| Channel Separation, dc | | | | 0.2 | | µV/V |
| f = 1kHz | | | | 130 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.2 | ±10 | pA |
| **Over Temperature** | | | | **See Typical Curve** | | pA |
| Input Offset Current | $I_{OS}$ | | | ±0.2 | ±10 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise | | f = 0.1 to 50kHz | | 8 | | µVrms |
| Input Voltage Noise Density | $e_n$ | f = 10kHz | | 30 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10kHz | | 0.5 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.3 | | (V+) + 0.3 | V |
| Common-Mode Rejection Ratio | CMRR | $V_S$ = +5.5V, –0.3V < $V_{CM}$ < (V+)-1.8 | 76 | 92 | | dB |
| **Over Temperature** | | **$V_S$ = +5.5V, –0.3V < $V_{CM}$ < (V+)-1.8** | **74** | | | dB |
| Common-Mode Rejection | CMRR | $V_S$ = +5.5V, –0.3V < $V_{CM}$ < 5.8V | 70 | 84 | | dB |
| **Over Temperature** | | **$V_S$ = +5.5V, –0.3V < $V_{CM}$ < 5.8V** | **68** | | | dB |
| Common-Mode Rejection | CMRR | $V_S$ = +2.7V, –0.3V < $V_{CM}$ < 3V | 66 | 80 | | dB |
| **Over Temperature** | | **$V_S$ = +2.7V, –0.3V < $V_{CM}$ < 3V** | **64** | | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 6 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 100kΩ, 10mV < $V_O$ < (V+) –10mV | 104 | 122 | | dB |
| **Over Temperature** | | **$R_L$ = 100kΩ, 10mV < $V_O$ < (V+) –10mV** | **100** | | | dB |
| | | $R_L$ = 5kΩ, 400mV < $V_O$ < (V+) –400mV | 96 | 120 | | dB |
| **Over Temperature** | | **$R_L$ = 5kΩ, 400mV < $V_O$ < (V+) –400mV** | **90** | | | dB |
| **FREQUENCY RESPONSE** | | $C_L$ = 100pF | | | | |
| Gain-Bandwidth Product | GBW | | | 1 | | MHz |
| Slew Rate | SR | | | 0.8 | | V/µs |
| Settling Time, 0.1% | | $V_S$ = 5.5V, 2V Step | | 5 | | µs |
| 0.01% | | $V_S$ = 5.5V, 2V Step | | 8 | | µs |
| Overload Recovery Time | | $V_{IN}$ • G = $V_S$ | | 2.5 | | µs |
| Total Harmonic Distortion + Noise | THD+N | $V_S$ = 5.5V, $V_O$ = 3Vp-p, G = 1, f = 1kHz | | 0.006 | | % |
| **OUTPUT** | | | | | | |
| Voltage Output Swing from Rail[1] | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 96dB | | 1 | | mV |
| | | $R_L$ = 100kΩ, $A_{OL}$ ≥ 104dB | | 3 | 10 | mV |
| **Over Temperature** | | **$R_L$ = 100kΩ, $A_{OL}$ ≥ 100dB** | | | **10** | mV |
| | | $R_L$ = 5kΩ, $A_{OL}$ ≥ 96dB | | 40 | 400 | mV |
| **Over Temperature** | | **$R_L$ = 5kΩ, $A_{OL}$ ≥ 90dB** | | | **400** | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±15 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | $V_S$ | | 2.7 | | 5.5 | V |
| Operating Voltage Range | | | | 2.5 to 5.5 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $V_S$ = 5.5V, $I_O$ = 0 | | 150 | 250 | µA |
| **Over Temperature** | | | | | **300** | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | 85 | °C |
| Operating Range | | | –55 | | 125 | °C |
| Storage Range | | | –65 | | 150 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SOT23-5 Surface Mount | | | | 200 | | °C/W |
| MSOP-8 Surface Mount | | | | 150 | | °C/W |
| 8-Pin DIP | | | | 100 | | °C/W |
| SO-8 Surface Mount | | | | 150 | | °C/W |
| TSSOP-14 Surface Mount | | | | 100 | | °C/W |
| 14-Pin DIP | | | | 80 | | °C/W |
| SO-14 Surface Mount | | | | 100 | | °C/W |

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

# SPECIFICATIONS: $V_S$ = 2.7V to 5.5V

At $T_A$ = +25°C, $R_L$ = 10kΩ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.
**Boldface** limits apply over the temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITION | OPA345NA, UA<br>OPA2345EA, UA<br>OPA4345EA, UA<br>MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = +5.5V, $V_{CM} = V_S/2$ | | ±0.2 | ±1 | mV |
| **Over Temperature** | | | | **±0.8** | **±1.2** | mV |
| **vs Temperature** | **$dV_{OS}/dT$** | | | **±3** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = 2.7V to 5.5V, $V_{CM}$ < (V+) -1.8V | | 30 | 200 | µV/V |
| **Over Temperature** | | **$V_S$ = 2.7V to 5.5V, $V_{CM}$ < (V+) -1.8V** | | | **250** | µV/V |
| Channel Separation, dc | | | | 0.2 | | µV/V |
| f = 1kHz | | | | 130 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.2 | ±10 | pA |
| **Over Temperature** | | | | **See Typical Curve** | | pA |
| Input Offset Current | $I_{OS}$ | | | ±0.2 | ±10 | pA |
| **NOISE** | | | | | | |
| Input Voltage Noise | | f = 0.1 to 50kHz | | 8 | | µVrms |
| Input Voltage Noise Density | $e_n$ | f = 10kHz | | 30 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10kHz | | 0.5 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | –0.3 | | (V+) + 0.3 | V |
| Common-Mode Rejection Ratio | CMRR | $V_S$ = +5.5V, –0.3V < $V_{CM}$ < (V+)-1.8 | 76 | 92 | | dB |
| **Over Temperature** | | **$V_S$ = +5.5V, –0.3V < $V_{CM}$ < (V+)-1.8** | **74** | | | dB |
| Common-Mode Rejection Ratio | CMRR | $V_S$ = +5.5V, –0.3V < $V_{CM}$ < 5.8V | 70 | 84 | | dB |
| **Over Temperature** | | **$V_S$ = +5.5V, –0.3V < $V_{CM}$ < 5.8V** | **68** | | | dB |
| Common-Mode Rejection Ratio | CMRR | $V_S$ = +2.7V, –0.3V < $V_{CM}$ < 3V | 66 | 80 | | dB |
| **Over Temperature** | | **$V_S$ = +2.7V, –0.3V < $V_{CM}$ < 3V** | **64** | | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| Common-Mode | | | | $10^{13}$ \|\| 6 | | Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$ = 100kΩ, 10mV < $V_O$ < (V+) –10mV | 104 | 122 | | dB |
| **Over Temperature** | | **$R_L$ = 100kΩ, 10mV < $V_O$ < (V+) –10mV** | **100** | | | dB |
| | | $R_L$ = 5kΩ, 400mV < $V_O$ < (V+) –400mV | 96 | 120 | | dB |
| **Over Temperature** | | **$R_L$ = 5kΩ, 400mV < $V_O$ < (V+) –400mV** | **90** | | | dB |
| **FREQUENCY RESPONSE** | | $C_L$ = 100pF | | | | |
| Gain-Bandwidth Product | GBW | | | 3 | | MHz |
| Slew Rate | SR | | | 2 | | V/µs |
| Settling Time, 0.1% | | G = 5, 2V Output Step | | 1.5 | | µs |
| 0.01% | | G = 5, 2V Output Step | | 1.6 | | µs |
| Overload Recovery Time | | $V_{IN} \bullet G = V_S$ | | 2.5 | | µs |
| Total Harmonic Distortion + Noise | THD+N | $V_S$ = 5.5V, $V_O$ = 2.5Vp-p, G = 5, f = 1kHz | | 0.006 | | % |
| **OUTPUT** | | | | | | |
| Voltage Output Swing from Rail[1] | | $R_L$ = 100kΩ, $A_{OL} \geq$ 96dB | | 1 | | mV |
| | | $R_L$ = 100kΩ, $A_{OL} \geq$ 104dB | | 3 | 10 | mV |
| **Over Temperature** | | **$R_L$ = 100kΩ, $A_{OL} \geq$ 100dB** | | | **10** | mV |
| | | $R_L$ = 5kΩ, $A_{OL} \geq$ 96dB | | 40 | 400 | mV |
| **Over Temperature** | | **$R_L$ = 5kΩ, $A_{OL} \geq$ 90dB** | | | **400** | mV |
| Short-Circuit Current | $I_{SC}$ | | | ±15 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | | See Typical Curve | | |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | $V_S$ | | 2.7 | | 5.5 | V |
| Operating Voltage Range | | | | 2.5 to 5.5 | | V |
| Quiescent Current (per amplifier) | $I_Q$ | $V_S$ = 5.5V, $I_O$ = 0 | | 150 | 250 | µA |
| **Over Temperature** | | | | | **300** | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | 85 | °C |
| Operating Range | | | –55 | | 125 | °C |
| Storage Range | | | –65 | | 150 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SOT23-5 Surface Mount | | | | 200 | | °C/W |
| MSOP-8 Surface Mount | | | | 150 | | °C/W |
| SO-8 Surface Mount | | | | 150 | | °C/W |
| TSSOP-14 Surface Mount | | | | 100 | | °C/W |
| SO-14 Surface Mount | | | | 100 | | °C/W |

NOTE: (1) Output voltage swings are measured between the output and power-supply rails.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage, V+ to V- | 7.5V |
| Signal Input Terminals, Voltage[2] | (V–) –0.5V to (V+) +0.5V |
| Current[2] | 10mA |
| Output Short-Circuit[3] | Continuous |
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –65°C to +150°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 10s) | 300°C |
| ESD Tolerance (Human Body Model) | 4000V |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION[1]

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER[2] | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| OPA344NA | SOT23-5 | DBV | –40°C to +85°C | B44 | OPA344NA/250 | Tape and Reel |
| " | " | " | " | " | OPA344NA/3K | Tape and Reel |
| OPA344UA | SO-8 | D | –40°C to +85°C | OPA344UA | OPA344UA | Rails |
| " | " | " | " | " | OPA344UA/2K5 | Tape and Reel |
| OPA344PA | 8-Pin Dip | P | –40° C to +85°C | OPA344PA | OPA344PA | Rails |
| OPA2344EA | MSOP-8 | DGK | –40°C to +85°C | C44 | OPA2344EA/250 | Tape and Reel |
| " | " | " | " | " | OPA2344EA/2K5 | Tape and Reel |
| OPA2344UA | SO-8 | D | –40°C to +85°C | OPA2344UA | OPA2344UA | Rails |
| " | " | " | " | " | OPA2344UA/2K5 | Tape and Reel |
| OPA2344PA | 8-Pin DIP | P | –40°C to +85°C | OPA2344PA | OPA2344PA | Rails |
| OPA4344EA | TSSOP-14 | PW | –40°C to +85°C | OPA4344EA | OPA4344EA/250 | Rails |
| " | " | " | " | " | OPA4344EA/2K5 | Tape and Reel |
| OPA4344UA | SO-14 | D | –40°C to +85°C | OPA4344UA | OPA4344UA | Rails |
| " | " | " | " | " | OPA4344UA/2K5 | Tape and Reel |
| OPA4344PA | 14-Pin DIP | N | –40°C to +85°C | OPA4344PA | OPA4344PA | Rails |
| OPA345NA | SOT23-5 | DBV | –40°C to +85°C | A45 | OPA345NA/250 | Tape and Reel |
| " | " | " | " | " | OPA345NA/3K | Tape and Reel |
| OPA345UA | SO-8 | D | –40°C to +85°C | OPA345UA | OPA345UA | Rails |
| " | " | " | " | " | OPA345UA/2K5 | Tape and Reel |
| OPA2345EA | MSOP-8 | DGK | –40°C to +85°C | B45 | OPA2345EA/250 | Tape and Reel |
| " | " | " | " | " | OPA2345EA/2K5 | Tape and Reel |
| OPA2345UA | SO-8 | D | –40°C to +85°C | OPA2345UA | OPA2345UA | Rails |
| " | " | " | " | " | OPA2345UA/2K5 | Tape and Reel |
| OPA4345EA | TSSOP-14 | PW | –40°C to +85°C | OPA4345EA | OPA4345EA/250 | Tape and Reel |
| " | " | " | " | " | OPA4345EA/2K5 | Tape and Reel |
| OPA4345UA | SO-14 | D | –40°C to +85°C | OPA4345UA | OPA4345UA | Rails |
| " | " | " | " | " | OPA4345UA/2K5 | Tape and Reel |

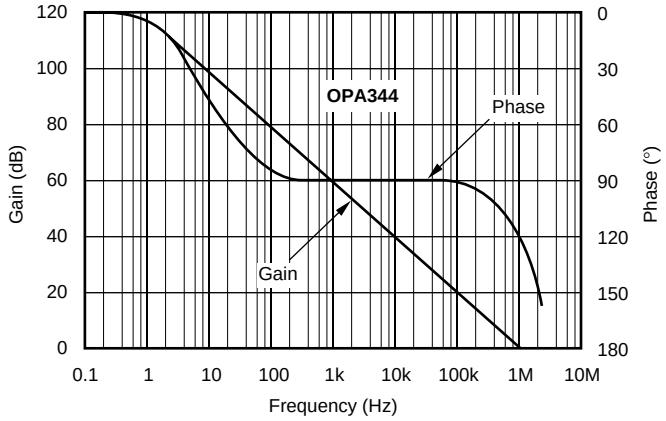
NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA344UA/2K5" will get a single 2500-piece Tape and Reel.

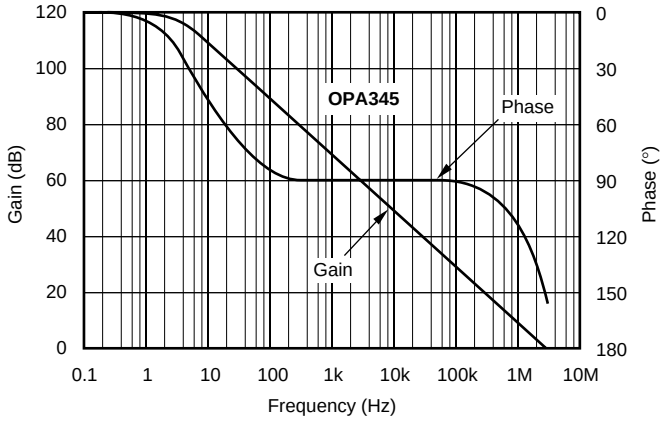
# TYPICAL PERFORMANCE CURVES

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

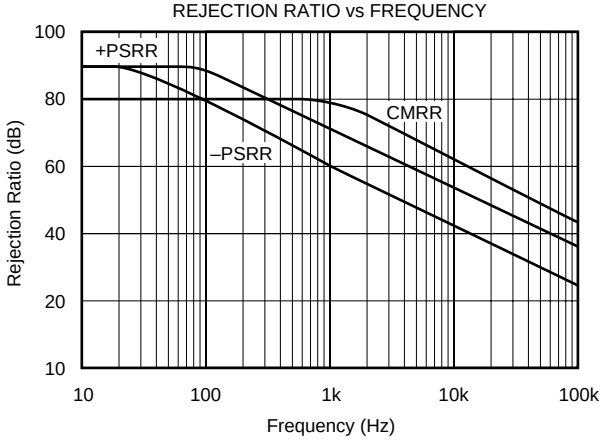
OPEN-LOOP GAIN/PHASE vs FREQUENCY



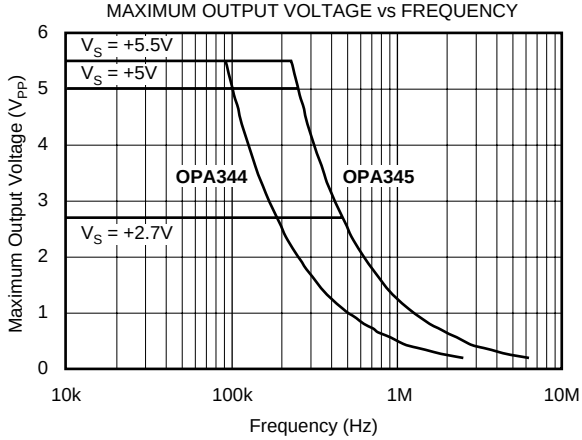

OPEN-LOOP GAIN/PHASE vs FREQUENCY



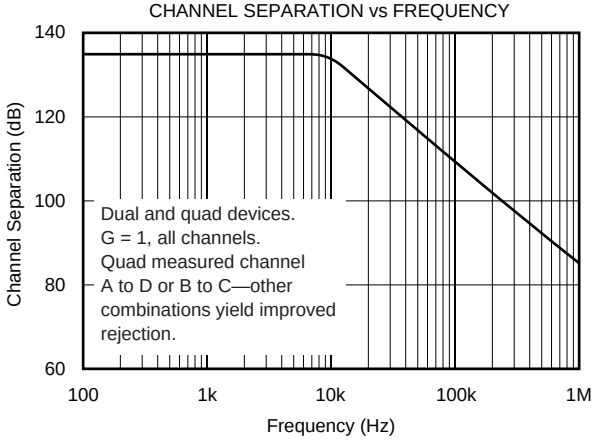

POWER SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



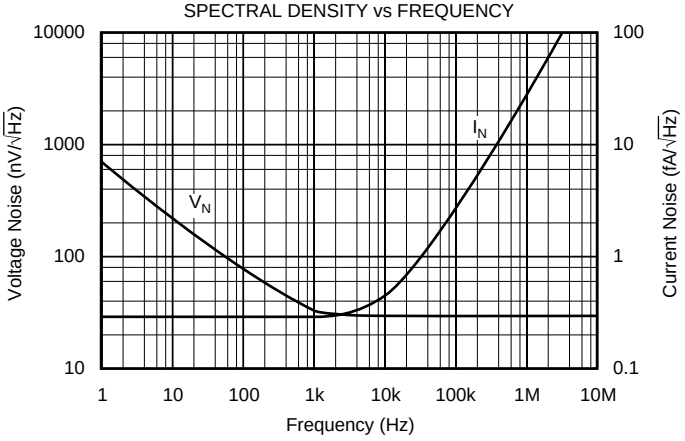

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY




CHANNEL SEPARATION vs FREQUENCY



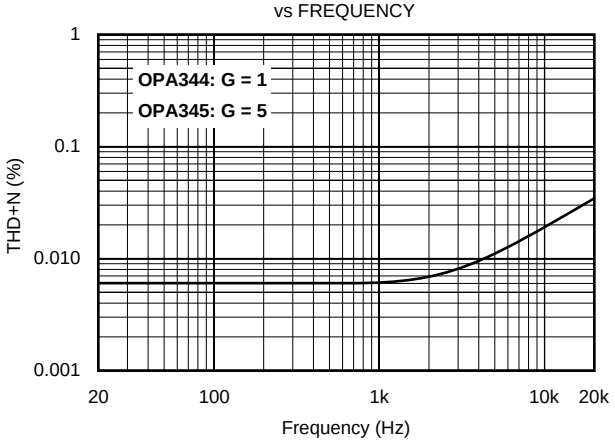

VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



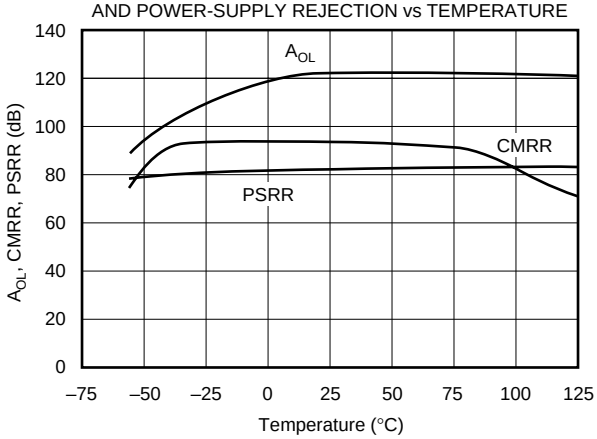
# TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

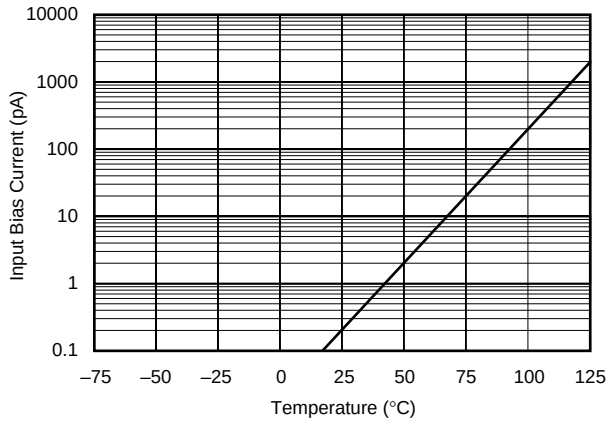
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



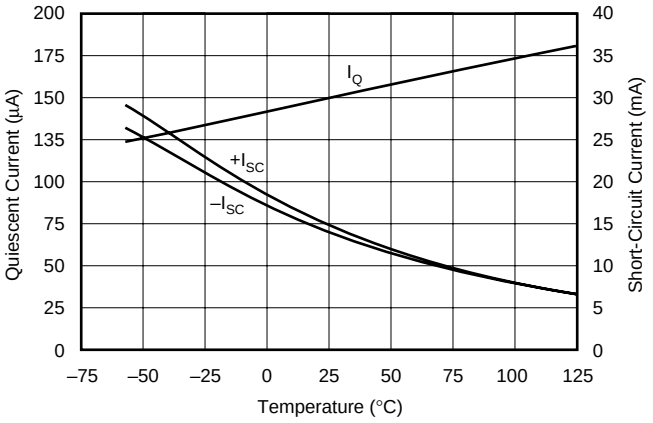

OPEN-LOOP GAIN, COMMON-MODE REJECTION RATIO, AND POWER-SUPPLY REJECTION vs TEMPERATURE



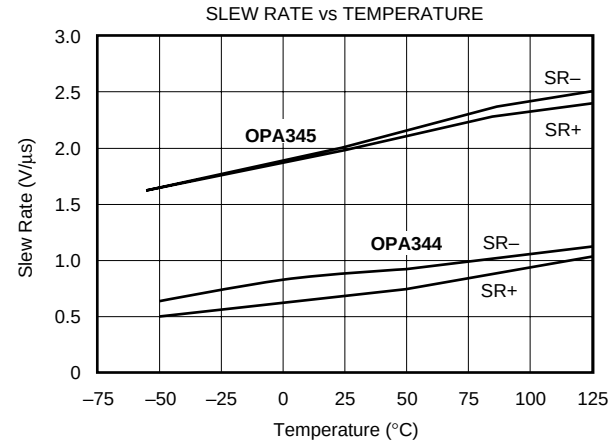

INPUT BIAS CURRENT vs TEMPERATURE



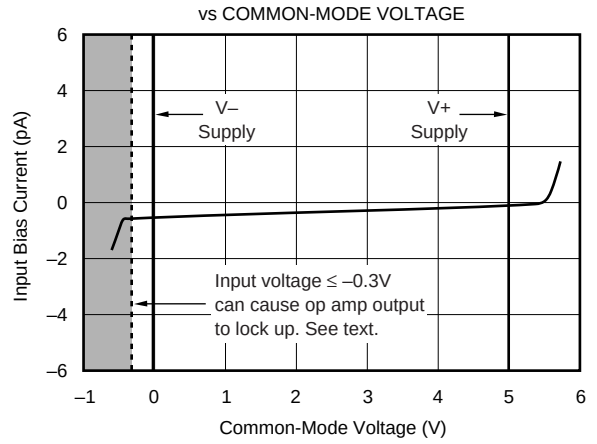

QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE




SLEW RATE vs TEMPERATURE



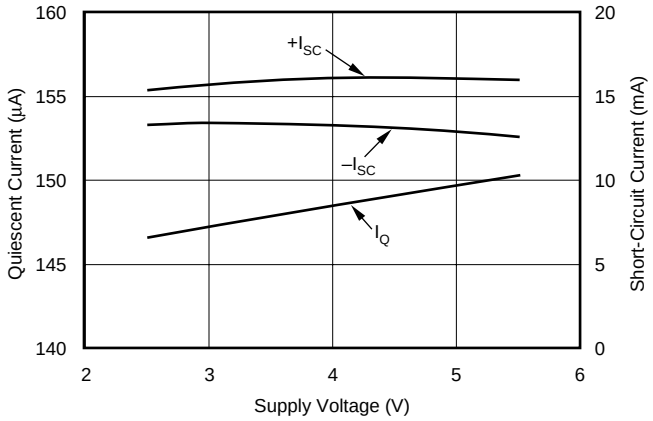

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



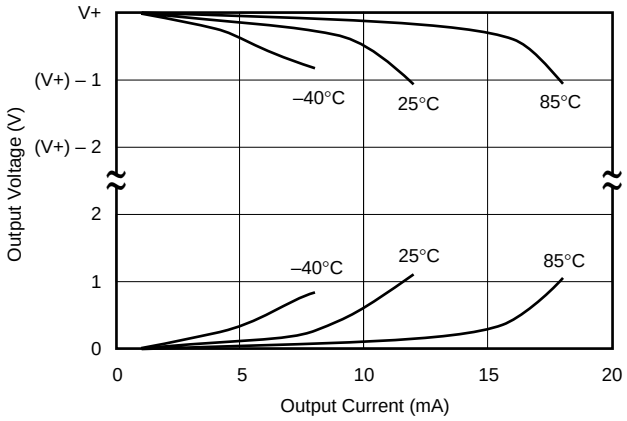
# TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

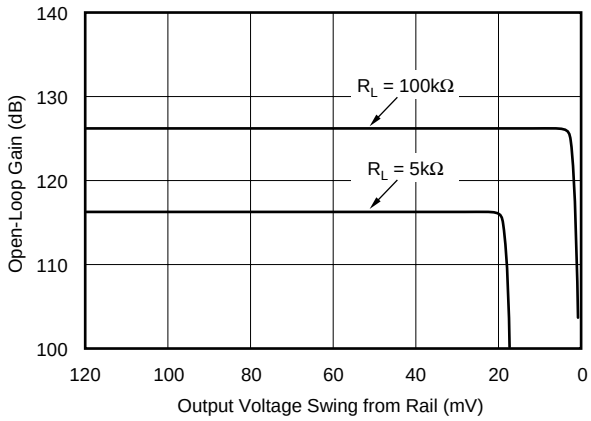
QUIESCENT CURRENT AND
SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



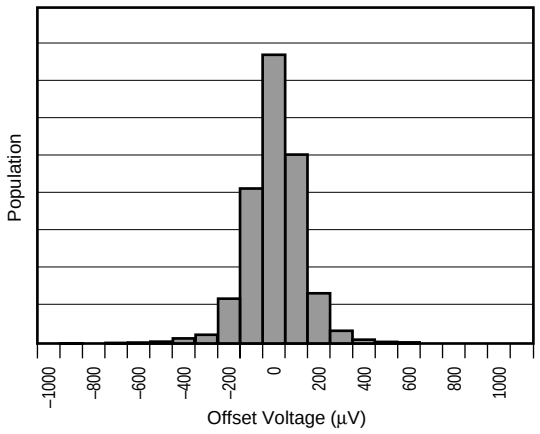

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



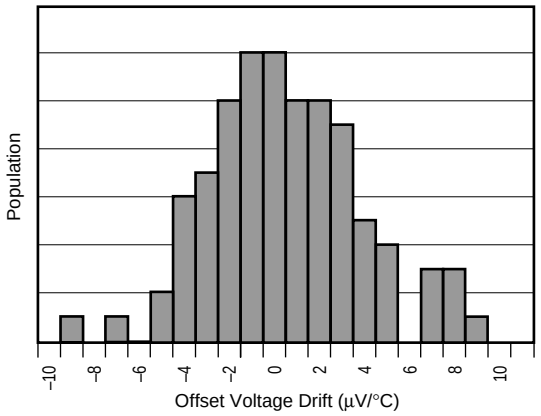

OPEN-LOOP GAIN vs OUTPUT VOLTAGE SWING



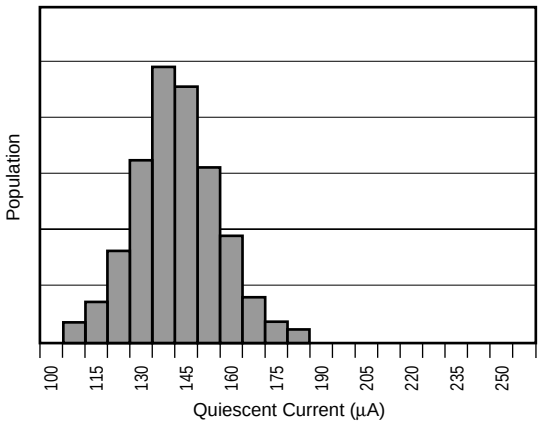

OFFSET VOLTAGE
PRODUCTION DISTRIBUTION




OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



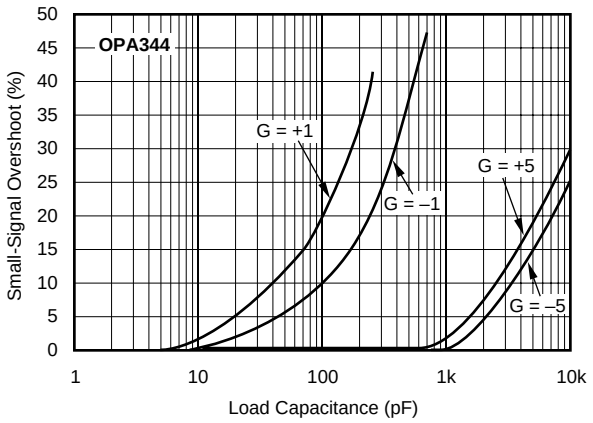

QUIESCENT CURRENT
PRODUCTION DISTRIBUTION



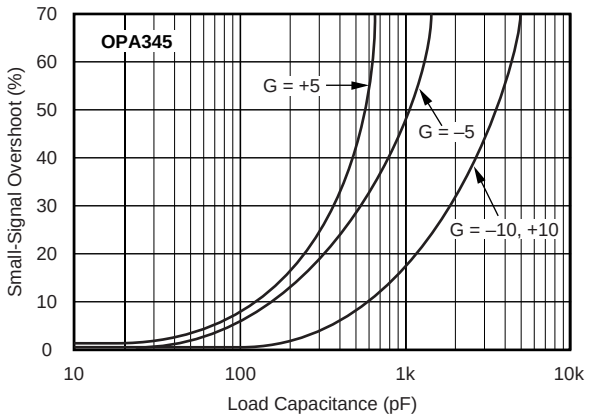
# TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A$ = +25°C, $V_S$ = +5V, and $R_L$ = 10kΩ connected to $V_S$/2, unless otherwise noted.

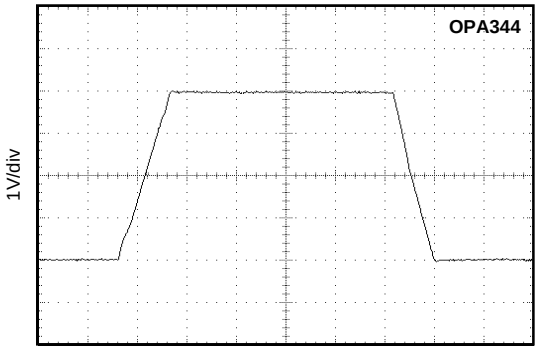
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



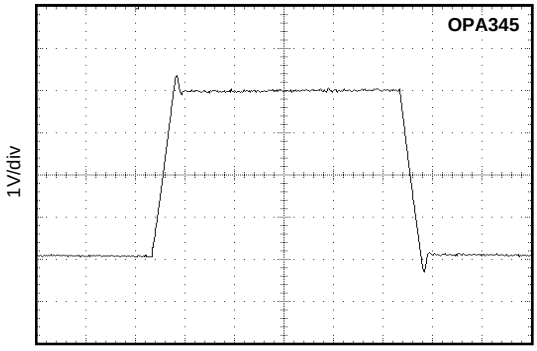

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



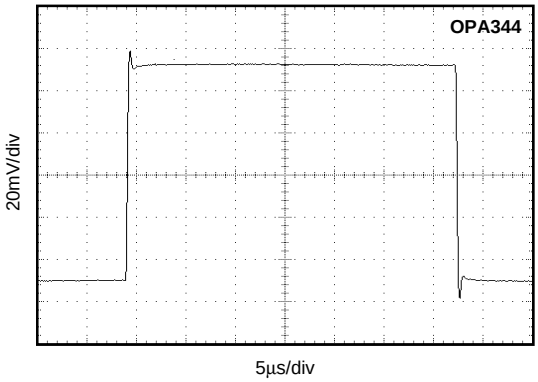

LARGE-SIGNAL STEP RESPONSE: OPA344
G = +1, $R_L$ = 10kΩ, $C_L$ = 100pF



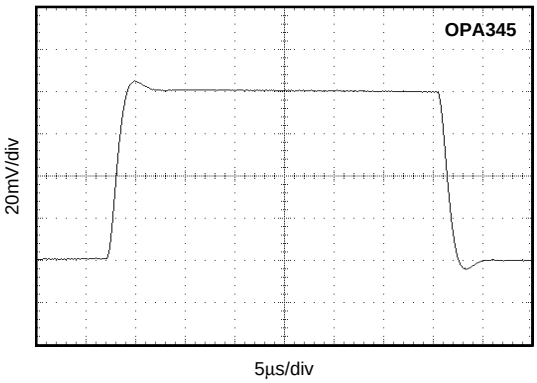

LARGE-SIGNAL STEP RESPONSE: OPA345
G = +5, $R_L$ = 10kΩ, $C_L$ = 100pF




SMALL-SIGNAL STEP RESPONSE: OPA344
G = +1, $R_L$ = 10kΩ, $C_L$ = 100pF




SMALL-SIGNAL STEP RESPONSE: OPA345
G = +5, $R_L$ = 10kΩ, $C_L$ = 100pF



# APPLICATIONS INFORMATION

OPA344 series op amps are unity gain stable and can operate on a single supply, making them highly versatile and easy to use. OPA345 series op amps are optimized for applications requiring higher speeds with gains of 5 or greater.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low supply applications. Figure 1 shows the input and output waveforms for the OPA344 in unity-gain configuration. Operation is from $V_S$ = +5V with a 10kΩ load connected to $V_S/2$. The input is a 5Vp-p sinusoid. Output voltage is approximately 4.997Vp-p.

Power supply pins should be bypassed with 0.01µF ceramic capacitors.

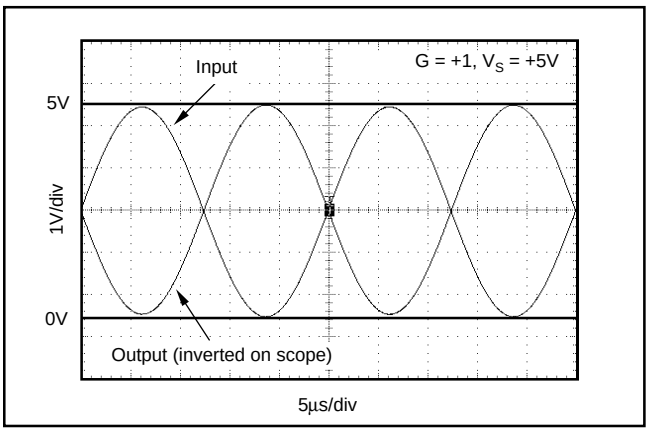



FIGURE 1. Rail-to-Rail Input and Output.

## OPERATING VOLTAGE

OPA344 and OPA345 series op amps are fully specified and ensured from +2.7V to +5.5V. In addition, many specifications apply from –40°C to +85°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Performance Curves.

## RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA344 and OPA345 series extends 300mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (see Figure 2). The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3V to 300mV above the positive supply, while the P-channel pair is on for inputs from 300mV below the negative supply to approximately (V+) –1.3V. There is a small transition region, typically (V+) – 1.5V to (V+) – 1.1V, in which both pairs are on. This 400mV transition region can vary 300mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.8V to (V+) – 1.4V on the low end, up to (V+) – 1.2V to (V+) – 0.8V on the high end. Within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region. For more information on designing with rail-to-rail input op amps, see Figure 3 “Design Optimization with Rail-to-Rail Input Op Amps.”

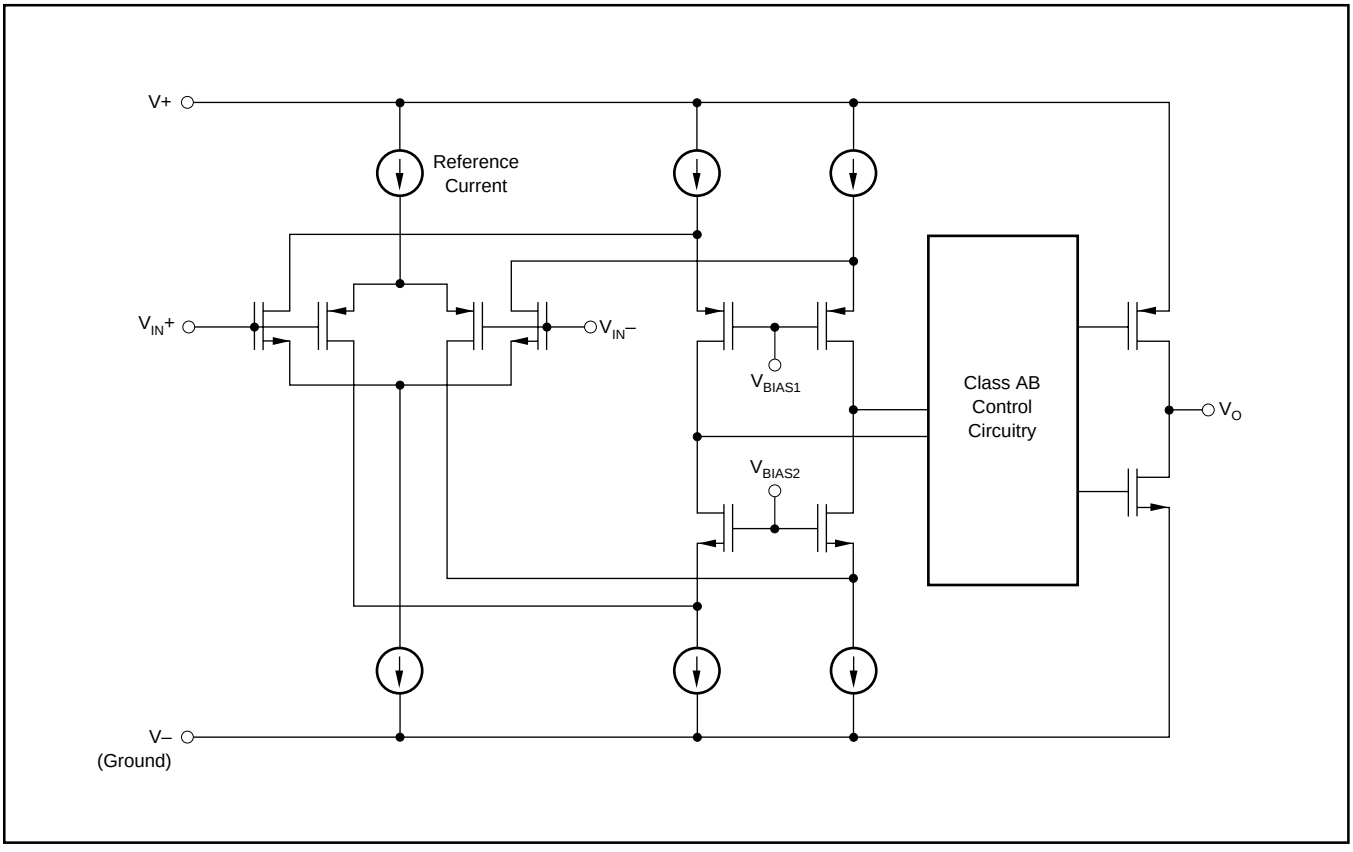



FIGURE 2. Simplified Schematic.

## DESIGN OPTIMIZATION WITH RAIL-TO-RAIL INPUT OP AMPS

Rail-to-rail op amps can be used in virtually any op amp configuration. To achieve optimum performance, however, applications using these special double-input-stage op amps may benefit from consideration of their special behavior.

In many applications, operation remains within the common-mode range of only one differential input pair. However some applications exercise the amplifier through the transition region of both differential input stages. Although the two input stages are laser trimmed for excellent matching, a small discontinuity may occur in this transition. Careful selection of the circuit configuration, signal levels and biasing can often avoid this transition region.

With a unity-gain buffer, for example, signals will traverse this transition at approximately 1.3V below V+ supply and may exhibit a small discontinuity at this point.

The common-mode voltage of the non-inverting amplifier is equal to the input voltage. If the input signal always remains less than the transition voltage, no discontinuity will be created. The closed-loop gain of this configuration can still produce a rail-to-rail output.

Inverting amplifiers have a constant common-mode voltage equal to $V_B$. If this bias voltage is constant, no discontinuity will be created. The bias voltage can generally be chosen to avoid the transition region.

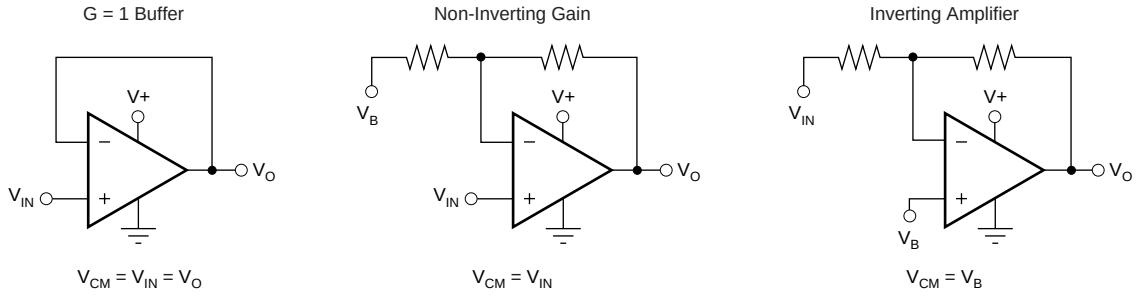



FIGURE 3. Design Optimization with Rail-to-Rail Input Op Amps.

### COMMON-MODE REJECTION

The CMRR for the OPA344 and OPA345 is specified in several ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ($V_{CM}$ < (V+) – 1.8V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at $V_S$ = 5.5V over the entire common-mode range is specified. Third, the CMRR at $V_S$ = 2.7V over the entire common-mode range is provided. These last two values include the variations seen through the transition region.

### INPUT VOLTAGE BEYOND THE RAILS

If the input voltage can go more than 0.3V below the negative power supply rail (single-supply ground), special precautions are required. If the input voltage goes sufficiently negative, the op amp output may lock up in an inoperative state. A Schottky diode clamp circuit will prevent this—see Figure 4. The series resistor prevents excessive current (greater than 10mA) in the Schottky diode and in the internal ESD protection diode, if the input voltage can exceed the positive supply voltage. If the signal source is limited to less than 10mA, the input resistor is not required.

### RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 600Ω loads connected to any potential between V+ and ground. For light resistive loads (> 50kΩ), the output voltage can typically swing to within 1mV from supply rail. With moderate resistive loads (2kΩ to 50kΩ), the output can swing to within a few tens of millivolts from the supply rails while maintaining high open-loop gain. See the typical performance curve "Output Voltage Swing vs Output Current."

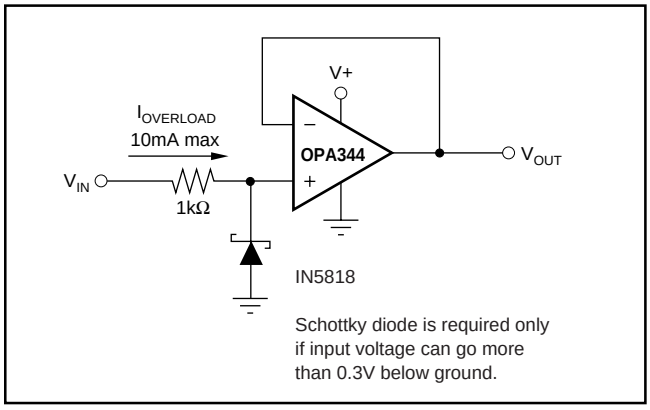



FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

### CAPACITIVE LOAD AND STABILITY

The OPA344 in a unity-gain configuration and the OPA345 in gains greater than 5 can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. See the typical

performance curve “Small-Signal Overshoot vs Capacitive Load.” In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, $R_S$, in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a dc error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_S/R_L$, and is generally negligible.

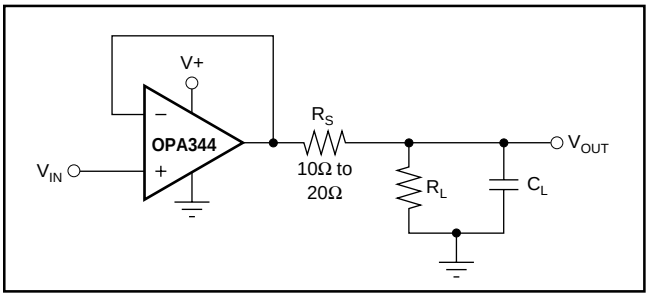



FIGURE 5. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

## DRIVING A/D CONVERTERS

The OPA344 and OPA345 series op amps are optimized for driving medium-speed sampling A/D converters. The OPA344 and OPA345 op amps buffer the A/D’s input capacitance and resulting charge injection while providing signal gain.

Figures 6 shows the OPA344 in a basic noninverting configuration driving the ADS7822. The ADS7822 is a 12-bit, micro-power sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA344, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the A/D’s input can be used to filter charge injection.

Figure 7 shows the OPA2344 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with $V_S$ = +2.7V to +5V with less than 500µA quiescent current.

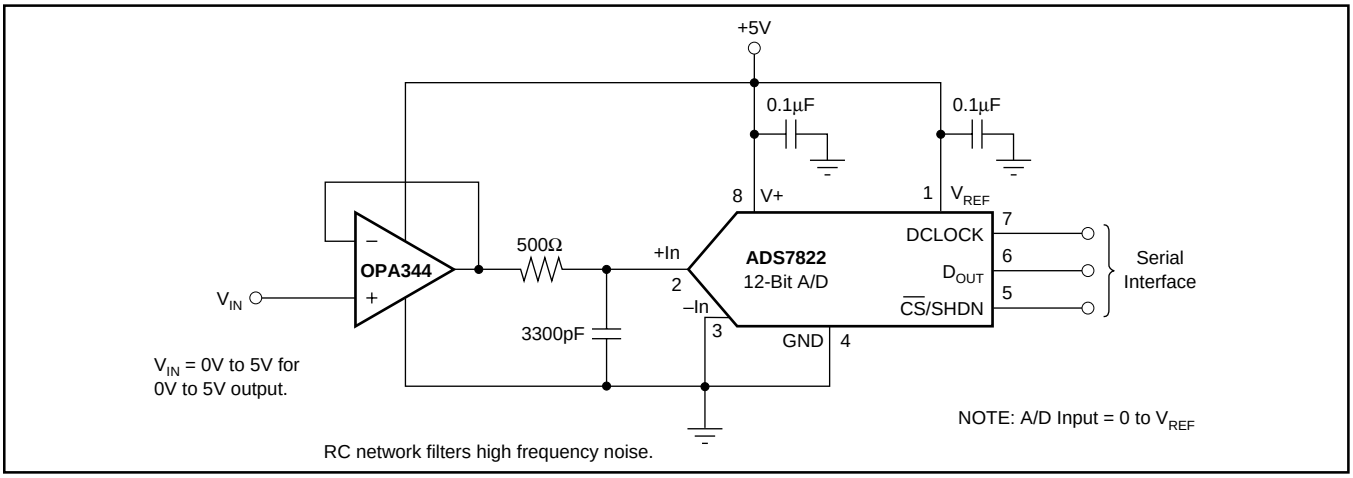



FIGURE 6. OPA344 in Noninverting Configuration Driving ADS7822.

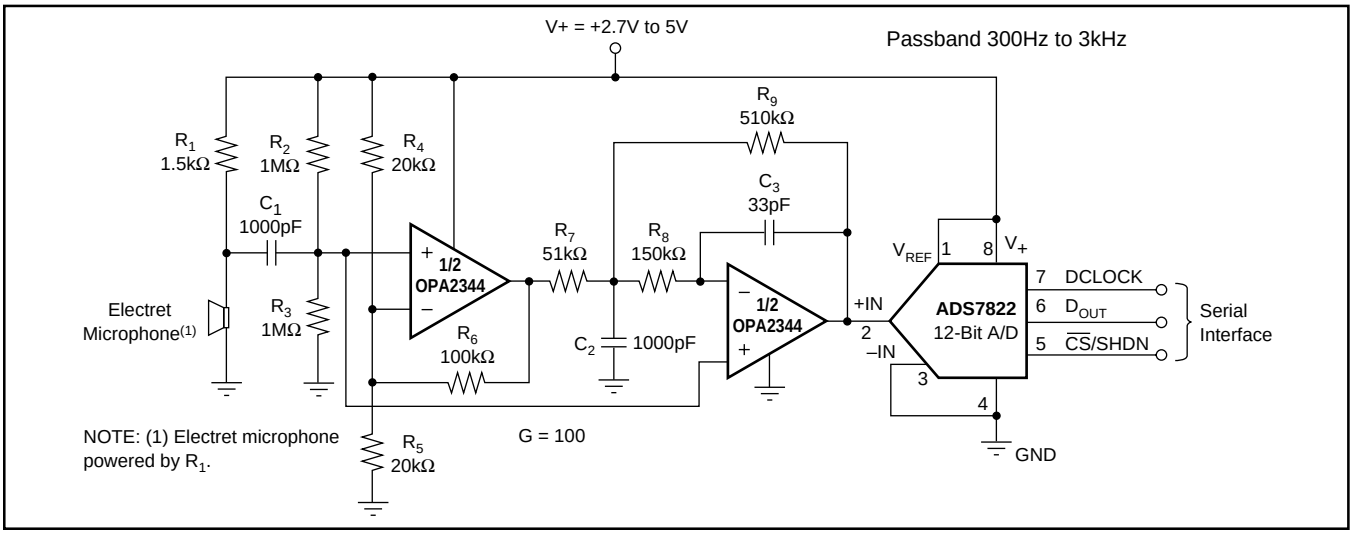



FIGURE 7. Speech Bandpass Filtered Data Acquisition System.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| OPA2344EA/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | NIPDAUAG \| SN | Level-2-260C-1 YEAR | -40 to 85 | C44 |
| OPA2344EA/2K5 | Active | Production | VSSOP (DGK) \| 8 | 2500 \| LARGE T&R | Yes | Call TI \| Nipdauag | Level-2-260C-1 YEAR | -40 to 85 | C44 |
| OPA2344UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2344UA |
| OPA2344UA/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2344UA |
| OPA2345EA/250 | Active | Production | VSSOP (DGK) \| 8 | 250 \| SMALL T&R | Yes | Call TI \| Nipdauag | Level-2-260C-1 YEAR | -40 to 85 | B45 |
| OPA2345UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2345UA |
| OPA2345UA/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 2345UA |
| OPA344NA/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | B44 |
| OPA344NA/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | B44 |
| OPA344PA | Active | Production | PDIP (P) \| 8 | 50 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | OPA344PA |
| OPA344UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 344UA |
| OPA344UA/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 344UA |
| OPA345NA/250 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | A45 |
| OPA345NA/3K | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | A45 |
| OPA345UA | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA 345UA |
| OPA4344EA/250 | Active | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | OPA 4344EA |
| OPA4344EA/2K5 | Active | Production | TSSOP (PW) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | OPA 4344EA |
| OPA4344UA | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4344UA |
| OPA4344UA/2K5 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4344UA |
| OPA4345UA | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OPA4345UA |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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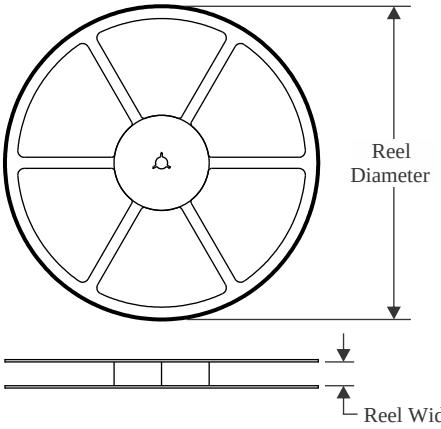
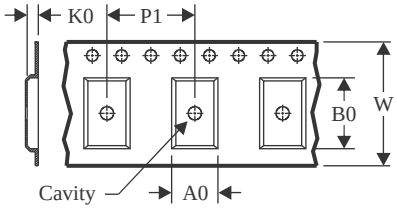
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

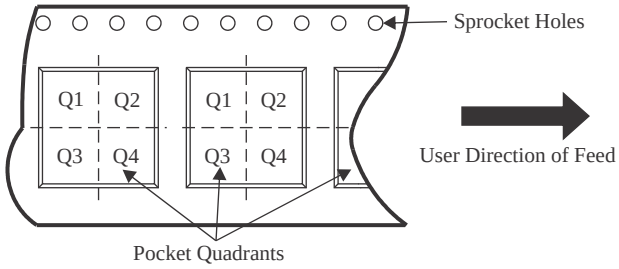



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

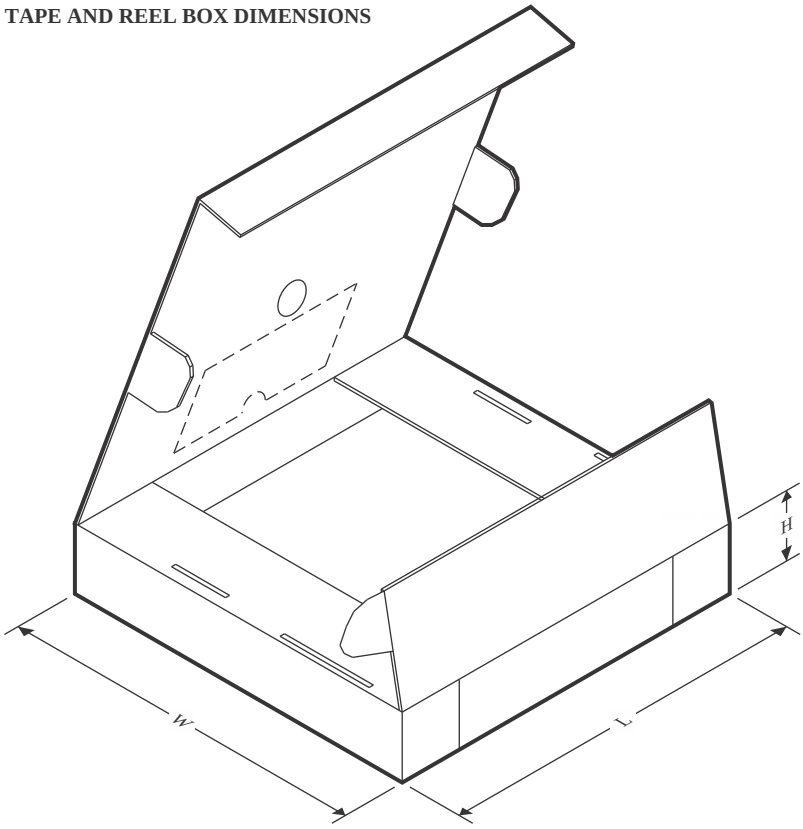
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2344UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2345UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA344NA/250 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA344NA/3K | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA344UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA345NA/250 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA345NA/3K | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA4344EA/250 | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4344EA/2K5 | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4344UA/2K5 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

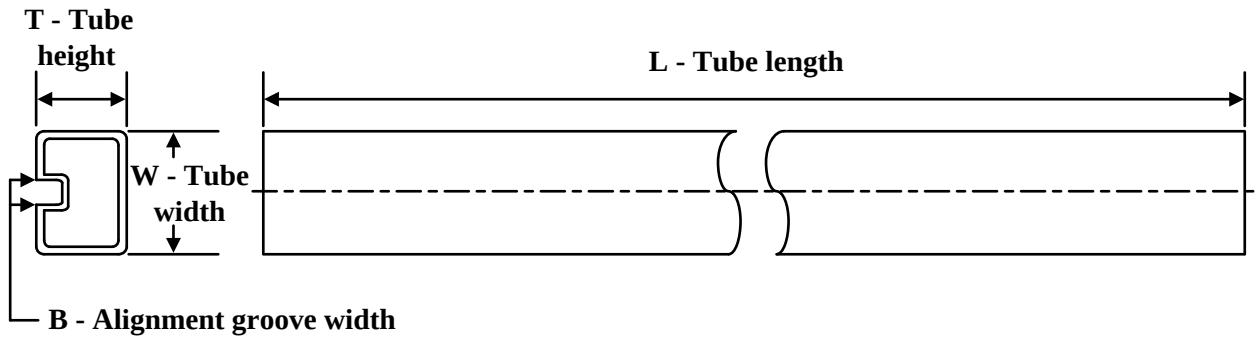
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

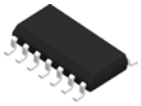
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2344UA/2K5 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA2345UA/2K5 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA344NA/250 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| OPA344NA/3K | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA344UA/2K5 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA345NA/250 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| OPA345NA/3K | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA4344EA/250 | TSSOP | PW | 14 | 250 | 210.0 | 185.0 | 35.0 |
| OPA4344EA/2K5 | TSSOP | PW | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA4344UA/2K5 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA2344UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA2345UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA344PA | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| OPA344UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA344UAG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA345UA | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| OPA4344UA | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA4344UAG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| OPA4345UA | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

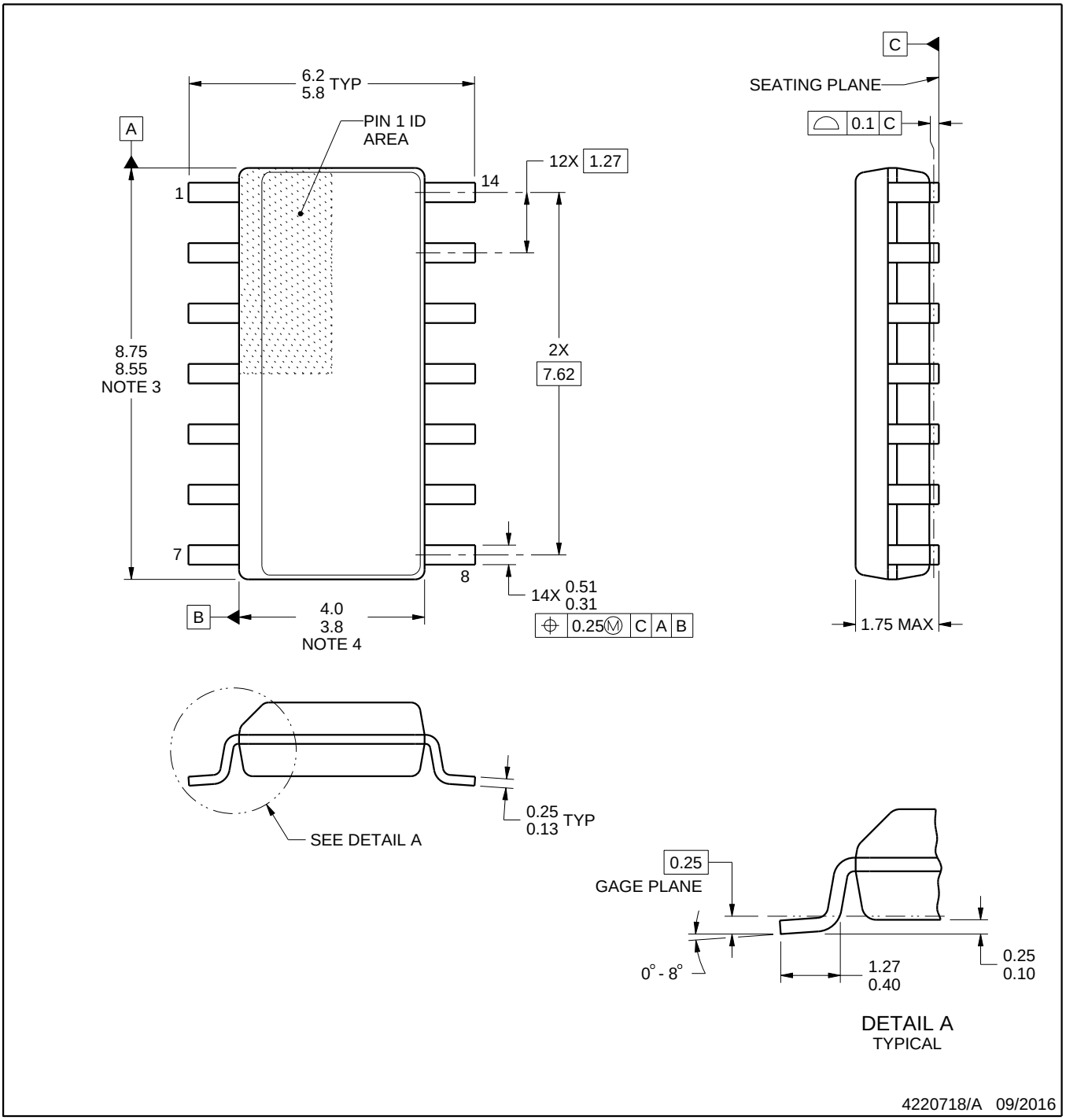


# PACKAGE OUTLINE

## D0014A

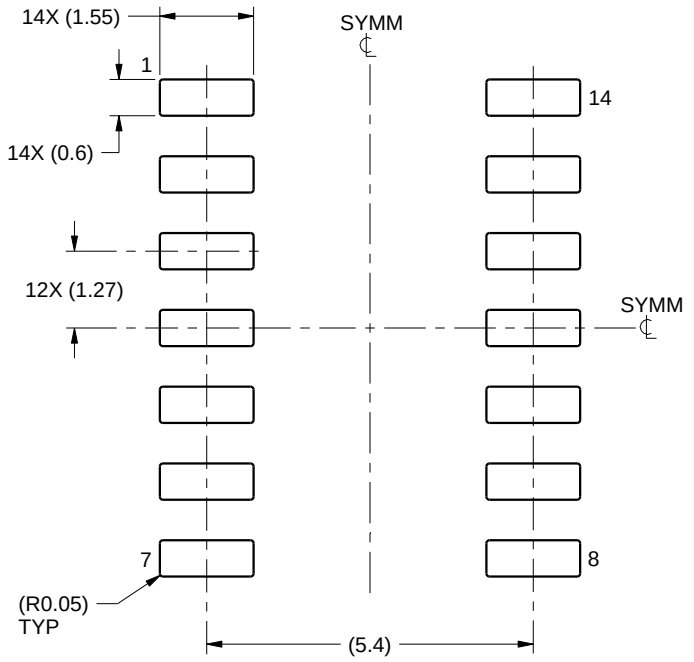
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

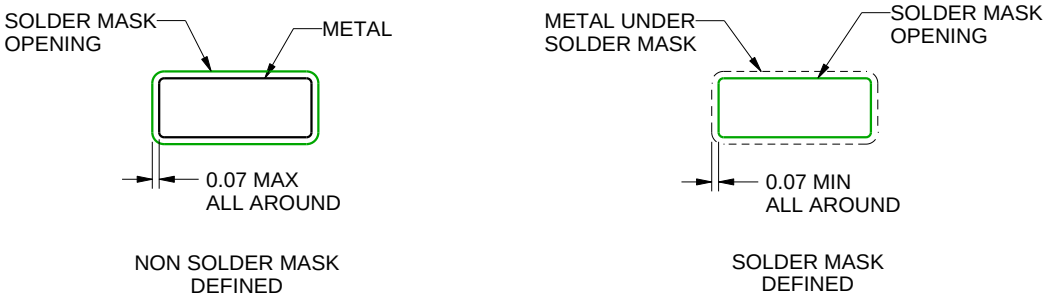



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

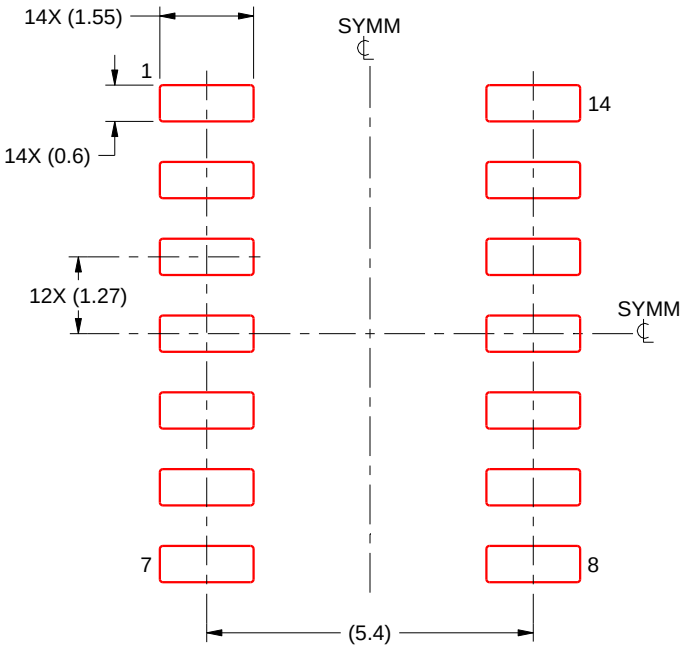
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

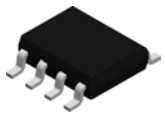



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

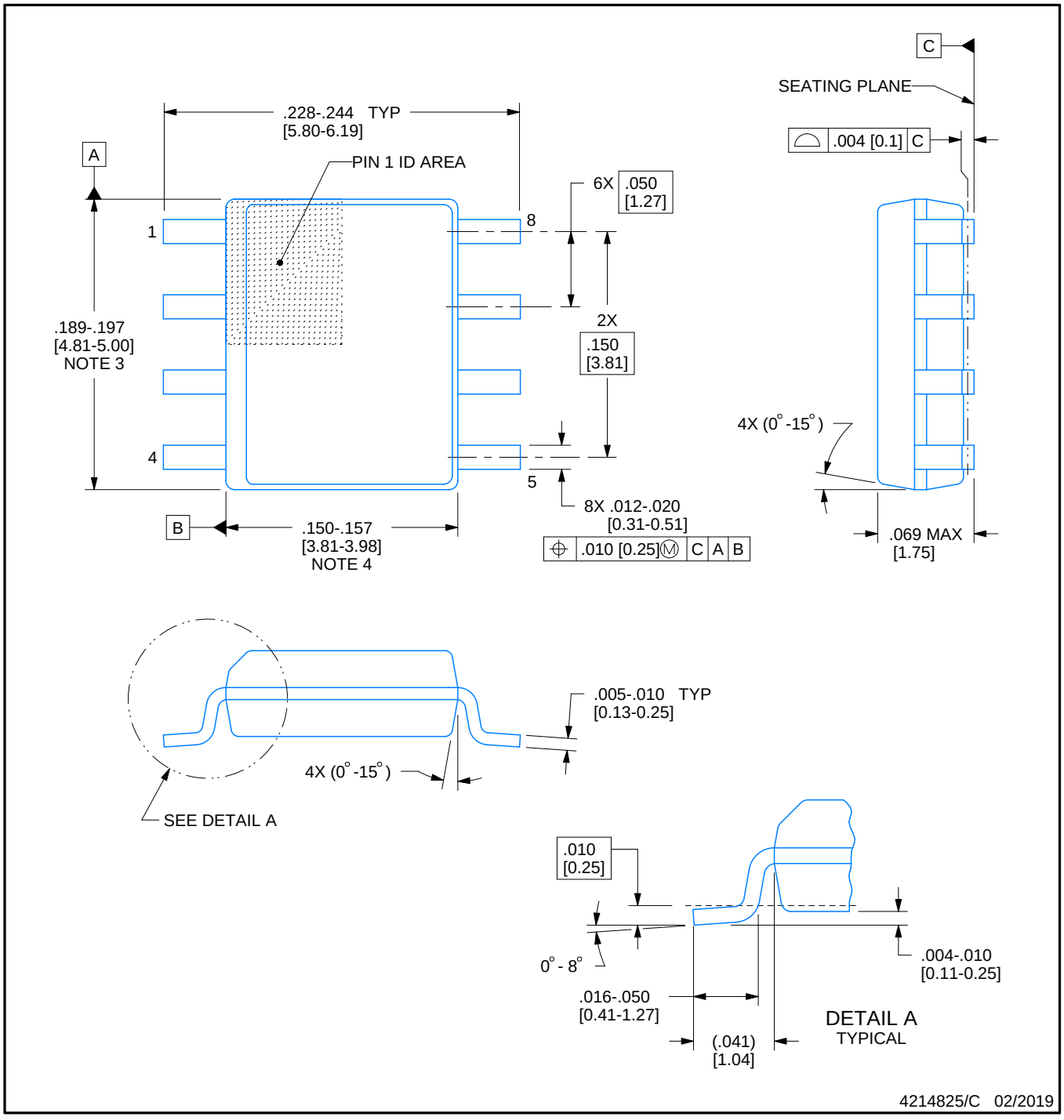


# PACKAGE OUTLINE

## D0008A

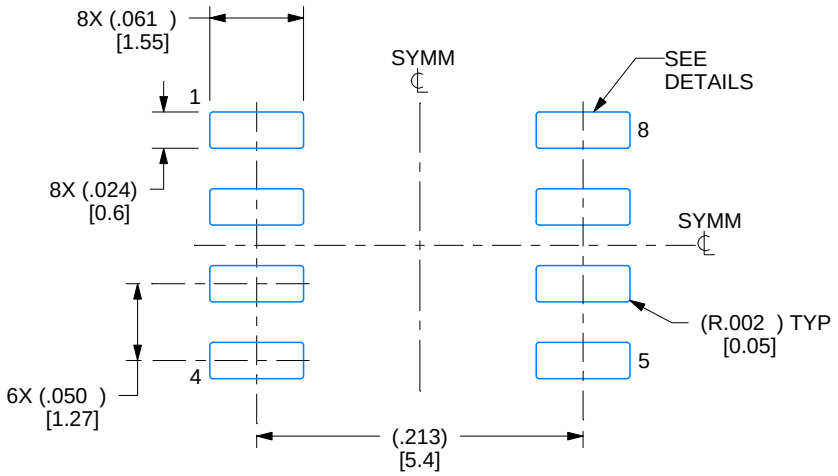
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

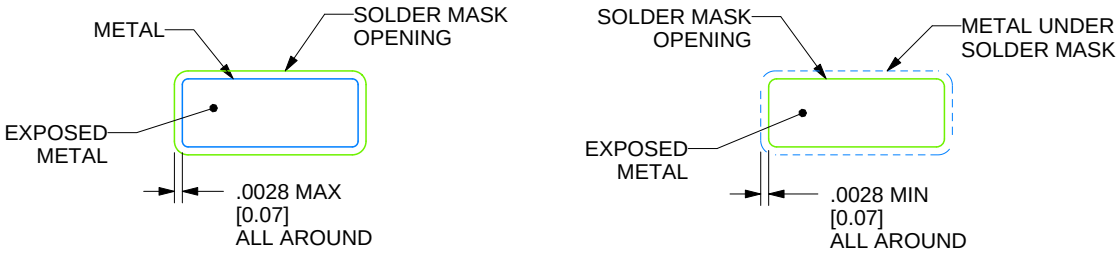



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

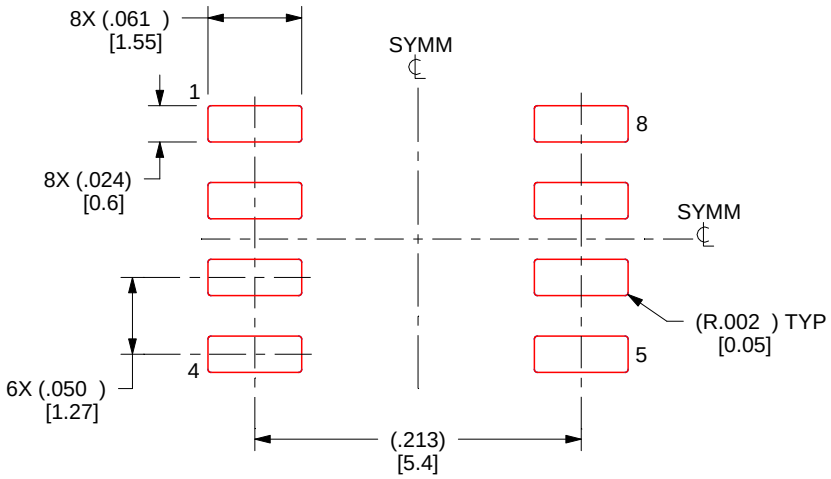
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

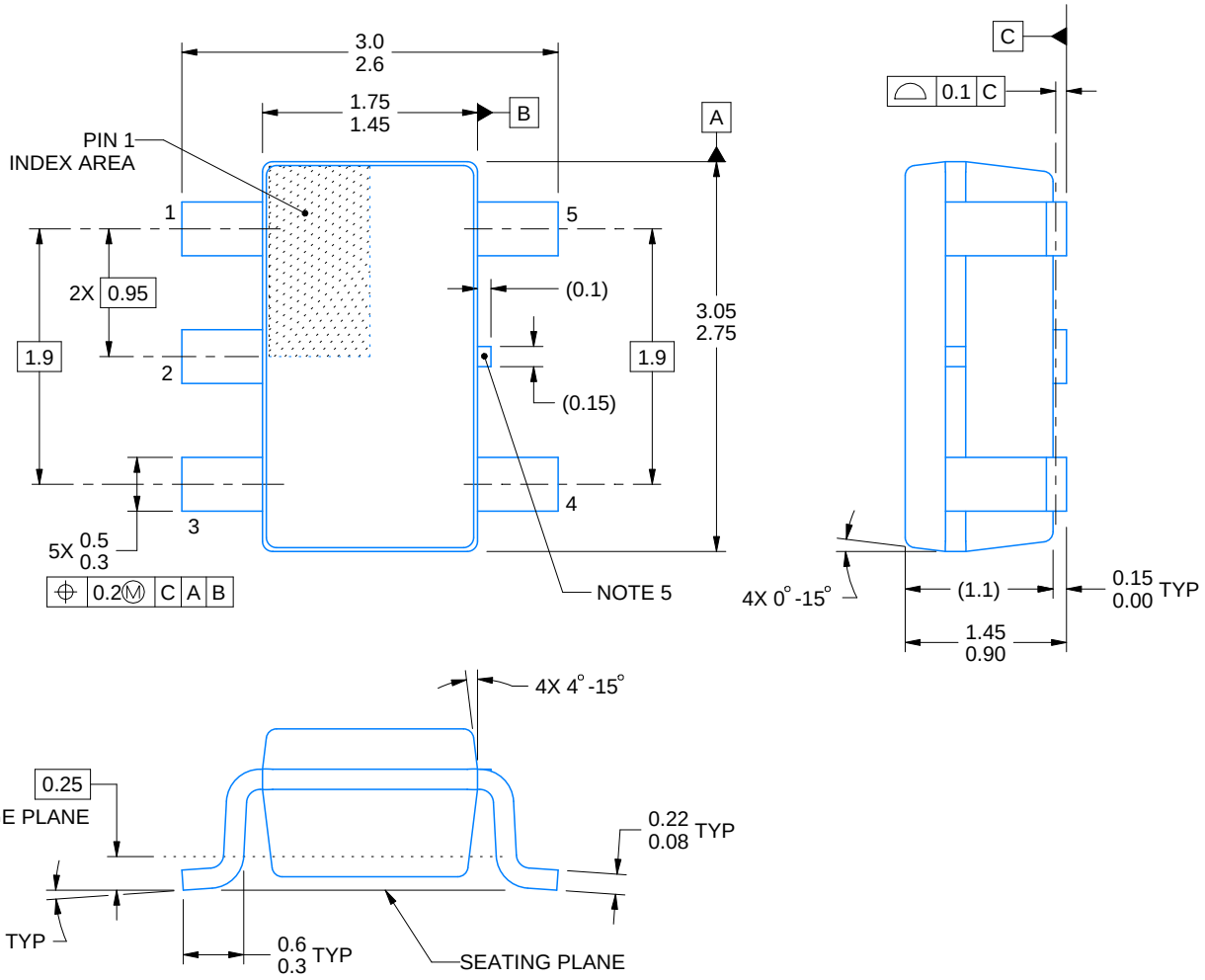
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

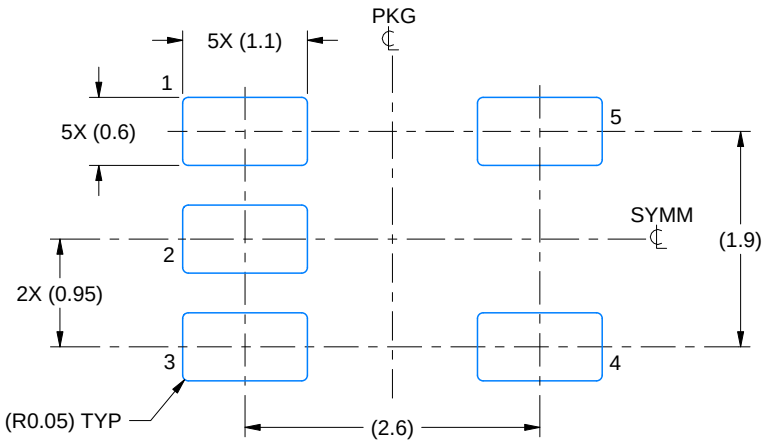
SMALL OUTLINE TRANSISTOR



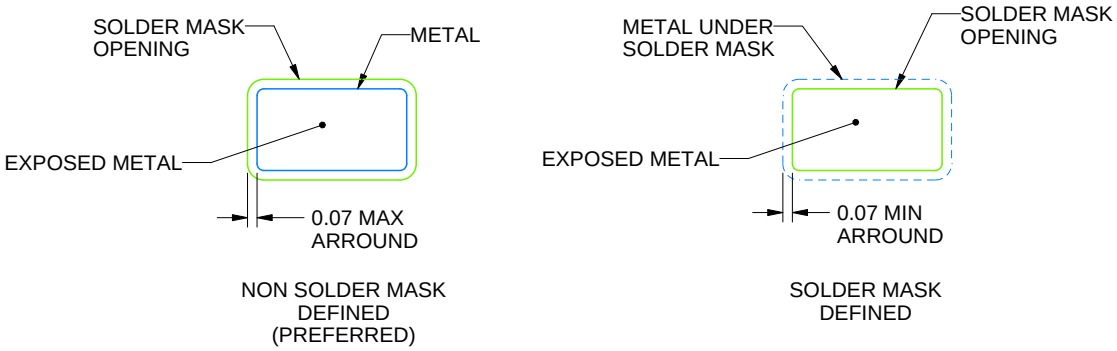

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

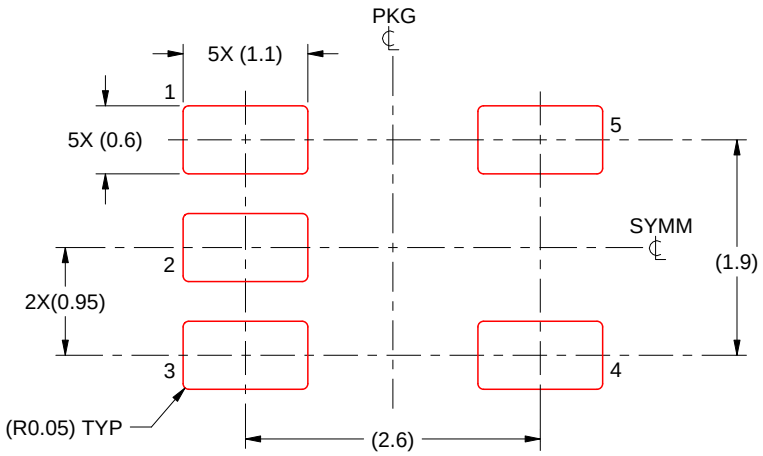



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

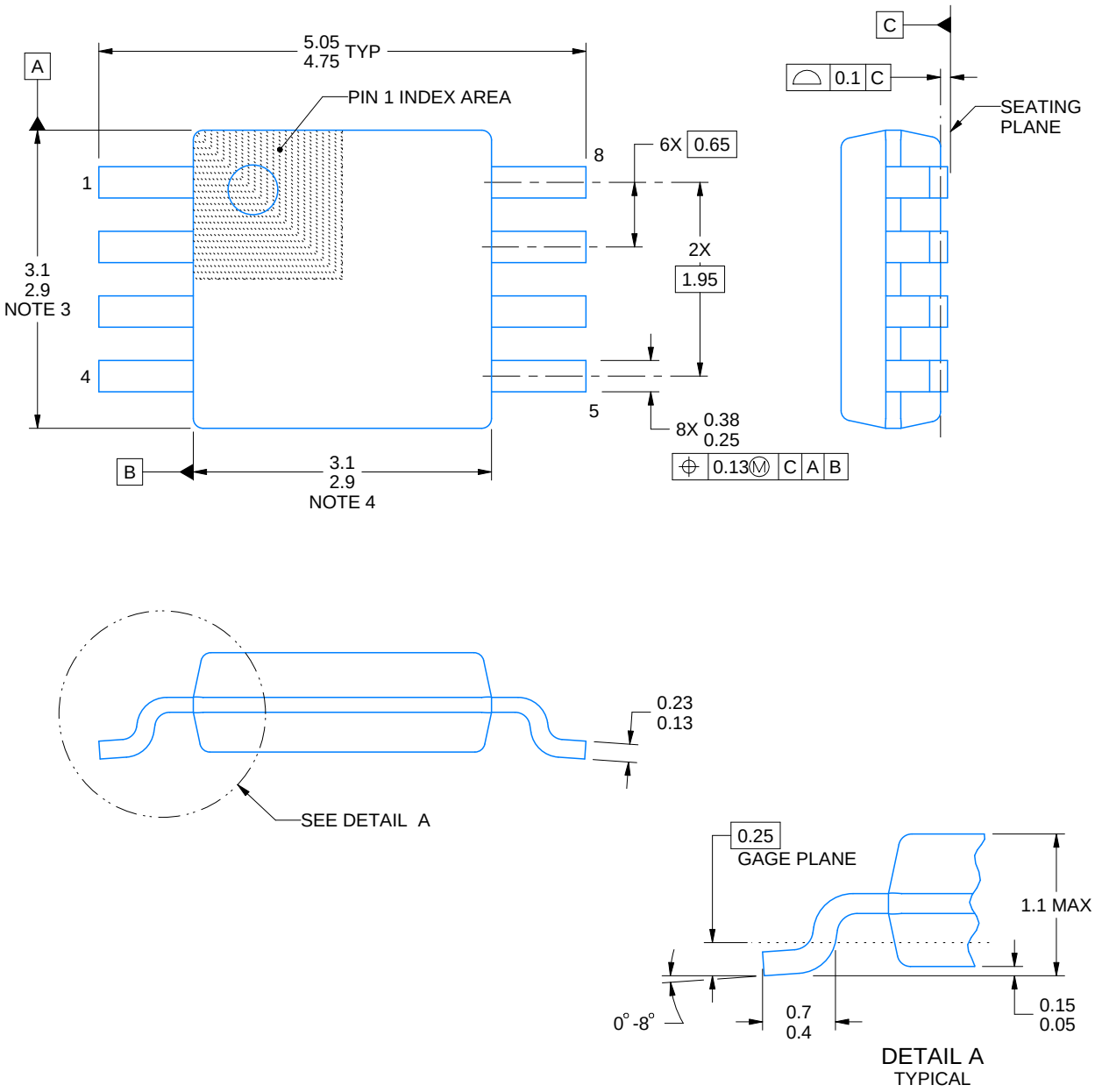
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

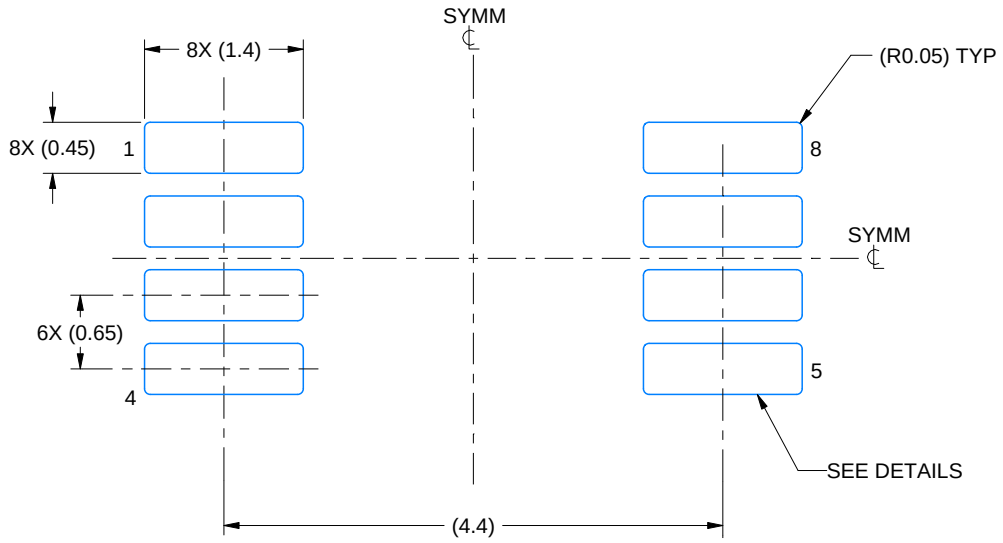
SMALL OUTLINE PACKAGE



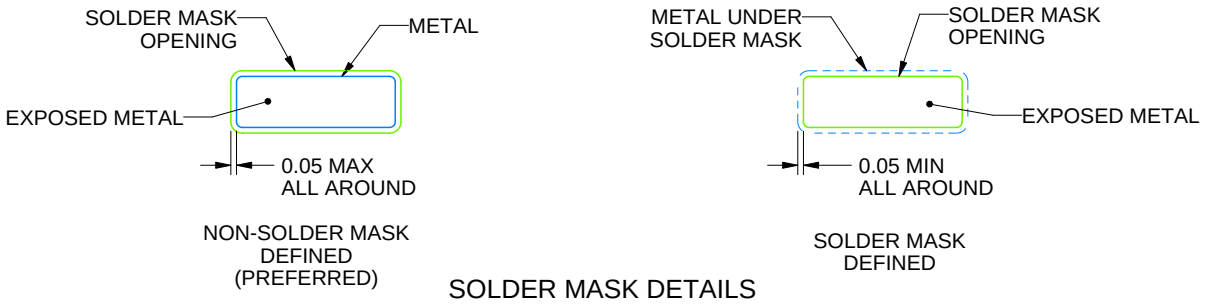

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

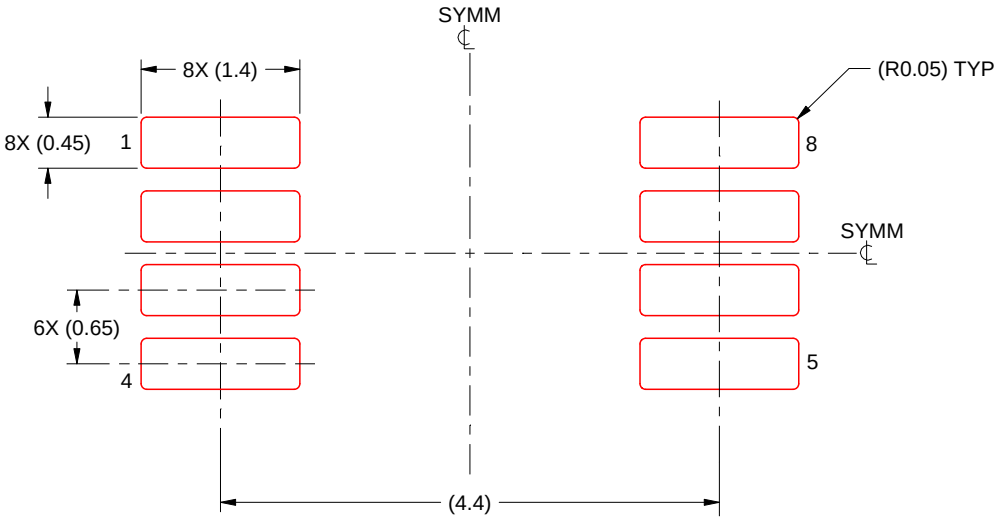



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



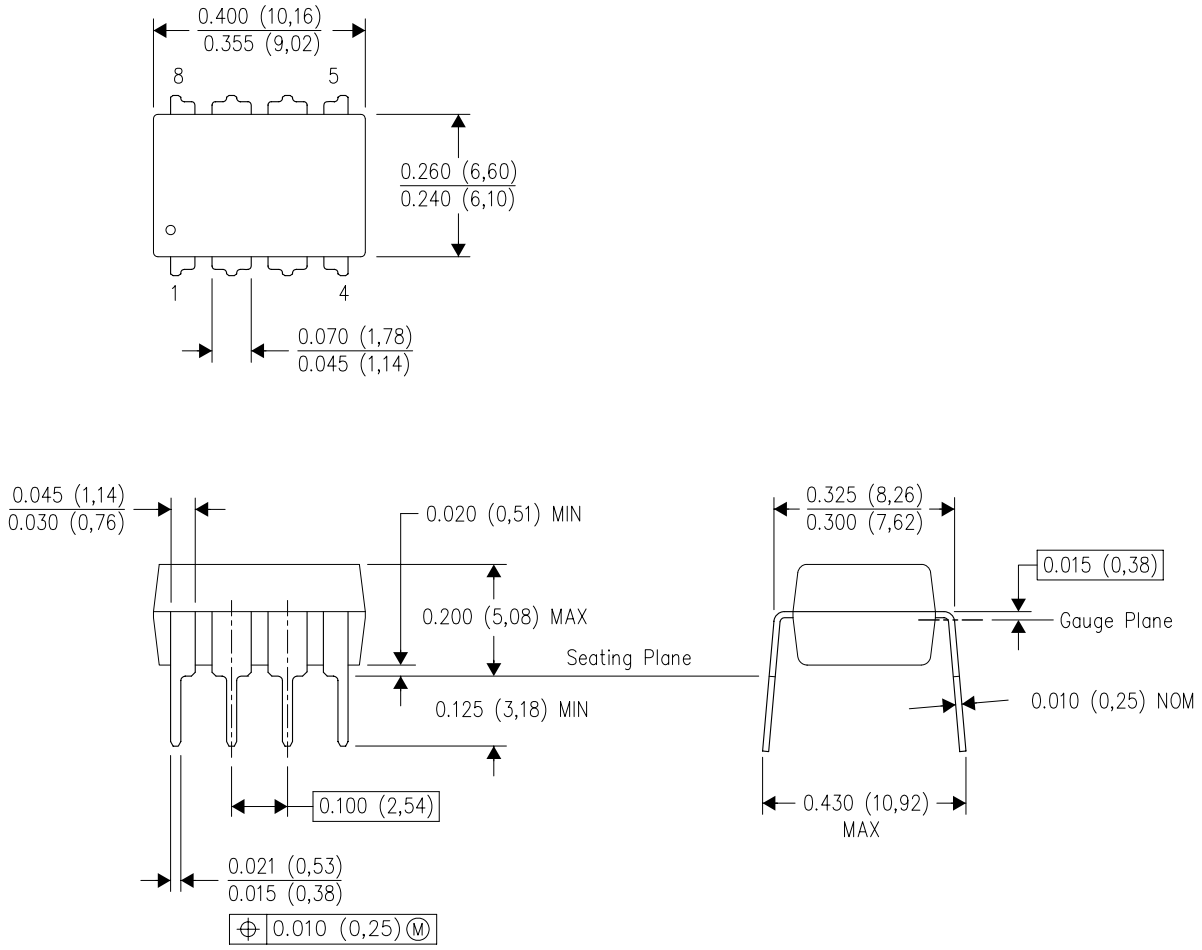

SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



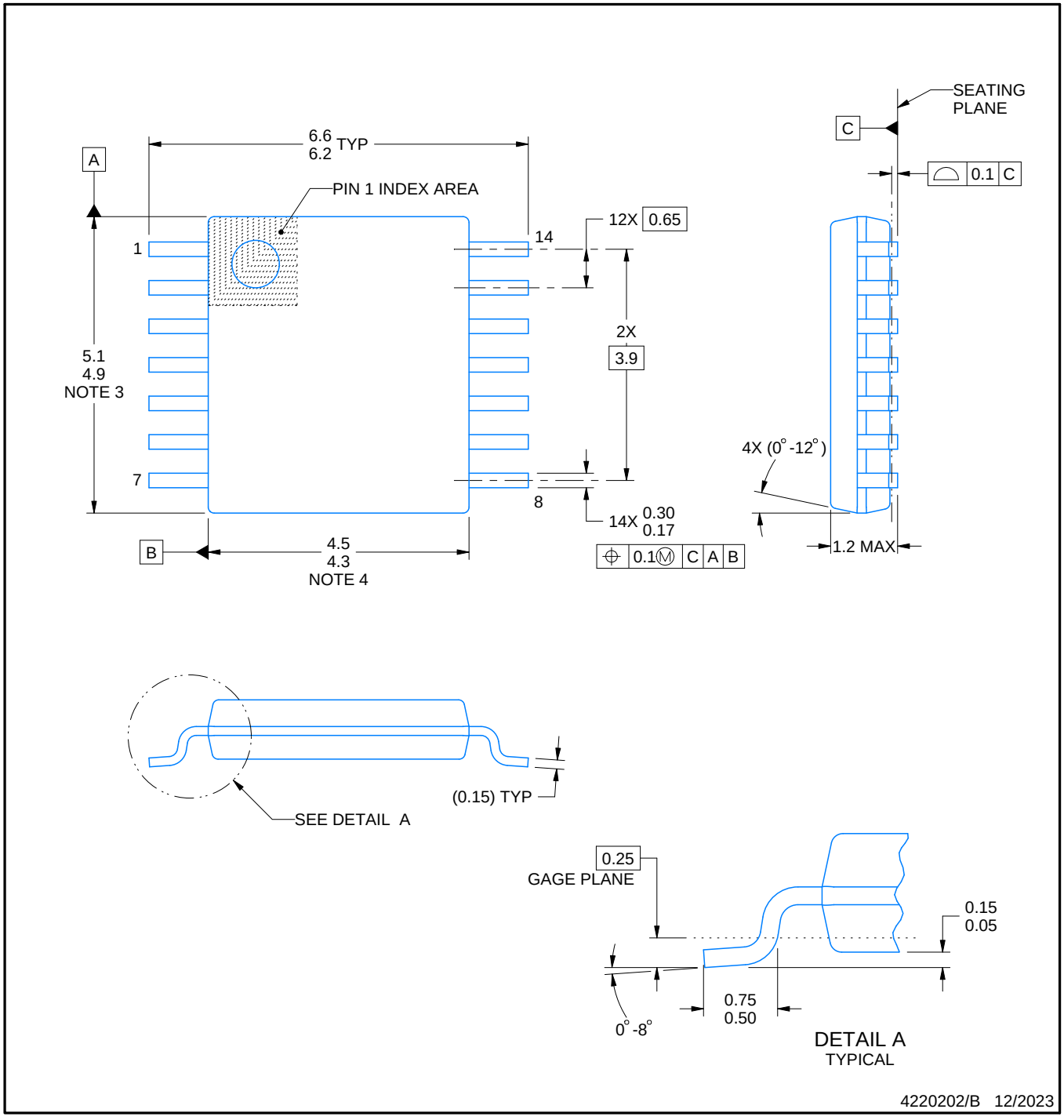

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# PACKAGE OUTLINE

## PW0014A

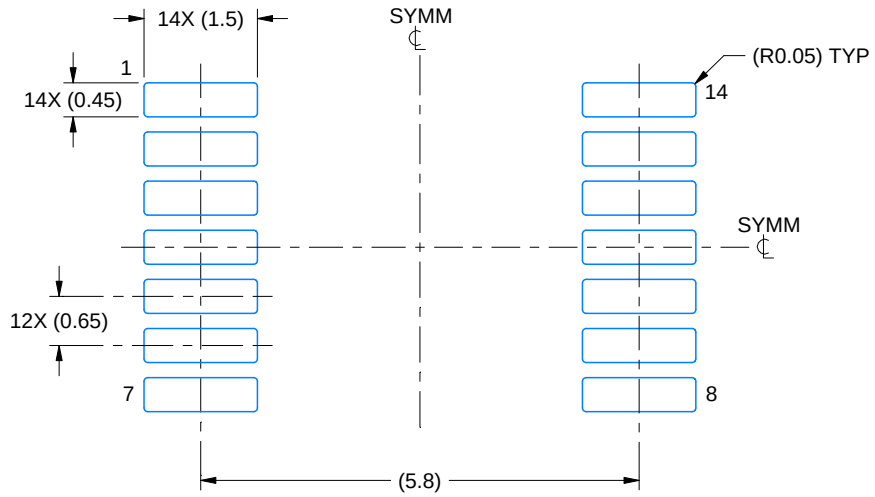
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

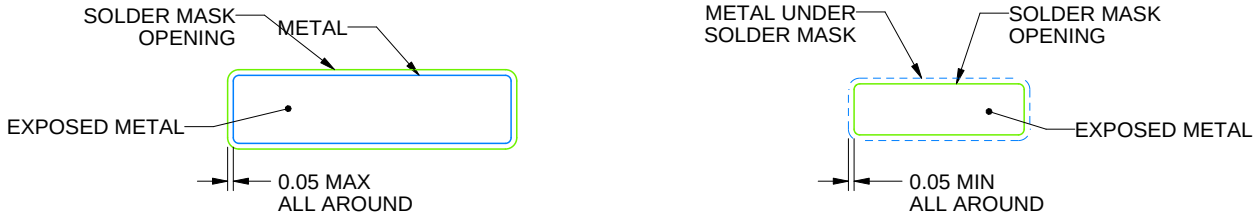



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

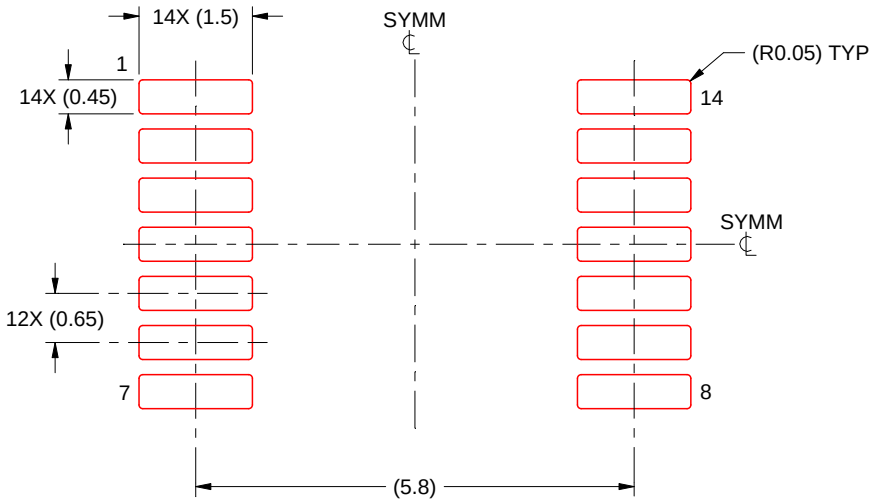



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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