Very Low-Power, Dual, Current-Feedback Operational Amplifier

FEATURES

- REDUCED BANDWIDTH CHANGE VERSUS GAIN
- 150MHz BANDWIDTH G = +2
- > 80MHz BANDWIDTH TO GAIN > +10
- LOW DISTORTION: < –65dBc at 5MHz
- HIGH OUTPUT CURRENT: 110mA
- SINGLE-SUPPLY OPERATION: +5V to +12V
- DUAL-SUPPLY OPERATION: ±2.5V to ±6V
- LOW SUPPLY CURRENT: 1.9mA Total
- POWER SHUTDOWN VERSION: MSOP-10

APPLICATIONS

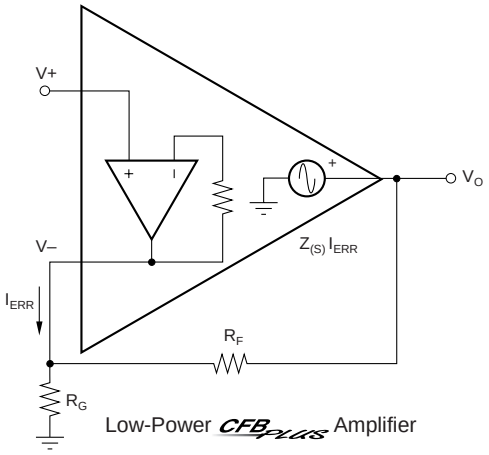
- LOW-POWER BROADCAST VIDEO DRIVERS
- μPOWER ACTIVE FILTERS
- SHORT-LOOP ADSL CO DRIVERS
- MULTICHANNEL SUMMING AMPLIFIERS
- PROFESSIONAL CAMERAS
- DIFFERENTIAL ADC INPUT DRIVERS

DESCRIPTION

The OPA2683 provides a new level of performance for dual, very low-power, wideband, current-feedback amplifiers. This CFB_{PLUS} amplifier is among the first to use an internally closed-loop input buffer stage that significantly enhances performance over earlier low-power, current-feedback (CFB) amplifiers. This new architecture provides many of the advantages of a more ideal CFB amplifier while retaining the benefits of very low-power operation. The closed-loop input stage buffer gives a very low and linearized impedance path at the inverting input to sense the feedback error current. This improved inverting input impedance gives exceptional bandwidth retention to much higher gains and improved harmonic distortion over earlier solutions limited by inverting input linearity. Beyond simple high gain applications, the OPA2683 CFB_{PLUS} amplifier can allow the gain setting element to be set with considerable freedom from amplifier bandwidth interaction. This flexibility allows frequency response peaking elements to be added, multiple input inverting summing circuits to have greater bandwidth, and low-power differential line drivers to meet the demanding requirements of DSL.

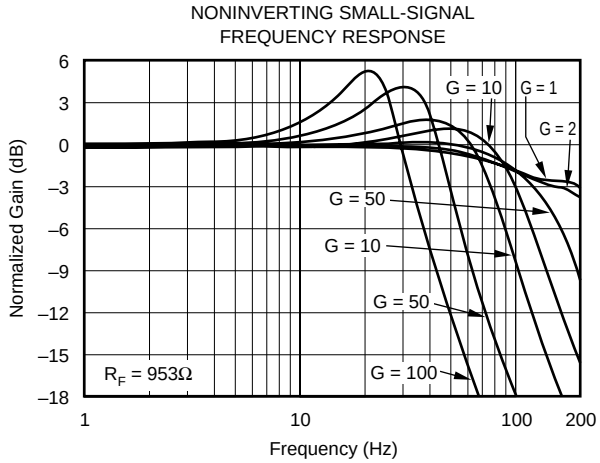
The output capability for the OPA2683 also sets a new mark in performance for very low-power, current-feedback amplifiers. Delivering a full $\pm 4V_{PP}$ swing on ±5V supplies, the OPA2683 also has the output current to support this swing into a 100Ω load. This minimal output headroom requirement is complemented by a similar 1.2V input stage headroom, giving exceptional capability for single +5V operation.

The OPA2683's low 1.9mA total supply current is precisely trimmed at +25°C. This trim, along with low shift over temperature and supply voltage, gives a very robust design over a wide range of operating conditions. Further system power reduction is possible using the shutdown feature of the MSOP-10 package.



Low-Power CFB_{PLUS} Amplifier

U.S. Patent No. 6,724,260



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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: ID, IDCN	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating: Human Body Model (HBM)	2000V
Charged Device Model (CDM)	1000V

NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

OPA2683 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA684	OPA2684	OPA3684	OPA4684	Low-Power CFB
OPA691	OPA2691	OPA3691	—	High Slew Rate CFB
OPA695	OPA2695	OPA3695	—	> 500MHz CFB

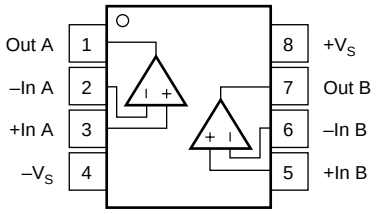
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2683	SO-8	D	–40°C to +85°C	OPA2683	OPA2683ID	Rails,100
"	"	"	"	"	OPA2683IDR	Tape and Reel, 2500
OPA2683	SOT23-8	DCN	–40°C to +85°C	B83	OPA2683IDCNT	Tape and Reel, 250
"	"	"	"	"	OPA2683IDCNR	Tape and Reel, 3000
OPA2683	MSOP-10	DGS	–40°C to +85°C	BUI	OPA2683IDGST	Tape and Reel, 250
"	"	"	"	"	OPA2683IDGSR	Tape and Reel, 2500

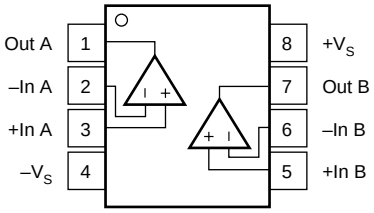
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

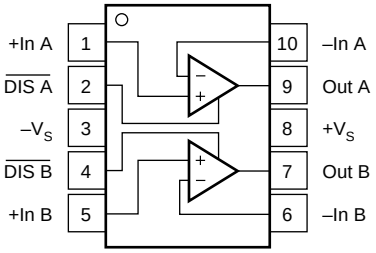
Top View **SO-8**

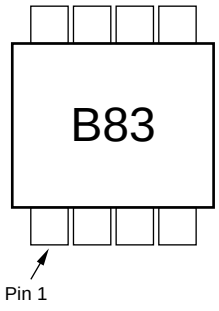


Top View **SOT23-8**



Top View **MSOP-10**





ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 953\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA2683ID, IDCN, IDGS						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O = 0.5V_{PP}$)	G = +1, $R_F = 953k\Omega$	200				MHz	typ	C
	G = +2, $R_F = 953\Omega$	150	124	121	117	MHz	min	B
	G = +5, $R_F = 953\Omega$	121				MHz	typ	C
	G = +10, $R_F = 953\Omega$	94				MHz	typ	B
	G = +20, $R_F = 953\Omega$	72				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O = 0.5V_{PP}$, $R_F = 953\Omega$	37	15	14	14	MHz	min	B
Peaking at a Gain of +1	$R_F = 953\Omega$, $V_O = 0.5V_{PP}$	1.8	6.5	7.7	8.0	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 4V_{PP}$	63				MHz	typ	C
Slew Rate	G = –1, V_O = 4V Step (see Figure 2)	540	450	450	430	V/µs	min	B
	G = +2, V_O = 4V Step	400	345	338	336	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	4.6				ns	typ	C
	G = +2, V_O = 4V Step	7.8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–63	–54	–54	–54	dBc	max	B
	$R_L \geq 1k\Omega$	–71	–55	–55	–55	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–67	–62	–62	–62	dBc	max	B
	$R_L \geq 1k\Omega$	–77	–67	–66	–66	dBc	max	B
Input Voltage Noise	f > 1MHz	4.4	5.0	5.5	5.8	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	5.1	5.8	6.4	6.7	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	11.6	11.9	12.3	12.4	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, $V_O = 1.4V_P$, $R_L = 150\Omega$	0.13				%	typ	C
Differential Phase	G = +2, NTSC, $V_O = 1.4V_P$, $R_L = 150\Omega$	0.06				deg	typ	C
Channel-to-Channel Isolation	f = 5MHz	70				dB	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 1k\Omega$	700	**300**	270	250	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.5	**±3.5**	±4.1	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	±2.0	**±4.5**	±5.1	±5.3	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			±15	±15	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±3.0	**±10**	±11	±11.5	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±20	±20	nA°/C	max	B
INPUT								
Common-Mode Input Range(5) (CMIR)		±3.75	**±3.65**	±3.65	±3.60	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	60	**53**	52	52	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop, DC	5.0				Ω	typ	C
OUTPUT								
Voltage Output Swing	1kΩ Load	±4.1	**±4.0**	±4.0	±3.9	V	min	A
Current Output, Sourcing	V_O = 0	150	**120**	115	110	mA	min	A
Current Output, Sinking	V_O = 0	–110	**–100**	–95	–90	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.007				Ω	typ	C
DISABLE (Disabled LOW) (MSOP-10 Only)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, Both Channel	–200	**–300**	–340	–360	µA	max	A
Disable Time	V_{IN} = +1, See Figure 1	60				ms	typ	C
Enable Time	V_{IN} = +1, See Figure 1	40				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±70				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.4	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V, Each Channel	80	**120**	130	135	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Max Operating Voltage Range			**±6**	±6	±6	V	max	A
Min Operating Voltage Range		±2				V	typ	C
Max Quiescent Current	V_S = ±5V, Both Channels	1.88	**2.06**	2.08	2.10	mA	max	A
Min Quiescent Current	V_S = ±5V, Both Channels	1.88	**1.70**	1.6	1.54	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	62	**55**	54	54	dB	typ	A
TEMPERATURE RANGE								
Specification: D, DCN, DGS		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DCN SOT23-8		150				°C/W	typ	C
DGS MSOP-10		140				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +2°C at high temperature limit for over-temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterizationand simulation. (C) Typical value only for information.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 1.2kΩ, R_L = 1kΩ, and G = +2 (see Figure 3 for AC performance only), unless otherwise noted.

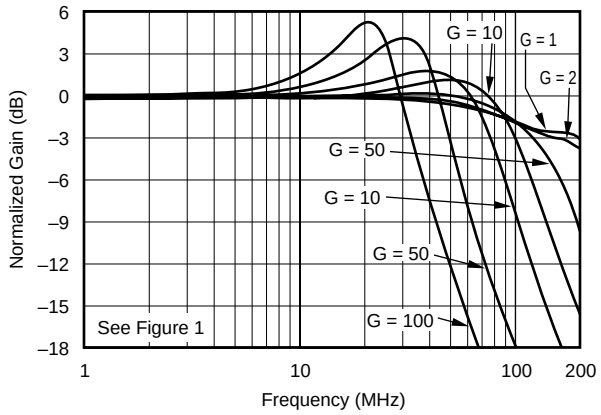
PARAMETER	CONDITIONS	OPA2683ID, IDCN, IDGS						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.2V_{PP})	G = +1, R_F = 1.2kΩ	145				MHz	typ	
	G = +2, R_F = 1.2kΩ	119	96	92	90	MHz	min	B
	G = +5, R_F = 1.2kΩ	95				MHz	typ	C
	G = +10, R_F = 1.2kΩ	87				MHz	typ	C
	G = +20, R_F = 1.2kΩ	60				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}, R_F = 1.2kΩ	14	9	8	8	MHz	min	B
Peaking at a Gain of +1	R_F = 1.2kΩ, V_O < 0.5V_{PP}	1	6	8	8	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	70				MHz	typ	C
Slew Rate	G = +2, V_O = 2V Step	210	180	175	170	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	5.9				ns	typ	C
	G = +2, V_O = 2V Step	7.8				ns	typ	C
Harmonic Distortion	G = 2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–60	–54	–53	–53	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–66	–55	–55	–55	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–59	–58	–58	–58	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–74	–57	–56	–56	dBc	max	B
Input Voltage Noise	f > 1MHz	4.4	5.0	5.5	5.8	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	5.1	5.8	6.4	6.7	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	11.6	11.9	12.3	12.4	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.24				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.19				deg	typ	C
Channel-to-Channel Crosstalk	f = 5MHz	70				dB	type	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 1kΩ to V_S/2	700	**300**	270	250	kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	±1.0	**±3.0**	±3.6	±3.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	±2	**±4.5**	±5.1	±5.3	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±12	±12	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	±3	**±8**	±8.7	±8.9	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±15	±15	nA°/C	max	B
INPUT								
Least Positive Input Voltage(5)		1.1	**1.25**	1.29	1.34	V	max	A
Most Positive Input Voltage(5)		3.9	**3.75**	3.73	3.67	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = V_S/2	56	**51**	50	50	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop, DC	5.6				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	R_L = 1kΩ to V_S/2	4.2	**4.1**	4.1	4.0	V	min	A
Least Positive Output Voltage	R_L = 1kΩ to V_S/2	0.8	**0.9**	0.9	1.0	V	max	A
Current Output, Sourcing	V_O = V_S/2	80	**65**	63	58	mA	min	A
Current Output, Sinking	V_O = V_S/2	–70	**–52**	–50	–45	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.009				Ω	typ	C
DISABLE (Disabled LOW) (MSOP-10 Only)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, Both Channels	–200				µA	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±70				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.4	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V, Each Channel	80	**120**	130	135	µA	max	A
POWER SUPPLY								
Specified Single-Supply Operating Voltage		+5				V	typ	C
Max Single-Supply Operating Voltage			**+12**	+12	+12	V	max	A
Min Single-Supply Operating Voltage		+4				V	typ	C
Max Quiescent Current	V_S = +5V, Both Channels	1.58	**1.76**	1.76	1.76	mA	max	A
Min Quiescent Current	V_S = +5V, Both Channels	1.58	**1.36**	1.32	1.28	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	65				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DCN, DGS		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DCN SOT23-8		150				°C/W	typ	C
DGS MSOP-10		140				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +2°C at high temperature limit for over-temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

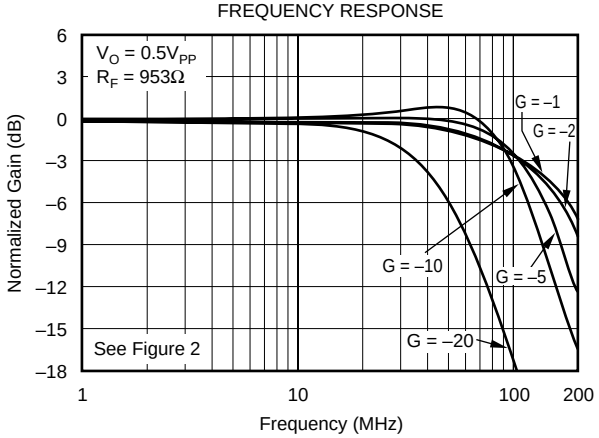
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.

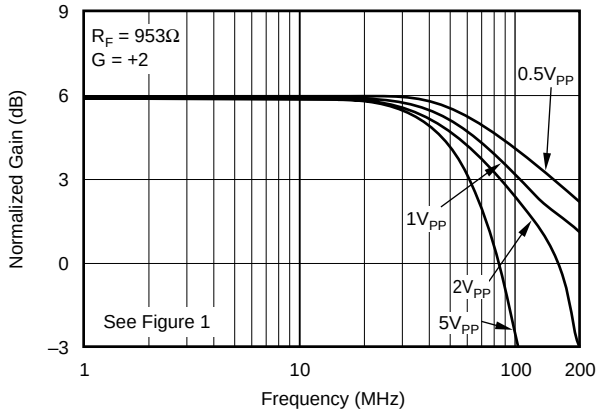
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



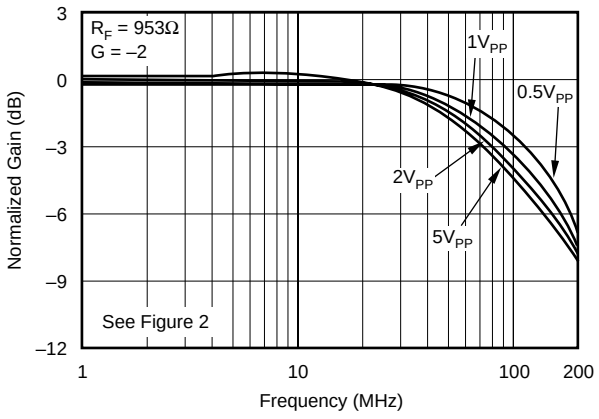
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



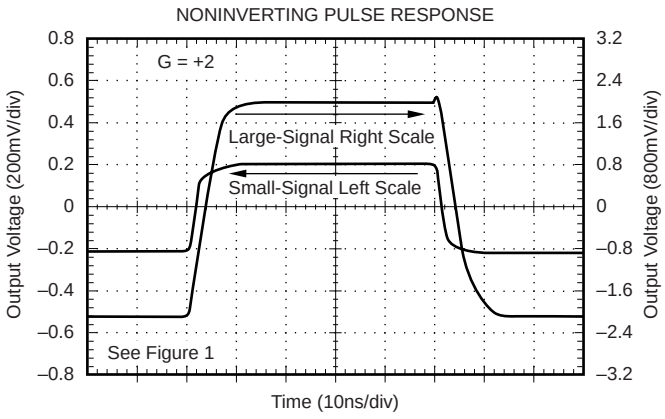
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



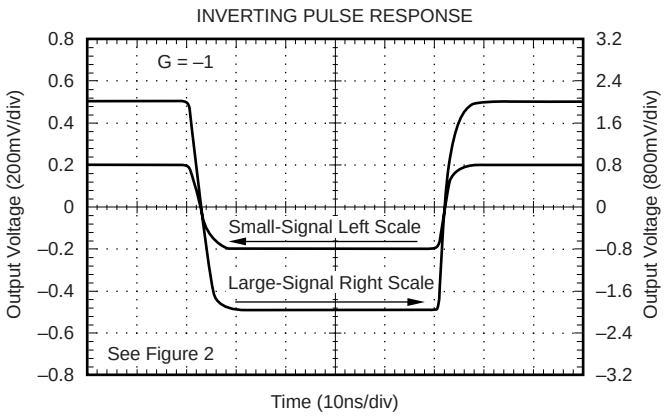
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



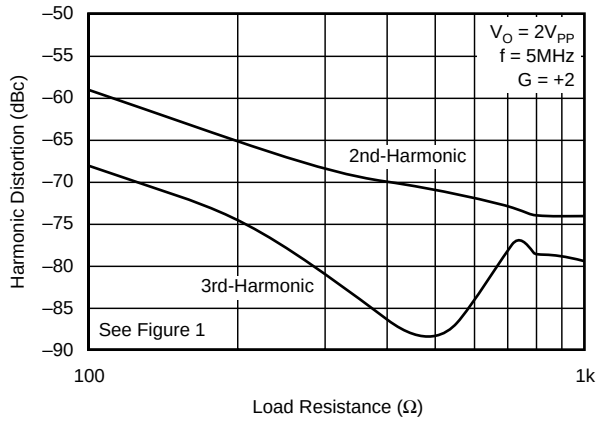
INVERTING PULSE RESPONSE



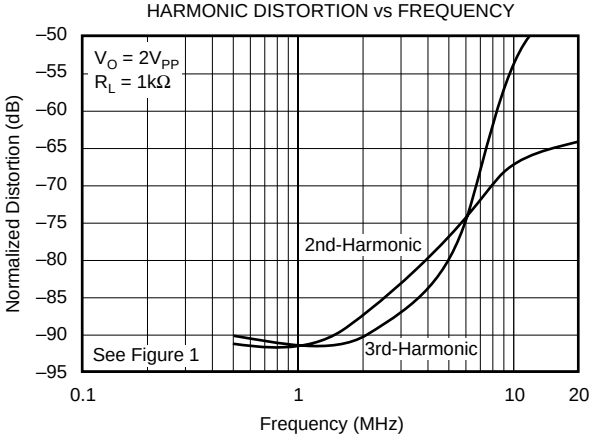
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.

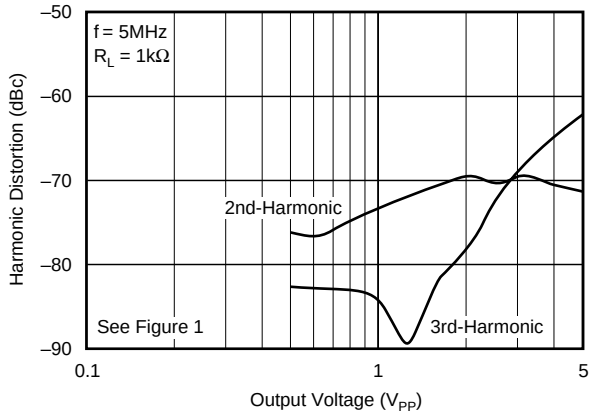
HARMONIC DISTORTION vs LOAD RESISTANCE



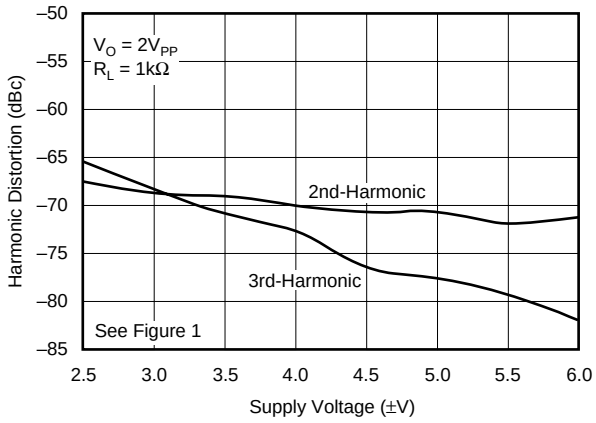
HARMONIC DISTORTION vs FREQUENCY



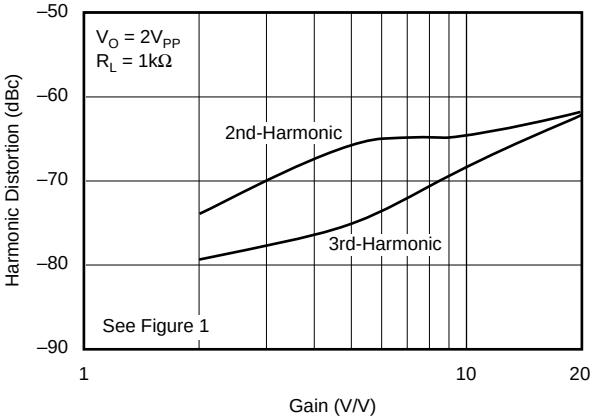
HARMONIC DISTORTION vs OUTPUT VOLTAGE



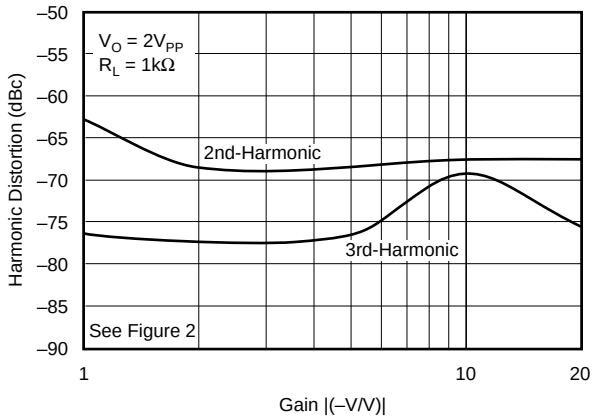
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



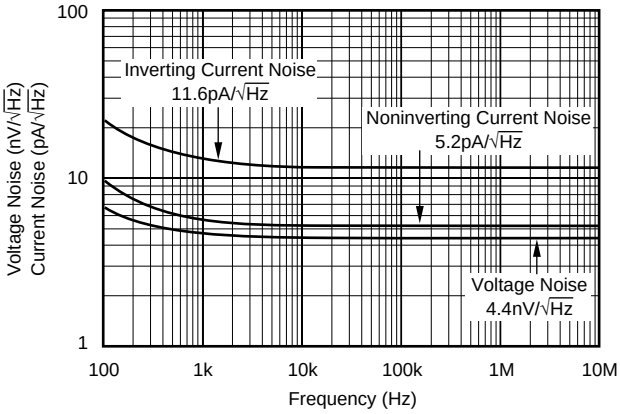
HARMONIC DISTORTION vs INVERTING GAIN



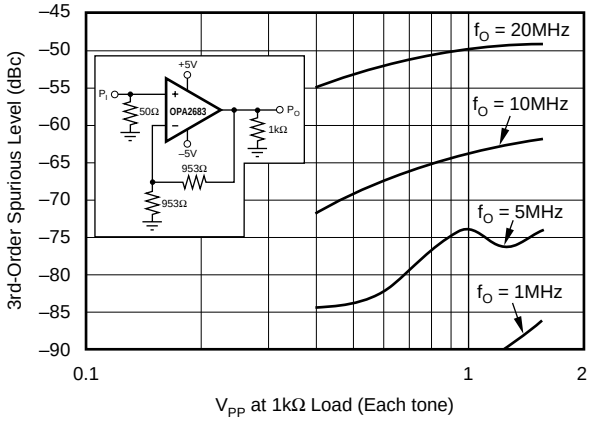
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.

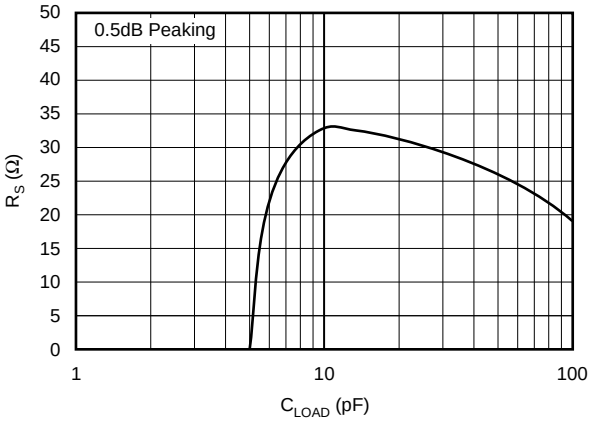
INPUT VOLTAGE AND CURRENT NOISE DENSITY



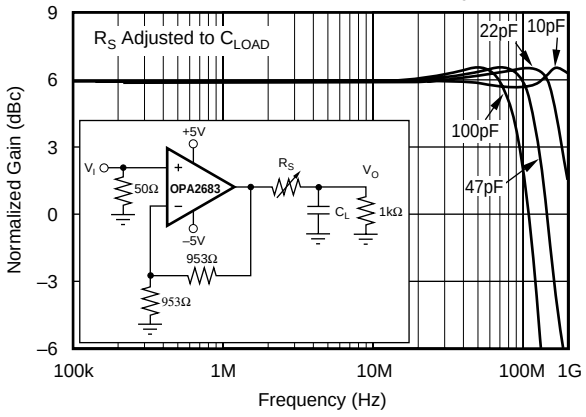
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



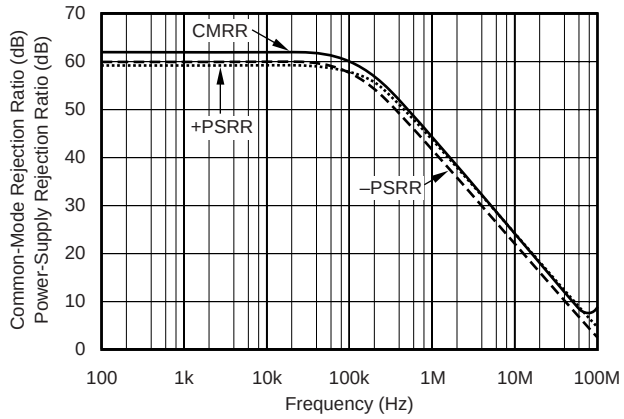
R_S vs C_{LOAD}



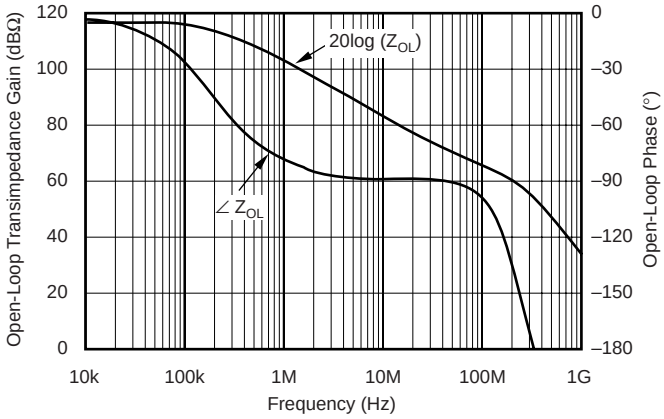
SMALL-SIGNAL BANDWIDTH vs C_{LOAD}



CMRR AND PSRR vs FREQUENCY



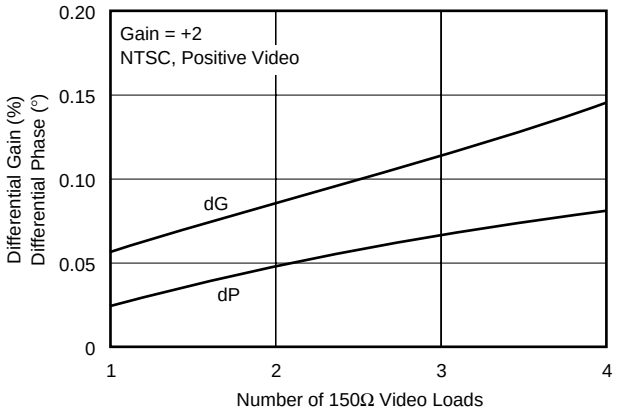
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE



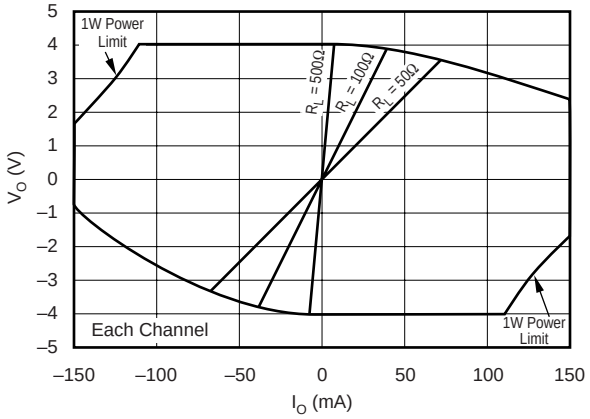
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.

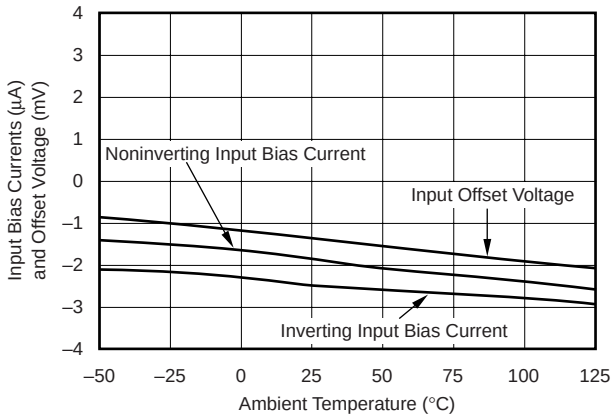
COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



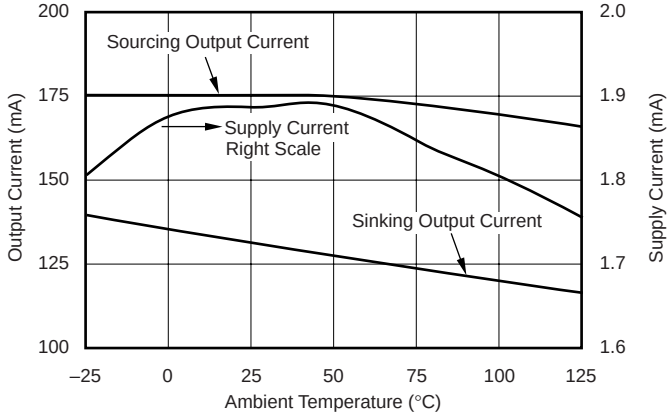
OUTPUT CURRENT AND VOLTAGE LIMITATIONS



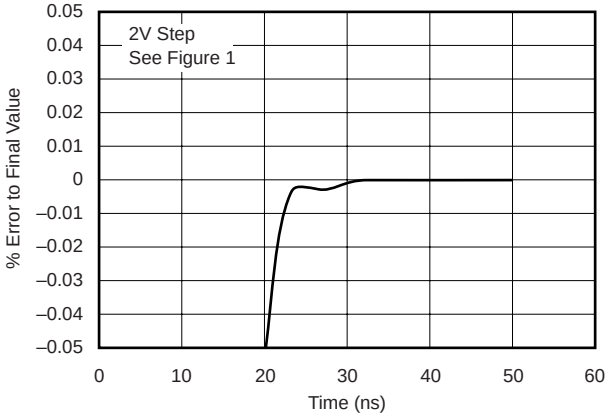
TYPICAL DC DRIFT OVER TEMPERATURE



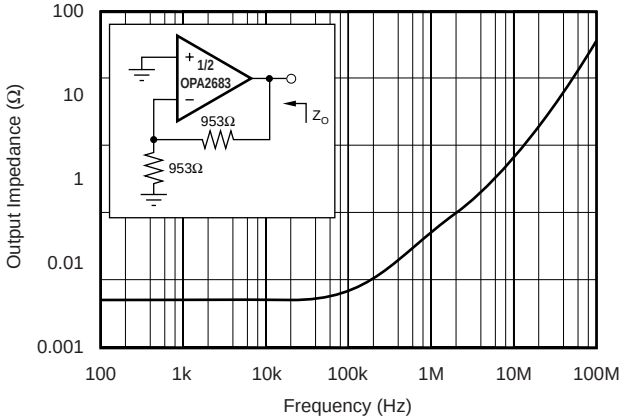
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



SETTLING TIME



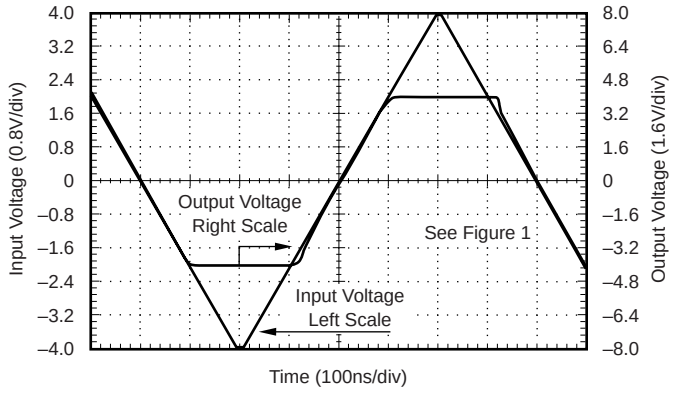
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



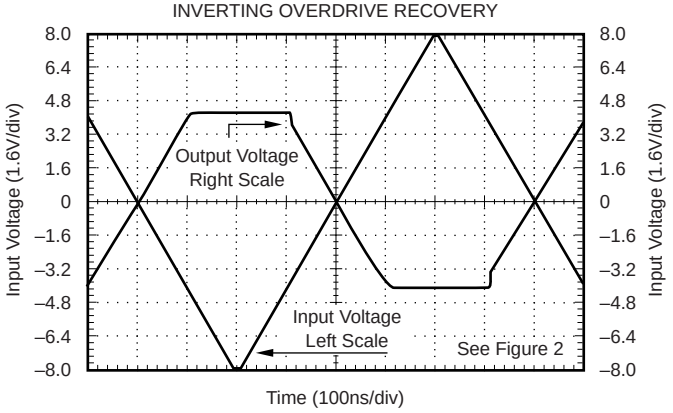
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.

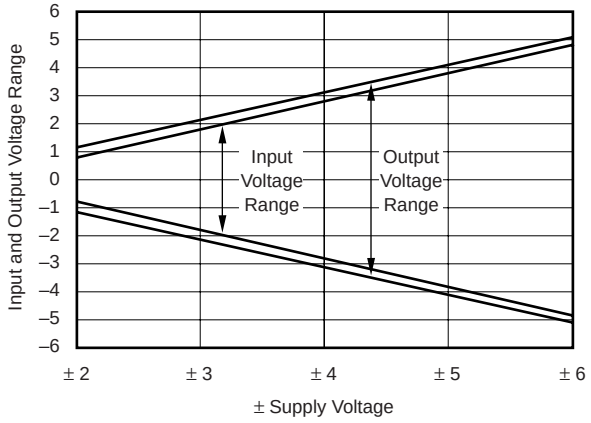
NONINVERTING OVERDRIVE RECOVERY



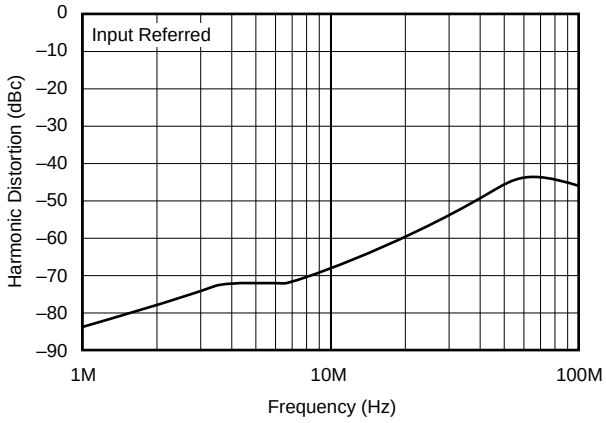
INVERTING OVERDRIVE RECOVERY



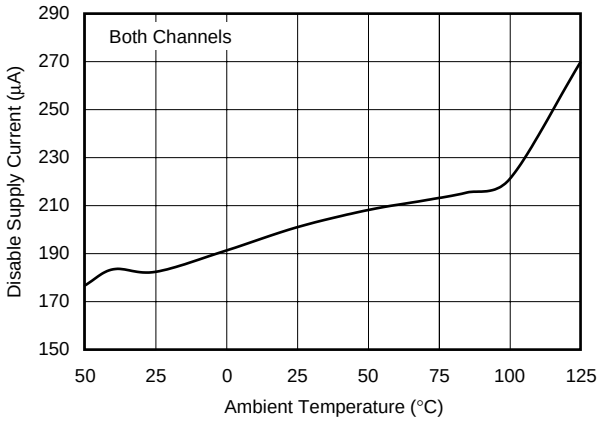
INPUT AND OUTPUT RANGE vs SUPPLY VOLTAGE



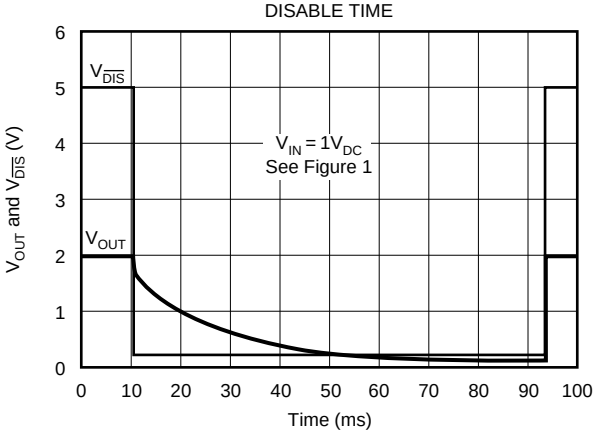
CHANNEL-TO-CHANNEL CROSSTALK



DISABLE SUPPLY CURRENT vs TEMPERATURE

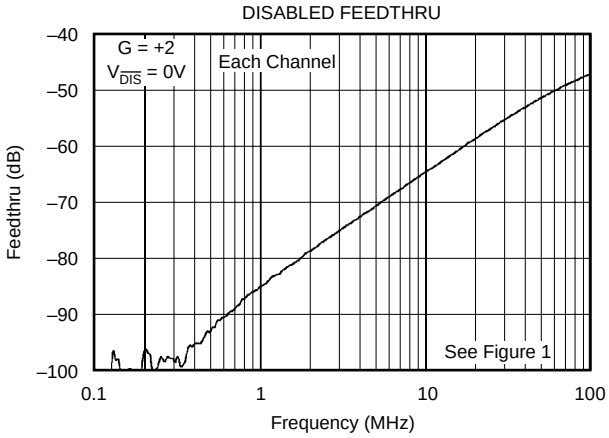


DISABLE TIME



TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

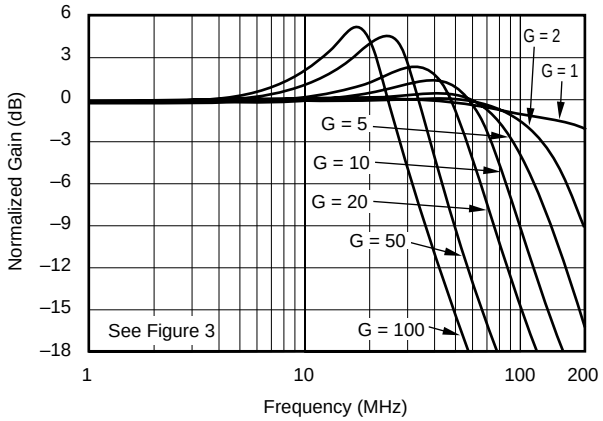
T_A = +25°C, G = +2, R_F = 953Ω, and R_L = 1kΩ, unless otherwise noted.



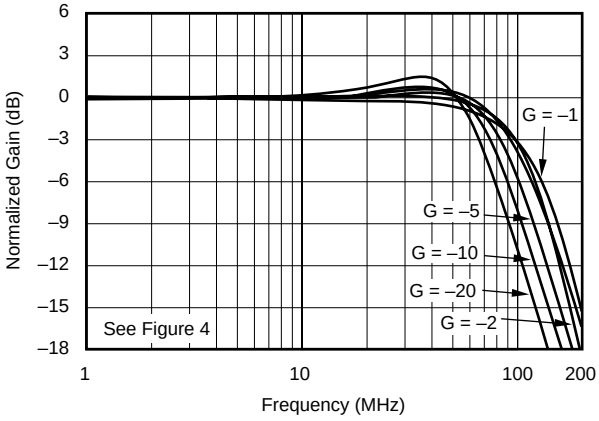
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, V_S = 5V, G = +2, R_F = 1.2kΩ, and R_L = 1kΩ, unless otherwise noted.

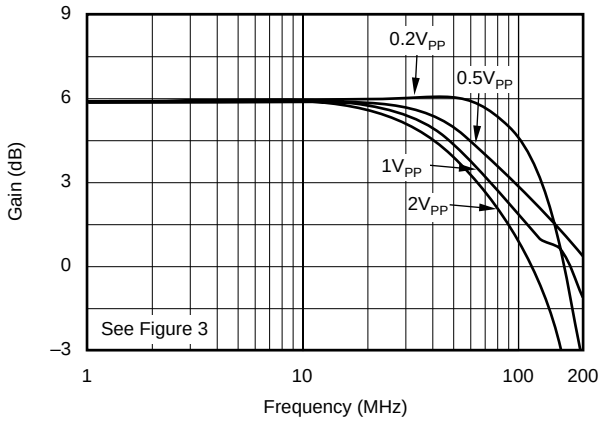
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



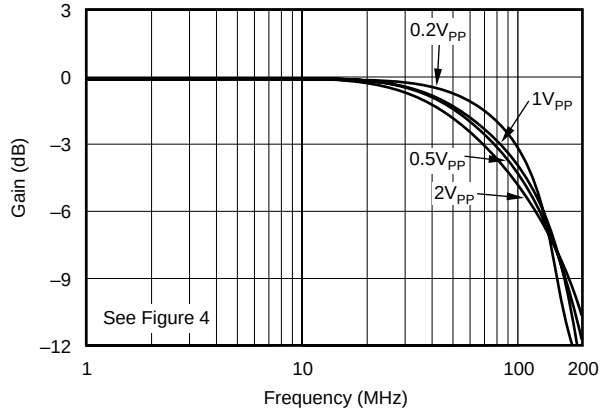
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



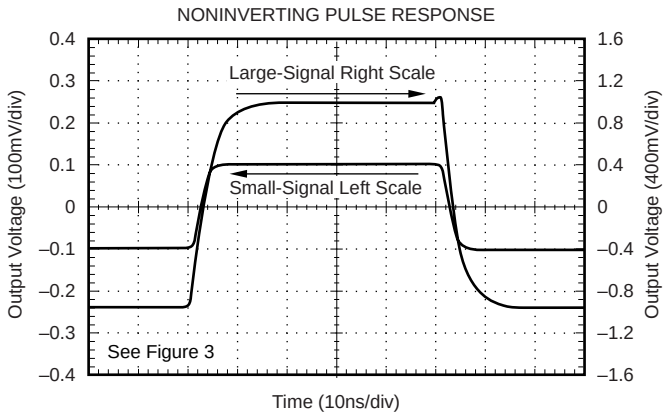
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



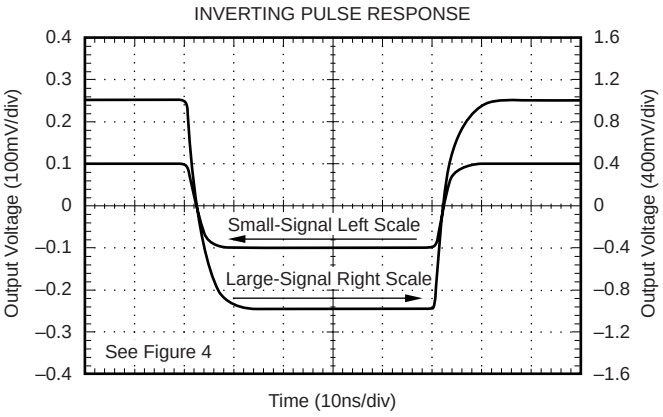
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



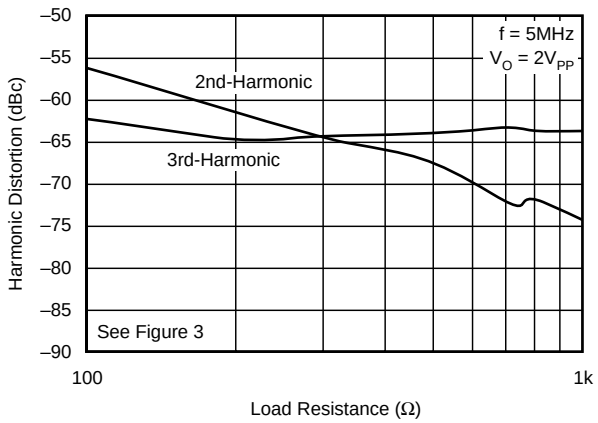
INVERTING PULSE RESPONSE



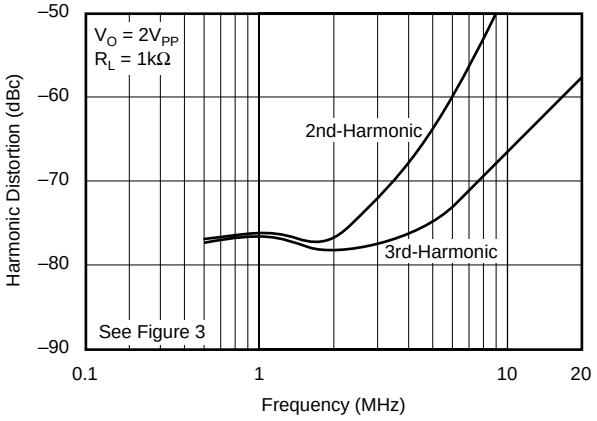
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

T_A = +25°C, V_S = 5V, G = +2, R_F = 1.2kΩ, and R_L = 1kΩ, unless otherwise noted.

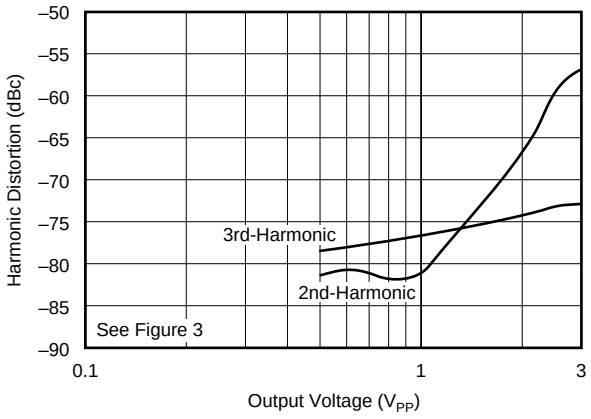
HARMONIC DISTORTION vs LOAD RESISTANCE



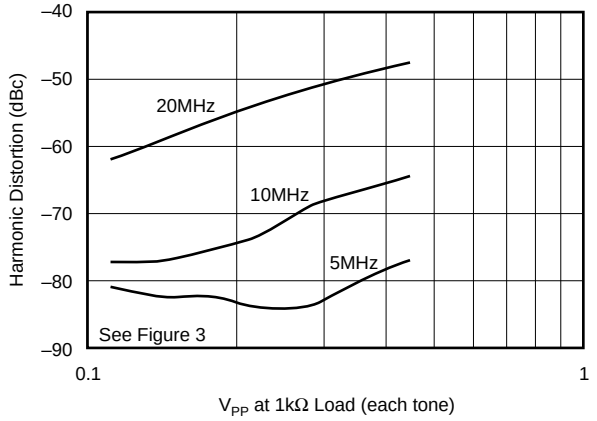
HARMONIC DISTORTION vs FREQUENCY



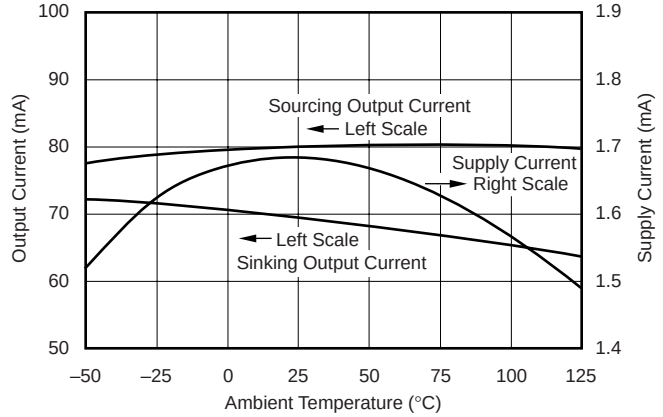
HARMONIC DISTORTION vs OUTPUT VOLTAGE



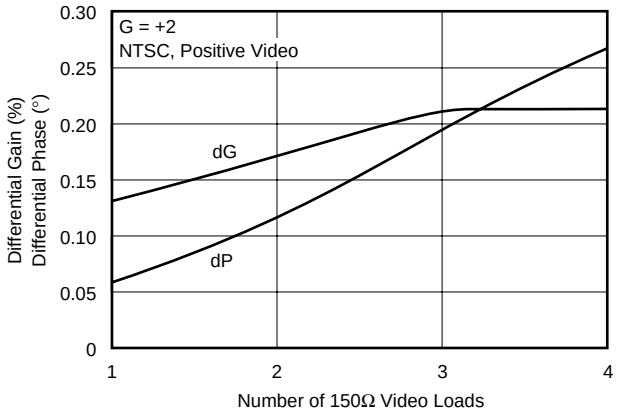
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



APPLICATIONS INFORMATION

LOW-POWER, CURRENT-FEEDBACK OPERATION

The dual channel OPA2683 gives a new level of performance in low-power, current-feedback op amps. Using a new input stage buffer architecture, the OPA2683 CFB_{PLUS} amplifier holds nearly constant AC performance over a wide gain range. This closed-loop internal buffer gives a very low and linearized impedance at the inverting node, isolating the amplifier's AC performance from gain element variations. This low impedance allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current- feedback performance of gain bandwidth independence. This low-power amplifier also delivers exceptional output power—its ±4V swing on ±5V supplies with > 100mA output drive gives excellent performance into standard video loads or doubly-terminated 50Ω cables. This dual-channel device can provide adequate drive for several emerging differential driver applications with exceptional power efficiency. Single +5V supply operation is also supported with similar bandwidths but reduced output power capability. For higher output power in a dual current-feedback op amp, consider the OPA2684, OPA2691, or OPA2677.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit used as the basis of the ±5V Electrical and Typical Characteristics for each channel. For test purposes, the input impedance is set to 50Ω with a resistor to ground, and the output impedance is set to a 1kΩ load. Voltage swings reported in the characteristics are taken directly at the input and output pins. For the circuit of Figure 1, the total effective load will be 1kΩ || 1.9kΩ = 656Ω. Gain changes are most easily accomplished by simply resetting the R_G value, holding R_F constant at its recommended value of 953Ω.

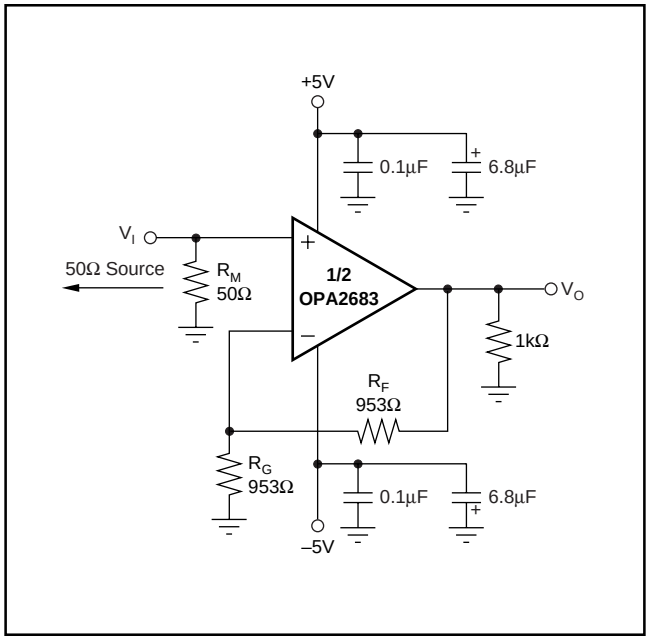


FIGURE 1. DC-Coupled, G = +2V/V, Bipolar Supply Specifications and Test Circuit.

Figure 2 shows the DC-coupled, gain of –1V/V, dual power-supply circuit used as the basis of the inverting Typical Characteristics for each channel. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is typically higher and the distortion performance is slightly improved. An additional input resistor, R_M, is included in Figure 2 to set the input impedance equal to 50Ω. The parallel combination of R_M and R_G set the input impedance. As the desired gain increases for the inverting configuration, R_G is adjusted to achieve the desired gain, while R_M is also adjusted to hold a 50Ω input match. A point will be reached where R_G will equal 50Ω, R_M is removed, and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, increasing R_F will increase the gain. However, this will reduce the achievable bandwidth as the feedback resistor increases from its recommended value of 953Ω. If the source does not require an input match to 50Ω, either adjust R_M to get the desired load, or remove it and let the R_G resistor alone provide the input load.

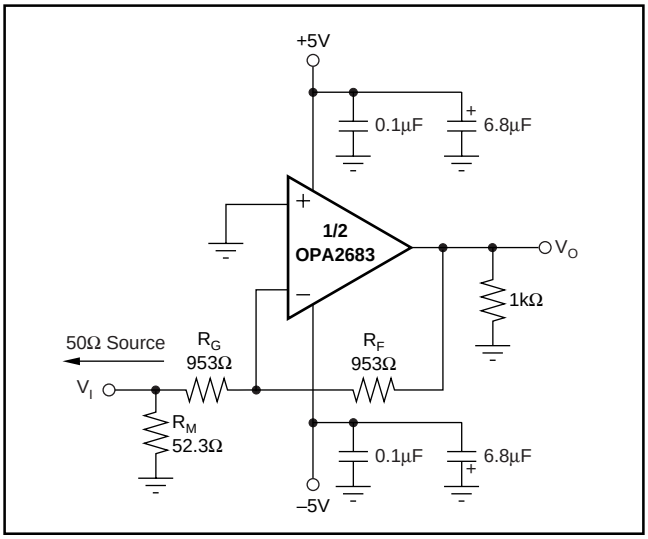


FIGURE 2. DC-Coupled, G = –1V/V, Bipolar Supply Specifications and Test Circuit.

These circuits show ±5V operation. The same circuit can be applied with bipolar supplies from ±2.5V to ±6V. Internal supply independent biasing gives nearly the same performance for the OPA2683 over this wide range of supplies. Generally, the optimum feedback resistor value (for nominally flat frequency response at G = +2) will increase in value as the total supply voltage across the OPA2683 is reduced from ±5V.

See Figure 3 for the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis only for the +5V Electrical and Typical Characteristics for each channel. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 10kΩ resistors) to the noninverting input. The input signal is then AC-coupled

into this midpoint voltage bias. The input voltage can swing to within 1.25V of either supply pin, giving a $2.5V_{PP}$ input signal range centered between the supply pins. The input impedance of Figure 3 is set to give a 50Ω input match. If the source does not require a 50Ω match, remove this and drive directly into the blocking capacitor. The source will then see the 5kΩ load of the biasing network. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the noninverting input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar ±5V supply condition to re-optimize for a flat frequency response in +5V only, gain of +2, operation. On a single +5V supply, the output voltage can swing to within 0.9V of either supply pin while delivering more than 70mA output current, giving 3.2V output swing into 100Ω (8dBm maximum at a matched 50Ω load). The circuit of Figure 3 shows a blocking capacitor driving into a 1kΩ load. Alternatively, the blocking capacitor could be removed if the load is tied to a supply midpoint or to ground if the DC current required by the load is acceptable.

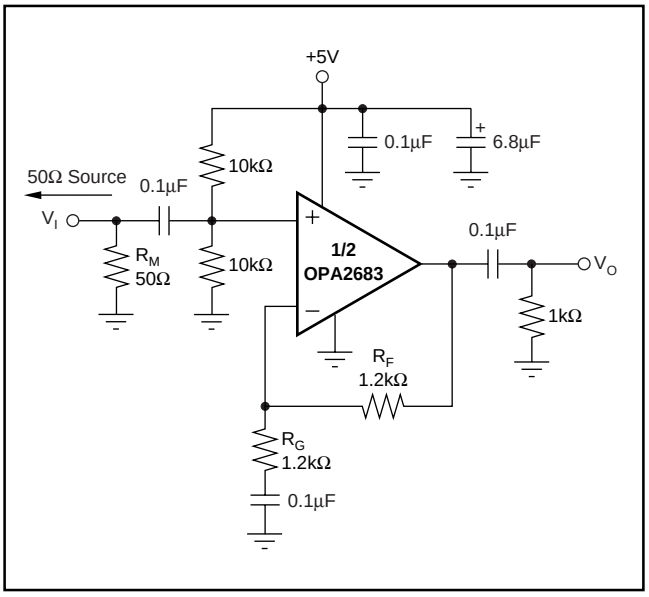


FIGURE 3. AC-Coupled, G = +2V/V, Single-Supply Specifications and Test Circuit.

Figure 4 shows the AC-coupled, single +5V supply, gain of –1V/V circuit configuration used as a basis for the +5V Typical Characteristics for each channel. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.1µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin. One advantage to inverting operation is that since there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages is possible. To retain a $1V_{PP}$ output capability, operation down to 3V supply is allowed. At +3V supply, the input stage is saturated, but for the inverting configuration of a current-feedback amplifier, wideband operation is retained even under this condition.

The circuits of Figure 3 and 4 show single-supply operation at +5V. These same circuits may be used up to single supplies of +12V with minimal change in the performance of the OPA2683.

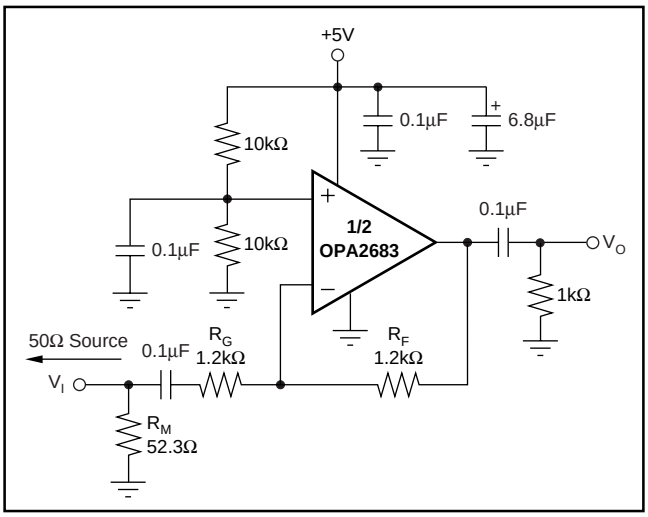


FIGURE 4. AC-Coupled, G = –1V/V, Single-Supply Specifications and Test Circuit.

DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog-to-Digital Converter (ADC) input interfaces or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA2683. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.

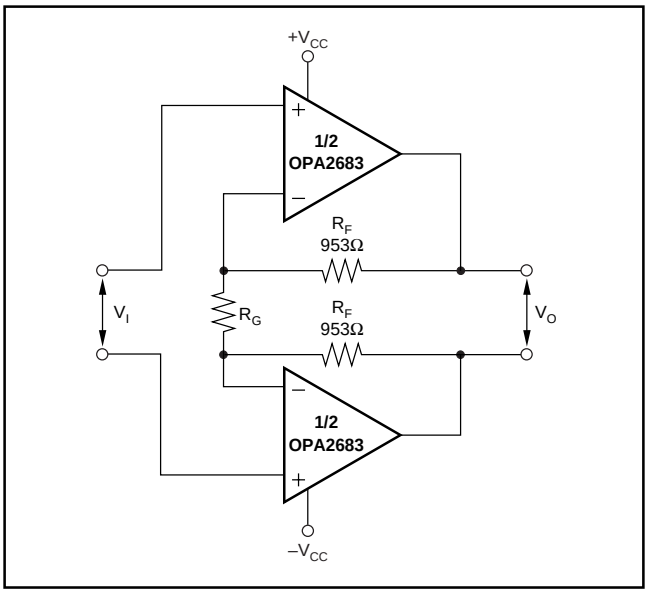


FIGURE 5. Noninverting Differential I/O Amplifier.

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 5 is:

$$A_D = 1 + 2 \bullet R_F / R_G \quad (1)$$

Since the OPA2683 is a CFB_{PLUS} amplifier, its bandwidth is principally controlled with the feedback resistor value; see Figure 5 for the recommended value of 953Ω. The differential gain, however, may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response. Since the inverting inputs of the OPA2683 are very low impedance closed-loop buffer outputs, the R_G element does not interact with the amplifier's bandwidth; wide ranges of resistor values and/or filter elements may be inserted here with minimal amplifier bandwidth interaction.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a concern, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also attenuate the common-mode signal through to the line.

Figure 6 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This provides a better noise performance than the noninverting configuration but does limit the flexibility in setting the input impedance separately from the gain.

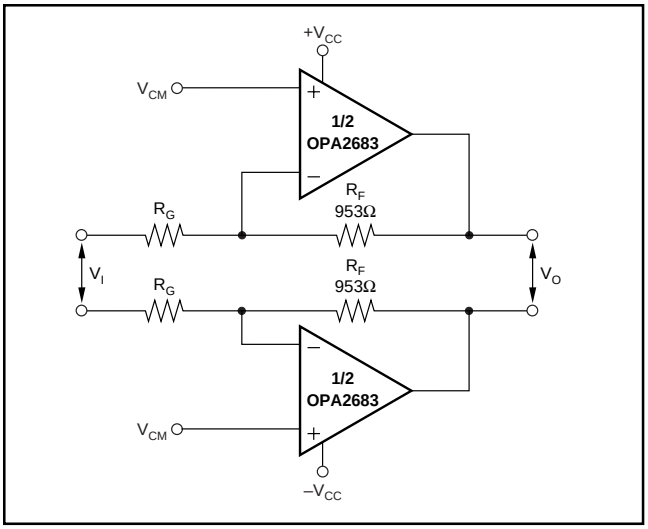


FIGURE 6. Inverting Differential I/O Amplifier.

The two noninverting inputs provide an easy common-mode control input. This is particularly simple if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving particularly easy common-mode control for single-supply operation. The OPA2683 used in this configuration does constrain the feedback to the 953Ω region for best frequency response. With R_F fixed, the input resistors may be adjusted to the desired gain but will also be changing the input impedance as well. The high-frequency common-mode gain for this circuit from input to output will be the same as for the signal gain. Again, if the source might include an undesired common-mode signal, that signal could be rejected at the input using blocking caps (for low frequency and DC common-mode) or a transformer coupling.

DC-COUPLED SINGLE TO DIFFERENTIAL CONVERSION

The previous differential output circuits were also set up to receive a differential input. A simple way to provide a DC-coupled single to differential conversion using a dual op amp is shown in Figure 7. Here, the output of the first stage is simply inverted by the second to provide an inverting version of a single amplifier design. This approach works well for lower frequencies but will start to depart from ideal differential outputs as the propagation delay and distortion of the inverting stage adds significantly to that present at the noninverting output pin.

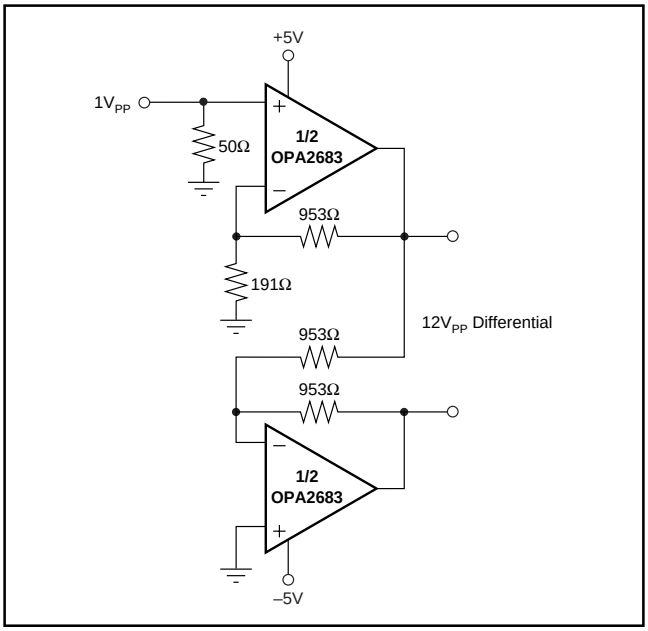


FIGURE 7. Single to Differential Conversion.

The circuit of Figure 7 is set up for a single-ended gain of 6 to the output of the first amplifier, then an inverting gain of –1 through the second stage to provide a total differential gain of 12. See Figure 8 for the 75MHz small-signal bandwidth delivered by the circuit of Figure 7. Large-signal distortion at $12V_{PP}$ output at 1MHz into the 1kΩ differential load is ≤ –76dBc.

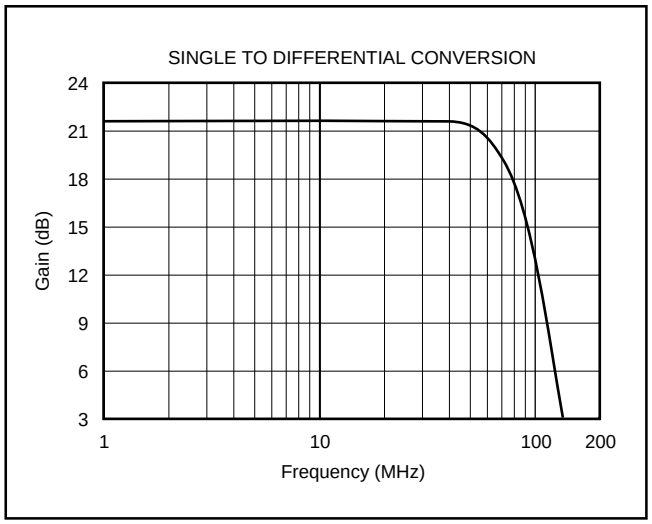


FIGURE 8. Small-Signal Bandwidth for Figure 7.

DIFFERENTIAL ACTIVE FILTER

The OPA2683 can provide a very capable gain block for low-power active filters. The dual design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. Figure 9 shows an example of a very low-power, 10MHz, 3rd-order Butterworth low-pass Sallen-Key filter. Often, these filters are designed at an amplifier gain of 1 to minimize amplifier bandwidth interaction with the desired filter shape. Since the OPA2683 shows minimal bandwidth change with gain, this feature would not be a constraint in this design. The example of Figure 9 designs the filter for a differential gain of 5 using the OPA2683. The resistor values have been adjusted slightly to account for the amplifier bandwidth effects.

While this circuit is bipolar, using ±5V supplies, it can easily be adapted to single-supply operation. This is typically done by providing a supply midpoint reference at the noninverting inputs, then adding DC blocking caps at each input and in series with the amplifier gain resistor, R_G. This will add two real zeroes in the response, transforming the circuit into a bandpass. Figure 10 shows the frequency response for the filter of Figure 9.

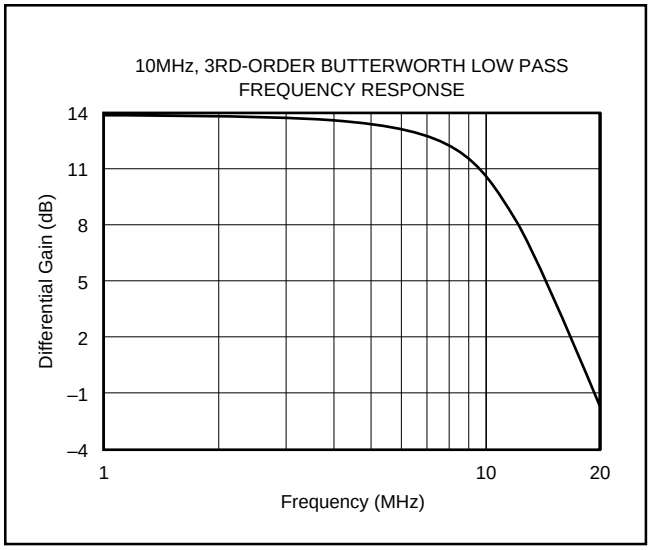


FIGURE 10. Frequency Response for 10MHz, 3rd-Order Butterworth Low-Pass Filter.

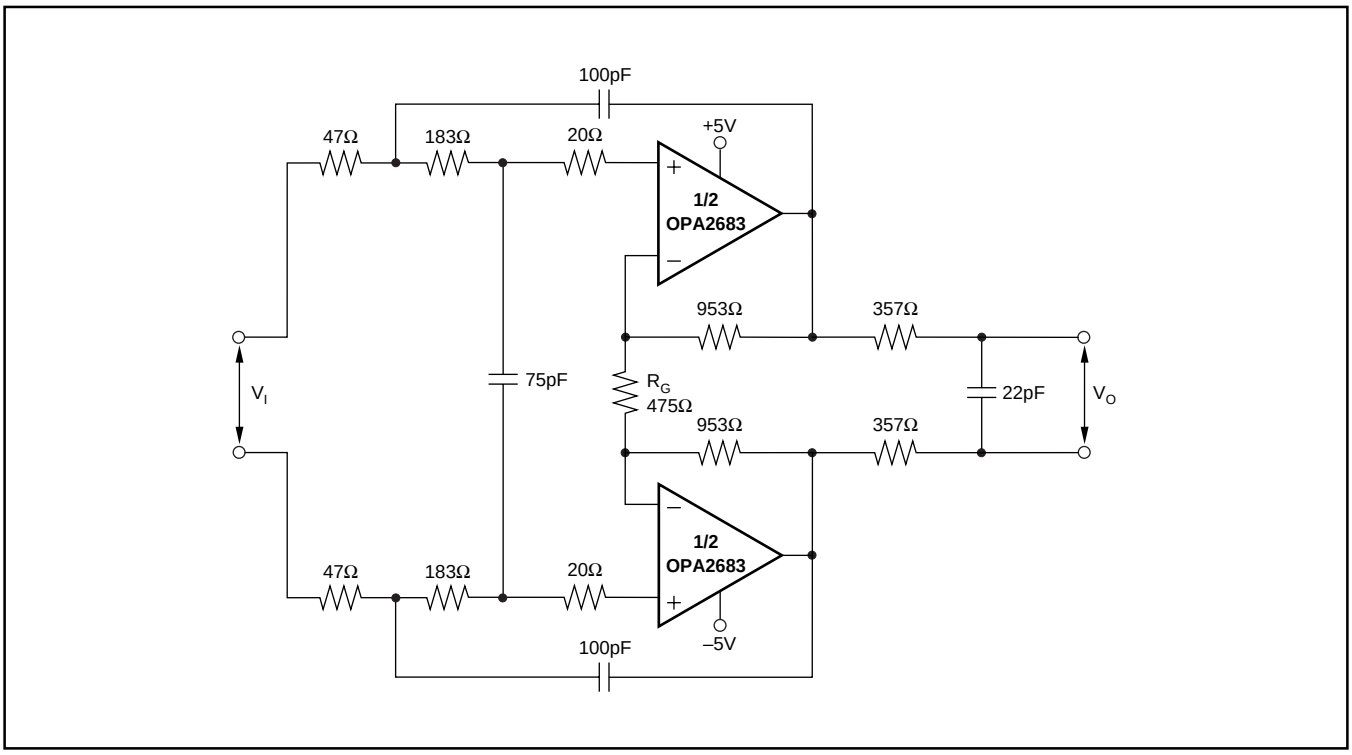


FIGURE 9. Low-Power, Differential I/O, 4th-Order Butterworth Active Filter.

SINGLE-SUPPLY, HIGH GAIN DIFFERENTIAL ADC DRIVER

Where a very low-power differential I/O interface to a moderate performance ADC is required, the circuit of Figure 11 may be considered. The circuit builds on the inverting differential I/O configuration of Figure 6 by adding the input transformer and the output low-pass filter. The input transformer provides a single-to-differential conversion where the input signal is still very low power—it also provides a gain of 2 and removes any common-mode signal from the inputs. This single +5V design sets a midpoint bias from the supply at each of the noninverting inputs.

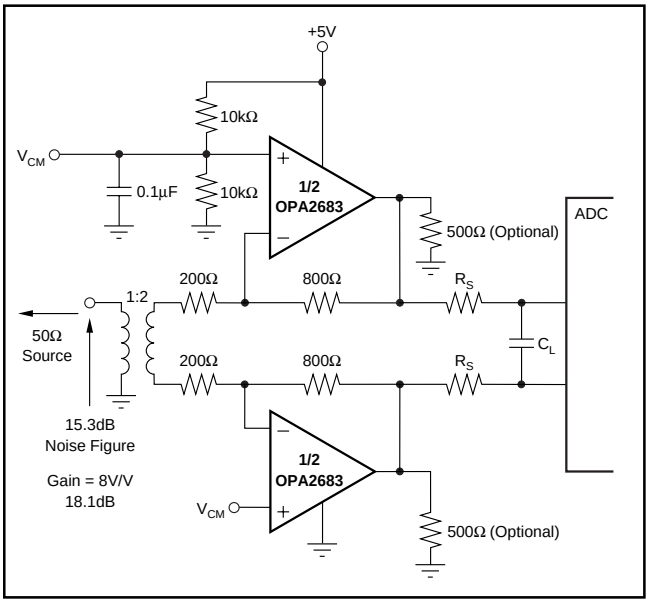


FIGURE 11. Single-Supply Differential ADC Driver.

This circuit also includes optional 500Ω pull-down resistors at the output. With a 2.5V DC common-mode operating point (set by V_{CM}), this will add 5mA to ground in the output stage. This essentially powers up the NPN side of the output stage significantly reducing distortion. It is important for good 2nd-order distortion to connect the grounds of these two resistors at the same point to minimize ground plane current for the differential output signal.

LOW-POWER MUX/LINE DRIVER

Using the shutdown feature, two OPA2683s can provide an easy low-power way to select one of two possible sources for moderate-resolution monitors. Figure 12 shows a recommended circuit where each of the outputs are combined in a way that provides a net gain of 1 to the matched 75Ω load with a 75Ω output impedance. This brings the two outputs for each color together through a 78.7Ω resistor with a slightly > 2 gain provided by the amplifiers. When one channel is shutdown, the feedback network is still present, slightly attenuating the signal and combining in parallel with the 78.7Ω to give a 75Ω source impedance.

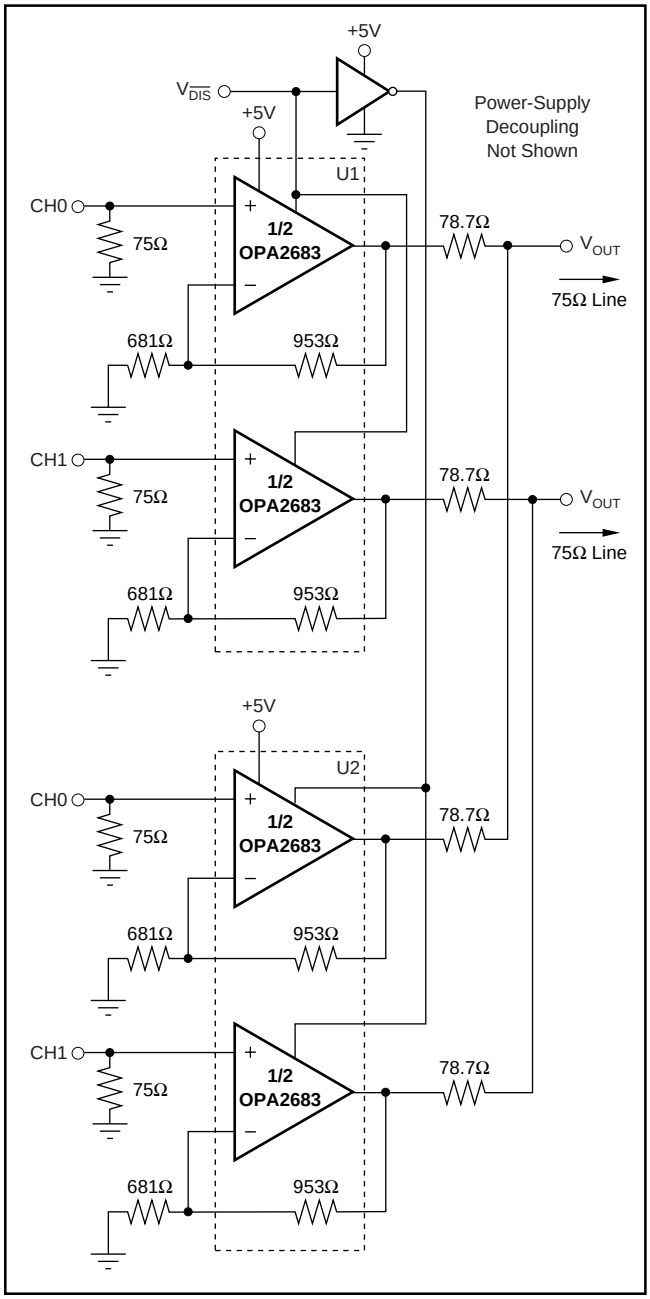


FIGURE 12. Frequency Response for 10MHz, 3rd-Order Butterworth Low-Pass Filter.

Since the OPA2683 does not disable quickly, this approach is not suitable for pixel-by-pixel multiplexing—however, it does provide an easy way to switch between two possible RGB sources. The output swing provided by the active channel will divide back through the inactive channel feedback to appear at the inverting input of the OFF channel. To retain good pulse fidelity, or low distortion, this divided down output signal at the inverting inputs of the OFF channels, plus the OFF channel input signals, should not exceed $0.7V_{PP}$. As the signal across the buffers of the inactive channels exceeds $0.7V_{PP}$, diodes across the inputs may begin to turn on causing a nonlinear load to the active channel. This will degrade signal linearity under those conditions.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2683 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2683ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2683IDCN	SOT23-8	DEM-OPA-SOT-2A	SBOU001
OPA2683IDGS	MSOP-10	DEM-OPA-MSOP-2B	SBOU040

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2683 product folder.

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for higher speed designs where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA683 is available in the product folder on the TI web site (www.ti.com). This is the single channel model for the OPA2683—simply use two of these to implement an OPA2683 simulation. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. However, they are less accurate in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

Any current-feedback op amp like the OPA2683 can hold high bandwidth over signal-gain settings with the proper adjustment of the external resistor values. A low-power part like the OPA2683 typically shows a larger change in bandwidth due to the significant contribution of the inverting input impedance to loop-gain changes as the signal gain is changed. Figure 13 shows a simplified analysis circuit for any current-feedback amplifier.

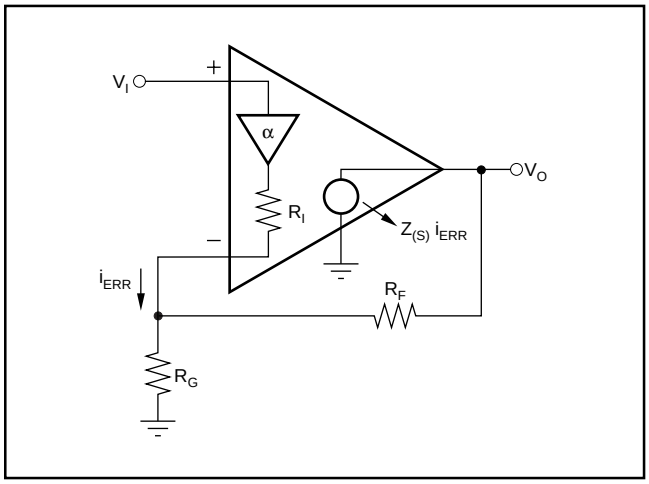


FIGURE 13. Current-Feedback Transfer Function Analysis Circuit.

The key elements of this current-feedback op amp model are:

$\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \Rightarrow$ Buffer output impedance

$i_{ERR} \Rightarrow$ Feedback error current signal

$Z(s) \Rightarrow$ Frequency dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$. The closed-loop input stage buffer used in the OPA2683 gives a buffer gain more closely approaching 1.00 and this shows up in a slightly higher CMRR than previous current-feedback op amps.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2683 reduces this element to approximately 5.0Ω using the loop gain of the closed-loop input buffer stage. This significant reduction in output impedance, on very low power, contributes significantly to extending the bandwidth at higher gains.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 13 gives Equation 2:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F + R_I\,NG}{Z_{(S)}}} \qquad \left[NG = \left(1+\frac{R_F}{R_G}\right)\right] \qquad (2)$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 2 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 2 determines the frequency response. Equation 3 shows this as the loop-gain equation.

$$\frac{Z_{(S)}}{R_F + R_I\,NG} = \text{Loop Gain} \qquad (3)$$

If $20 \cdot \log(R_F + NG \cdot R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 3, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 2 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 3 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA2683 is internally compensated to give a maximally flat frequency response for R_F = 953Ω at NG = 2 on ±5V supplies. That optimum value goes to 1.2kΩ on a single +5V supply. Normally, with a current-feedback amplifier, it is possible to adjust the feedback resistor to hold this bandwidth up as the gain is increased. The CFB_{PLUS} architecture has reduced the contribution of the inverting input impedance to provide exceptional bandwidth to higher gains without adjusting the feedback resistor value. The Typical Characteristics show the small-signal bandwidth over gain with a fixed feedback resistor.

Putting a closed-loop buffer between the noninverting and inverting inputs does bring some added considerations. Since the voltage at the inverting output node is now the output of a locally closed-loop buffer, parasitic external capacitance on this node can cause frequency response peaking for the transfer function from the noninverting input voltage to the inverting node voltage. While it is always important to keep the inverting node capacitance low for any current-feedback op amp, it is critically important for the OPA2683. External layout capacitance in excess of 2pF will start to peak the frequency response. This peaking can be easily reduced by then increasing the feedback resistor value—but it is preferable, from a noise and dynamic range standpoint, to keep that capacitance low, allowing a close to nominal 953Ω feedback resistor for flat frequency response. Very high parasitic capacitance values on the inverting node (> 5pF) can possibly cause input stage oscillation that cannot be filtered by a feedback element adjustment.

An added consideration is that at very high gains, 2nd-order effects in the inverting output impedance cause the overall response to peak up. If desired, it is possible to retain a flat frequency response at higher gains by adjusting the feedback resistor to higher values as the gain is increased. Since the exact value of feedback that will give a flat frequency response at high gains depends strongly in inverting and output node parasitic capacitance values, it is best to experiment in the specific board with increasing values until the desired flatness (or pulse response shape) is obtained. In general, increasing R_F (and then adjusting R_G to the desired gain) will move towards flattening the response, while decreasing it will extend the bandwidth at the cost of some peaking. The OPA683 data sheet gives an example of this optimization of R_F versus gain.

OUTPUT CURRENT AND VOLTAGE

The OPA2683 provides output voltage and current capabilities that can support the needs of driving doubly-terminated 50Ω lines. If the 1kΩ load of Figure 1 is changed to a 100Ω load, the total load is the parallel combination of the 100Ω load, and the 1.9kΩ total feedback network impedance. This 95Ω load will require no more than 42mA output current to support the ±4.0V minimum output voltage swing specified for 1kΩ loads. This is well below the specified minimum +120/–90mA specifications over the full temperature range.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2683's output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the electrical characteristic tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin can destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This resistor will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short-circuit, while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. Always place the 0.1μF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2683 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S vs C_{LOAD} and the resulting frequency response at the load. The 1kΩ resistor shown in parallel with the load capacitor is a measurement path and may be omitted. The required series resistor value may be reduced by increasing the feedback resistor value from its nominal recommended value. This will increase the phase margin for the loop gain, allowing a lower series resistor to be effective in reducing the peaking due to capacitive load. SPICE simulation can be effectively used to optimize this approach. Parasitic capacitive loads greater than 5pF can begin to degrade the performance of the OPA2683. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2683 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA2683 provides very low distortion in a low-power part. The CFB_{PLUS} architecture also gives two significant areas of distortion improvement. First, in operating regions where the 2nd-harmonic distortion due to output stage nonlinearities is very low (frequencies < 1MHz, low output swings into light loads) the linearization at the inverting node provided by the CFB_{PLUS} design gives 2nd-harmonic distortions that extend into the –90dBc region. Previous current-feedback amplifiers have been limited to approximately –85dBc due to the nonlinearities at the inverting input. The second area of distortion improvement comes in a distortion performance that is largely gain independent. To the extent that the distortion at a specific output power is output stage dependent, 3rd-harmonics particularly, and to a lesser extend 2nd-harmonic distortion, remains constant as the gain increases. This is due to the constant loop gain versus signal gain provided by the CFB_{PLUS} design. As shown in the Typical Characteristics, while the 3rd-harmonic is constant with gain, the 2nd-harmonic degrades at higher gains. This is largely due to board parasitic issues. Slightly imbalanced load return currents will couple into the gain resistor to cause a portion of the 2nd-harmonic distortion. At high gains, this imbalance has more gain to the output giving increased 2nd-harmonic distortion.

Relative to alternative amplifiers with < 2mA supply current, the OPA2683 holds much lower distortion at higher frequencies (> 5MHz) and to higher gains. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a lower 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. A low-power part like the OPA2683 includes quiescent boost circuits to provide the full-power bandwidth shown in the Typical Characteristics. These act to increase the bias in a very linear fashion only when high slew rate or output power are required. This also acts to actually reduce the distortion slightly at higher output power levels. The Typical Characteristics show the 2nd-harmonic holding constant from $500mV_{PP}$ to $5V_{PP}$ outputs while the 3rd-harmonics actually decrease with increasing output power.

The OPA2683 has an extremely low 3rd-order harmonic distortion, particularly for light loads and at lower frequencies. This also gives low 2-tone, 3rd-order intermodulation distortion as shown in the Typical Characteristics. Since the OPA2683 includes internal power boost circuits to retain good full-power performance at high frequencies and outputs, it does not show a classical 2-tone, 3rd-order intermodulation intercept characteristic. Instead, it holds relatively low and constant 3rd-order intermodulation spurious levels over power. The Typical Characteristics show this spurious level as a dBc below the carrier at fixed center frequencies swept over single-tone power at a matched 50Ω load. These spurious levels drop significantly (> 12dB) for lighter loads than the 100Ω used in that plot. Converter inputs, for instance, will see ≤ 82dBc 3rd-order spurious to 10MHz for full-scale inputs. For even lower 3rd-order intermodulation distortion to much higher frequencies, consider the OPA2691.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2683 offers an excellent balance between voltage and current noise terms to achieve low output noise in a low-power amplifier. The inverting current noise (11.6pA/$\sqrt{Hz}$) is lower than most other current-feedback op amps while the input voltage noise (4.4nV/$\sqrt{Hz}$) is lower than any unity-gain stable, comparable slew rate, < 5mA/ch voltage-feedback op amp. This low input voltage noise was achieved at the price of higher noninverting input current noise (5.1pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 200Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 14 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

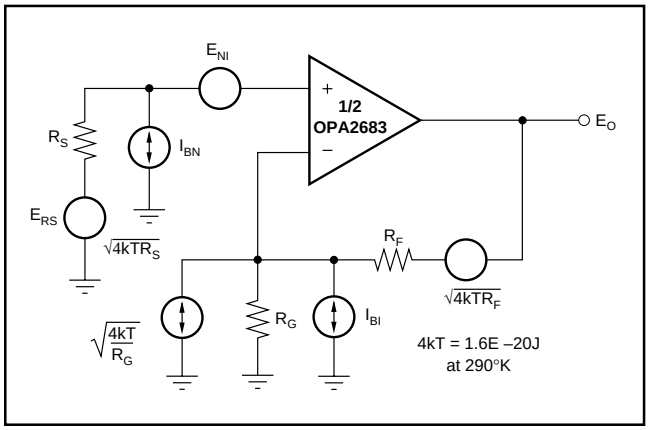


FIGURE 14. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms presented in Figure 14.

(4)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 5.

(5)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA2683 circuit and component values (see Figure 1) will give a total output spot noise voltage of 15.2nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 7.6nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 4.4nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. As the gain is increased, this fixed output noise power term contributes less to the total output noise and the total input referred voltage noise given by Equation 5 will approach just the 4.4nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 in the circuit of Figure 1, adjusting only the gain resistor to 50Ω, will give a total input referred noise of 4.6nV/$\sqrt{Hz}$. A more complete description of op amp noise analysis can be found in TI application note AB-103, *Noise Analysis for High-Speed Op Amps* (SBOA066), located at www.ti.com.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA2683 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high slew rate voltage-feedback amplifiers. The two input bias currents, however, are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \bullet V_{OS}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$

where NG = noninverting signal gain

$= \pm(2 \bullet 3.5mV) \pm (4.5\mu A \bullet 25\Omega \bullet 2) \pm (953\Omega \bullet 10mA)$

$= \pm 7.0mV + 0.23mV \pm 9.5mV$

$= \pm 16.73mV$

While the last term, the inverting bias current error, is dominant in this low-gain circuit, the input offset voltage will become the dominant DC error term as the gain exceeds 5V/V. Where improved DC precision is required in a high-speed amplifier, consider the OPA656 single and OPA2822 dual voltage-feedback amplifiers.

DISABLE OPERATION

The OPA2683 provides an optional disable feature that may be used to reduce system power when channel operation is not required. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA2683 will operate normally. To disable, the control pin must be asserted LOW. Figure 14 shows a simplified internal circuit for the disable control feature.

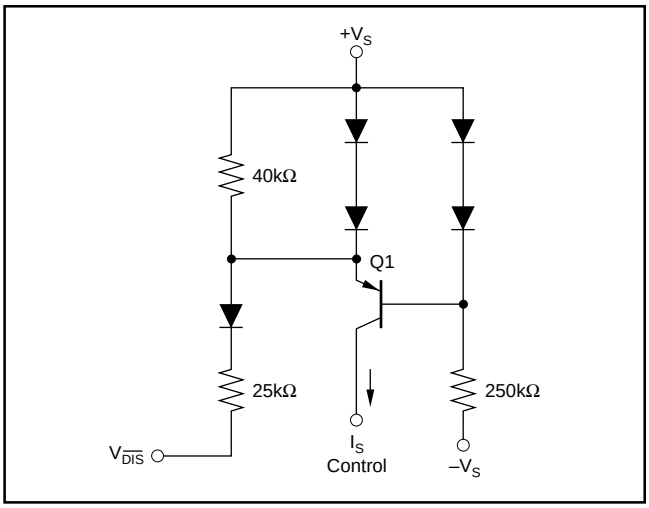


FIGURE 14. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 250kΩ resistor while the emitter current through the 40kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 40kΩ resistor eventually turning on these two diodes (≈ 33μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 14.

When disabled, the output and input nodes go to a high impedance state. If the OPA2683 is operating in a gain of +1 (with a 1.2kΩ feedback resistor still required for stability), this will show a very high impedance (1.7pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

The OPA2683 provides very high power gain on low quiescent current levels. When disabled, internal high impedance nodes discharge slowly which, with the exceptional power gain provided, give a self powering characteristic that leads to a slow turn off characteristic. Typical full turn off times to rated 100µA disabled supply current are 60ms. Turn on times are very fast—less than 40ns.

THERMAL ANALYSIS

The OPA2683 will not require external heatsinking for most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA2683IDCN (SOT23-8 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 100Ω load to $2.5V_{DC}$.

$P_D = 10V \bullet 2.1mA + 2 \bullet (5^2 /(4 \bullet (100\Omega \parallel 1.9k\Omega))) = 153mW$

Maximum $T_J = +85°C + (0.153W \bullet 150°C/W) = 108°C$

This maximum operating junction temperature is well below most system level targets. Most applications will be lower than this since an absolute worst-case output stage power in both channels simultaneously was assumed in this calculation.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2683 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.01µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2683. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the peaking at higher gains, while decreasing it will give a more peaked frequency response at lower gains. The 800Ω feedback resistor used in the Electrical Characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 953Ω feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines**. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended Rs vs C_{LOAD}. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2683 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact a higher impedance environment will improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2683 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2683 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Rs vs C_{LOAD}. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high-speed part like the OPA2683 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2683 onto the board.

INPUT AND ESD PROTECTION

The OPA2683 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum 13V across the supply pins is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 15.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2683), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

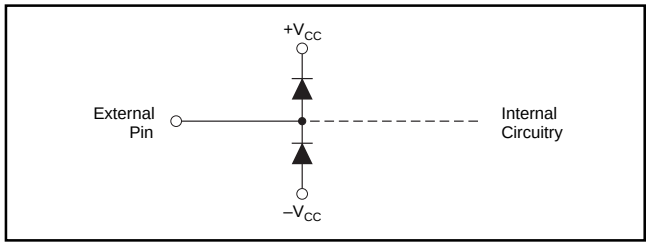


FIGURE 15. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/09	H	2	Package/Ordering Information	Changed package markings for D (SO-8) and DGS (MSOP-10) packages.
7/08	G	2	Absolute Maximum Ratings	Changed minimum storage temperature from –40°C to –65°C.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2683ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2683
OPA2683ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2683
OPA2683IDCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B83
OPA2683IDCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B83
OPA2683IDCNRG4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
OPA2683IDCNT	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B83
OPA2683IDCNT.A	Active	Production	SOT-23 (DCN) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B83
OPA2683IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BUI
OPA2683IDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BUI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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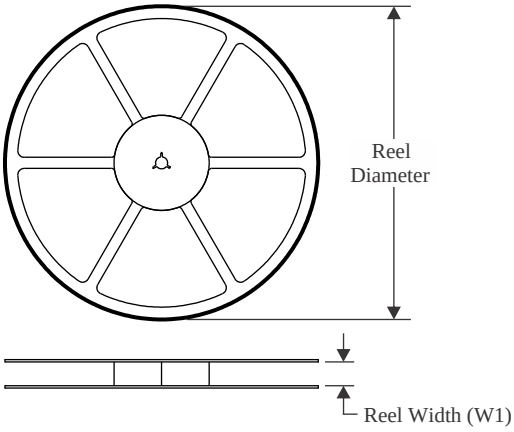
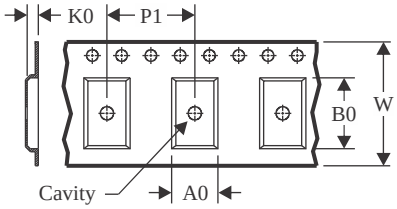
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

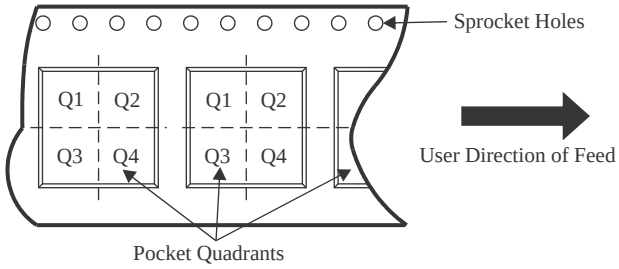


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

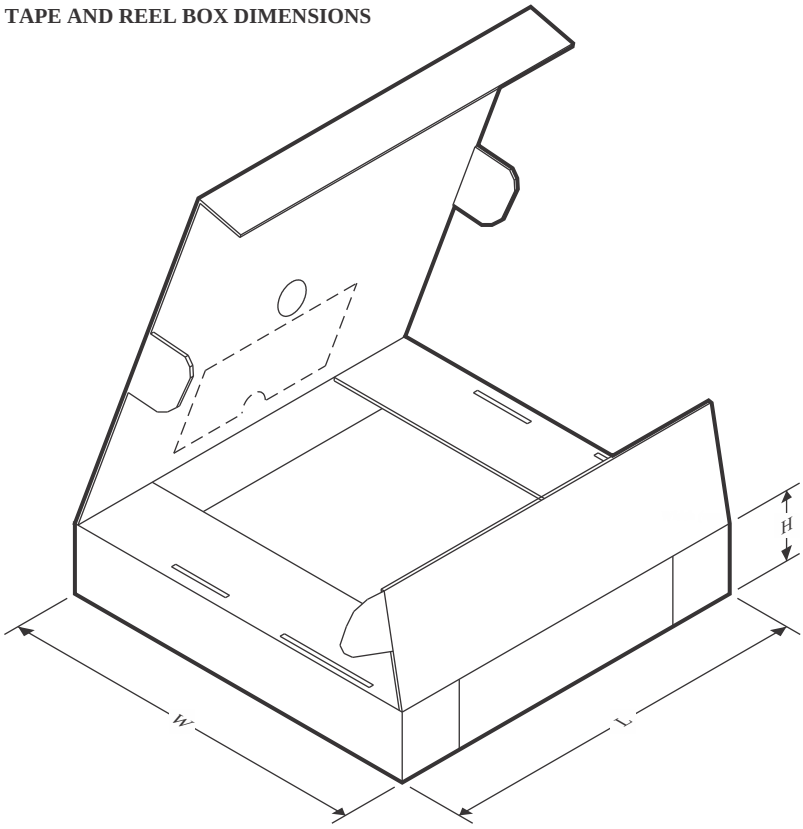
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2683IDCNR	SOT-23	DCN	8	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2683IDCNT	SOT-23	DCN	8	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2683IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

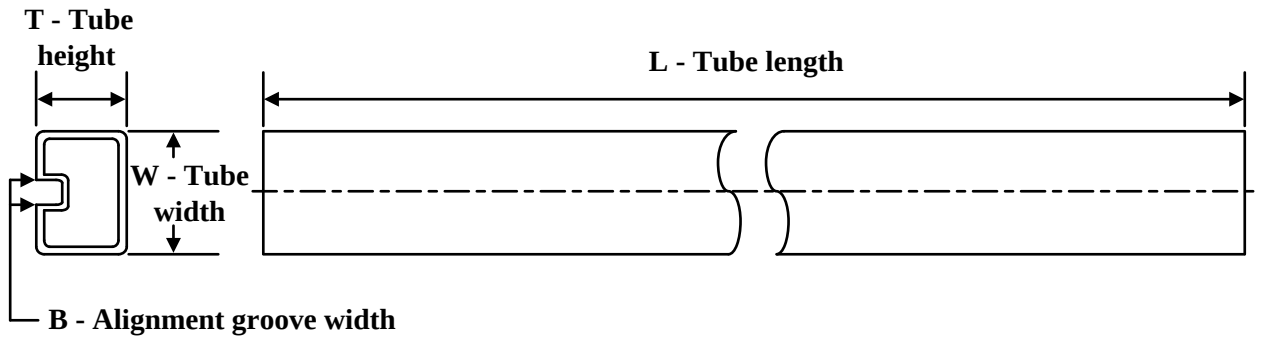
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2683IDCNR	SOT-23	DCN	8	3000	213.0	191.0	35.0
OPA2683IDCNT	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2683IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0

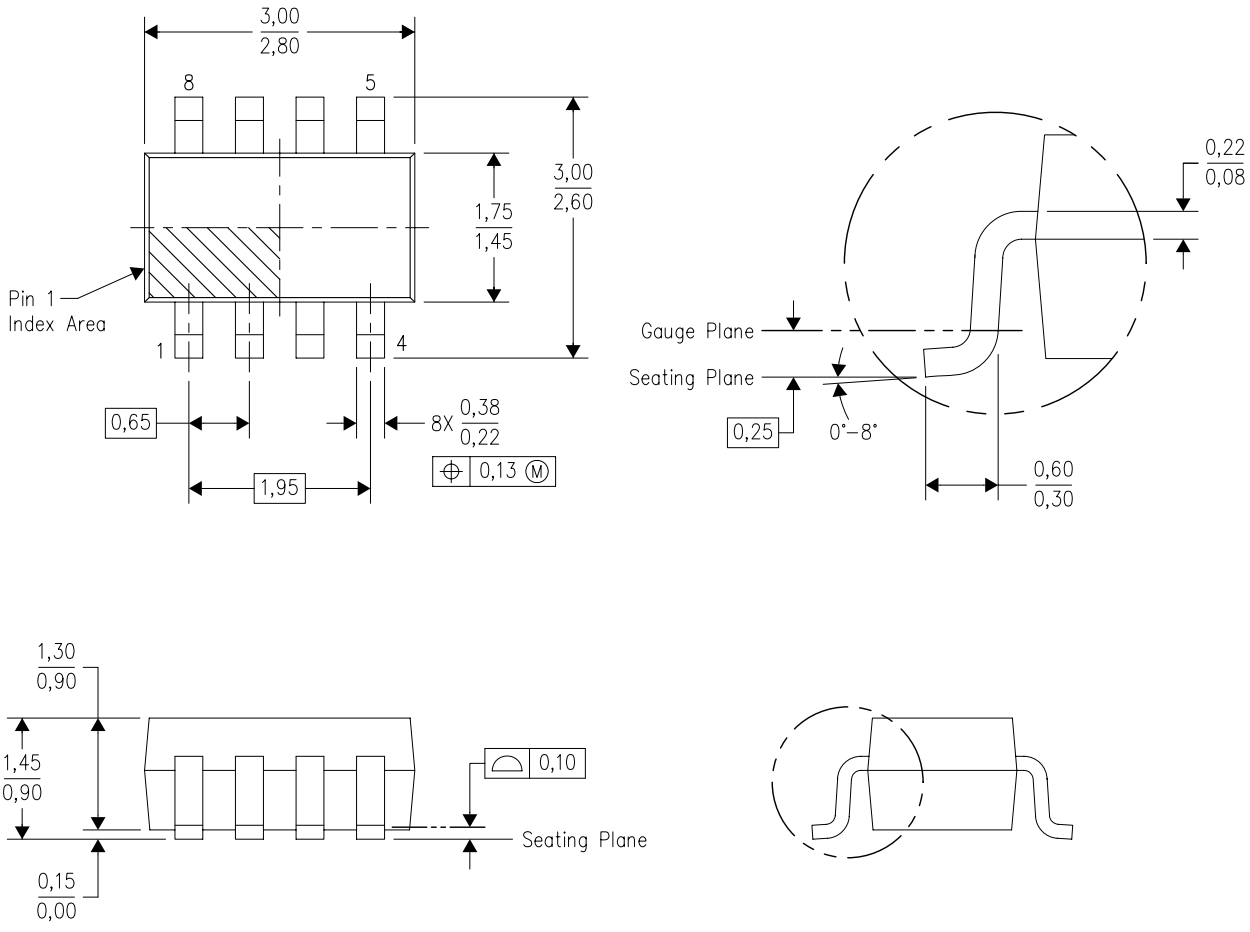
TUBE



*All dimensions are nominal

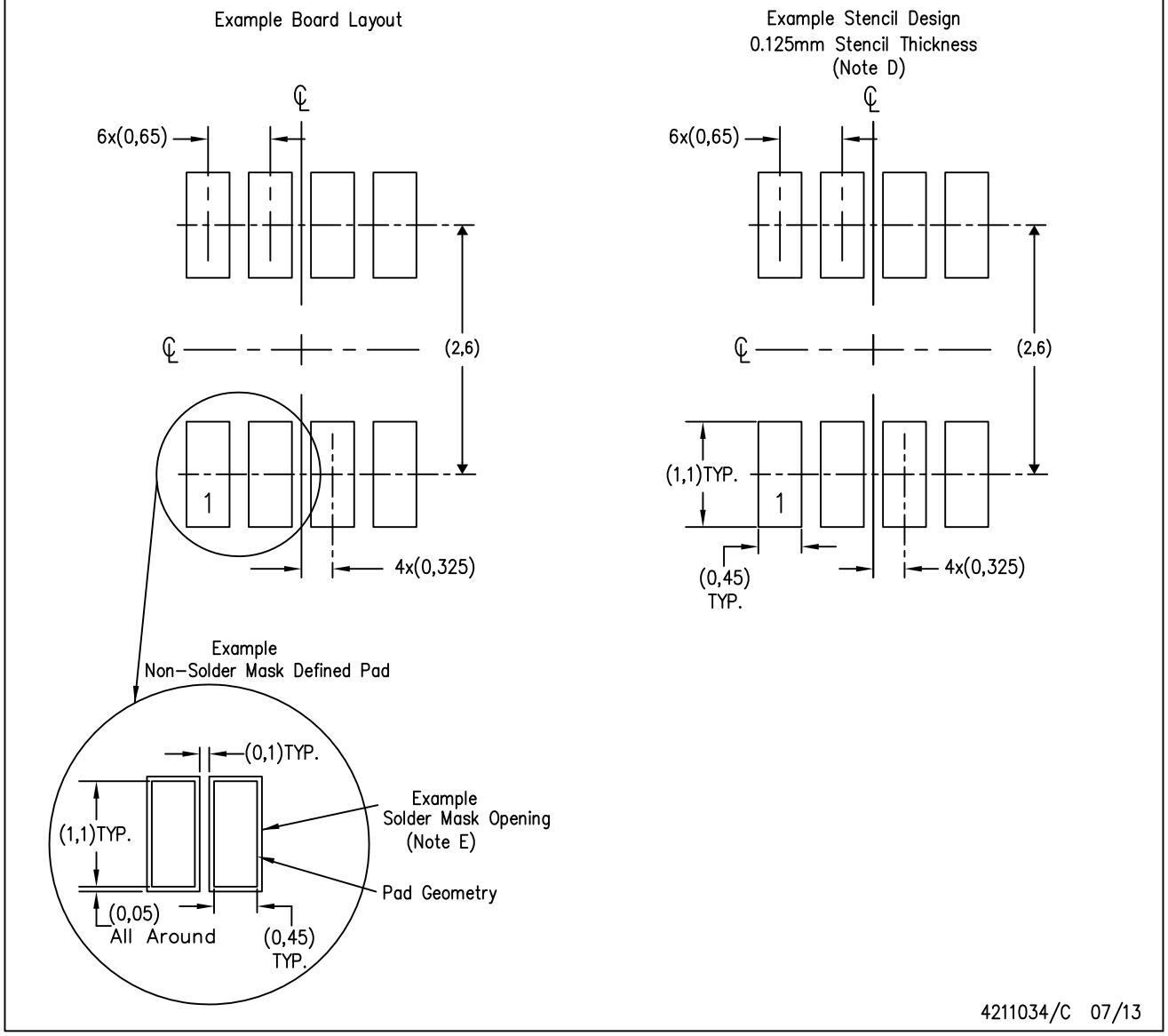
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2683ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2683ID.A	D	SOIC	8	75	506.6	8	3940	4.32

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



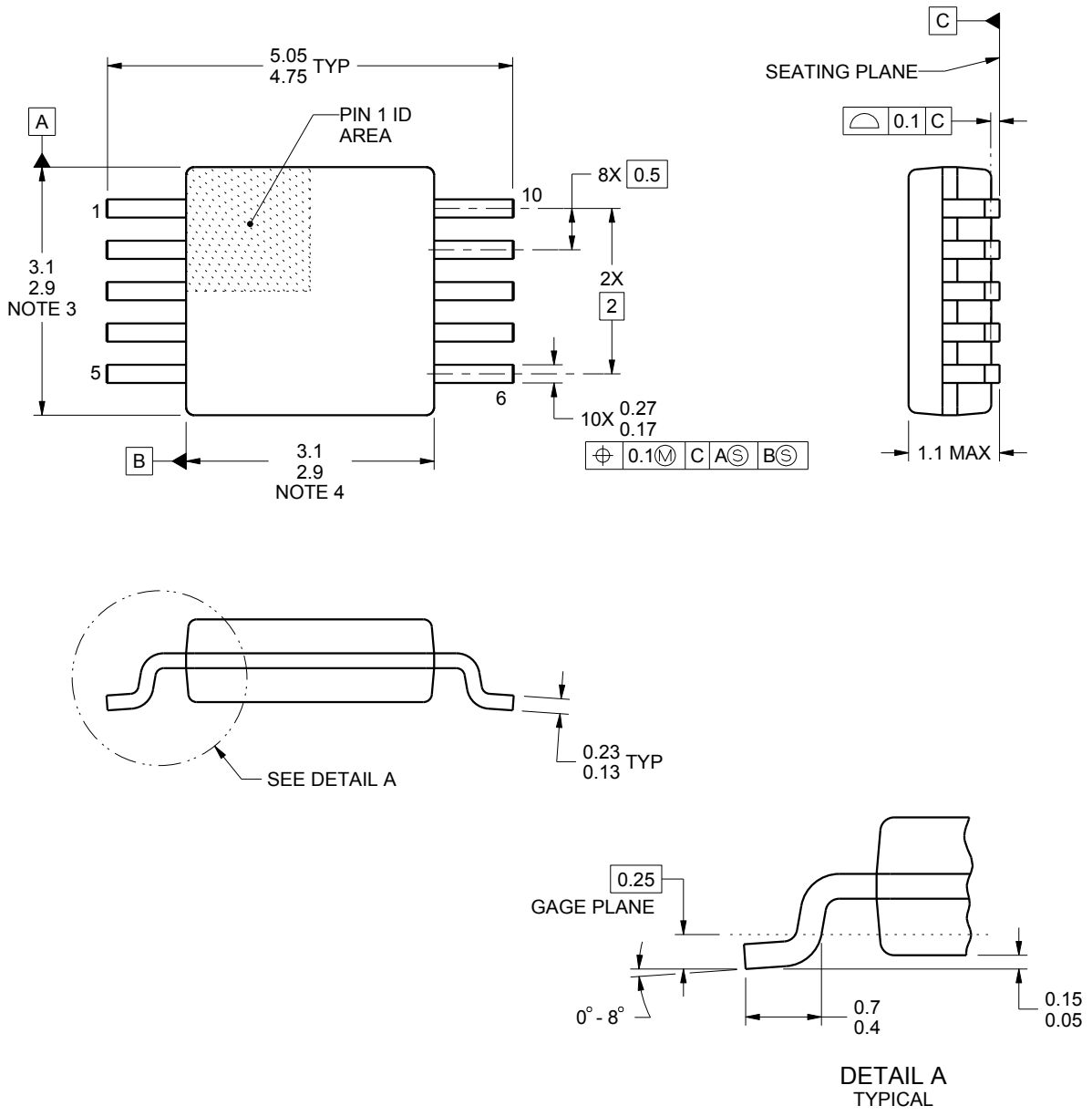
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DGS0010A

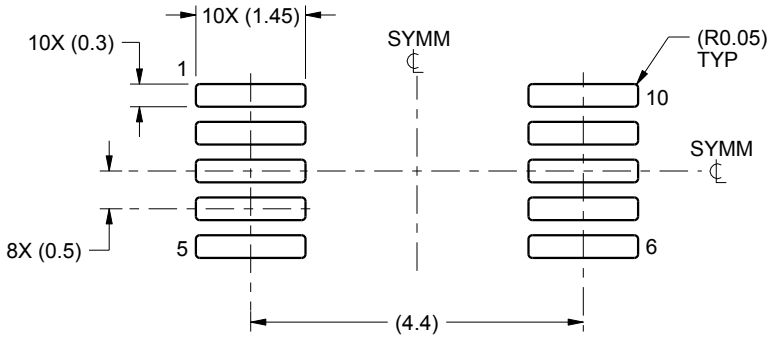
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

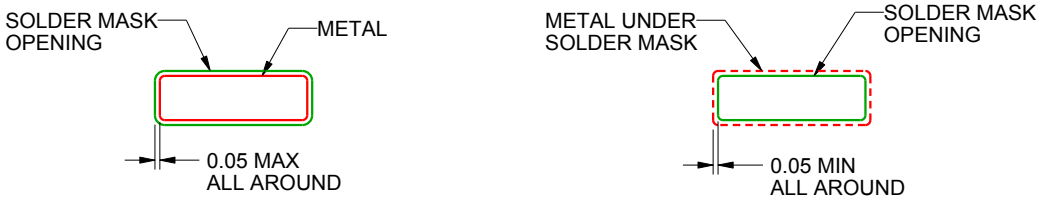


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

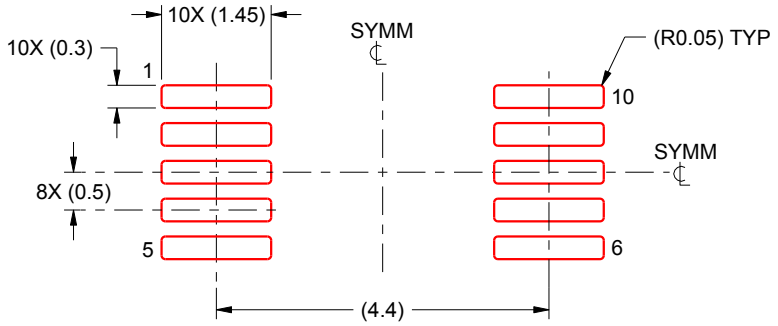


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

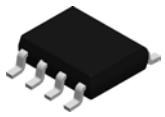


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

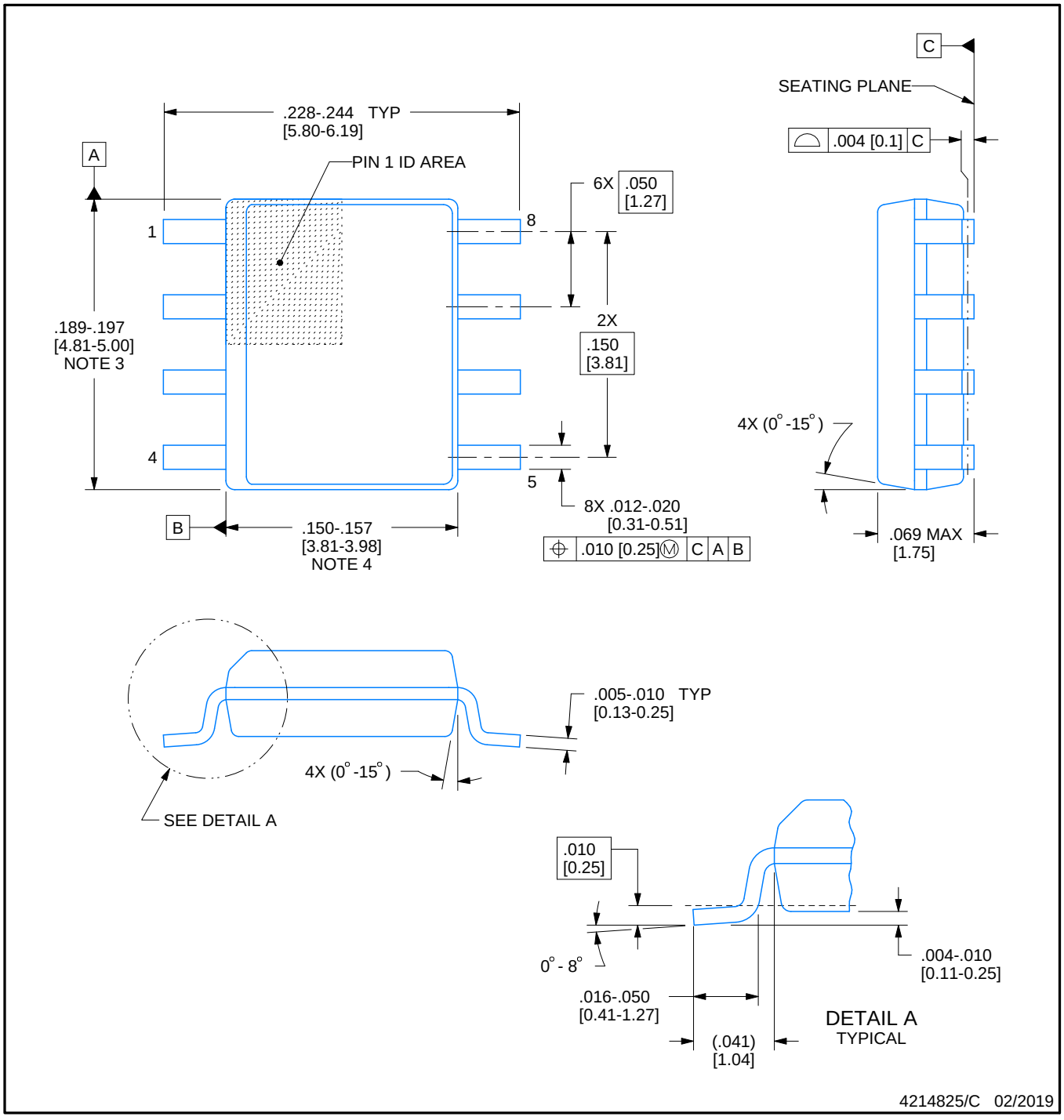


PACKAGE OUTLINE

D0008A

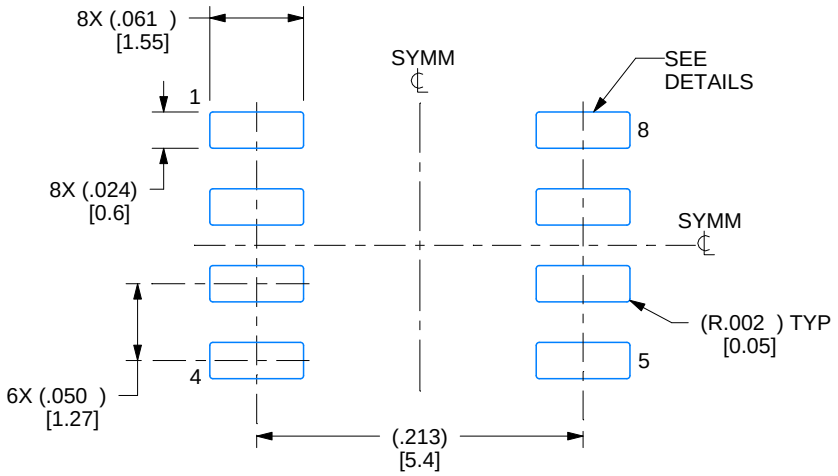
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

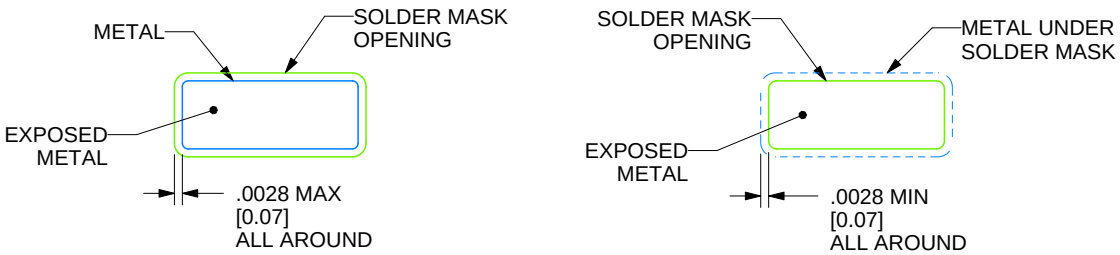


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

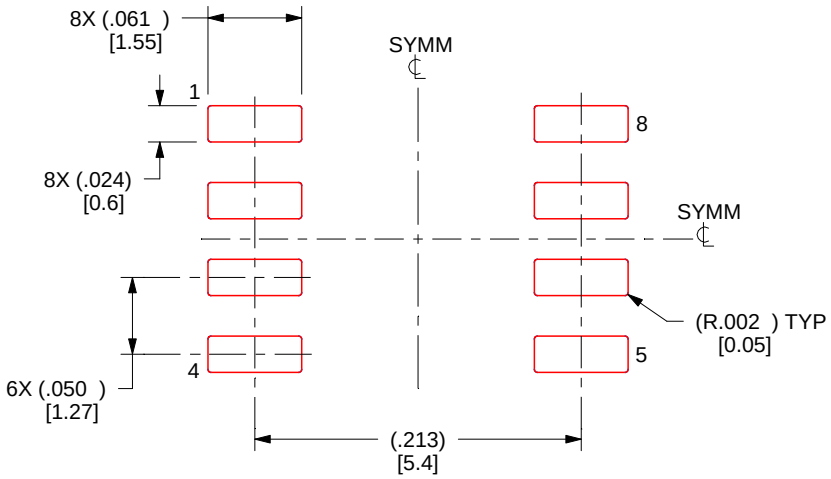
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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