OPA1688 36V、单电源、10MHz、轨到轨输出 SoundPlus™ 音频运算放大器

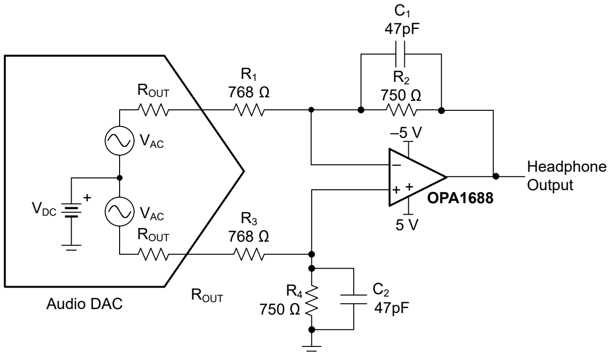
Texas Instruments
Burr-Brown Audio

1 特性

- THD+N，50mW，32 Ω，1kHz，－109dB
- 宽电源电压范围：
  - 4.5V 至 36V，±2.25V 至 ±18V
- 低失调电压：±0.25 mV
- 低温漂：±0.5μV/°C
- 增益带宽：10MHz
- 低输入偏置电流：±10pA
- 低静态电流：每个放大器 1.6 mA
- 低噪声：$8\text{nV}/\sqrt{\text{Hz}}$
- 已过滤 EMI 和 RFI 的输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨到轨输出
- 高共模抑制：120dB
- 封装：
  - 业界通用 SOIC-8
  - *微型* WSON-8

2 应用

- 专业麦克风和无线系统
- 专业音频混合器和控制平面
- 吉他放大器和其他乐器放大器
- A/V 接收器
- 书架立体声音响系统
- 专业音频放大器（机架式）
- DJ 设备
- 转盘
- 特殊功能模块



耳机放大器电路配置

3 说明

OPA1688 36V、单电源、低噪声 SoundPlus™ 音频运算放大器能够在 4.5V (±2.25V) 至 36V (±18V) 的电源电压范围内运行。这些最新补充的高压音频运算放大器与 OPA16xx 器件搭配，为用户提供了广泛的带宽、噪声和功率选择，可以满足各种应用的需要。OPA1688 采用 WSON 微型封装，并且失调电压、漂移和静态电流均较低。该器件还具有高带宽、快速转换率和高输出电流驱动能力。

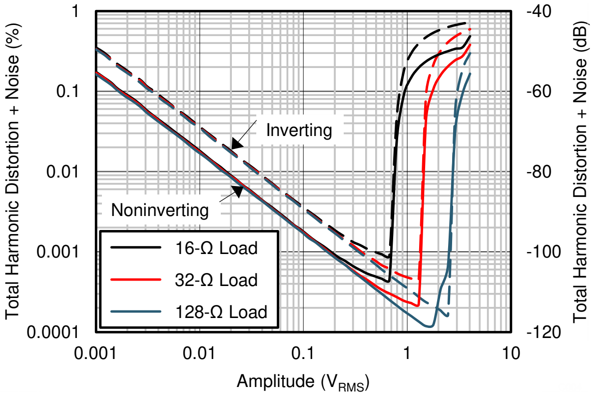
大多数运算放大器仅有一个指定的电源电压，OPA1688 系列则有所不同，可在 4.5V 至 36V 的额定电压范围内运行。超过电源轨的输入信号不会导致反相。输入可在负电源轨以下 100mV 到顶轨以上 2V 范围内正常运行。请注意，该器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 之内运行时，性能会受到影响。

OPA1688 额定运行温度为 -40°C 至 +85°C。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
OPA1688	SOIC (8)	4.90mm × 3.91mm
	WSON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



出色的 THD 性能
（f = 1kHz，BW = 80kHz，V_S = ±5V）

English Data Sheet: SBOS724

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2015) to Revision A (June 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Added operating temperature to *Recommended Operating Conditions* table; moved from *Electrical Characteristics* table	4
• Deleted redundant power supply row from *Electrical Characteristics* table; content already listed in *Recommended Operating Conditions* table	5
• Deleted redundant specified temperature row from *Electrical Characteristics* table; content already listed in *Recommended Operating Conditions* table	5
• Deleted operating temperature row from *Electrical Characteristics* table; moved content to *Recommended Operating Conditions* table	5

5 Device Comparison Table

DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPA1688	1650 µA	10 MHz	8 nV/$\sqrt{\text{Hz}}$
OPA165x	2000 µA	18 MHz	4.5 nV/$\sqrt{\text{Hz}}$
OPA166x	1500 µA	22 MHz	3.3 nV/$\sqrt{\text{Hz}}$

6 Pin Configuration and Functions

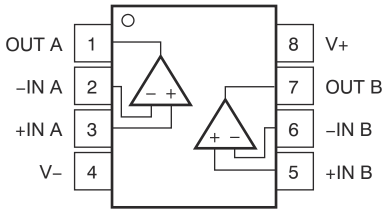

图 6-1. D (SOIC-8) Package, Top View

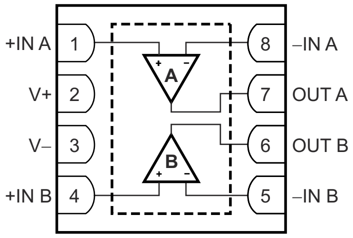

图 6-2. DRG (WSON-8) Package, Top View

表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
	NO.			
NAME	D (SOIC)	DRG (WSON)		
– IN A	2	8	Input	Inverting input, channel A
– IN B	6	5	Input	Inverting input, channel B
+IN A	3	1	Input	Noninverting input, channel A
+IN B	5	4	Input	Noninverting input, channel B
OUT A	1	7	Output	Output, channel A
OUT B	7	6	Output	Output, channel B
V –	4	3	Power	Negative (lowest) power supply
V+	8	2	Power	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage, V_S				±20 (40, single supply)	V
Signal input pins	Voltage[2]	Common-mode	$(V-) - 0.5$	$(V+) + 0.5$	V
		Differential[4]		±0.5	V
	Current			±10	mA
Output short circuit[3]			Continuous		
Temperature	Temperature range		–55	150	°C
	Junction temperature			150	°C
	Storage, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) See *节 8.4.2* section for more information.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S $(V+ - V-)$	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		85	°C
Operating temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA1688		UNIT
		D (SOIC)	DRG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	36.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}, R_L = 2 kΩ		0.00005%		
				–126		dB
		G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}, R_L = 600 Ω		0.000051%		
				–126		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 128 Ω		0.000153%		
				–116		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 32 Ω		0.000357%		
				–109		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 16 Ω		0.000616%		
				–104		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	G = 1		10		MHz
SR	Slew rate	G = 1		8		V/µs
	Full-power bandwidth(1)	V_O = 1 V_{PP}		1.3		MHz
	Overload recovery time	V_{IN} × gain > V_S		200		ns
	Channel separation (dual)	f = 1 kHz		–120		dB
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1, 10-V step		3		µs
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		2.5		μV_{PP}
e_n	Input voltage noise density(2)	f = 100 Hz		14		nV/√Hz
		f = 1 kHz		8		
i_n	Input current noise density	f = 1 kHz		1.8		fA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		±0.25	±1.5	mV
		T_A = –40°C to +85°C			±1.6	
dV_{OS}/dT	V_{OS} over temperature(2)	T_A = –40°C to +85°C		±0.5	±2	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +85°C		±1	±2.5	µV/V
	Channel separation, dc	At dc		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		±10	±20	pA
		T_A = –40°C to +85°C			±1.5	nA
I_{OS}	Input offset current	T_A = 25°C		±3	±7	pA
		T_A = –40°C to +85°C			±250	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range(3)		(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +85°C	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +85°C	104	120		
INPUT IMPEDANCE						
	Differential			100 || 7		MΩ || pF
	Common-mode			6 || 1.5		10^{12}Ω || pF

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±2.25 V to ±18 V, $V_{CM} = V_{OUT} = V_S / 2$, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to +85°C	108	130		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +85°C		118		
OUTPUT						
V_O	Voltage output swing from rail	I_L = ±1 mA	(V–) + 0.1 V		(V+) – 0.1 V	mV
		V_S = 36 V, R_L = 10 kΩ		70	90	
		V_S = 36 V, R_L = 2 kΩ		330	400	
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A		60		Ω
I_{SC}	Short-circuit current			±75		mA
C_{LOAD}	Capacitive load drive			See 节 7.6		pF
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		1.6	1.8	mA
		I_O = 0 A, T_A = –40°C to +85°C			2	

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) Common-mode range can extend to the top rail with reduced performance.

7.6 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

表 7-1. List of Typical Characteristics

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THD+N vs Frequency	图 7-17
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7.6 Typical Characteristics

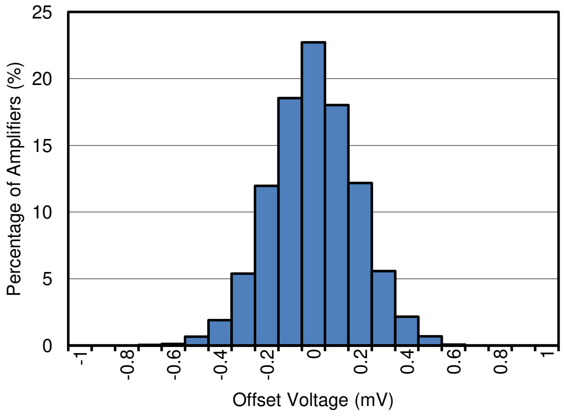
at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

表 7-1. List of Typical Characteristics (continued)

DESCRIPTION	FIGURE
Channel Separation vs Frequency	图 7-43

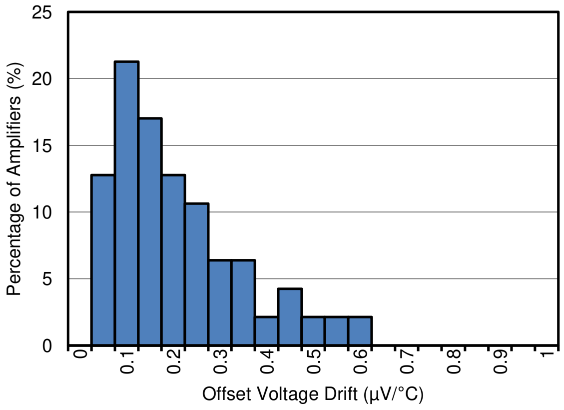
7.6 Typical Characteristics

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



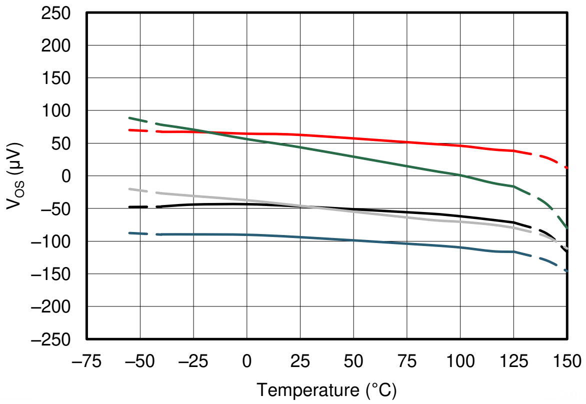
Distribution taken from 5185 amplifiers

图 7-1. Offset Voltage Production Distribution



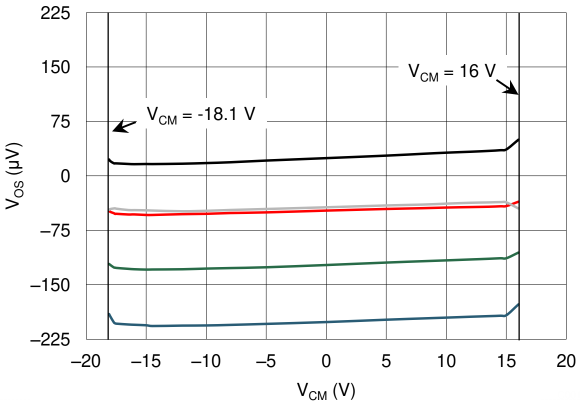
Distribution taken from 47 amplifiers, T_A = –40°C to +125°C

图 7-2. Offset Voltage Drift Production Distribution



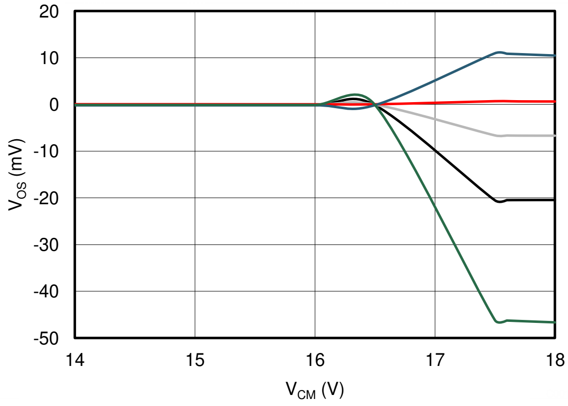
5 typical units shown, V_S = ±18 V

图 7-3. Offset Voltage vs Temperature



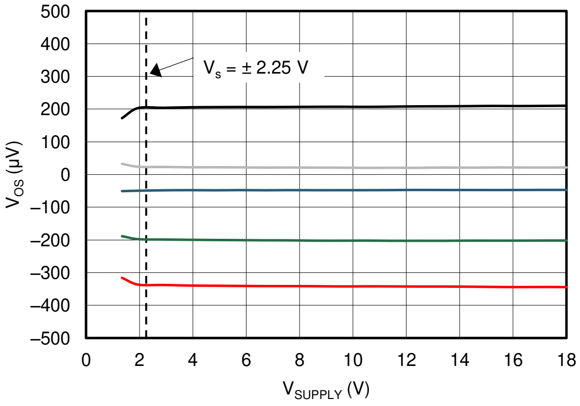
5 typical units shown, V_S = ±18 V

图 7-4. Offset Voltage vs Common-Mode Voltage



5 typical units shown, V_S = ±18 V

图 7-5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

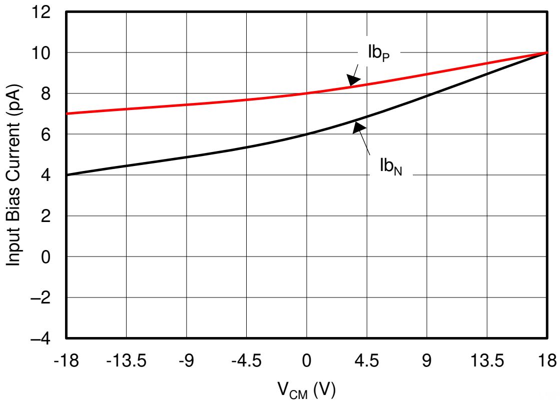


5 typical units shown, V_S = ±2.25 V to ±18 V

图 7-6. Offset Voltage vs Power Supply

7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



T_A = 25°C

图 7-7. Input Bias Current vs Common-Mode Voltage

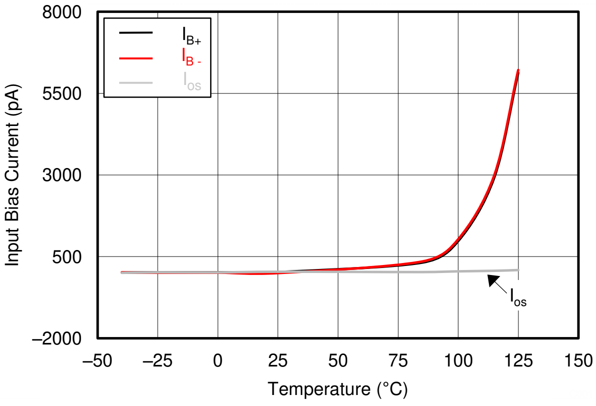


图 7-8. Input Bias Current vs Temperature

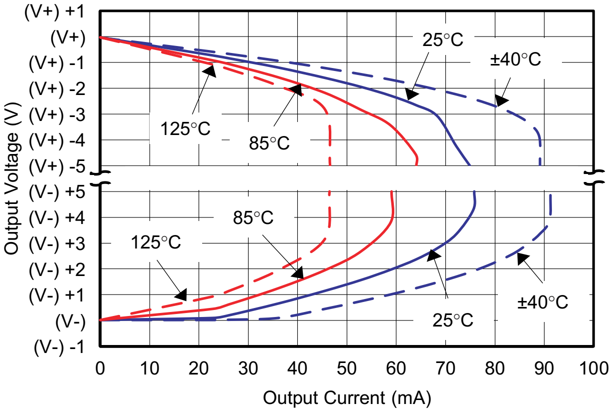


图 7-9. Output Voltage Swing vs Output Current (Maximum Supply)

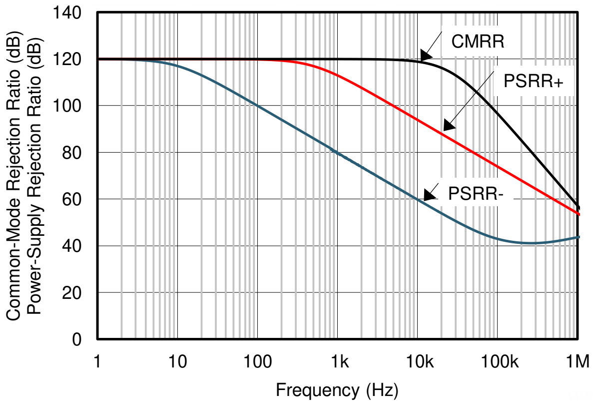


图 7-10. CMRR and PSRR vs Frequency (Referred-to-Input)

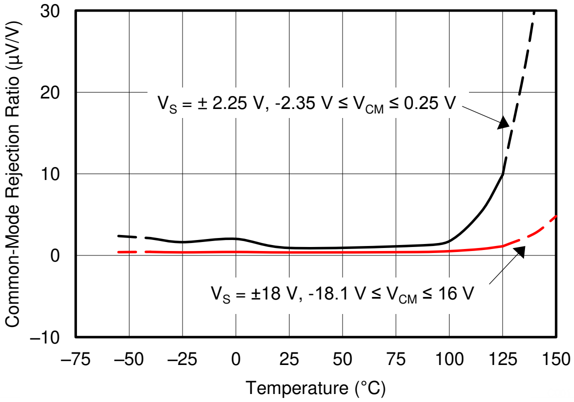


图 7-11. CMRR vs Temperature

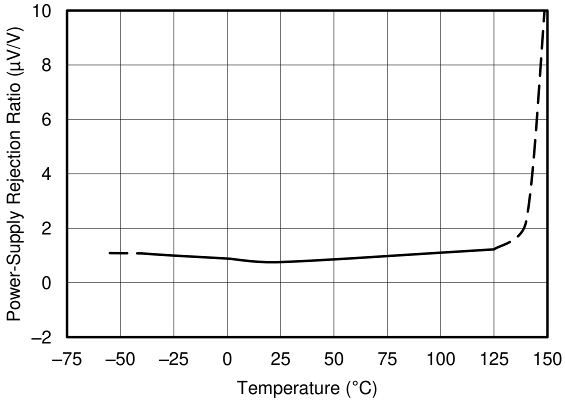
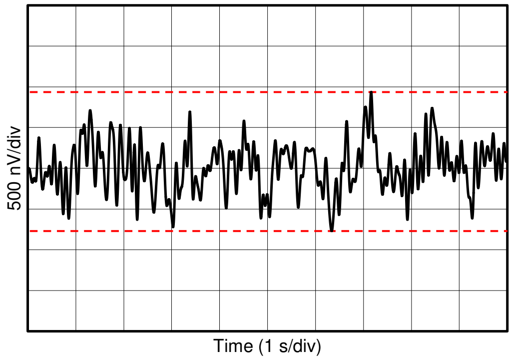


图 7-12. PSRR vs Temperature

7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



Peak-to-peak noise = 1.70 µV_{PP}

图 7-13. 0.1-Hz to 10-Hz Noise

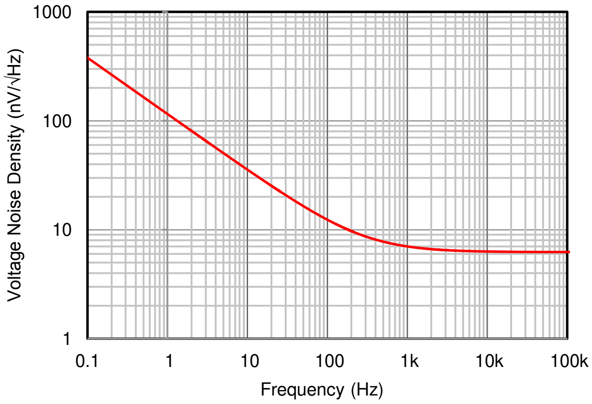
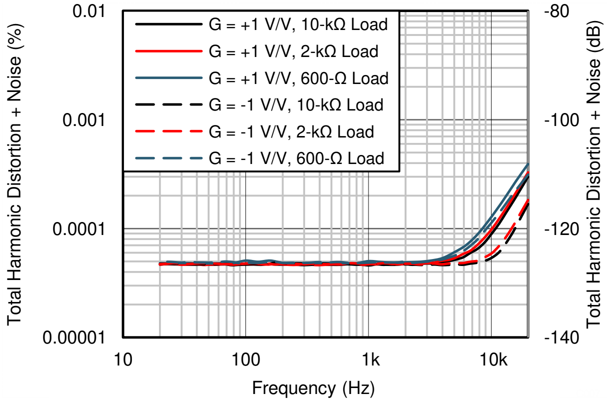
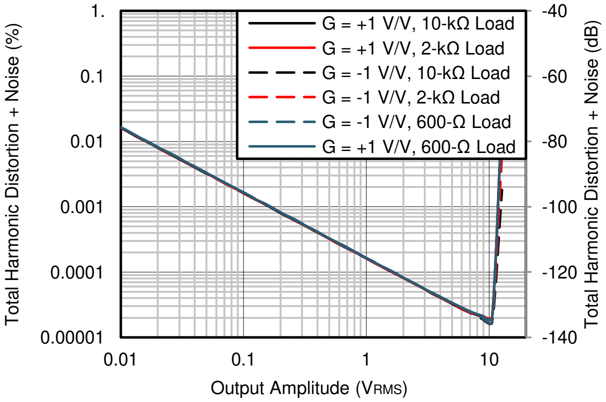


图 7-14. Input Voltage Noise Spectral Density vs Frequency



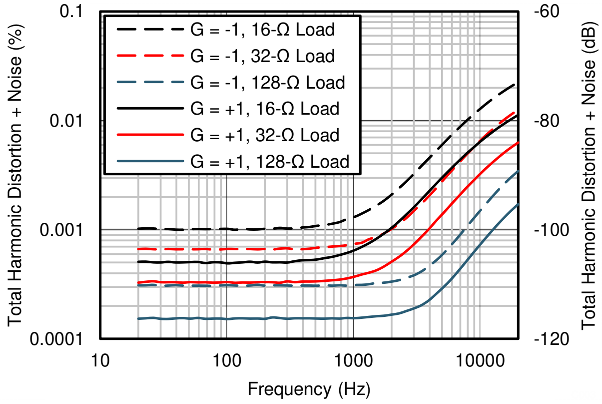
V_{OUT} = 3.5 V_{RMS}, BW = 50 kHz

图 7-15. THD+N Ratio vs Frequency



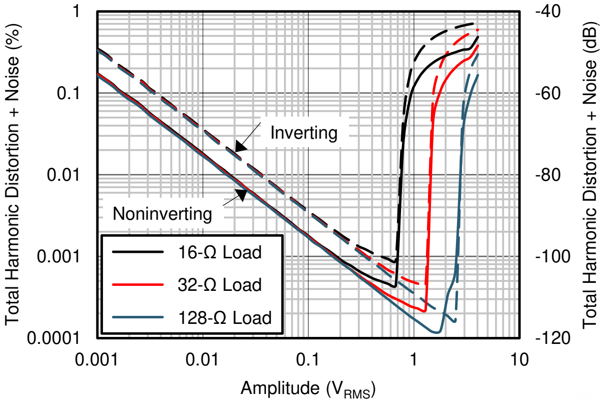
f = 1 kHz, BW = 80 kHz

图 7-16. THD+N vs Output Amplitude



P_{OUT} = 10 mW, BW = 80 kHz, V_S = ±5 V

图 7-17. THD+N vs Frequency



f = 1 kHz, BW = 80 kHz, V_S = ±5 V

图 7-18. THD+N vs Amplitude

7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

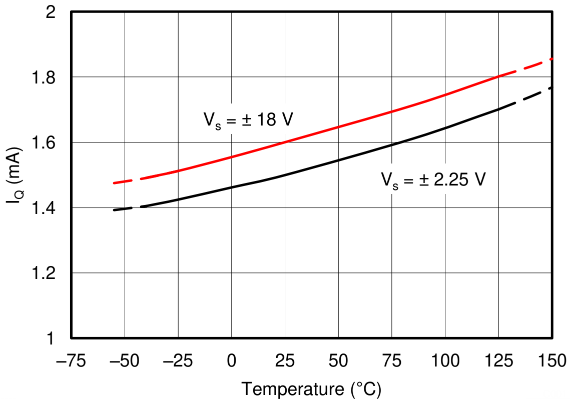


图 7-19. Quiescent Current vs Temperature

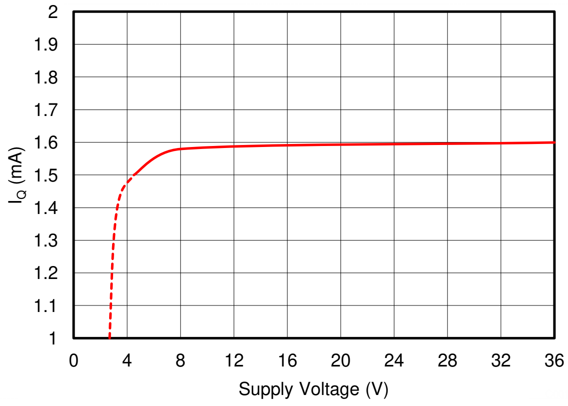
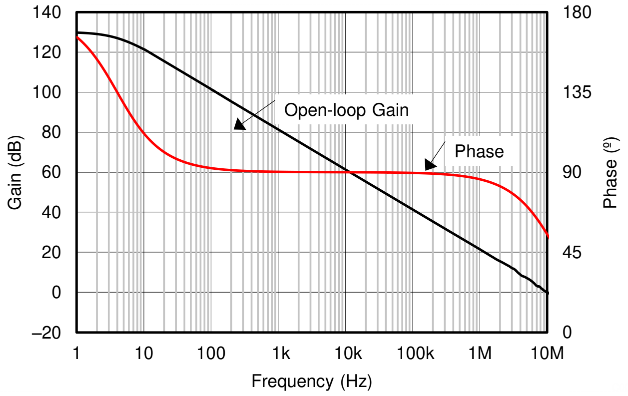


图 7-20. Quiescent Current vs Supply Voltage



C_{LOAD} = 15 pF

图 7-21. Open-Loop Gain and Phase vs Frequency

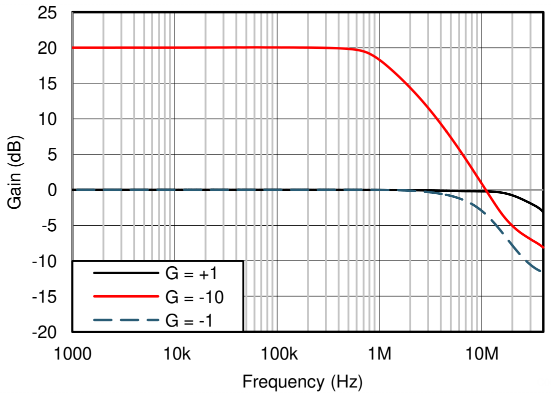
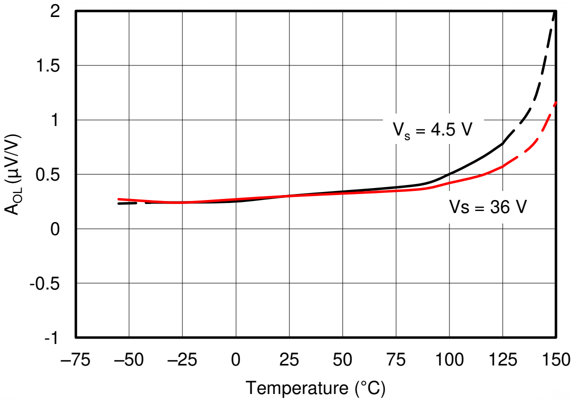


图 7-22. Closed-Loop Gain vs Frequency



R_L = 10 kΩ

图 7-23. Open-Loop Gain vs Temperature

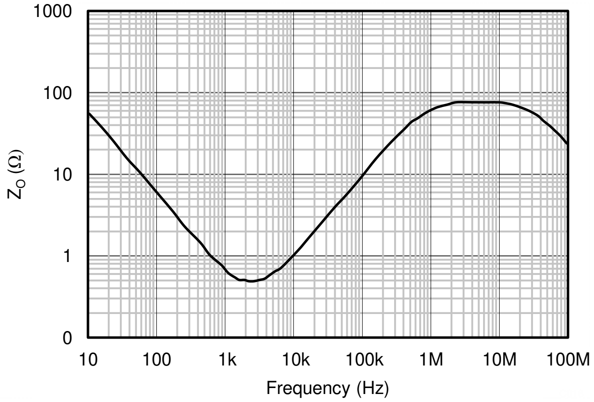


图 7-24. Open-Loop Output Impedance vs Frequency

7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

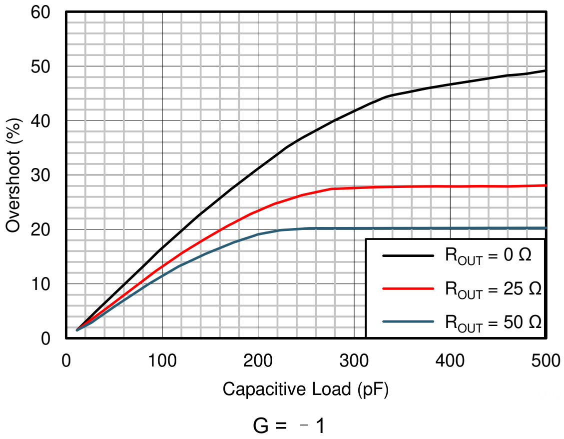


图 7-25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

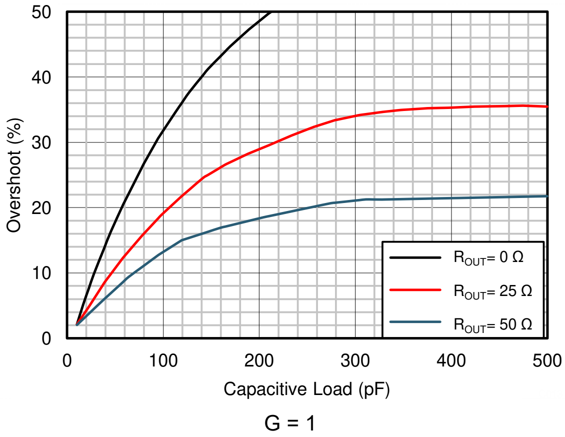


图 7-26. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

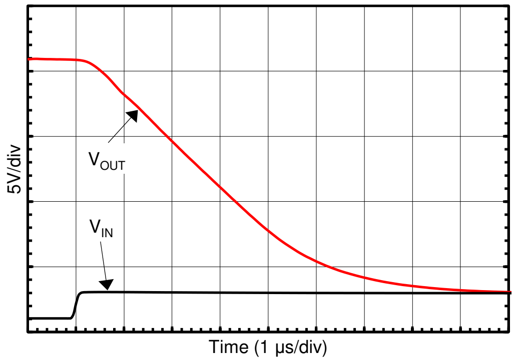


图 7-27. Positive Overload Recovery

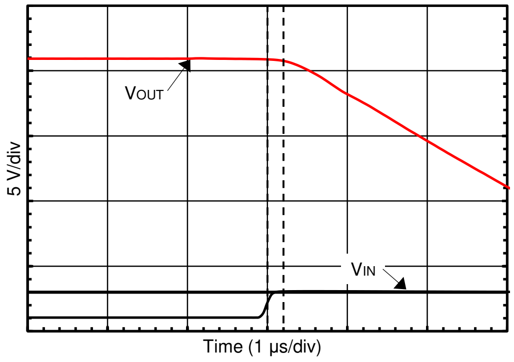


图 7-28. Positive Overload Recovery (Zoomed In)

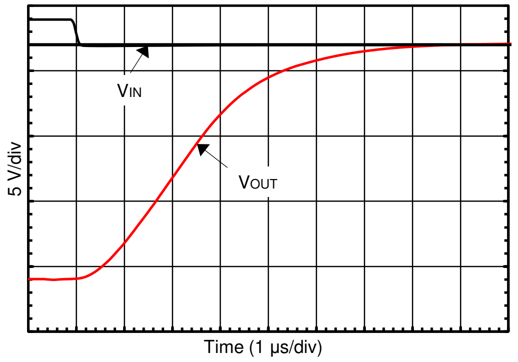


图 7-29. Negative Overload Recovery

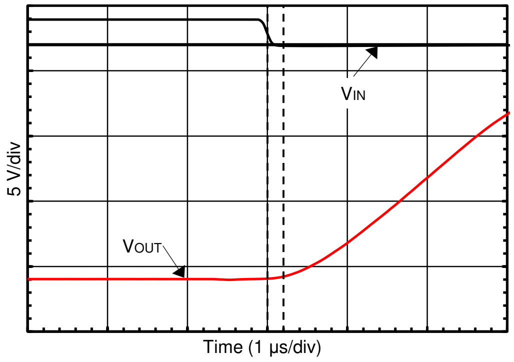
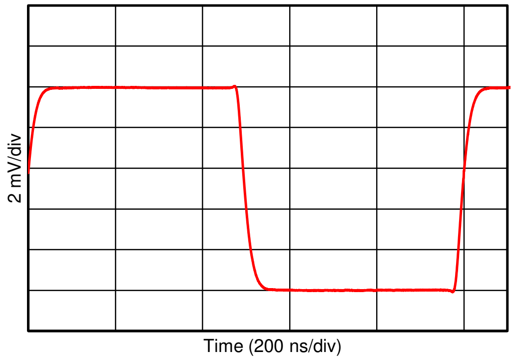


图 7-30. Negative Overload Recovery (Zoomed In)

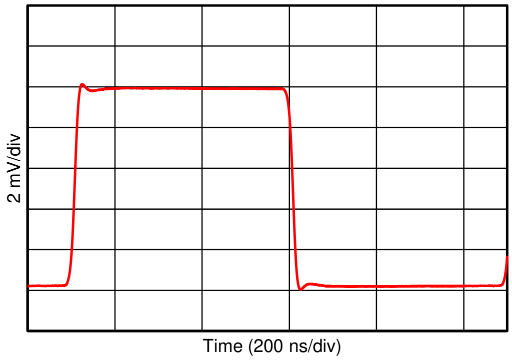
7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



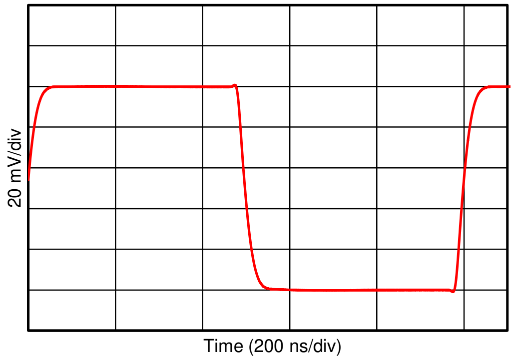
10 mV, G = –1, R_L = 1 kΩ, C_L = 10 pF

图 7-31. Small-Signal Step Response



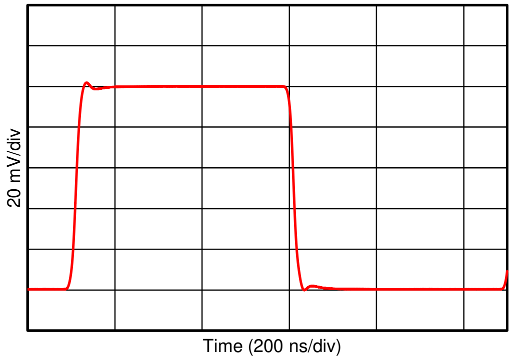
10 mV, G = 1, C_L = 10 pF

图 7-32. Small-Signal Step Response



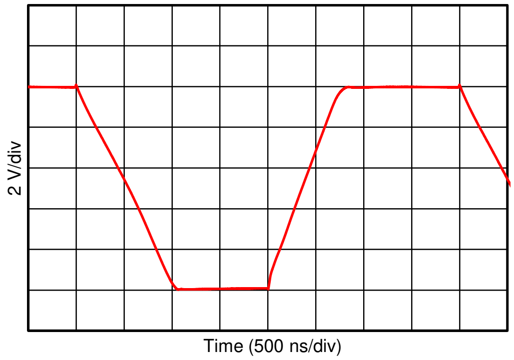
100 mV, G = –1, R_L = 1 kΩ, C_L = 10 pF

图 7-33. Small-Signal Step Response



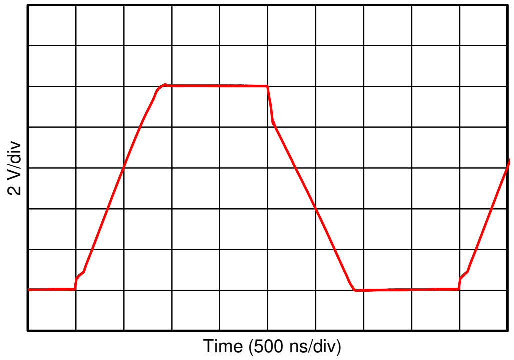
100 mV, G = 1, C_L = 10 pF

图 7-34. Small-Signal Step Response



10 V, G = –1, R_L = 1 kΩ, C_L = 10 pF

图 7-35. Large-Signal Step Response

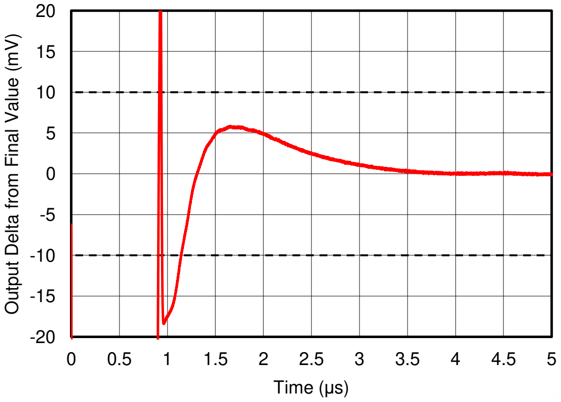


10 V, G = 1, C_L = 10 pF

图 7-36. Large-Signal Step Response

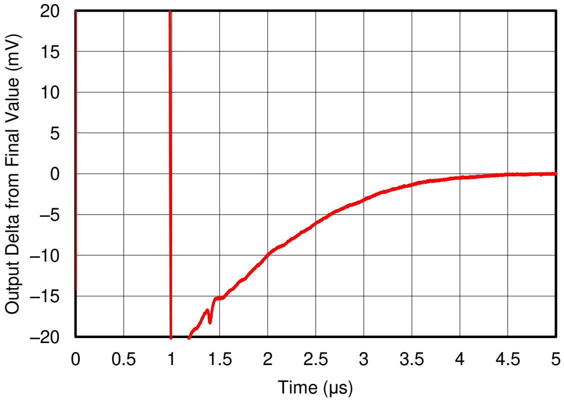
7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = 1, C_L = 10 pF, 0.1% settling = ±10 mV

图 7-37. Large-Signal Settling Time (10-V Positive Step)



G = 1, C_L = 10 pF, 0.1% settling = ±10 mV

图 7-38. Large-Signal Settling Time (10-V Negative Step)

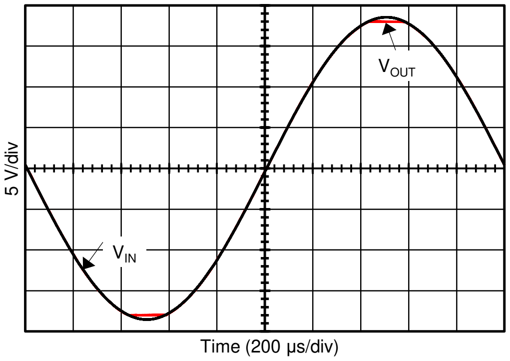


图 7-39. No Phase Reversal

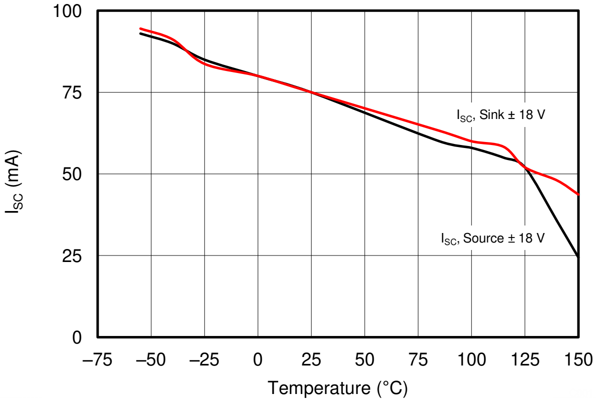


图 7-40. Short-Circuit Current vs Temperature

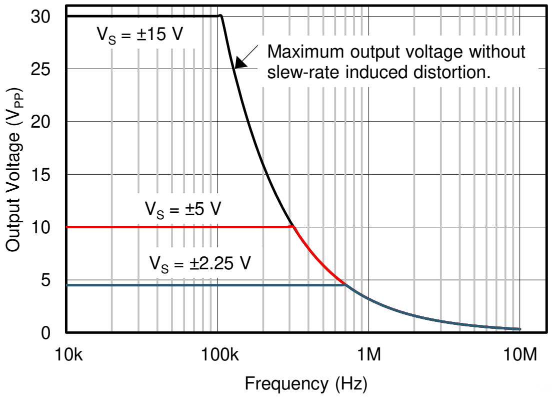
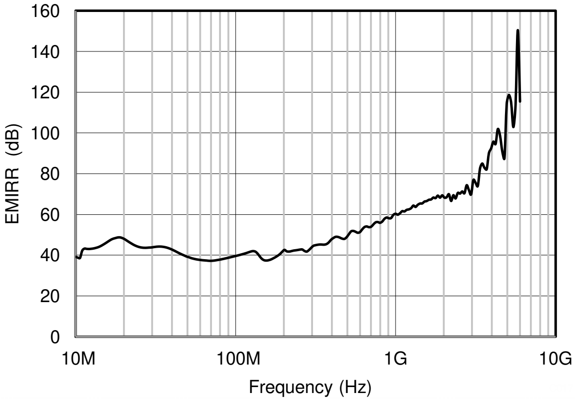


图 7-41. Maximum Output Voltage vs Frequency



P_{RF} = –10 dBm, V_{SUPPLY} = ±18 V, V_{CM} = 0 V

图 7-42. EMIRR vs Frequency

7.6 Typical Characteristics (continued)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

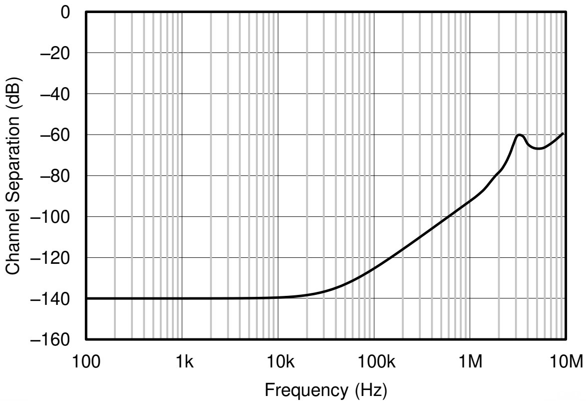


图 7-43. Channel Separation vs Frequency

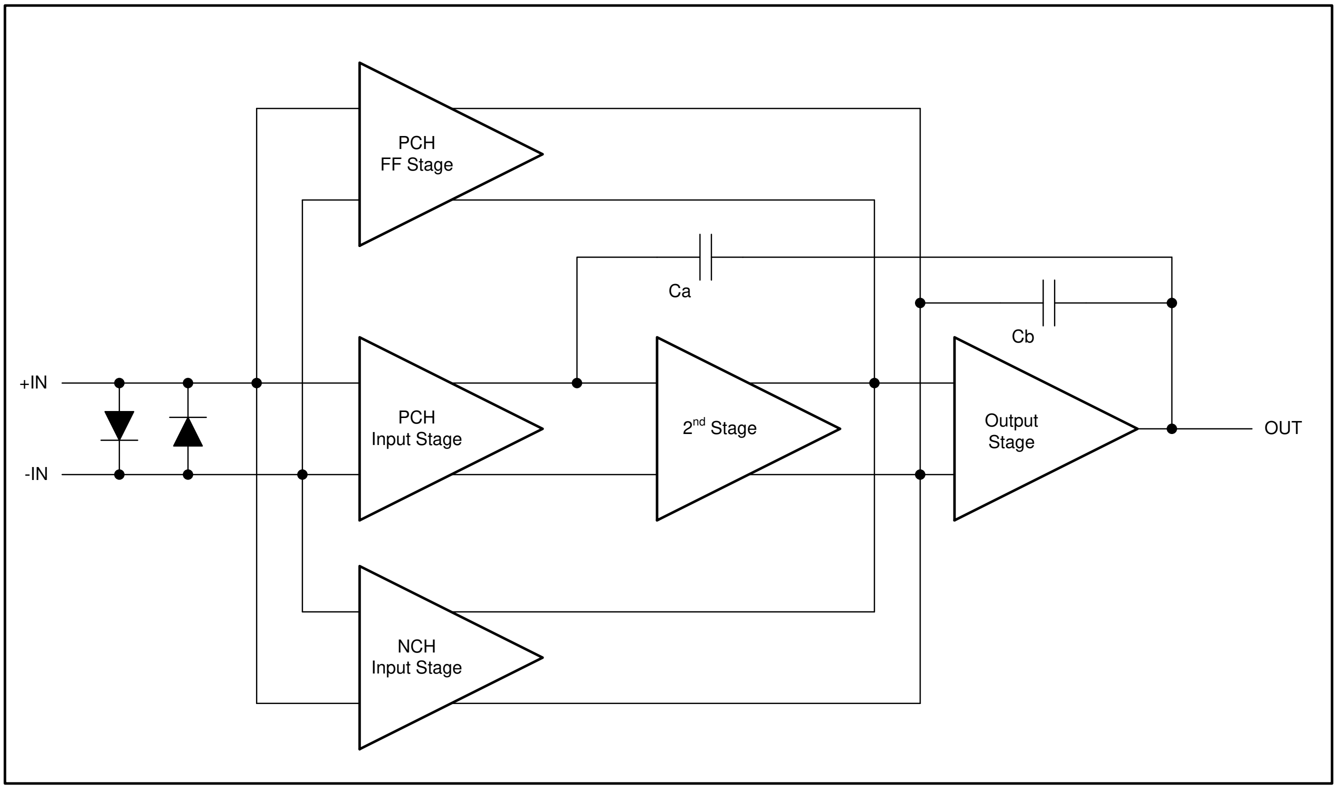
8 Detailed Description

8.1 Overview

The OPA1688 op amp provides high overall performance, making the device an excellent choice for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL}, and superior THD.

节 8.2 shows the simplified diagram of the OPA1688 design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

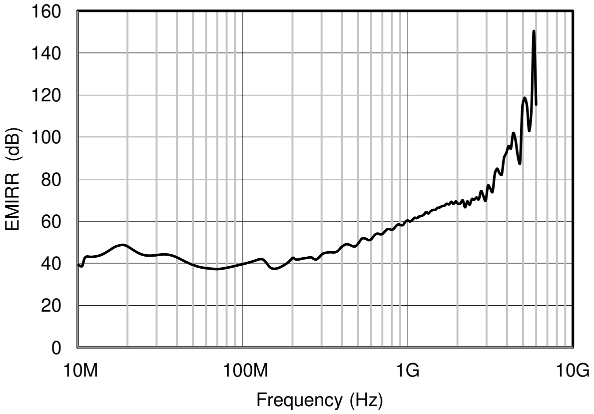
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 EMI Rejection

The OPA1688 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA1688 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 8-1 shows the results of this testing on the OPA1688. 表 8-1 shows the EMIRR IN+ values for the OPA1688 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 8-1 can be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.



P_{RF} = –10 dBm, V_{SUPPLY} = ±18 V, V_{CM} = 0 V

图 8-1. EMIRR Testing

表 8-1. OPA1688 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, and ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, and UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, and L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, and S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, and S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, and C-band (4 GHz to 8 GHz)	114 dB

8.3.2 Phase-Reversal Protection

The OPA1688 has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA1688 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. 图 8-2 shows this performance.

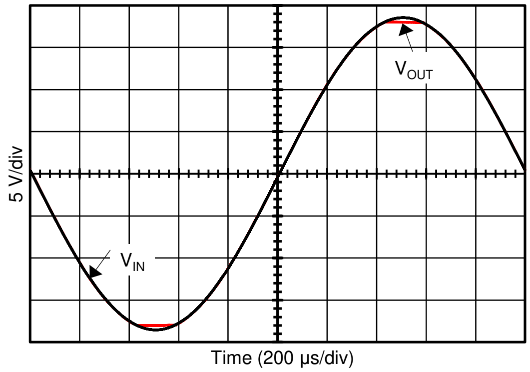


图 8-2. No Phase Reversal

8.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPA1688 are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. 图 8-3 and 图 8-4 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}; see the *Feedback Plots Define Op Amp AC Performance* application bulletin, available for download from www.ti.com, for details of analysis techniques and application circuits.

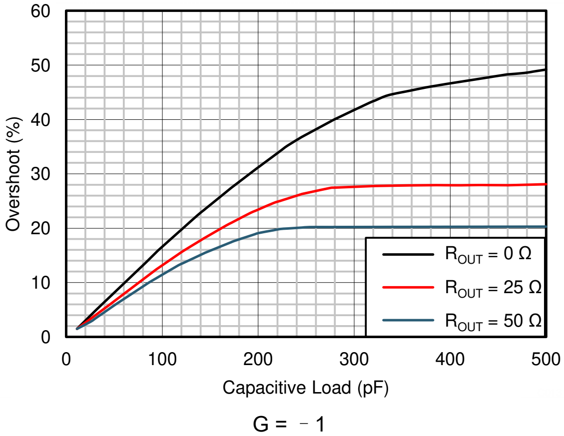


图 8-3. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

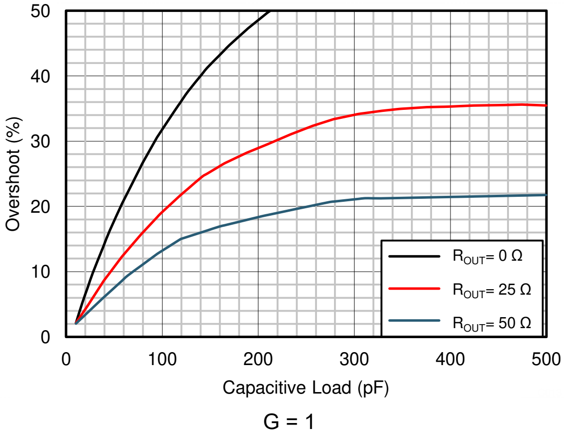


图 8-4. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA1688 extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. 表 8-2 summarizes the typical performance in this range.

表 8-2. Typical Performance Range (V_S = ±18 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
Offset voltage vs temperature (T_A = –40°C to 85°C)		10		μV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/μs
Noise at f = 1 kHz		22		nV/ $\sqrt{Hz}$

8.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 8-5 illustrates the ESD circuits contained in the OPA1688 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

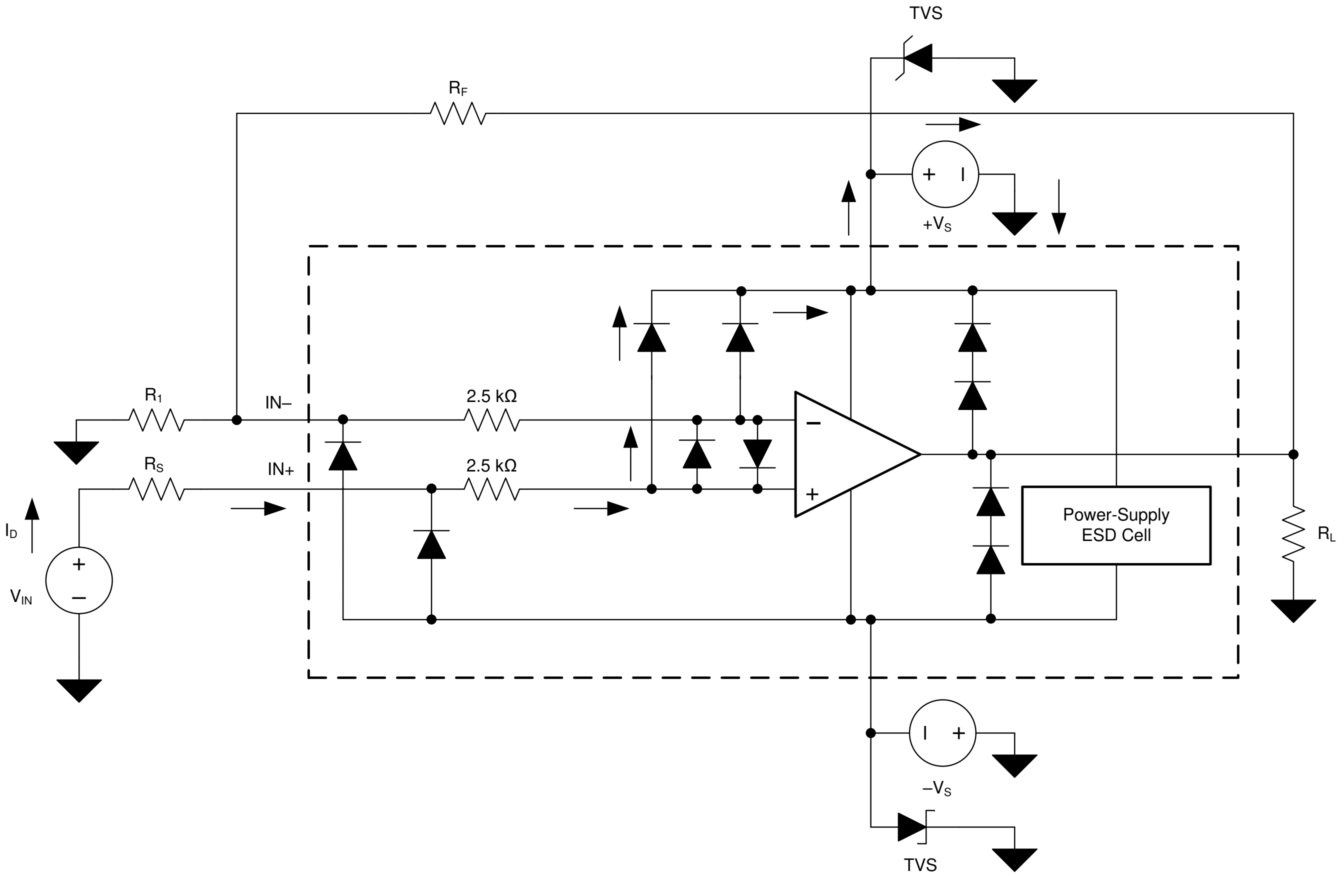


图 8-5. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA1688 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (图 8-5), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 8-5 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (+V_S) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If +V_S can sink the current, one of the upper input steering diodes conducts and directs current to +V_S. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (+V_S or –V_S) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply pins; see 图 8-5. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPA1688 input pins are protected from excessive differential voltage with back-to-back diodes; see 图 8-5. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPA1688. 图 8-5 illustrates an example configuration that implements a current-limiting feedback resistor.

8.4.3 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPA1688 is approximately 200 ns.

9 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The OPA1688 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

9.2 Typical Application

9.2.1 Headphone Amplifier Circuit Configuration

This application example highlights only a few of the circuits where the OPA1688 can be used.

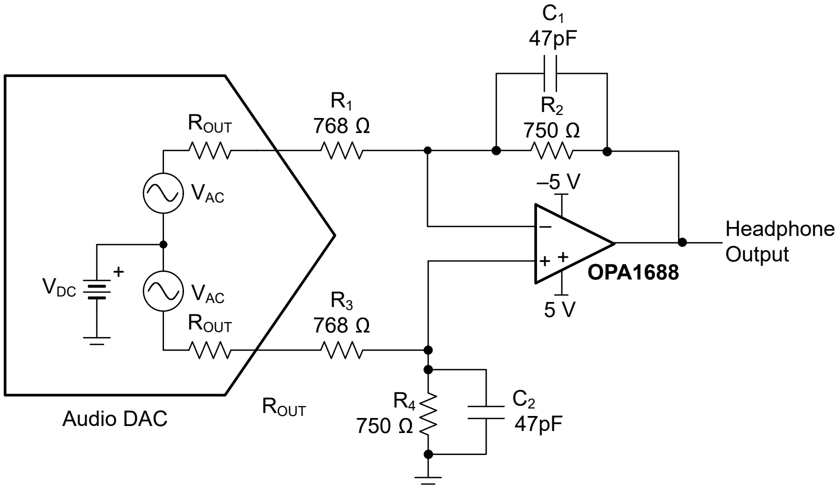


图 9-1. Headphone Amplifier Circuit Configuration for Audio DACs that Output a Differential Voltage (Single Channel Shown)

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 10 V (±5 V)
- Headphone loads: 16 Ω to 600 Ω
- THD+N: > 100 dB (1-kHz fundamental, 1 V_{RMS} in 32 Ω, 22.4-kHz measurement bandwidth)
- Output power (before clipping): 50 mW into 32 Ω

9.2.1.2 Detailed Design Procedure

The OPA1688 offers an excellent combination of specifications for headphone amplifier circuits (such as low noise, low distortion, capacitive load stability, and relatively high output current). Furthermore, the low-power supply current and small package options make the OPA1688 an excellent choice for headphone amplifiers in portable devices. A common headphone amplifier circuit for audio digital-to-analog converters (DACs) with differential voltage outputs is illustrated in 图 9-1. This circuit converts the differential voltage output of the DAC to a single-ended, ground-referenced signal and provides the additional current necessary for low-impedance headphones. For $R_2 = R_4$ and $R_1 = R_3$, the output voltage of the circuit is given by 方程式 1:

$$V_{OUT} = 2 \times V_{AC} \frac{R_2}{R_1 + R_{OUT}} \quad (1)$$

where

- R_{OUT} is the output impedance of the DAC
- $2 \times V_{AC}$ is the unloaded differential output voltage

The output voltage required for headphones depends on the headphone impedance as well as the headphone efficiency. Both values can be provided by the headphone manufacturer, with headphone efficiency usually given as a sound pressure level (SPL) produced with 1 mW of input power and denoted by the Greek letter η. The SPL at other input power levels can be calculated from the efficiency specification using 方程式 2:

$$\text{SPL (dB)} = \eta + 10 \log\left(\frac{P_{IN}}{1 \text{ mW}}\right) \quad (2)$$

At extremely high power levels, the accuracy of this calculation decreases as a result of secondary effects in the headphone drivers. 图 9-2 allows the SPL produced by a pair of headphones of a known sensitivity to be estimated for a given input power.

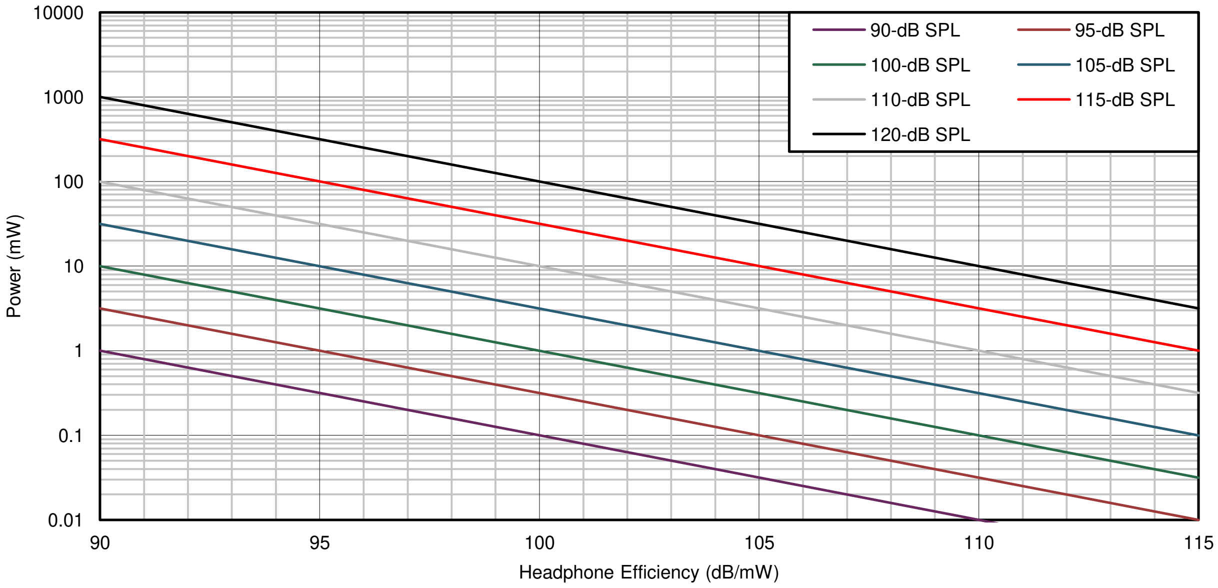


图 9-2. SPLs Produced for Various Headphone Efficiencies and Input Power Levels

For example, a pair of headphones with a 95-dB/mW sensitivity given a 3-mW input signal produces a 100-dB SPL. If these headphones have a nominal impedance of 32 Ω, then 方程式 3 and 方程式 4 describe the voltage and current from the headphone amplifier, respectively:

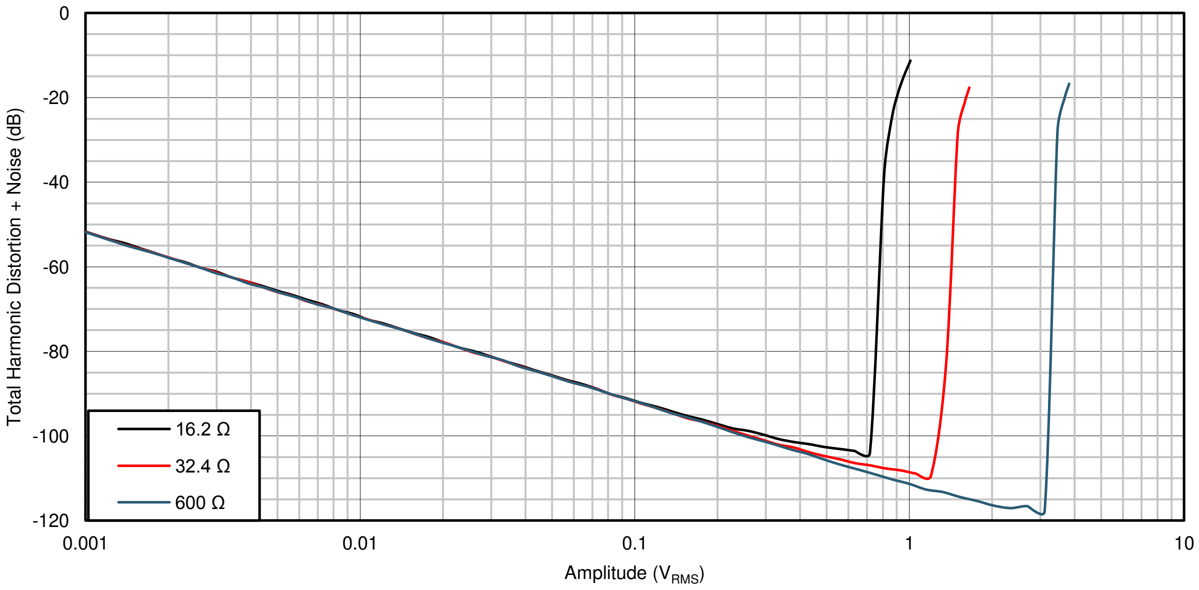
$$V = \sqrt{P_{IN} \times R_{HP}} = \sqrt{3\ \text{mW} \times 32\ \Omega} = 310\ \text{mV}_{RMS} \quad (3)$$

$$I = \sqrt{\frac{P_{IN}}{R_{HP}}} = \sqrt{\frac{3\ \text{mW}}{32\ \Omega}} = 9.68\ \text{mA}_{RMS} \quad (4)$$

Headphones can present a capacitive load at high frequencies that can destabilize the headphone amplifier circuit. Many headphone amplifiers use a resistor in series with the output to maintain stability; however this solution also compromises audio quality. The OPA1688 is able to maintain stability into large capacitive loads; therefore, a series output resistor is not necessary in the headphone amplifier circuit. TINA-TI™ simulations illustrate that the circuit in 图 9-1 has a phase margin of approximately 50° with a 400-pF load connected directly to the amplifier output.

9.2.1.3 Application Curves

The headphone amplifier circuit in 图 9-1 is tested with three common headphone impedances: 16 Ω, 32 Ω, and 600 Ω. The total harmonic distortion and noise (THD+N) for increasing output voltages is given in 图 9-3. This measurement is performed with a 1-kHz input signal and a measurement bandwidth of 22.4 kHz. The maximum output power and THD+N before clipping are given in 表 9-1. The maximum output power into low-impedance headphones is limited by the output current capabilities of the amplifier. For high-impedance headphones (600 Ω), the output voltage capabilities of the amplifier are the limiting factor. The circuit in 图 9-1 is tested using ±5-V supplies that are common in many portable systems. However, using higher supply voltages increases the output power into 600-Ω headphones.



Input signal = 1 kHz, measurement bandwidth = 22.4 kHz

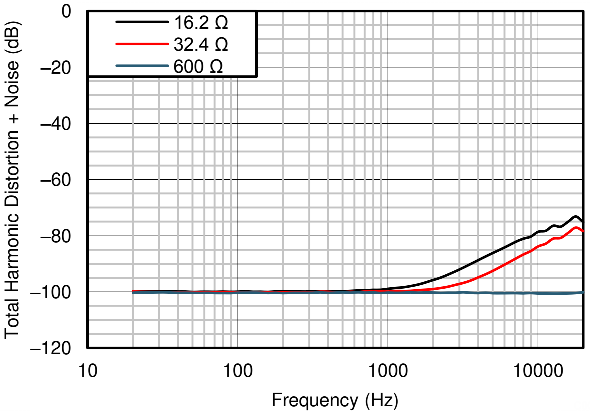
图 9-3. THD+N for Increasing Output Voltages Into Three Load Impedances

表 9-1. Maximum Output Power and THD+N Before Clipping for Different Load Impedances

LOAD IMPEDANCE (Ω)	MAXIMUM OUTPUT POWER BEFORE CLIPPING (mW)	THD+N AT MAXIMUM OUTPUT POWER (dB)
16	32	–104.1
32	50	–109.5
600	16	–117.8

图 9-4, 图 9-5, and 图 9-6 further illustrate the exceptional performance of the OPA1688 as a headphone amplifier.

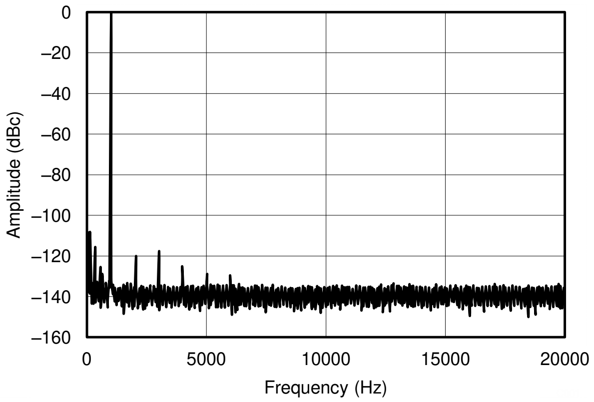
图 9-4 shows the THD+N over frequency for a 500-mV$_{RMS}$ output signal into the same three load impedances previously tested.



90-kHz measurement bandwidth

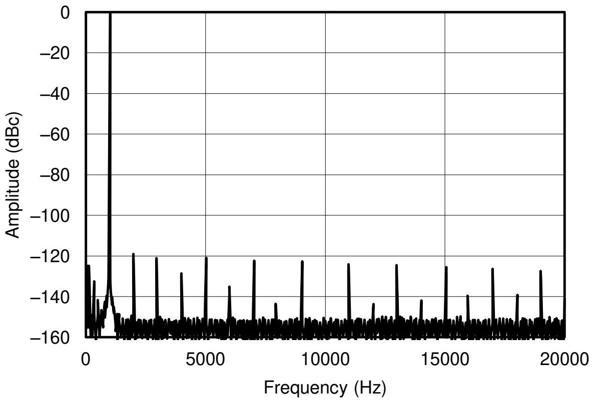
图 9-4. THD+N Measured over Frequency for a 500-mV$_{RMS}$ Output Level

图 9-5 and 图 9-6 show the output spectrum of the OPA1688 at low (1 mW) and high (50 mW) output power levels into a 32-Ω load. The distortion harmonics in both cases are approximately 120 dB below the fundamental.



Third harmonic is dominant at a level of –117.6 dB relative to the fundamental

图 9-5. Output Spectrum of a 1-mW, 1-kHz Tone into a 32-Ω Load



Highest harmonic is the second harmonic at –119 dB below the fundamental

图 9-6. Output Spectrum of a 50-mW, 1-kHz Tone Into a 32-Ω Load, Immediately Below the Onset of Clipping

10 Power Supply Recommendations

The OPA1688 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in 节 *7.6*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see also 节 *7.1*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see also 节 *11*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. 图 11-1 illustrates how keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

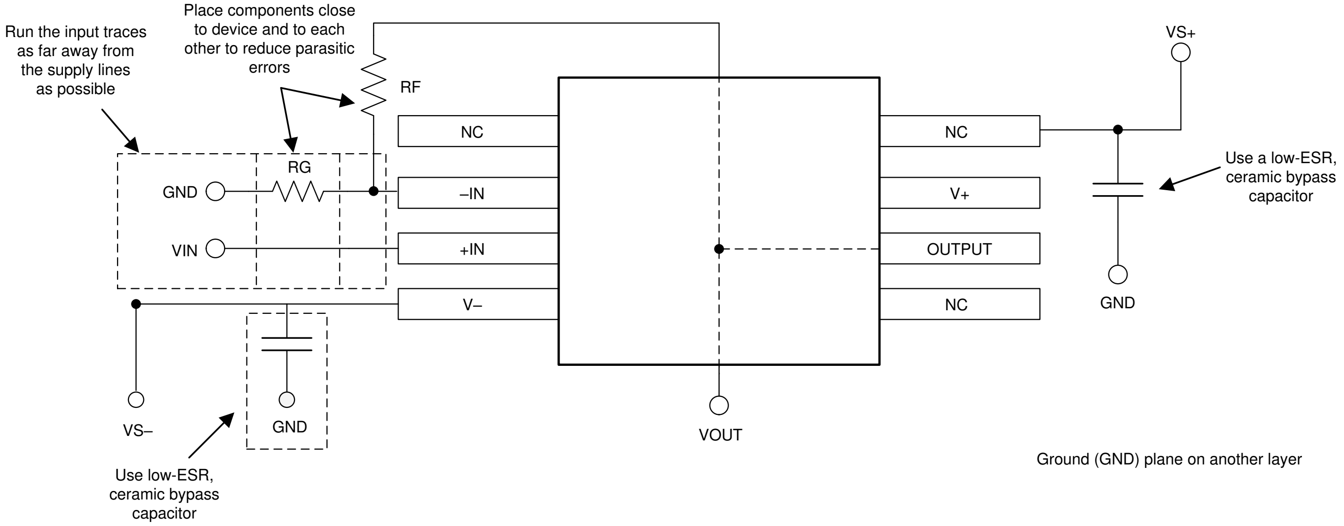


图 11-1. Operational Amplifier Board Layout for a Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI 是可帮助评估模拟电路性能的设计和仿真环境。在进行布局和制造之前创建子系统设计和原型解决方案，可降低开发成本并缩短上市时间。

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

12.2 Documentation Support

12.2.1 Related Documentation

- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Op Amps for Everyone* application note
- Texas Instruments, *Capacitive Load Drive Solution Using an Isolation Resistor* reference design

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1688ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1688A	Samples
OPA1688IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1688A	Samples
OPA1688IDRGR	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1688	Samples
OPA1688IDRGT	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1688	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

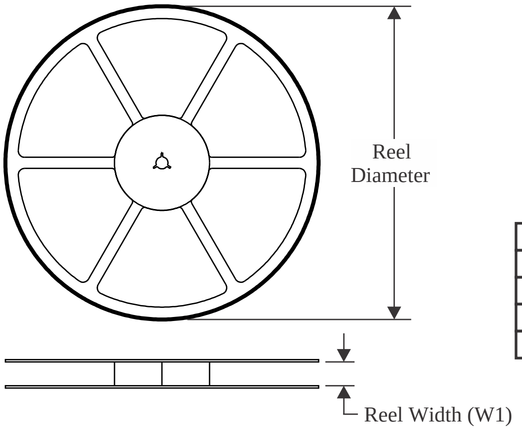
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

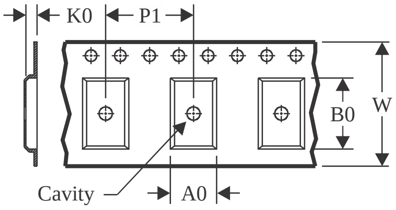
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

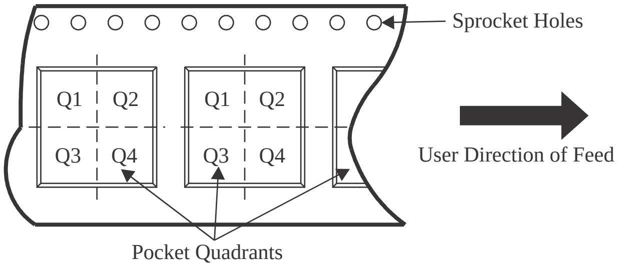


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

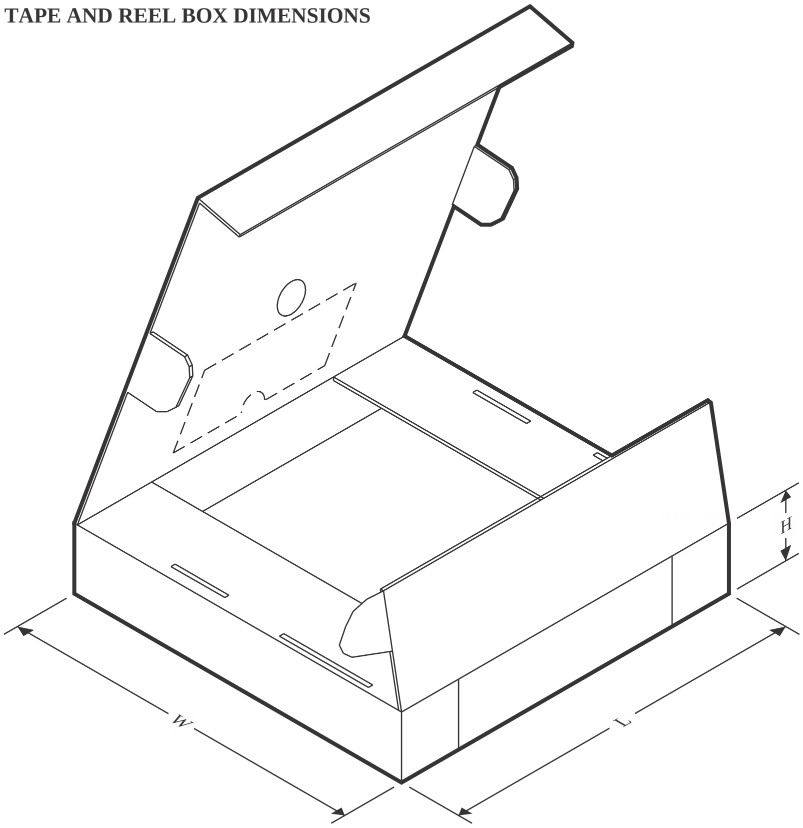
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1688IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1688IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1688IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

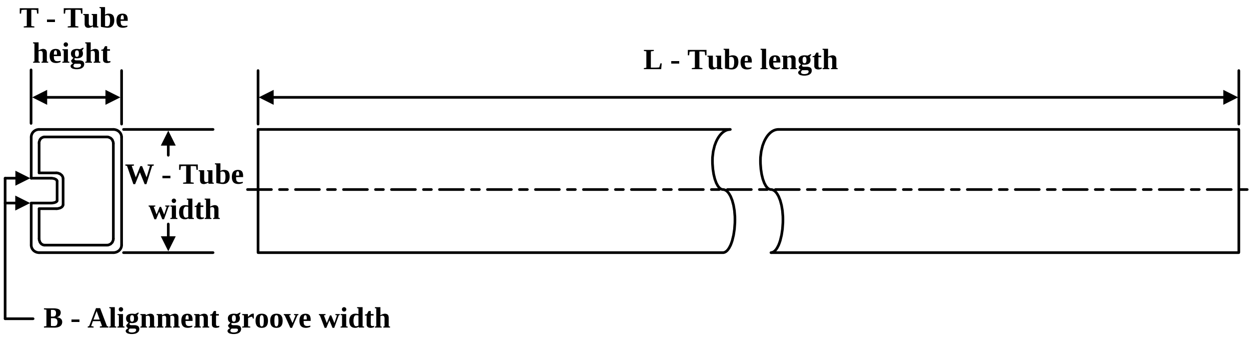
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1688IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA1688IDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA1688IDRGT	SON	DRG	8	250	210.0	185.0	35.0

TUBE



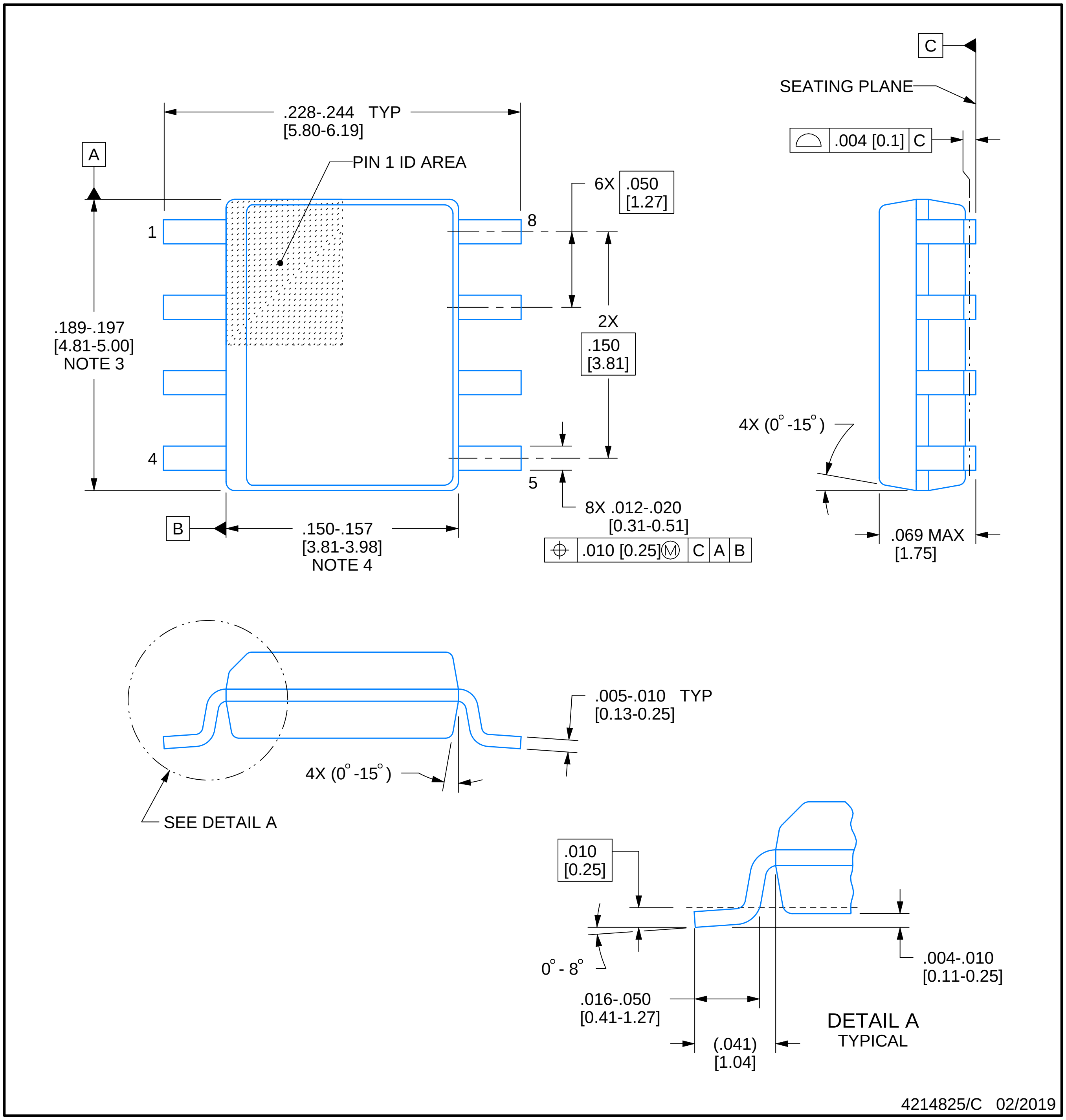
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1688ID	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

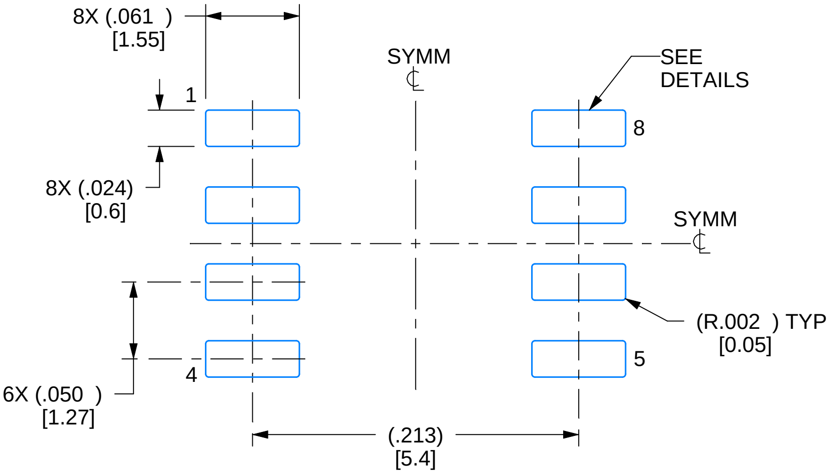
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

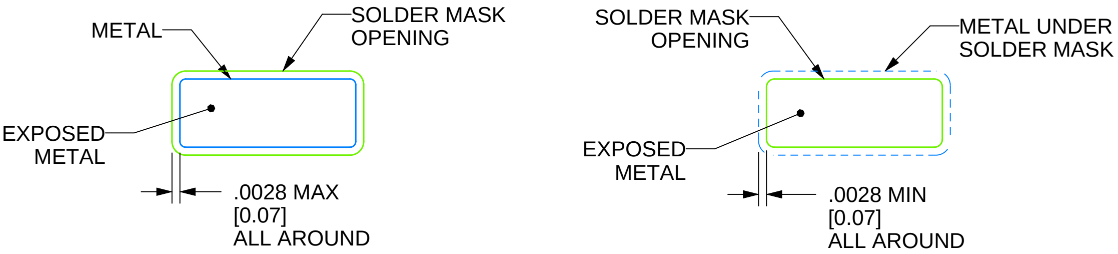


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

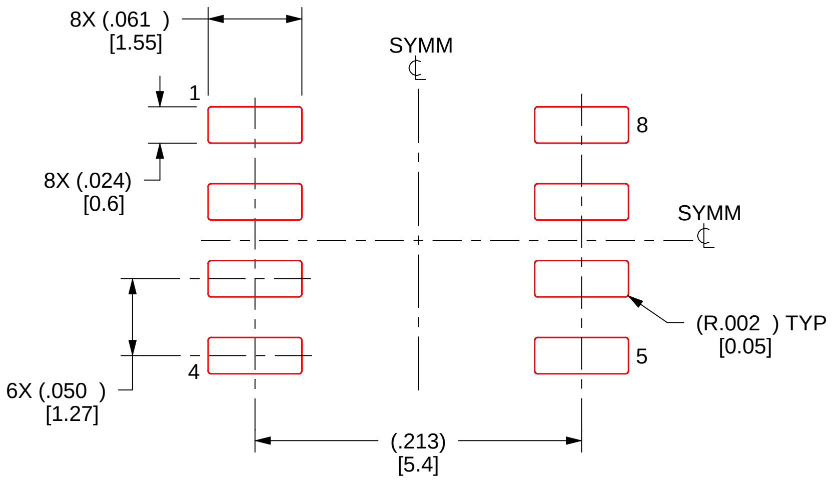
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

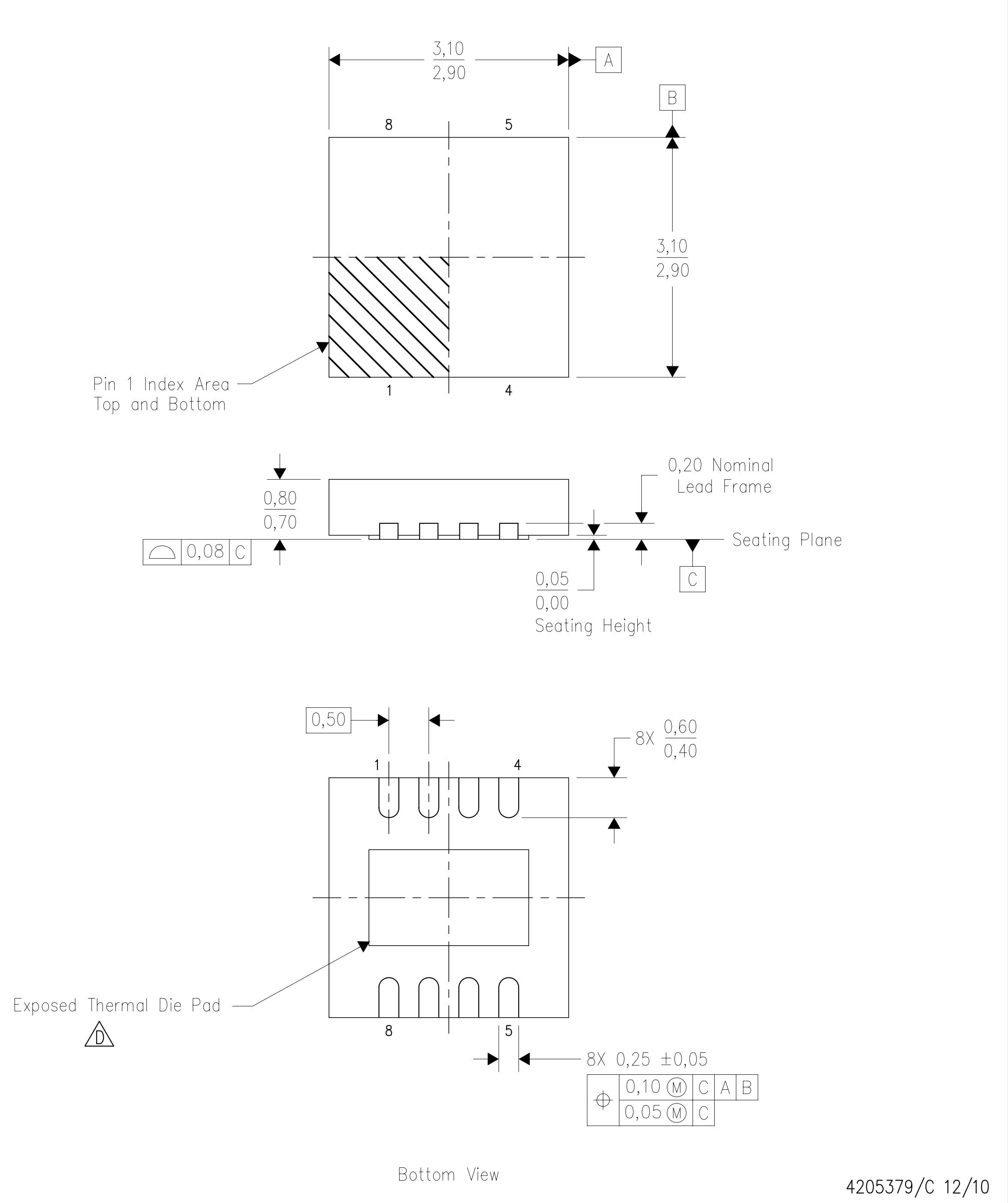


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

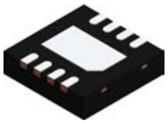
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. JEDEC MO-229 package registration pending.

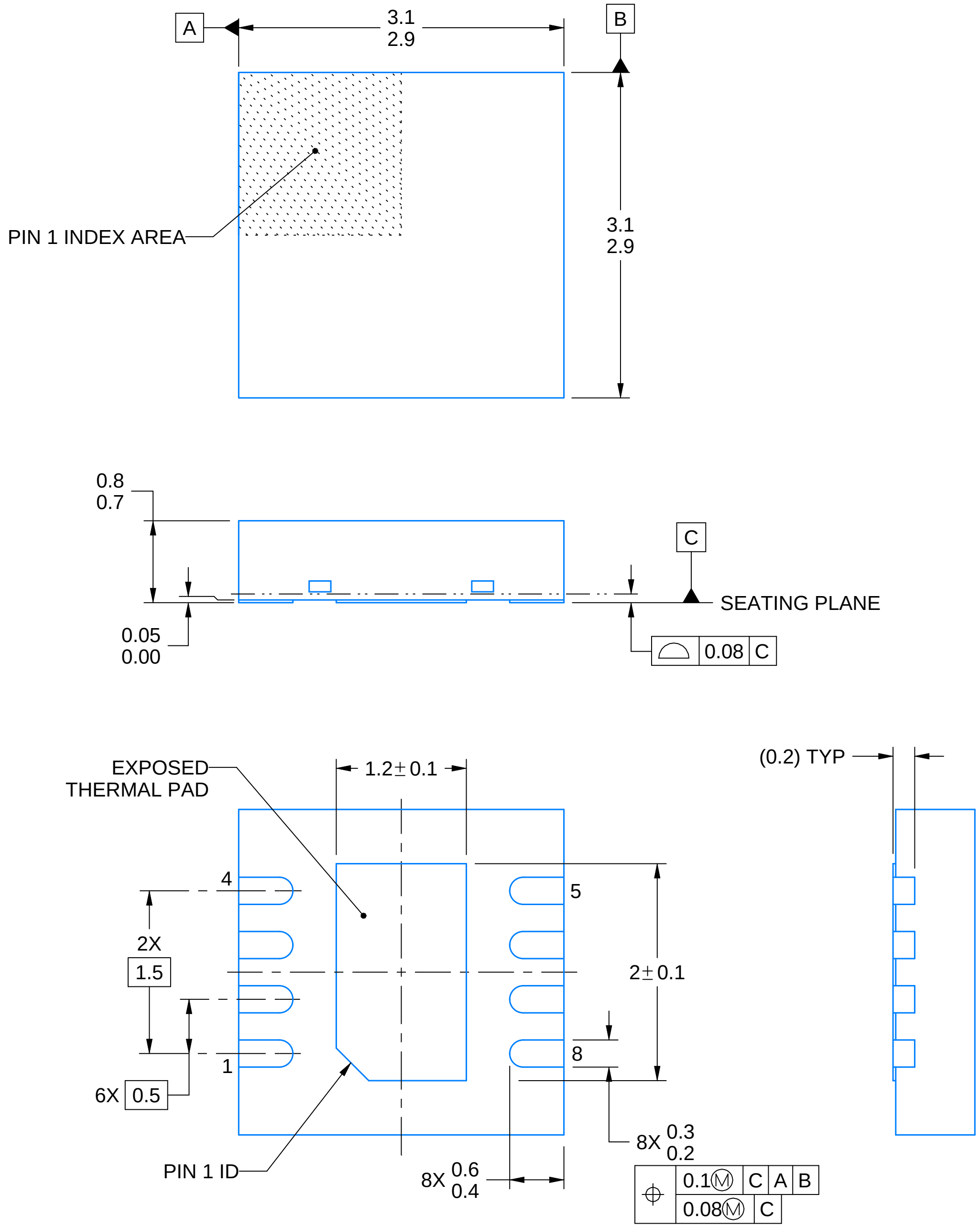
DRG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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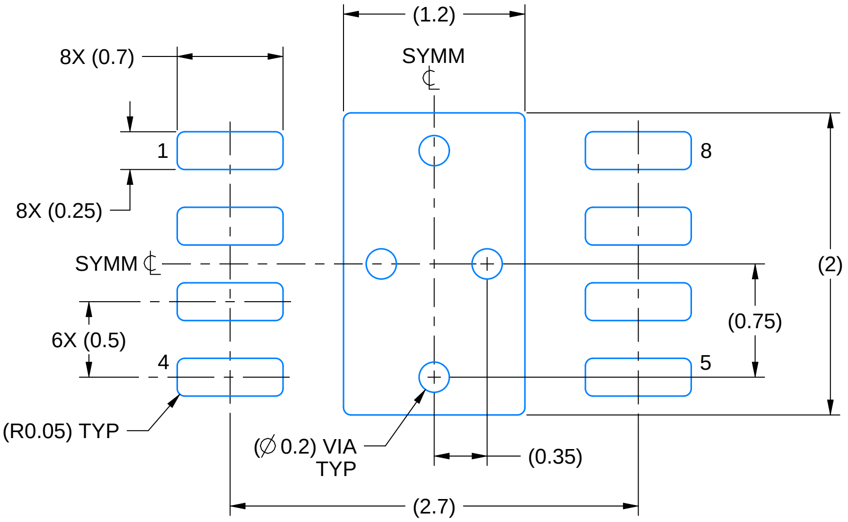
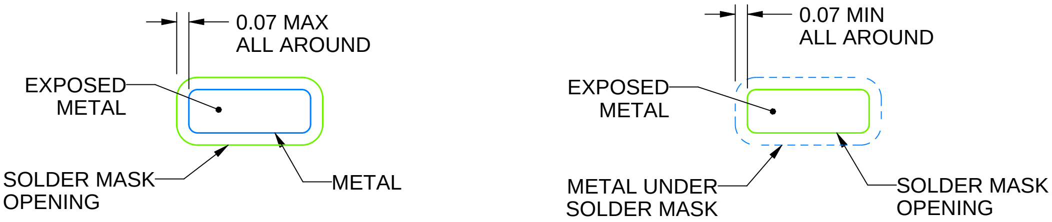
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



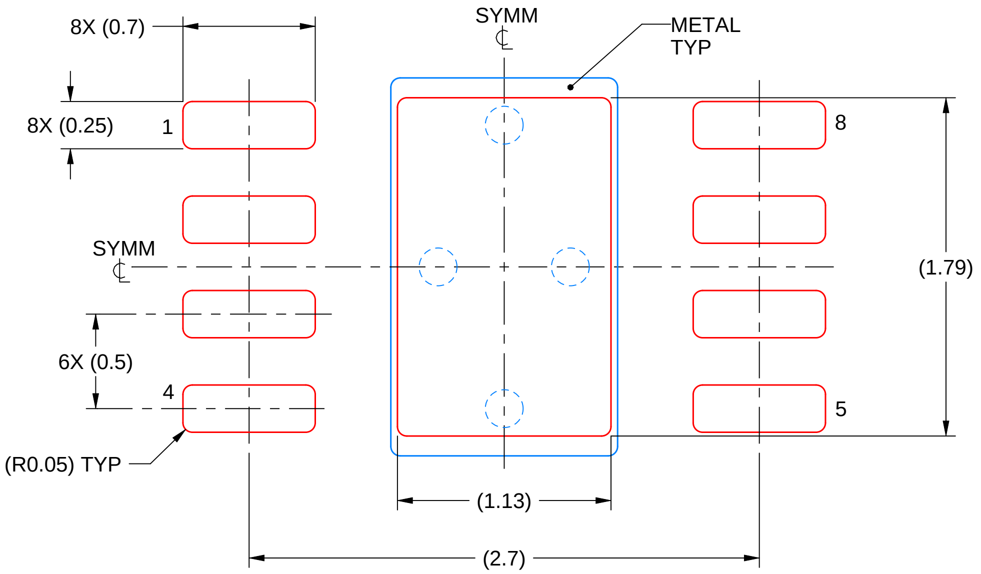
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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