

# MC3487 四路差分线路驱动器

## 1 特性

- 符合或超出 ANSI TIA/EIA-422-B 和 ITU 建议 V.11 的要求
- 三态 TTL 兼容输出
- 快速转换时间
- 高阻抗输入
- 5V 单电源
- 上电和下电保护

## 2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动

## 3 说明

MC3487 提供四个独立的差分线路驱动器，旨在符合 ANSI TIA/EIA-422-B 和 ITU 建议 V.11 规范。每个驱动器有一个缓冲的 TTL 兼容输入，用于降低电流和最大限度降低负载。

当适当的输出使能处于逻辑低电平时，驱动器输出使用三态电路在任何一对差分输出提供高阻抗状态。如果输出使能为低电平，则在上电和下电转换时间内，内部电路在差分输出为高阻抗状态。

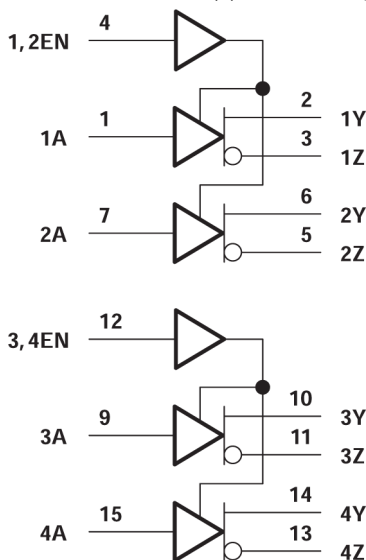
MC3487 旨在与 MC3486 四路线路接收器配合使用来实现卓越性能。该器件采用 16 引脚 Dual-In-Line 封装，通过 5V 单电源供电运行。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
MC3486	D (SOIC, 16)	19.3mm × 9.4mm
	N (PDIP, 16)	19.3mm × 9.4mm
	NS (SOP, 16)	10.2mm × 7.8mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



逻辑图 (正逻辑)



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## 4 Pin Configuration and Functions

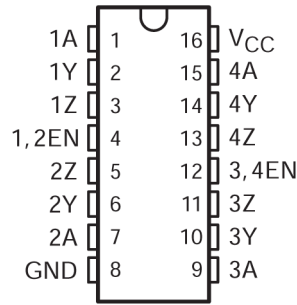


图 4-1. D, N, or NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I	Single Ended Data Input for Channel 1
1Y	2	O	Non-Inverting Output for Differential Driver on Channel 1
1Z	3	O	Inverting Output of Differential Driver on Channel 1
1,2EN	4	I	Enable Input for Channels 1 and 2
2Z	5	O	Inverting Output of Differential Driver on Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2A	7	I	Single Ended Data Input for Channel 2
GND	8	GND	Device Ground
3A	9	I	Single Ended Data Input for Channel 3
3Y	10	O	Non-Inverting Output for Differential Driver on Channel 3
3Z	11	O	Inverting Output of Differential Driver on Channel 3
3,4EN	12	I	Enable Input for Channels 3 and 4
4Z	13	O	Inverting Output of Differential Driver on Channel 4
4Y	14	O	Non-Inverting Output for Differential Driver on Channel 4
4A	15	I	Single Ended Data Input for Channel 4
V <sub>CC</sub>	16	P	5V Power Supply Positive Terminal Connection

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = Ground.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$ (see (2))	Supply voltage		7	V
$V_I$	Input voltage		5.5	V
$V_O$	Output voltage		7	V
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential output voltage,  $V_{OD}$ , are with respect to the network ground terminal.

### 5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$T_A$	Operating free-air temperature	0		70	°C

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16-PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$V_{OH}$	High-level output voltage	$V_{IL} = 0.8 \text{ V}$ ,	$V_{IH} = 2 \text{ V}$ ,	$I_{OH} = -20 \text{ mA}$	2.5		V
$V_{OL}$	Low-level output voltage	$V_{IL} = 0.8 \text{ V}$ ,	$V_{IH} = 2 \text{ V}$ ,	$I_{OL} = 48 \text{ mA}$		0.5	V
$ V_{OD} $	Differential output voltage	$R_L = 100 \ \Omega$	See <a href="#">图 6-1</a>		2		
$\Delta  V_{OD} $	Change in magnitude of differential output voltage <sup>(1)</sup>	$R_L = 100 \ \Omega$	See <a href="#">图 6-1</a>			$\pm 0.4$	V
$V_{OC}$	Common-mode output voltage <sup>(2)</sup>	$R_L = 100 \ \Omega$	See <a href="#">图 6-1</a>			3	V
$\Delta  V_{OC} $	Change in magnitude of common-mode output voltage <sup>(1)</sup>	$R_L = 100 \ \Omega$	See <a href="#">图 6-1</a>			$\pm 0.4$	V
$I_O$	Output current with power off	$V_{CC} = 0$	$V_O = 6 \text{ V}$			100	$\mu\text{A}$
			$V_O = -0.25 \text{ V}$			-100	
$I_{OZ}$	High-impedance-state output current	Output enables at 0.8 V	$V_O = 2.7 \text{ V}$			100	$\mu\text{A}$
			$V_O = 0.5 \text{ V}$			-100	
$I_I$	Input current at maximum input voltage	$V_I = 5.5 \text{ V}$				100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_I = 2.7 \text{ V}$				50	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.5 \text{ V}$				-400	$\mu\text{A}$
$I_{OS}$	Short-circuit output current <sup>(3)</sup>	$V_I = 2 \text{ V}$			-40	-140	mA
$I_{CC}$	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled, No load				85	

- (1)  $\Delta |V_{OD}|$  and  $\Delta |V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.
- (2) In ANSI Standard TIA/EIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .
- (3) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

## 5.5 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V}$

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$C_L = 15 \text{ pF}$ ,	See <a href="#">图 6-2</a>		20	ns
$t_{PHL}$	Propagation delay time, high- to low-level output				20	
$t_{sk}$	Skew time	$C_L = 15 \text{ pF}$ ,	See <a href="#">图 6-2</a>		6	ns
$t_{(OD)}$	Differential-output transition time	$C_L = 15 \text{ pF}$ ,	See <a href="#">图 6-3</a>		20	ns
$t_{PZH}$	Output enable time to high level	$C_L = 50 \text{ pF}$ ,	See <a href="#">图 6-4</a>		30	ns
$t_{PZL}$	Output enable time to low level				30	
$t_{PHZ}$	Output disable time from high level	$C_L = 50 \text{ pF}$ ,	See <a href="#">图 6-4</a>		25	ns
$t_{PLZ}$	Output disable time from low level				30	

## 6 Parameter Measurement Information

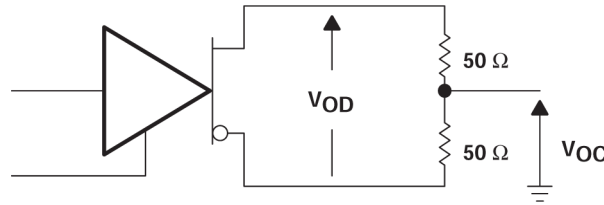
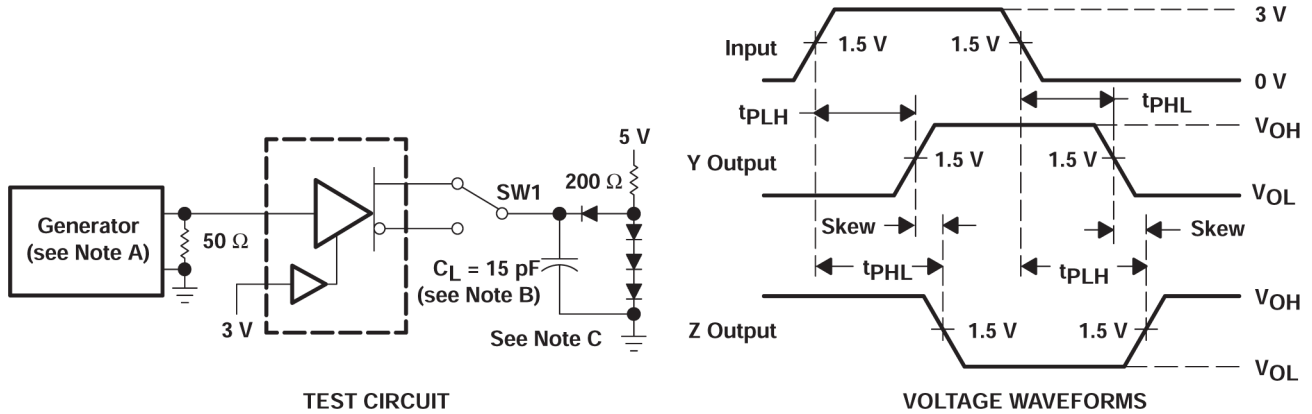
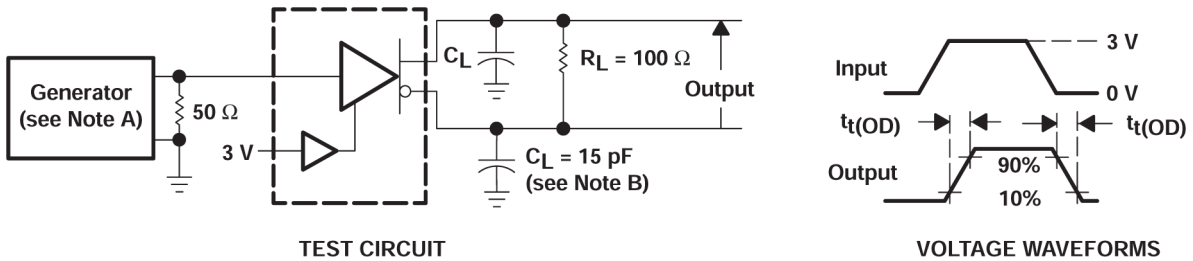


图 6-1. Differential and Common-Mode Output Voltages



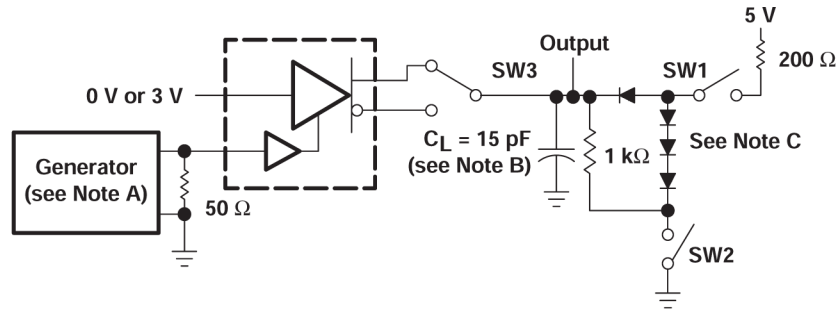
- A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ , duty cycle = 50%  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

图 6-2. Test Circuit and Voltage Waveforms

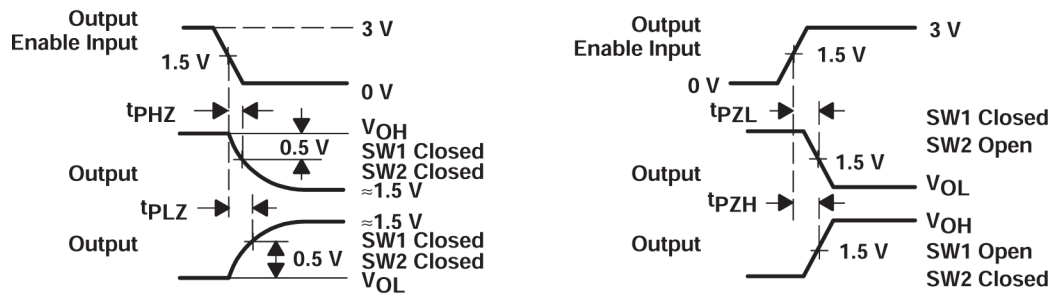


- A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ , duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.

图 6-3. Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ , duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

图 6-4. Driver Test Circuit and Voltage Waveforms

## 7 Device Functional Modes

表 7-1. Function Table (Each Driver)

INPUT	OUTPUT ENABLE <sup>(1)</sup>	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = TTL high level, L = TTL low level, X = irrelevant, Z = High impedance

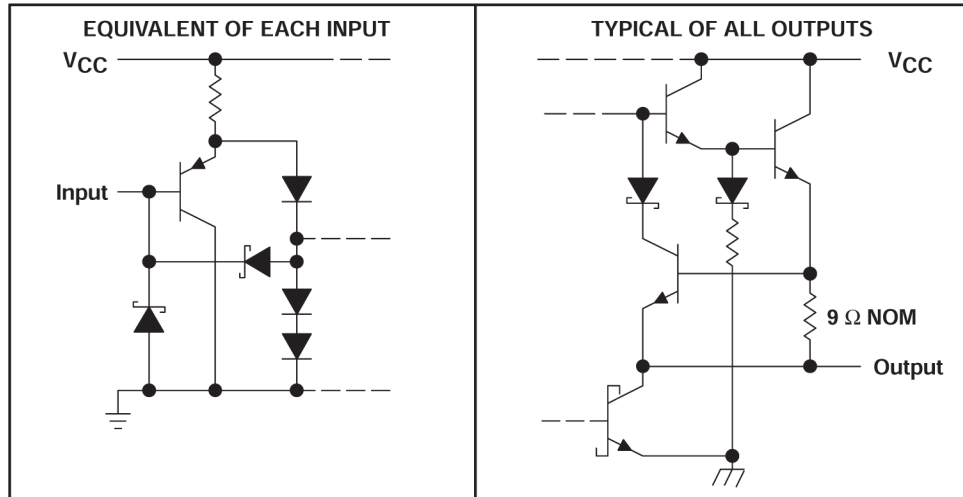


图 7-1. Schematics of Inputs and Outputs



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.2 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.5 术语表

[TI 术语表](#)      本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (February 2004) to Revision D (March 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3487D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	MC3487	
MC3487DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

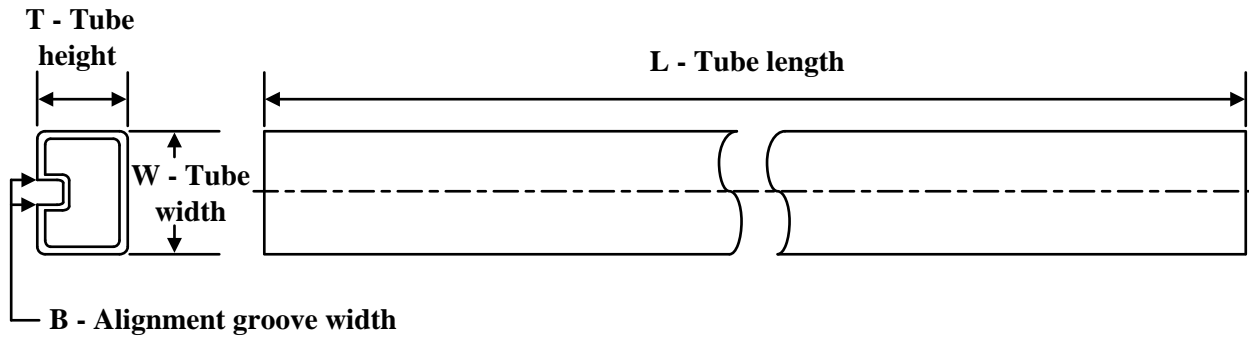
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3487DR	SOIC	D	16	2500	340.5	336.1	32.0
MC3487DR	SOIC	D	16	2500	353.0	353.0	32.0
MC3487NSR	SOP	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



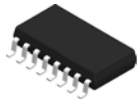
N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

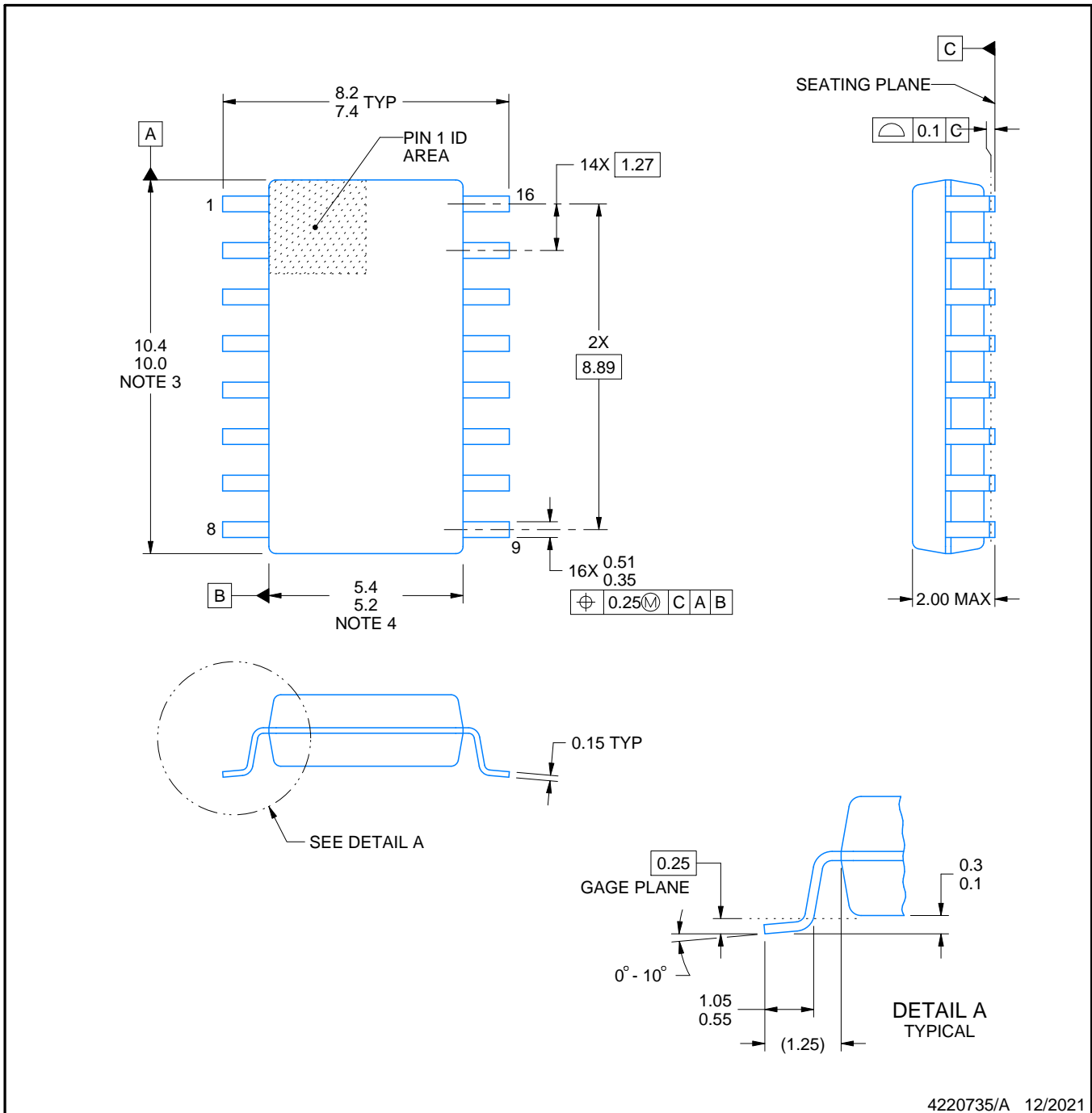


# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

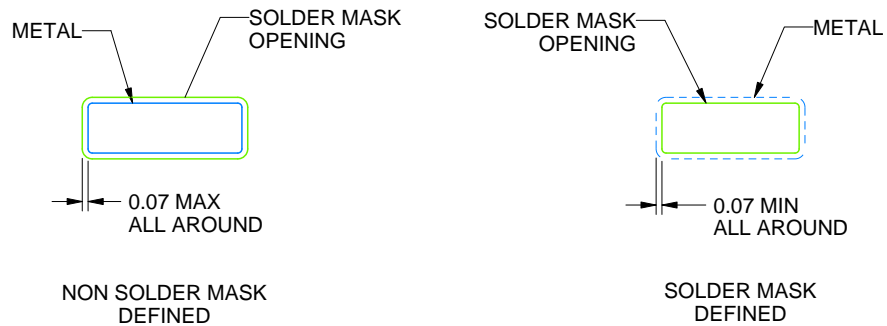
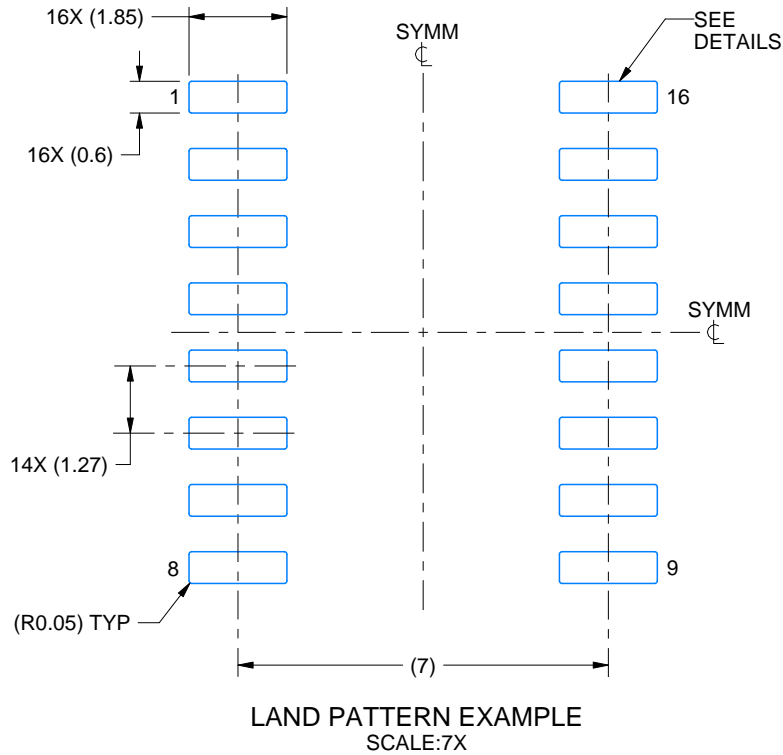
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

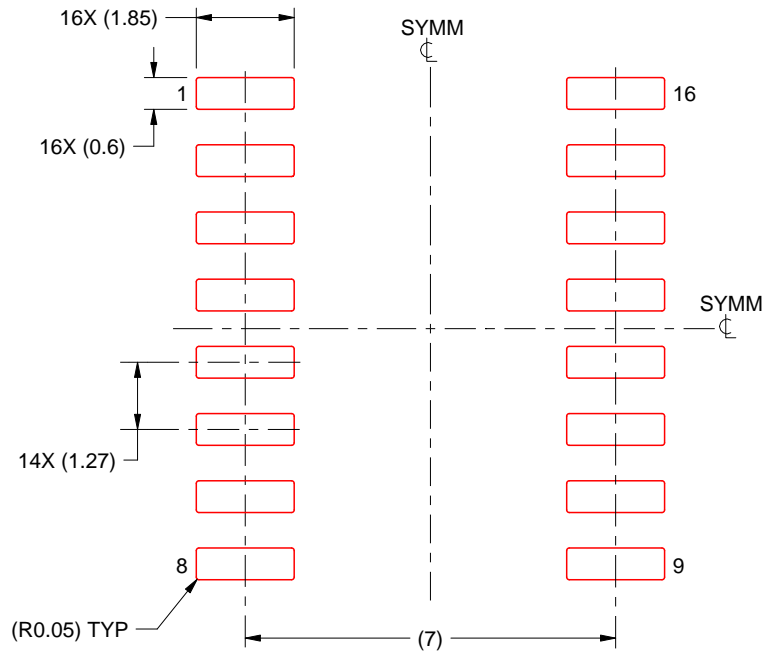
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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