

## LM74610-Q1 零 IQ 反极性保护智能二极管控制器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 超出人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件充电器件模型 (CDM) ESD 分类等级 C4B
- 最低反向电压：45V
- 正极引脚无正电压限制
- 适用于外部 N 沟道金属氧化物半导体场效应晶体管 (MOSFET) 的电荷泵栅极驱动器
- 功耗比肖特基二极管/PFET 解决方案更低
- 低反极性泄漏电流
- 零 IQ
- 2 $\mu$ s 内快速响应反极性情况
- 40°C 至 125°C 工作环境温度
- 可用于 OR-ing 应用
- 符合 CISPR25 EMI 规范
- 选用了合适的瞬态电压抑制器 (TVS) 二极管，满足汽车类 ISO7637 瞬态要求

### 2 应用

- 高级驾驶员辅助系统 (ADAS)
- 信息娱乐系统
- 电动工具 (工业)
- 传输控制单元 (TCU)
- 电池 OR-ing 应用

### 3 说明

LM74610-Q1 是一款控制器器件，可与 N 沟道 MOSFET 一同用于反极性保护电路。其设计用于驱动外部 MOSFET，串联电源时可模拟理想二极管整流器。该机制的独特优势在于不以接地为参考，因此 I<sub>q</sub> 为零。

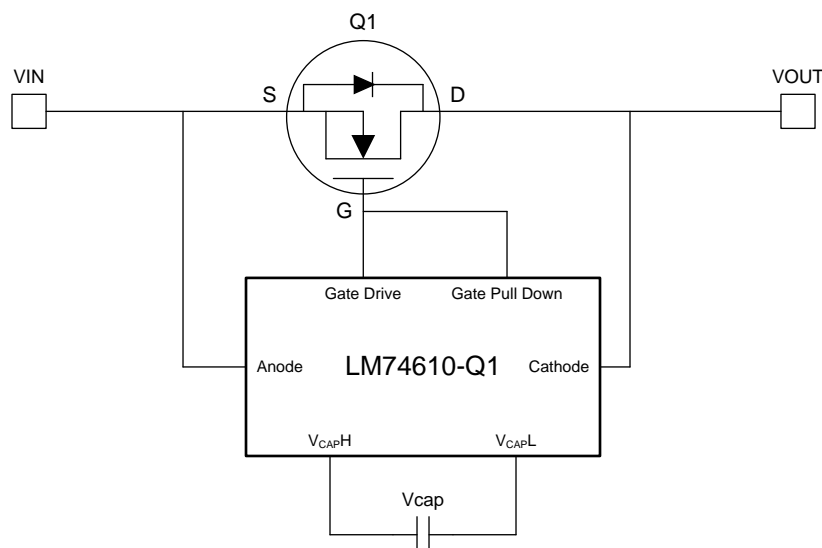
LM74610-Q1 控制器为外部 N 沟道 MOSFET 提供栅极驱动，并配有快速响应内部比较器，可使 MOSFET 栅极在反极性情况下放电。这种快速降压特性有效限制了检测到反极性时反向电流的大小和持续时间。此外，该器件设计选用了合适的 TVS 二极管，符合 CISPR25 5 类 EMI 规范和汽车类 ISO7637 瞬态要求。

#### 器件信息<sup>(1)</sup>

部件号	封装	封装尺寸 (标称值)
LM74610-Q1	VSSOP (8)	3.0mm x 5.0mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

#### 智能二极管配置



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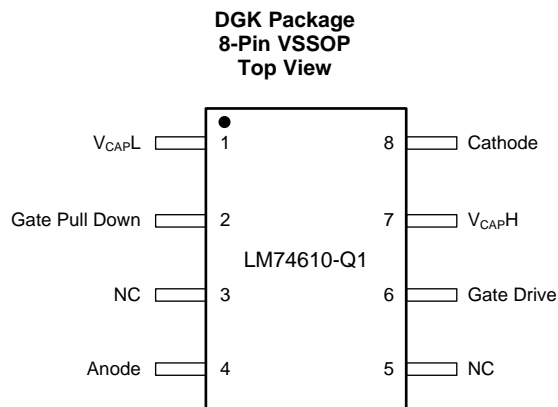
## 4 修订历史记录

### Changes from Original (July 2015) to Revision A

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## 5 Pin Configuration and Functions



### Pin Functions

PIN NO.	NAME	DESCRIPTION
1	VcapL	Charge Pump Output, connect to an external charge pump capacitor
2	Gate Pull Down	Connect to the gate of the external MOSFET for fast turn OFF in the case of reverse polarity
3	NC	No connect. Leave floating or connect to Anode pin
4	Anode	Anode of the diode, connect to source of the external MOSFET
5	NC	No connect. Leave floating or connect to gate drive pin
6	Gate Drive	Gate Drive output, Connect to the Gate of the external MOSFET
7	VcapH	Charge Pump Output, connect to an external charge pump capacitor
8	Cathode	Cathode of the diode, connect to Drain of the external MOSFET

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Cathode to Anode (For a 2ms time duration) <sup>(2), (3)</sup>	-3	45	V
Cathode to Anode (Continuous) <sup>(3)</sup>	-3	42	V
VcapH to VcapL	-0.3	7	V
Anode to VcapL	-0.3	3	V
Gate Drive, Gate Pull Down to VcapL	-0.3	7	V
Ambient Temperature (TA-MAX) <sup>(4)</sup>	-40	125	°C
Case Temperature (TC-MAX)	-40	125	°C
Storage temperature range, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) 42V continuous (and 45V transients for 2ms) absmx condition from Cathode to Anode. Suitable to use with TVS SMBJ28A and SMBJ14A at the anode.
- (3) Reverse voltage rating only. There is no positive voltage limitation for the LM74610-Q1 Anode terminal.
- (4) The device performance is ensured over this Ambient Temperature range as long the Case Temperature does not exceed the MAX value.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge <sup>(1)</sup>	Human body model (HBM), per AEC Q100-002 <sup>(2)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±750
			V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Cathode To Anode			42	V
Ambient Temperature (TA-MAX)	-40		125	°C
Case Temperature (TC-MAX)			125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM74610-Q1 VSSOP 8 PINS	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	181	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	73	
R <sub>θJB</sub>	Junction-to-board thermal resistance	102	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	11	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	100	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Electrical Characteristics

 T<sub>A</sub> = 25°C unless otherwise noted. Minimum and Maximum limits are specified through test, design, validation or statistical correlation. Typical values represent the most likely parametric norm at T<sub>A</sub> = 25°C and are provided for reference purpose only. V<sub>Anode-Cathode</sub> = 0.55V for all tests. <sup>(1)</sup>

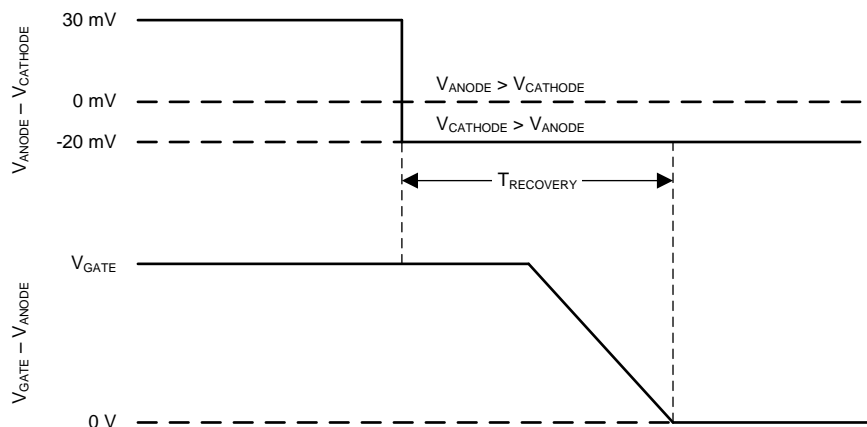
- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the table of Electrical Characteristics.

## Electrical Characteristics (continued)

$T_A = 25^\circ\text{C}$  unless otherwise noted. Minimum and Maximum limits are specified through test, design, validation or statistical correlation. Typical values represent the most likely parametric norm at  $T_A = 25^\circ\text{C}$  and are provided for reference purpose only.  $V_{\text{Anode-Cathode}} = 0.55\text{V}$  for all tests.<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{Anode to Cathode}}$	Minimum Startup Voltage across External MOSFET's Body Diode	External MOSFET $V_{\text{GS}} = 0\text{V}$	0.48			V
$V_{\text{cap}}$ Threshold	Charge Pump Capacitor Drive Thresholds	Vcap Upper Threshold		6.3		V
		Vcap Lower Threshold		5.15		V
$I_{\text{Gate up}}$	Gate Drive Pull up current	$V_{\text{Gate to Anode}} = 2\text{V}$	8.9	9.4		$\mu\text{A}$
$I_{\text{Gate down}}$	Gate Drive pull down current during forward voltage	$V_{\text{Gate to Anode}} = 4\text{V}$	6.35	6.8		$\mu\text{A}$
$I_{\text{Gate pull down}}$	Gate drive pull down current when reverse voltage is sensed	$V_{\text{Gate Pull Down}} = V_{\text{Anode}} + 2\text{V}$		160		mA
$I_{\text{Charge Current}}$	Charging current for the charge pump capacitor	$V_{\text{Anode to Cathode}} = 0.55\text{V}$	40	46		$\mu\text{A}$
$I_{\text{Discharge Current}}$	VCAP Current Consumption to power the controller when MOSFET is ON	$V_{\text{cap}} = 6.6\text{V}$		0.95		$\mu\text{A}$
$T_{\text{Recovery}}$	Time to shut off MOSFET when voltage is reversed (Equivalent to diode reverse recovery time)	$V_{\text{Anode to Cathode}} = -20\text{mV}$ $C_{\text{gate}} = 4\text{nF}$		2.2	5 <sup>(2)</sup>	$\mu\text{s}$
D	Duty Cycle	Iload = 3 A, $T_A = 25^\circ\text{C}$		98%		
		Iload = 3 A, $T_A = 125^\circ\text{C}$		92%		
$I_{\text{LKG}}$	Reverse Leakage Current	$V_{\text{Anode to Cathode}} = -13.5\text{V}$		60	110 <sup>(2)</sup>	$\mu\text{A}$
$I_{\text{q}}$	Quiescent Current to GND			0		$\mu\text{A}$
$I_{\text{Anode}}$	Current into Anode pin	Current into Anode pin when $V_{\text{Anode - Cathode}} = 0.3\text{V}$ .		30		$\mu\text{A}$

(2) Limit applies over the full Operating Temperature Range  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .



**Figure 1. Gate Shut Down Timing in the Event of Reverse Polarity**

## 6.6 Typical Characteristics

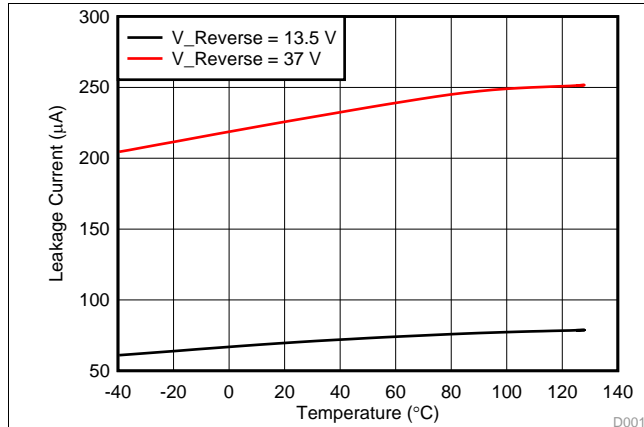


Figure 2. Reverse Leakage at Negative Voltages

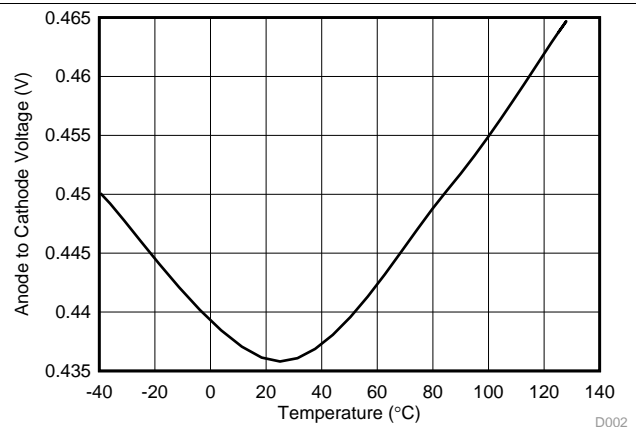


Figure 3. Anode to Cathode Startup Voltage

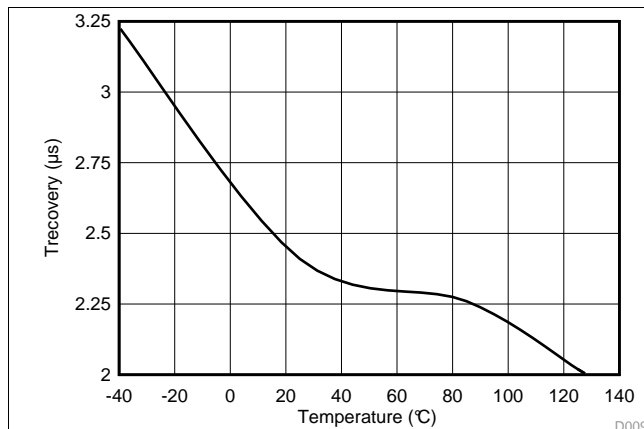


Figure 4. Reverse Recovery Time ( $T_{Recovery}$ )

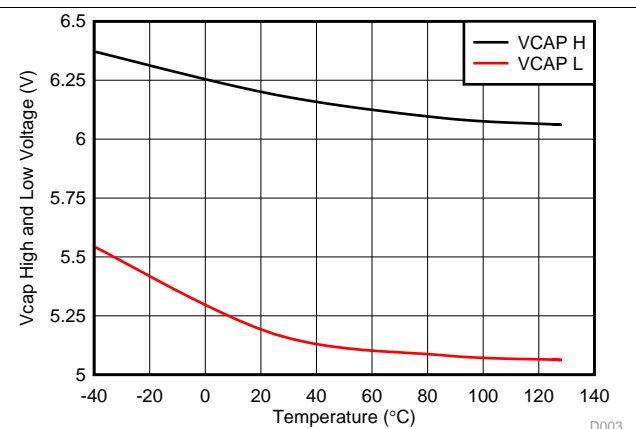


Figure 5. VcapH and VcapL Voltage Threshold

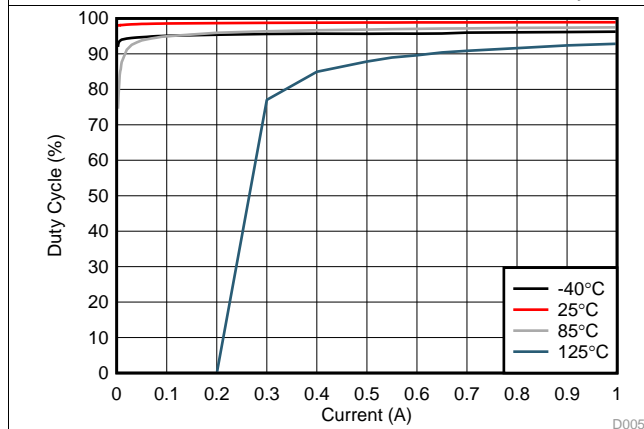


Figure 6. Duty Cycle of the Output Voltage at Startup

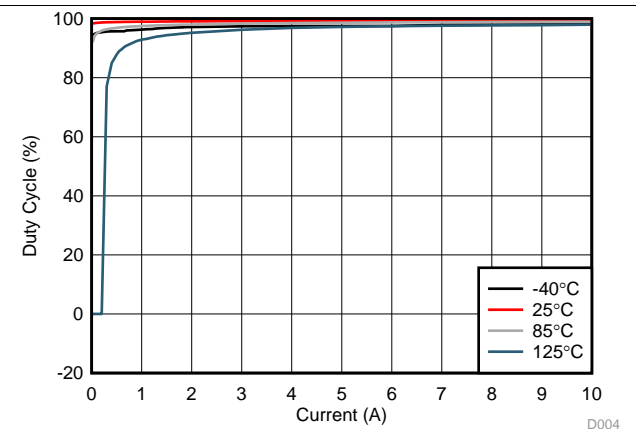


Figure 7. Duty Cycle of the Output Voltage

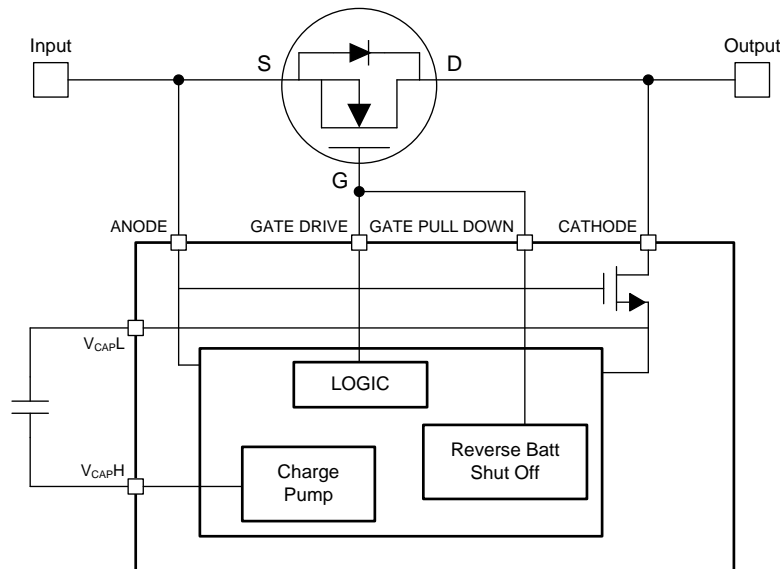
## 7 Detailed Description

### 7.1 Overview

Most systems in automotive or industrial applications require fast response reverse polarity protection at the input stage. Schottky diodes or PFETs are typically used in most power systems to protect the load in case of negative polarity. The disadvantage of using diodes is high voltage drop during forward conduction, which reduces the available voltage and increases the associated power losses. PFET solutions are inefficient for high load current and low input voltage. These situations often occur during start-stop or cold crank. The other disadvantages of PFET include higher  $I_q$  and higher system cost. Using an N-Channel MOSFET with a controller IC can be a highly effective and more efficient substitute in reverse polarity protection circuitry. The ON state forward voltage loss in a MOSFET depends upon the  $R_{DS(ON)}$  of the MOSFET. The power losses become substantially lower than the Schottky diode for the equivalent current. This solution has a small increase in complexity; however it eliminates the need for diode heatsinks or a large thermal copper area in PCB layout for high power applications, that a diode would need.

The LM74610-Q1 is a zero  $I_q$  controller that is combined with an external N-channel MOSFET to replace a diode or PFET reverse polarity solution in power systems. The voltage across the MOSFET source and drain is constantly monitored by the LM74610-Q1 Anode and Cathode pins. An internal charge pump is used to provide the GATE drive for the external MOSFET. The forward conduction is through the MOSFET 98% of the time. The forward conduction is through the MOSFET body diode for 2% of time when energy is stored in an external charge pump capacitor  $V_{cap}$  Figure 9. This stored energy is used to drive the gate of MOSFET. The voltage drop depends on the  $R_{DS(ON)}$  of a particular MOSFET in use, which is significantly smaller than a PFET. The LM74610-Q1 has no ground reference which makes it identical to a diode.

### 7.2 Functional Block Diagram

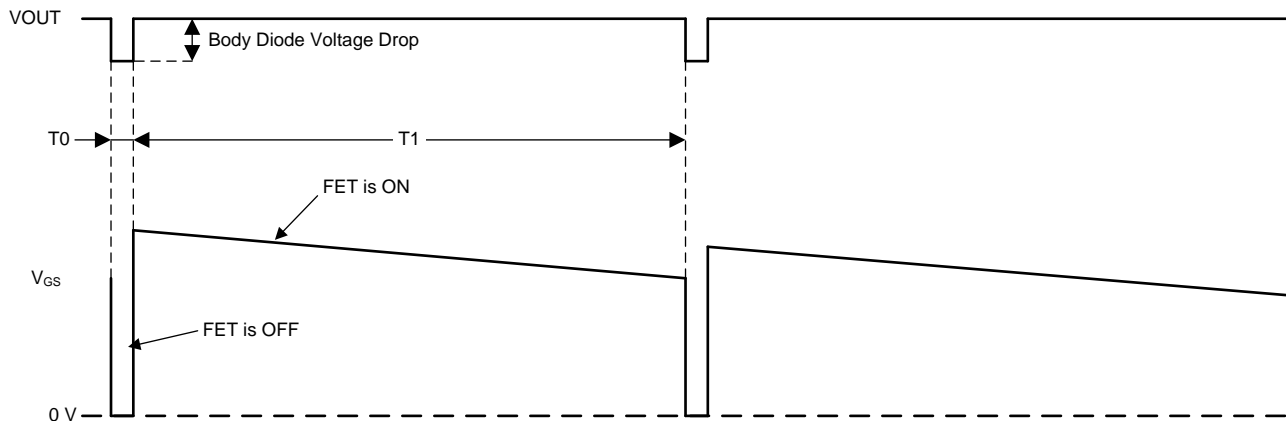


### 7.3 Feature Description

#### 7.3.1 During T0

When power is initially applied, the load current ( $I_D$ ) will flow through the body diode of the MOSFET and produce a voltage drop ( $V_f$ ) during T0 in Figure 8. This forward voltage drop ( $V_f$ ) across the body diode of the MOSFET is used to charge up the charge pump capacitor  $V_{cap}$ . During this time, the charge pump capacitor  $V_{cap}$  is charged to a higher threshold of 6.3V (typical).

## Feature Description (continued)



**Figure 8. Output Voltage and  $V_{GS}$  Operation at 1A Output Current**

### 7.3.2 During T1

Once the voltage on the capacitor reaches a higher voltage level of 6.3V (typical), the charge pump is disabled and the MOSFET turns ON. The energy stored in the capacitor is used to provide the gate drive for the MOSFET (T1 in Figure 8). When the MOSFET is ON, it provides a low resistive path for the drain current to flow and minimizes the power dissipation associated with forward conduction. The power losses during the MOSFET ON state depend primarily on the  $R_{DS(ON)}$  of the selected MOSFET and load current. At time when the capacitor voltage reaches its lower threshold  $V_{capL}$  5.15V (typical), the MOSFET gate turns OFF. The drain current  $I_D$  will then begin to flow through the body diode of the MOSFET, causing the MOSFET body diode voltage drop to appear across Anode and Cathode pins. The charge pump circuitry is re-activated and begins charging the  $V_{cap}$ . The LM74610-Q1 operation keeps the MOSFET ON at approximately 98% duty cycle (typical) regardless of the external charge pump capacitor value. This is the key factor to minimizing the power losses. The forward voltage drop during this time is limited by the  $R_{DS(ON)}$  of the MOSFET.

### 7.3.3 Pin Operation

#### 7.3.3.1 Anode and Cathode Pins

The LM74610-Q1 Anode and Cathode pins are connected to the source and drain of the external MOSFET. The current into the Anode pin is 30  $\mu$ A (typical). When power is initially applied, the load current flows through the body diode of the external MOSFET, the voltage across Anode and Cathode pins is equal to the forward diode drop ( $V_f$ ). The minimum value of  $V_f$  required to enable the charge pump circuitry is 0.48V. Once the MOSFET is turned ON, the Anode and Cathode pins constantly sense the voltage difference across the MOSFET to determine the magnitude and polarity of the voltage across it. When the MOSFET is on, the voltage difference across Anode and Cathode pins depends on the  $R_{DS(ON)}$  and load current. If voltage difference across source and drain of the external MOSFET becomes negative, this is sensed as a fault condition by Anode and Cathode pins and gate is turned off by Gate Pull Down pin as shown in Figure 1. The reverse voltage threshold across Anode and Cathode to detect the fault condition is -20 mV. The consistent sensing of voltage polarity across the MOSFET enables the LM74610-Q1 to provide a fast response to the power source failure and limit the amount and duration of the reverse current flow.

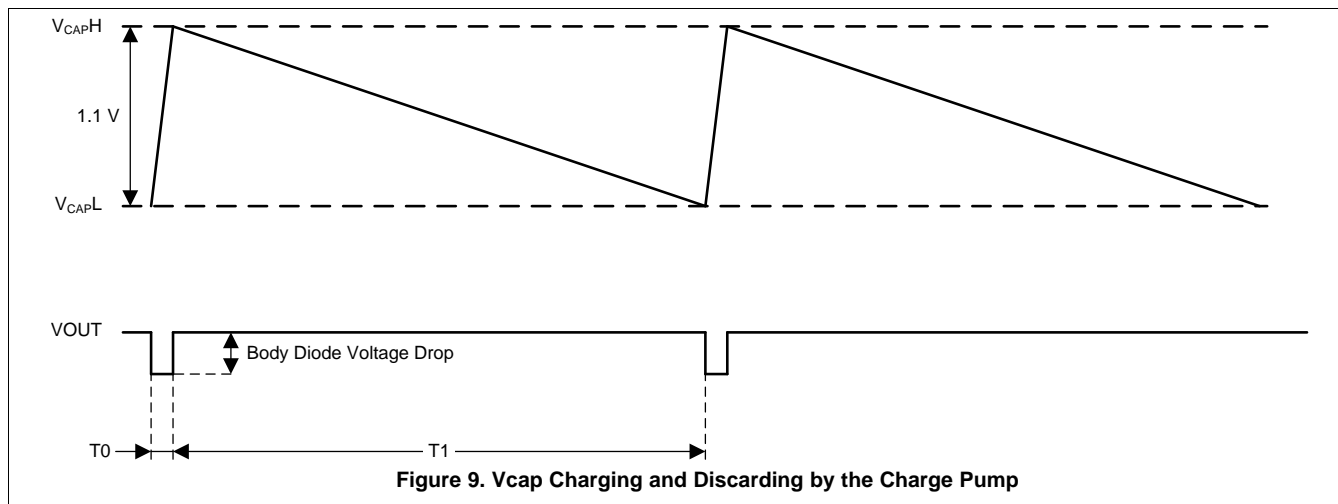
#### 7.3.3.2 $V_{capH}$ and $V_{capL}$ Pins

$V_{capH}$  and  $V_{capL}$  are high and low voltage thresholds respectively that the LM74610-Q1 uses to detect when to turn the charge pump circuitry ON and OFF. The capacitor charging and discharging time can be correlated to the duty cycle of the MOSFET gate. Figure 9 shows the voltage behavior across the  $V_{cap}$ . During the time period T0, the capacitor is storing energy from the charge pump. The MOSFET is turned off and current flow is only through the body diode during this time period. The conduction through body diode of the MOSFET is for a



**Feature Description (continued)**

very small period of time (2% typical) which rules out the chances of overheating the MOSFET, regardless of the output current. Once the capacitor voltage reaches its high threshold, the MOSFET is turned off and charge pump circuitry is deactivated until the Vcap reaches its low voltage threshold (T1). The voltage difference between Vcap high and low threshold is typically 1.15V. The LM74610-Q1 charge pump has 46µA charging capability with 5-8MHz frequency.



**Figure 9. Vcap Charging and Discharging by the Charge Pump**

The Vcap current consumption is 1 µA (typical) to drive the gate. The MOSFET OFF time (T0) and ON time (T1) can be calculated using the following expression

$$\Delta T = C \frac{dV}{dI} \tag{1}$$

**Where:**

- C = Vcap Capacitance
- dV = 1.15V
- dI = 46 µA for charging
- dI = 0.95 µA for discharging

**Note:** Temperature dependence of these parameters – The duty cycle is dependent on temperature since the capacitance variation over temperature has a direct correlation to the MOSFET OFF and ON periods and the frequency. If the capacitor varies 20% the periods and the frequency will also vary by 20% so it is recommended to use a quality X7R/COG cap and not to place the cap in close proximity to high temperature devices. The variation of the capacitor does not have a thermal impact in the application as the duty cycle does not change.

**7.3.3.3 Gate Drive Pin**

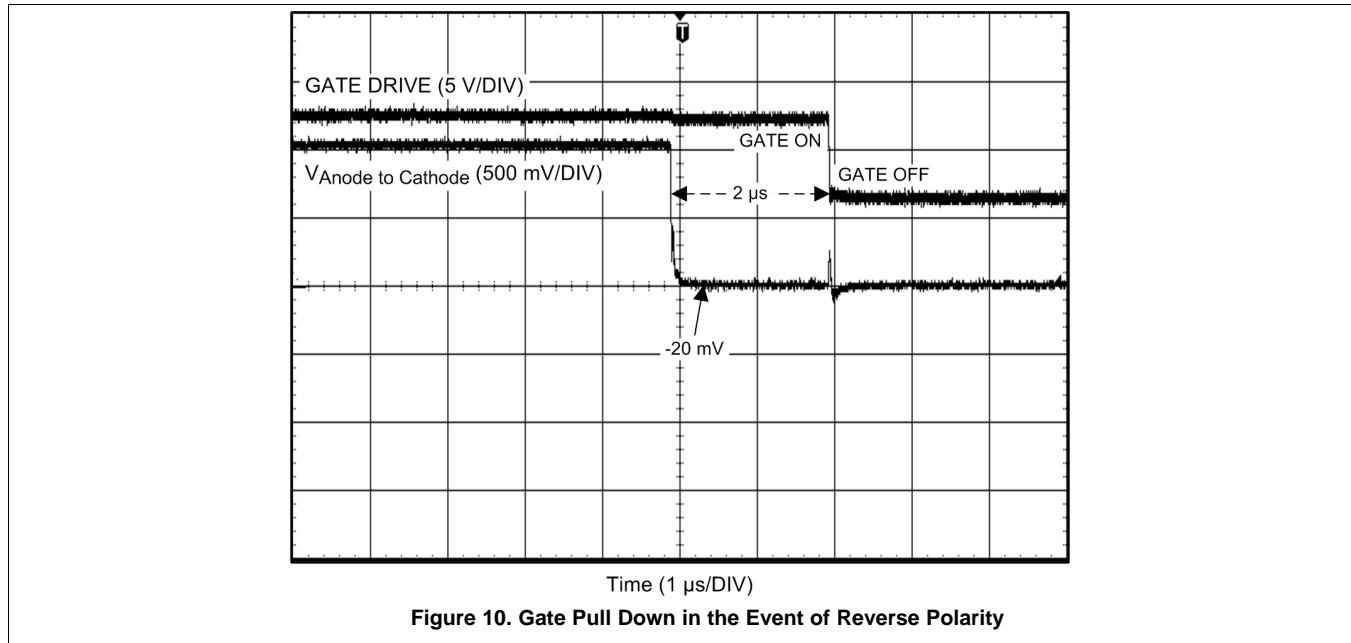
When the charge pump capacitor is charged to the high voltage level of 6.3V (typ), the Gate Drive pin provides a 6.8µA (typ) of drive current. When the charge pump capacitor reaches its lower voltage threshold of 5.15V (typ), Gate is pulled down to the Anode voltage (Vin). When Anode voltage goes negative, the Gate voltage is pulled down to Anode voltage with 160mA pull down current.

**7.3.3.4 Gate Pull Down Pin**

The Gate Pull Down pin is connected to the Gate Drive pin in a typical application circuit. When the controller detects negative polarity, possibly due to failure of the input supply or voltage ripple, the Pull-Down quickly discharges the MOSFET gate through a discharge transistor. This fast pull down react/s regardless of the Vcap charge level. If the input supply abruptly fails, as would happen if the supply gets shorted to ground, a reverse current will temporarily flow through the MOSFET. This reverse current can be due to parallel connected supplies and load capacitance and is dependent upon the R<sub>DS(ON)</sub> of the MOSFET. When the negative voltage across the Anode and Cathode pins due to reverse current reaches -20mV (typical), the LM74610-Q1 immediately reacts

## Feature Description (continued)

and discharges the MOSFET gate capacitance as shown in Figure 10. A MOSFET with 5nF of effective gate capacitance can be turned off by the LM74610-Q1 within 2μs (typical). The fast turnoff time minimizes the reverse current flow from MOSFET drain by opening the circuit. The reverse leakage current does not exceed 110μA for a constant 13.5V reverse voltage across Anode and Cathode pins. The reverse leakage current for a Schottky diode is 15mA under the same voltage and temperature conditions.



## 7.4 Device Functional Modes

The LM74610-Q1 operates in two modes:

- **Body Diode Conduction Mode**

The LM74610-Q1 solution works like a conventional diode during this time with higher forward voltage drop. The power dissipation during this time can be given as:

$$P_{\text{Dissipation}} = (V_{\text{Forward Drop}}) \times (I_{\text{Drain Current}}) \quad (2)$$

However, the current only flows through the body diode while the MOSFET gate is being charged to  $V_{\text{GS(TH)}}$ . This conduction is only for 2% duty cycle, therefore it does not cause any thermal issues.

$$\text{Body Diode ON Time} = \frac{C \times (V_{\text{capH}} - V_{\text{capL}})}{I_{\text{Charge Current}}} \quad (3)$$

- **The MOSFET Conduction Mode**

The MOSFET is turned on during this time and current flow is only through the MOSFET. The forward voltage drop and power losses are limited by the  $R_{\text{DS(ON)}}$  of the specific MOSFET used in the solution. The LM74610-Q1 solution output is comprised of the MOSFET conduction mode for 98% of its duty cycle. This time period is given by the following expression:

$$\text{MOSFET ON Time} = \frac{C \times (V_{\text{capH}} - V_{\text{capL}})}{I_{\text{Discharge Current}}} \quad (4)$$

### 7.4.1 Duty Cycle Calculation

The LM74610-Q1 has an operating duty cycle of 98% at 25 °C and >90% at 125 °C. The duty cycle doesn't depend on the Vcap capacitance value. However, the variation in capacitance value over temperature has direct correlation to the switching frequency between the MOSFET and body diode. If the capacitance value decreases, the charging and discharging time will also decrease, causing more frequent switching between body diode and the MOSFET condition. The following expression can be used to calculate the duty cycle of the LM74610-Q1:

**Device Functional Modes (continued)**

$$\text{Duty Cycle (\%)} = \frac{(\text{MOSFET ON Time})}{(\text{MOSFET ON Time} + \text{Body Diode ON Time})} \times 100 \quad (5)$$

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LM74610-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. This device is connected to the N-Channel MOSFET as shown in Figure 11. The schematic for the typical application is shown in Figure 12 where the LM74610-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS+ and TVS- are not required for the LM74610-Q1. However, they are typically used to clamp the positive and negative voltage surges respectively. The output capacitor  $C_{out}$  is recommended to protect the immediate output voltage collapse as a result of line disturbance.

### 8.2 Typical Application

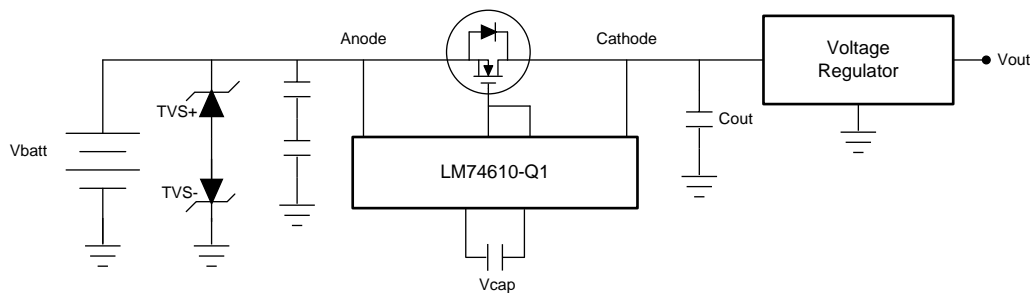


Figure 11. Typical System Application

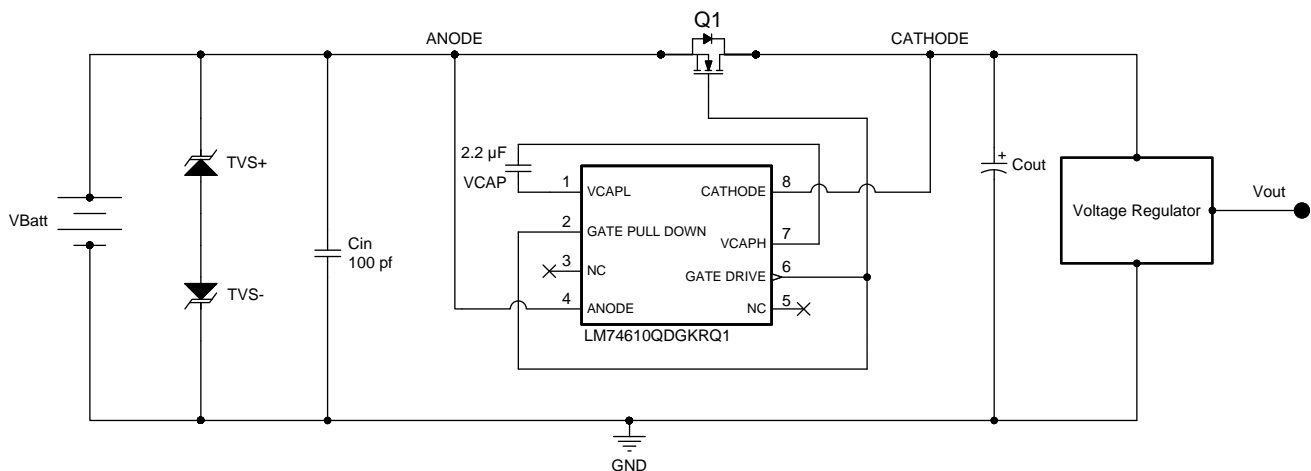


Figure 12. Typical Application Schematic

## Typical Application (continued)

### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	Max $V_{DS}$ of the MOSFET
Output Voltage	Max $V_{DS}$ of the MOSFET
Maximum Negative Voltage	-45V
Output Current Range	Maximum drain current
Transient Response, 3A Load Step	$\Delta V_o = \pm 5\%$

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

#### 8.2.2.1 Design Considerations

- Input voltage range
- Output current range
- Body Diode forward voltage drop for the selected MOSFET
- MOSFET Gate threshold voltage

#### 8.2.2.2 Startup Voltage

The LM74610-Q1 will not initiate the charge pump operation if a closed loop system is in standby mode or the drain current is smaller than 1mA (typical). This is due to a minimum body diode voltage requirement of the LM74610-Q1 controller. If the drain current is too small to produce a minimum voltage drop of 0.48V at 25°C, the charge pump circuitry will remain off and the MOSFET will act just like a diode. It is very important to know the body diode voltage parameter of a MOSFET before implementing it into the Smart Diode solution. Some N-channels MOSFETs have very low body diode voltage at higher temperature. This makes their drain current requirement higher to achieve 0.48V across the body diode in order to initiate the LM74610-Q1 controller at higher temperatures.

#### 8.2.2.3 Capacitor Selection

A ceramic capacitor should be placed between  $V_{capL}$  and  $V_{capH}$ . The capacitor acts as a holding tank to power up the control circuitry when the MOSFET is on.

When the MOSFET is off, this capacitor is charged up to higher voltage threshold of ~6.3V. Once this voltage is reached, the Gate Drive of LM74610-Q1 will provide drive for the external MOSFET. When the MOSFET is ON, the voltage across its body diode is collapsed because the forward conduction is through the MOSFET. During this time, the capacitor acts as a supply for the Gate Drive to keep the MOSFET ON.

The capacitor voltage will gradually decay when the MOSFET is ON. Once the capacitor voltage reaches a lower voltage threshold of 5.15V, the MOSFET is turned off and the capacitor gets recharged again for the next cycle.

A capacitor value of 220nF to 4.7µF with X7R/COG characteristic and 16V rating or higher is recommended for this application. A higher value capacitor sets longer MOSFET ON time and OFF time; however, the duty cycle remains at ~98% for MOSFET ON time irrespective of capacitor value.

If the  $V_{cap}$  value is 2.2µF, the MOSFET ON time and OFF time can be calculated using [Equation 1](#) :

$$\text{MOSFET ON Time} = (2.2\mu\text{F} \times 1.15\text{V}) / 0.95\mu\text{A} = 2.66 \text{ seconds} \quad (6)$$

$$\text{Body Diode ON Time} = (2.2\mu\text{F} \times 1.15\text{V}) / 46\mu\text{A} = 55 \text{ milliseconds} \quad (7)$$

The duty cycle can be calculated using [Equation 5](#) :

$$\text{Duty Cycle \%} = 2.66\text{sec} / (2.66\text{sec} + 0.055\text{sec}) = 98\% \quad (8)$$

### 8.2.2.4 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current  $I_D$ , the maximum drain-to-source voltage  $V_{DS(MAX)}$ , the gate-to-source threshold voltage  $V_{GS(TH)}$  and the drain-to-source On resistance  $R_{DS(ON)}$ . The maximum continuous drain current,  $I_D$ , rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode,  $I_S$ , is typically rated the same as, or slightly higher than the drain current, but body diode current only flows for a small period while the MOSFET gate is being charged to  $V_{GS(TH)}$ . The LM74610-Q1 can provide up to 5V  $V_{GS}$  to drive the external MOSFET, therefore the  $V_{GS}$  threshold of the selected MOSFET must be  $\leq 3V$ .

The voltage across the MOSFET's body diode must be higher than 0.48V at low current. The body diode voltage for MOSFETs typically decreases as the ambient temperature increases. This will increase the source current requirement to achieve the minimum body diode drain-to-source voltage for the charge pump to initiate. The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. Although there are no positive  $V_{DS}$  limitation. However, it is recommended to use MOSFETs with voltage rating up to 45V for automotive applications, since the LM74610-Q1 has a reverse voltage limit of -45V. Table 2 shows the examples of recommended MOSFETs to be used with the LM74610-Q1.

### 8.2.3 Application Curves

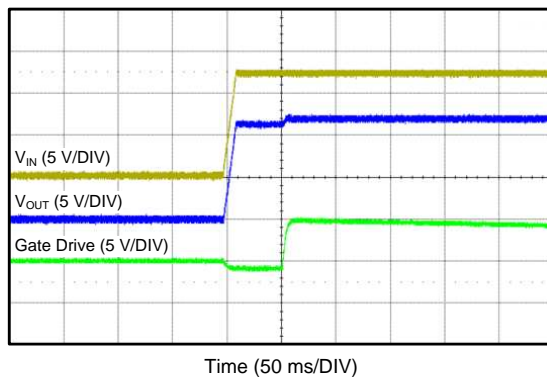


Figure 13. Startup Relative to VIN

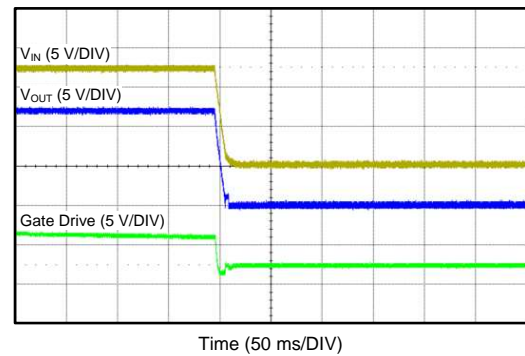


Figure 14. Shutdown Relative to VIN

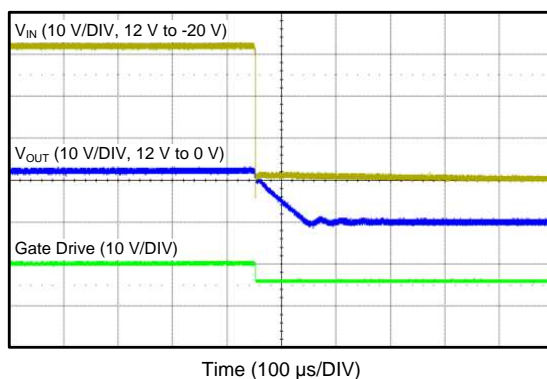


Figure 15. Response to Reverse polarity

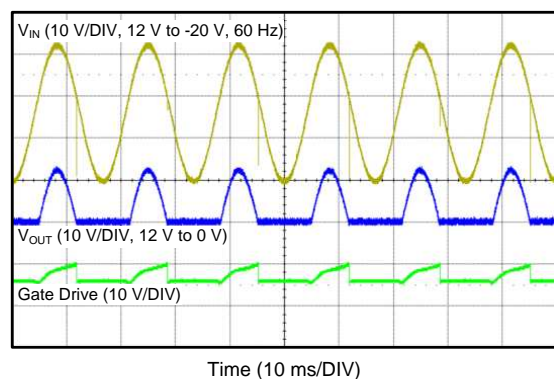
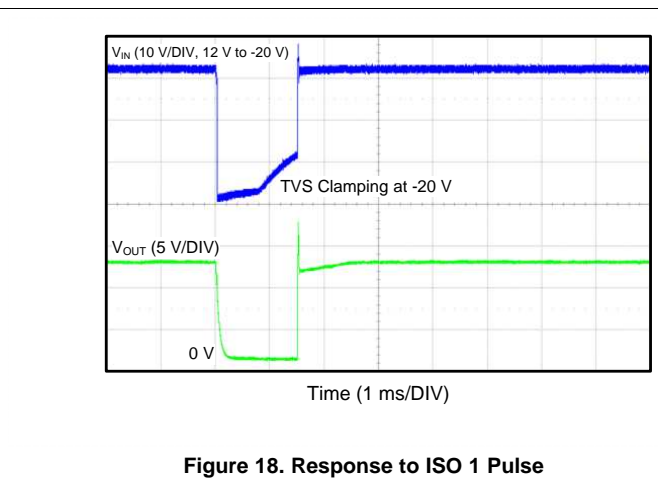
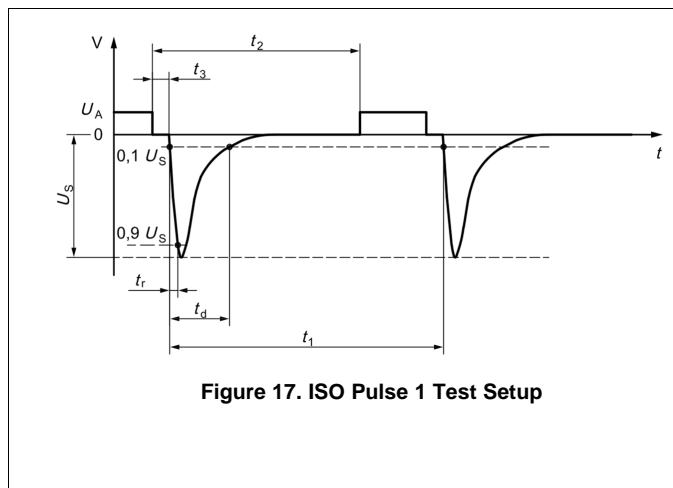


Figure 16. Response to a 60Hz AC Input



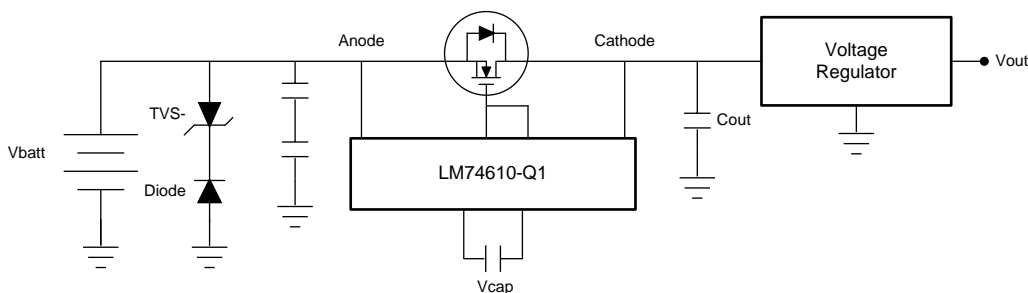
### 8.2.4 Selection of TVS Diodes in Automotive Reverse Polarity Applications

TVS diodes can be used in automotive systems for protection against transients. There are 2 types of TVS diode, one that offers bi-directional clamping and one that is uni-directional. In the application circuit show in Figure 11, 2 unidirectional TVS diodes are used. TVS + does the clamping for positive pulses as seen in load dump and TVS- does the clamping for negative pulses such as seen in the ISO specs.

There are two important specs to be aware of: breakdown voltage and clamping voltage. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typ 1mA. Clamping voltage is the voltage the TVS diode clamps to in high current pulse situations.

In the case of an ISO 7637-2 pulse 1, the voltages go to -150V with a generator impedance of 10Ω. This translates to 15A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage. A rule of thumb with TVS diode voltage selection is that the breakdown voltage should be higher than worst case steady state voltages seen in the system. TVS diodes are meant to clamp pulses and not meant for steady state voltages.

The value of the TVS + is selected such that the breakdown voltage of the TVS is higher than 24V which is a commonly used battery for jump start. LM74610-Q1 does not have a positive voltage limit so the selection of the voltage rating of TVS + is determined by the max voltage tolerated by the downstream electronics. If the downstream parts can withstand at least 37V (suppressed load dump) then there is no need to use the TVS+. In this case it can be replaced with a diode as seen in Figure 19. A 1A diode with a 30A surge current rating and at least 40V reverse voltage rating is recommended. In case positive clamping voltage is desired then SMBJ24A/SMBJ26A is recommended for TVS + as seen in Figure 11.



**Figure 19. Typical Application without Positive Voltage Clamping**

The value of the TVS - is selected such that 2 criteria are met. The breakdown voltage of the TVS should be higher than the max reverse battery voltage which is typically 15V. The second criterion is that the abs max rating for reverse voltage of the LM74610 is not exceeded (-45V).

In case of reverse voltage pulses such as in ISO specs, the LM74610 turns the MOSFET off. When the MOSFET turns off the voltage seen by the LM74610, Anode to Cathode is - (clamping voltage of TVS- (plus) the output capacitor voltage). If the max voltage on output capacitors is 16V, then the clamping voltage of the TVS- should not exceed,  $45V - 16V = 29V$ .

SMBJ14A/SMBJ15A/SMBJ16A TVS diodes can be used for TVS-. The breakdown voltage of SMBJ14A is 15.6V and SMBJ16A is 17.8V. This meets criteria one. The clamping voltage of SMBJ14A is 23.2V and SMBJ16A is 26V. This meets the second criteria.

Bi-directional TVS diodes are not recommended due to their symmetrical clamping specs. SMBJ24CA has a breakdown voltage of 26.7V and a clamping voltage of 38.9V. The breakdown voltage meets the criteria for being higher than 24V. However the clamping voltage is 38.9V. The high clamping voltage is not an issue for the positive pulses however for a negative ISO pulse, the abs max of the LM74610 can be violated. Voltage across Anode to Cathode in this case is  $-(38.9V + 16V) = -54.9V$  which violates abs max rating of -45V.

As far as power levels for TVS diodes the 'B' in the SMBJ stands for 600W peak power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump case (ISO-16750-2 pulse B). For unsuppressed load dumps (ISO-16750-2 pulse A) higher power TVS diodes such as SMCJ or SMDJ may be required.

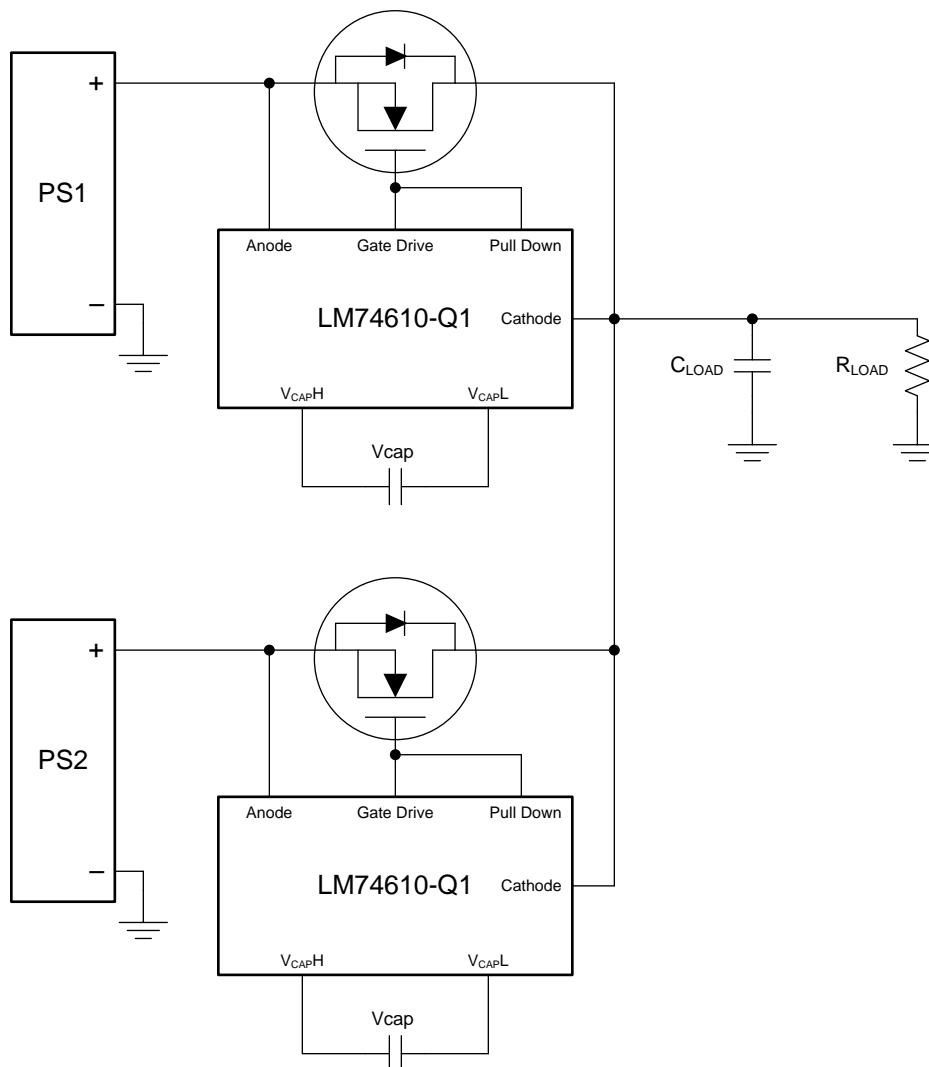
### 8.2.5 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In its simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, since each diode in an OR-ing application spends most of its time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74610-Q1 ICs combined with external N-Channel MOSFETs can be used to in OR-ing Solution as shown in [Figure 20](#). The source to drain voltage  $V_{DS}$  for each MOSFET is monitors by the Anode and Cathode pins of the LM74610-Q1. The forward conduction is through MOSFETs 98% of the time which avoids the diode forward voltage drop. The body diode of each MOSFET only conducts the remaining 2% of the time to allow the charge pump capacitor to be fully charged.

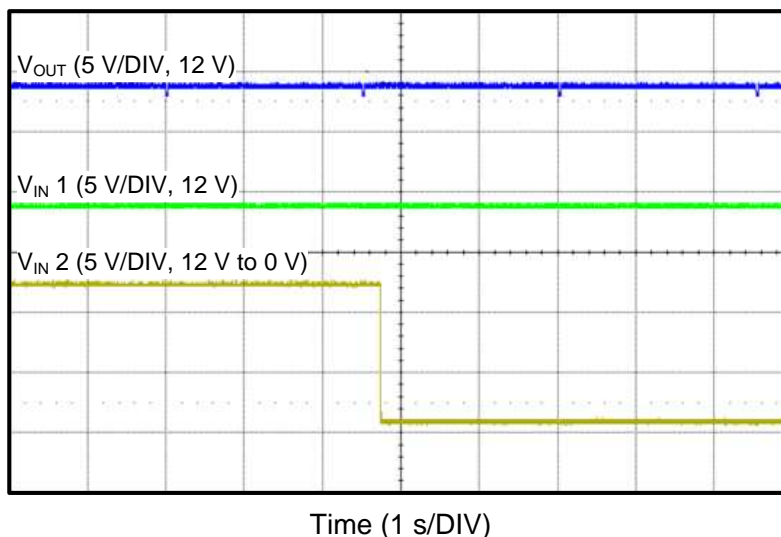
This is essential for an OR-ing device to fast detect the reverse current and instantly pull-down the MOSFET gate to block the reverse current flow. An effective OR-ing solution needs to be extremely fast to limit the reverse current amount and duration. The LM74610-Q1 devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (PS1, PS2) and the common load point respectively. When either of the power sources operates at lower voltage, the LM74610-Q1 detects a negative polarity and shuts down the Gate Drive through a fast Pull-Down within 2 $\mu$ sec (typical).





**Figure 20. Typical OR-ing Application**

If one of the power supplies fails in LM74610-Q1 OR-ing controller application, the output remains uninterrupted. This behavior is similar to diode OR-ing. [Figure 21](#)


**Figure 21. LM74610-Q1 OR-ing waveform**

### 8.2.6 Design Requirements

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**NOTE**

Startup voltage is the voltage drop is needed for the controller to turn ON. It directly influences the Minimum output current at which the MOSFET turns ON.

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**Table 2. Recommended MOSFET Examples<sup>(1)</sup>**

Part No	Voltage (V) Current	Drain Current at 25C	R <sub>dson</sub> mΩ @ 4.5V	V <sub>gs</sub> Threshold(V)	Diode voltage @ 2A at 125C/175C	Package; Footprint	Qual
CSD17313Q2 Q1	30	5	26	1.8	0.65	SON; 2 x 2	Auto
SQJ886EP	40	60	5.5	2.5	0.5	PowerPAK SO-8L; 5 x 6	Auto
SQ4184EY	40	29	5.6	2.5	0.5	SO-8; 5 x 6	Auto
Si4122DY	40	23.5	6	2.5	0.5	SO-8; 5 x 6	Auto
RS1G120MN	40	12	20.7	2.5	0.6	HSOP8; 5 x 6	Auto
RS1G300GN	40	30	2.5	2.5	0.5	HSOP8; 5 x 6	Auto
CSD18501Q5 A	40	22	3.3	2.3	0.53	SON; 5 x 6	Industrial
SQD40N06-14L	60	40	17	2.5	0.5	TO-252; 6 x 10	Auto
SQ4850EY	60	12	31	2.5	0.55	SO-8; 5 x 6	Auto
CSD18532Q5 B	60	23	3.3	2.2	0.53	SON; 5 x 6	Industrial
IPG20N04S4 L-07A	40	20	7.2	2.2	0.48	PG-TDSON-8-10; 5 x 6	Auto
IPB057N06N	60	45	5.7	3.3	0.55	PG-TO263-3; 10 x 15	Auto
IPD50N04S4 L	40	50	7.3	2.2	0.50	PG-TO252-3-313; 6 x 10	Auto

(1) The LM74610-Q1 solution is not limited to the MOSFETs included in this table. It only shows examples of compatible MOSFETs.

**Table 2. Recommended MOSFET Examples<sup>(1)</sup> (continued)**

Part No	Voltage (V) Current	Drain Current at 25C	Rdson mΩ @ 4.5V	Vgs Threshold (V)	Diode voltage @ 2A at 125C/175C	Package; Footprint	Qual
BUK9Y3R5-40E	40	100	3.8	2.1	0.48	LFPK56; Power-SO8 (SOT669); 5 x 6	Auto
IRF7478PbF-1	60	7	30	3	0.55	SO-8; 5 x 6	Industrial
SQJ422EP	40	75	4.3	2.5	0.50	PowerPAK SO-8L; 5 x 6	Auto
IRL1004	40	130	6.5	1	0.60	TO-220AB	Auto
AUIRL7736	40	112	2.2	3	0.65	DirectFET®; 5 x 6	Auto

**Table 3. Recommended TVS Combination to meet ISO7637 Specifications (Note 4)**

TVS +	TVS-
SMA6T33AY	SMBJ14A/ SMA6T15AY
SMA6T30AY	SMBJ14A/ SMA6T15AY
SMA6T28AY	SMBJ14A/ SMA6T15AY

## 9 Power Supply Recommendations

While testing the LM74610-Q1 solution, it is important to use low impedance power supply which allows current sinking. If the power supply does not allow current sinking, it would prevent the current flow in the reverse direction in the event of reverse polarity. The MOSFET gate won't get pulled down immediately due to the absence of reverse current flow.

## 10 Layout

### 10.1 Layout Guidelines

- The VIN terminal is recommended to have a low-ESR ceramic bypass-capacitor. The typical recommended bypass capacitance is a 10- $\mu$ F ceramic capacitor with a X5R or X7R dielectric.
- The VIN terminal must be tied to the source of the MOSFET using a thick trace or polygon.
- The Anode pin of the LM74610-Q1 is connected to the Source of the MOSFET for sensing.
- The Cathode pin of the LM74610-Q1 is connected to the drain of the MOSFET for sensing.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick traces for source and drain of the MOSFET.
- The charge pump capacitor Vcap must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate Drive and Gate pull down pins of the LM74610-Q1 must be connected to the MOSFET gate without using vias.
- Obtaining acceptable performance with alternate layout schemes is possible, however this layout has been shown to produce good results and is intended as a guideline.

10.2 Layout Example

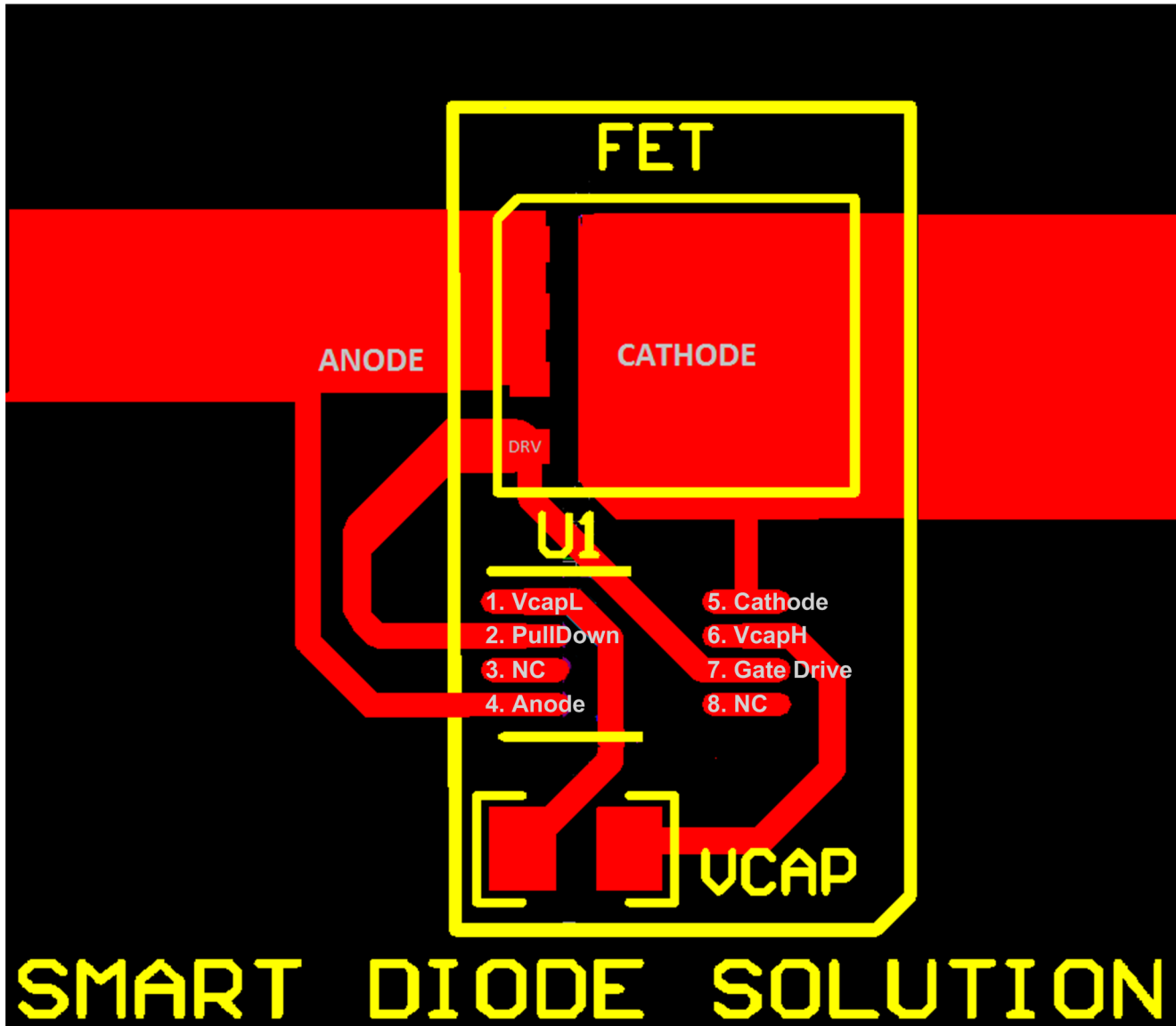


Figure 22. Layout Example

## 11 器件和文档支持

### 11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 11.2 商标

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### 11.3 静电放电警告



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### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74610QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDSK	<a href="#">Samples</a>
LM74610QDGKTQ1	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDSK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74610QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74610QDGKTQ1	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM74610QDGKTQ1	VSSOP	DGK	8	250	178.0	13.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74610QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM74610QDGKTQ1	VSSOP	DGK	8	250	210.0	185.0	35.0
LM74610QDGKTQ1	VSSOP	DGK	8	250	213.0	191.0	50.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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