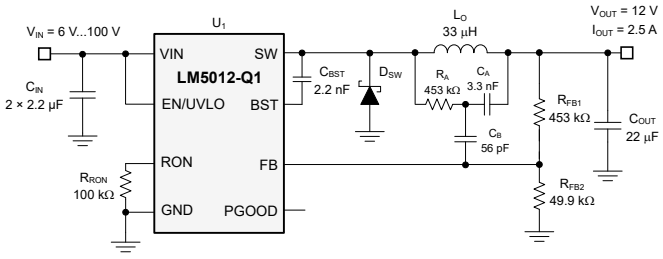
LM5012-Q1 具有超低 I_Q 的汽车类 100V 输入、2.5A 非同步直流/直流降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 +125°C 的环境温度范围
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 专为可靠耐用的应用而设计
  - 6V 至 100V 的宽输入电压范围
  - 具有 –40°C 至 +150°C 的结温范围
  - 固定 3.5 ms 内部软启动计时器
  - 峰值电流限制保护
  - 输入 UVLO 和热关断保护
- 针对超低 EMI 要求进行了优化
  - 符合 CISPR 25 5 类标准
- 适用于可扩展的汽车电源
  - 与 LM5163-Q1 和 LM5164-Q1（100V、0.5A 或 1A）以及 LM5013-Q1（100V、3.5A）引脚对引脚兼容
  - 最短导通时间和关闭时间低至 50 ns
  - 10 µA 空载睡眠电流
  - 3.1 µA 关断静态电流
- 通过集成技术减小解决方案尺寸，降低成本
  - COT 模式控制架构
  - 集成 100V、0.25 Ω 功率 MOSFET
  - 1.2V 内部电压基准
  - 无环路补偿组件
  - 内部 VCC 偏置稳压器和自举二极管
- 使用 WEBENCH® Power Designer 并借助 LM5013-Q1 创建定制稳压器设计

2 应用

- 混合动力、电动和动力总成系统
- 逆变器和电机控制
- 48V 至 12V 直流/直流转换器



典型应用，$V_{IN(nom)}$ = 48V、V_{OUT} = 12V、$I_{OUT(max)}$ = 2.5A、$F_{SW(nom)}$ = 300kHz

3 说明

LM5012-Q1 非同步降压转换器用于在宽输入电压范围内进行调节，从而更大限度地减少对外部浪涌抑制元件的需求。50ns 的最短可控导通时间有助于实现较大的降压转换比，支持从 48V 标称输入到低电压轨的直接降压转换，从而降低系统的复杂性并减少解决方案成本。LM5012-Q1 能够在输入电压突降至 6V 时根据需要以接近 100% 的占空比继续工作，因而是高性能 48V 电池汽车应用和 MHEV/EV 系统的理想选择。

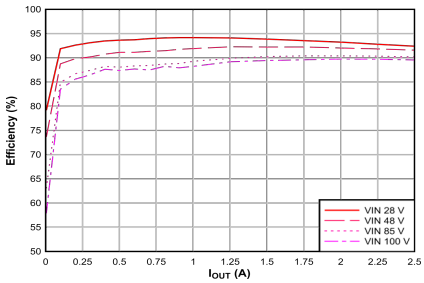
LM5012-Q1 具有集成式高侧功率 MOSFET，可提供高达 2.5A 的输出电流。恒定导通时间 (COT) 控制架构可提供几乎恒定的开关频率，具有出色的负载和线路瞬态响应。LM5012-Q1 的其他特性包括超低 I_Q 运行（可实现较高的轻负载效率）、创新的峰值过流保护、集成式 VCC 偏置电源和自举二极管、精密使能和输入 UVLO 以及具有自动恢复功能的热关断保护。开漏 PGOOD 指示器可提供进行定序、故障报告和输出电压监视功能。

LM5012-Q1 2.5A 符合汽车 AEC-Q100 1 级标准，采用 8 引脚 SO PowerPAD™ 集成电路封装。该器件的 1.27mm 引脚间距可以为高电压应用提供足够的间距。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
LM5012-Q1	DDA（SO PowerPAD，8）	4.89mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用效率，V_{OUT} = 12V

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2022	*	Initial Release

5 Device Comparison Table

Device	Description	Orderable Part Number	Package	V_{IN}	I_{OUT}
LM5163-Q1	Automotive 100-V input, 0.5-A synchronous buck converter	LM5163QDDARQ1	SO PowerPAD (8) integrated circuit package	100 V	0.5 A
LM5164-Q1	Automotive 100-V input, 1-A synchronous buck converter	LM5164QDDARQ1	SO PowerPAD (8) integrated circuit package	100 V	1 A
LM5012-Q1	Automotive 100-V, 2.5-A non-synchronous buck converter	LM5012QDDARQ1	SO PowerPAD (8) integrated circuit package	100 V	2.5 A
LM5012	100-V input, 2.5-A non-synchronous buck converter	LM5012DDAR	SO PowerPAD (8) integrated circuit package	100 V	2.5 A
LM5013-Q1	Automotive, 100-V, 3.5-A non-synchronous buck converter	LM5013QDDARQ1	SO PowerPAD (8) integrated circuit package	100 V	3.5 A
LM5013	100-V, 3.5-A non-synchronous buck converter	LM5013DDAR	SO PowerPAD (8) integrated circuit package	100 V	3.5 A

6 Pin Configuration and Functions

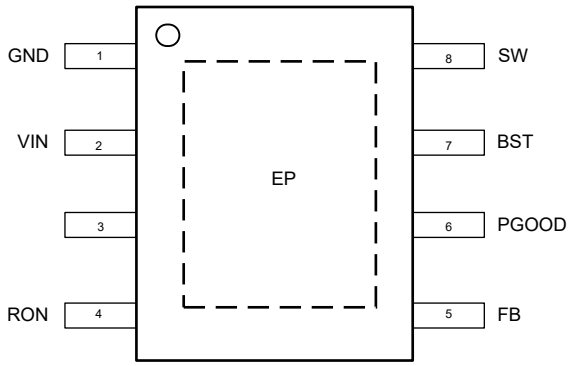


图 6-1. 8-Pin SO PowerPAD™ Integrated Circuit Package DDA Package (Top View)

表 6-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
GND	1	G	Ground connection for internal circuits
VIN	2	P	Regulator supply input pin to high-side power MOSFET and internal bias regulator. Connect directly to the input supply of the buck converter with short, low impedance paths.
EN/UVLO	3	I	Precision enable and undervoltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below 1.1 V, the converter is in shutdown mode with all functions disabled. If the UVLO voltage is greater than 1.1 V and below 1.5 V, the converter is in standby mode with the internal VCC regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
RON	4	I	On-time programming pin. A resistor between this pin and GND sets the buck switch on time.
FB	5	I	Feedback input of voltage regulation comparator
PGOOD	6	O	Power-good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10 kΩ to 100 kΩ.
BST	7	P	Bootstrap gate-drive supply. Required to connect a high-quality 2.2-nF, 50-V X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
SW	8	P	Switching node that is internally connected to the source of the high-side NMOS buck switch. Connect to the switching node of the power inductor and Schottky diode.
EP	—	—	Exposed pad of the package. No internal electrical connection. Connect the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN to GND	–0.3	100	V
Pin voltage	SW to GND	–1.5	100	V
Pin voltage	SW to GND, <20-ns transient	–3		V
Pin voltage	BST to GND	–3	105.5	V
Pin voltage	BST to SW	–0.3	5.5	V
Pin voltage	EN/UVLO to GND	–0.3	100	V
Pin voltage	FB, RON to GND	–0.3	5.5	V
Pin voltage	PGOOD to GND	–0.3	14	V
Boostrap capacitor	External BST to SW capacitor	1.5	2.5	nF
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent damage to the device. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operation Condition. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 (1) HBM ESD Classification Level 2		±2000	V
		Charge device model (CDM), per AEC-Q100-011, CDM ESD Classification Level C4B	All pins except corner pins	±500	V
			Corner pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

Over the operating junction temperature range (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage voltage range		6		100	V
	Pin voltage	SW to GND	–0.3		100	V
	Pin voltage	BST to GND	–0.3		105.5	V
	Pin voltage	BST to SW	–0.3		5.5	V
	Pin voltage	FB, RON to GND	–0.3		5.5	V
	Pin voltage	EN/UVLO to GND	–0.3		100	V
	PGOOD to GND		–0.3		14	V
I_{OUT}	Output current range			2	2.5	A
	F_{SW}				1000	kHz
t_{ON}	Programmable on-time		50		1000	ns
C_{BST}	External BST to SW capacitance		1.5	2.2	2.5	nF
T_J	Operating junction temperature		-40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		DDA (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (LM5013-Q1 EVM)	29.0	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{IN} = 24 V. Typical values are at T_J = 25°C and $V_{EN/UVLO}$ = 2 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{Q-SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$ = 0V		3.1	9.9	µA
$I_{Q-SLEEP}$	VIN sleep current	V_{EN} = 2.5 V, V_{FB} = 1.5 V, V_{BST} – V_{SW} = 5 V, non-switching		10	20	µA
$I_{Q-STANDBY}$	VIN standby current	V_{EN} = 1.2 V		25	40	µA
$I_{Q-ACTIVE}$	VIN Active current	V_{EN} = 2.5 V		450		µA
EN/UVLO						
$V_{SD-RISING}$	Shutdown threshold				1.1	V
$V_{SD-FALLING}$	Shutdown threshold		0.45			V
$V_{EN-RISING}$	EN threshold rising		1.43	1.5	1.6	V
$V_{EN-FALLING}$	EN threshold falling		1.35	1.4	1.47	V
FEEDBACK VOLTAGE						
V_{REF}	FB regulation voltage		1.181	1.2	1.218	V
TIMING						
t_{ON1}	On-time1	V_{VIN} = 12 V, R_{RON} = 75 kΩ		2550		ns
t_{ON2}	On-time2	V_{VIN} = 12 V, R_{RON} = 25 kΩ		830		ns

7.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C, V_{IN} = 24 V. Typical values are at T_J = 25°C and $V_{EN/UVLO}$ = 2 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON3}	On-time3	V_{VIN} = 48 V, R_{RON} = 75 kΩ		625		ns
t_{ON4}	On-time4	V_{VIN} = 48 V, R_{RON} = 25 kΩ		245		ns
t_{ON5}	On-time5	V_{VIN} = 100 V, R_{RON} = 75 kΩ		330		ns
t_{ON6}	On-time6	V_{VIN} = 100 V, R_{RON} = 25 kΩ		128		ns
PGOOD						
V_{PG-UTH}	FB upper threshold for PGOOD low to high	V_{FB} rising	1.1	1.14	1.2	V
V_{PG-LTH}	FB lower threshold for PGOOD high to low	V_{FB} falling	1.05	1.08	1.12	V
V_{PG-HYS}	PGOOD upper and lower threshold hysteresis	V_{FB} falling		60		mV
R_{PG}	PGOOD pulldown resistance	V_{FB} = 1 V		8		Ω
BOOTSTRAP						
V_{BST-UV}	Gate drive UVLO	V_{BST} falling		2.4	3.4	V
POWER SWITCH						
$R_{DSON-HS}$	High-side MOSFET R_{DSON}	I_{SW} = –100 mA		0.25		Ω
SOFT START						
t_{SS}	Internal soft-start		1.75	3.5	4.75	ms
CURRENT LIMIT						
I_{PEAK}	Peak current limit threshold		2.8	3.2	3.6	A
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			10		°C

(1) Specified by design. Not product tested.

7.6 Typical Characteristics

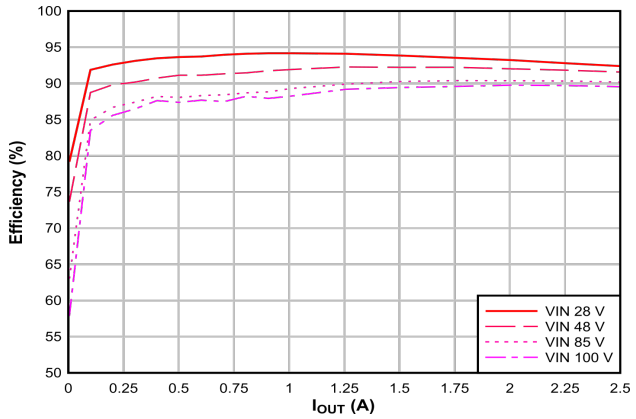


图 7-1. Conversion Efficiency (Linear Scale)

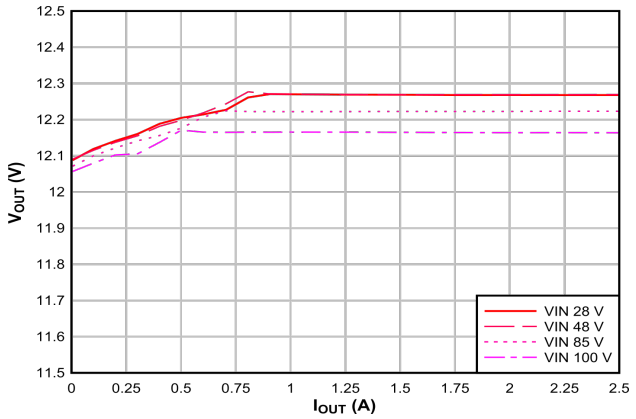


图 7-2. Load and Line Regulation

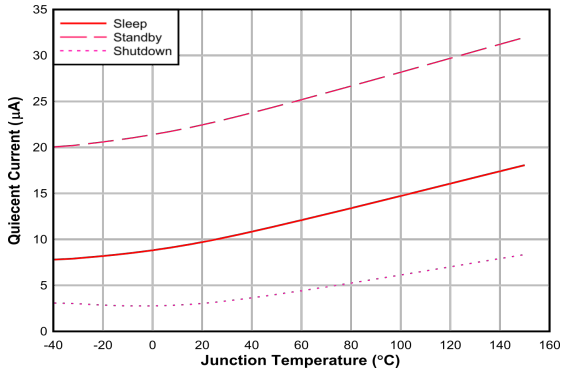


图 7-3. Shutdown, Sleep, and Supply Current Versus Temperature

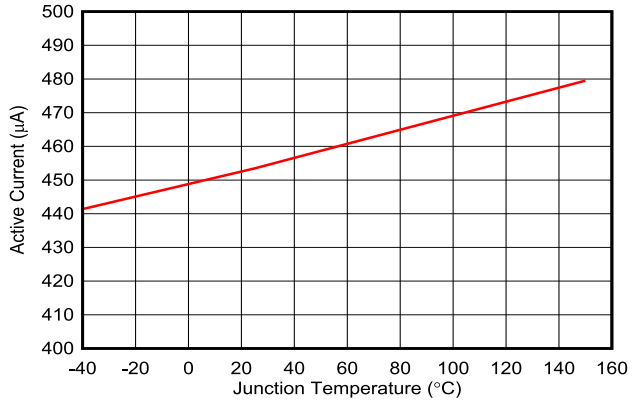


图 7-4. V_{IN} Active Current Versus Temperature

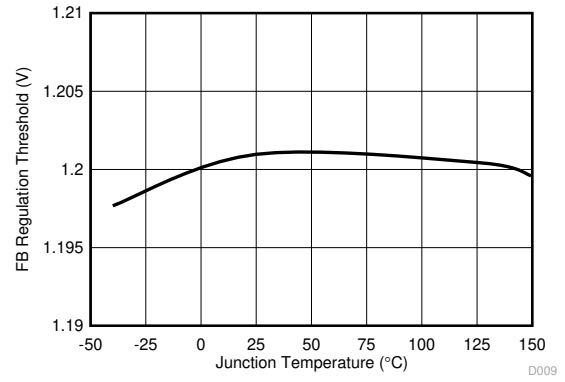


图 7-5. Feedback Comparator Threshold Versus Temperature

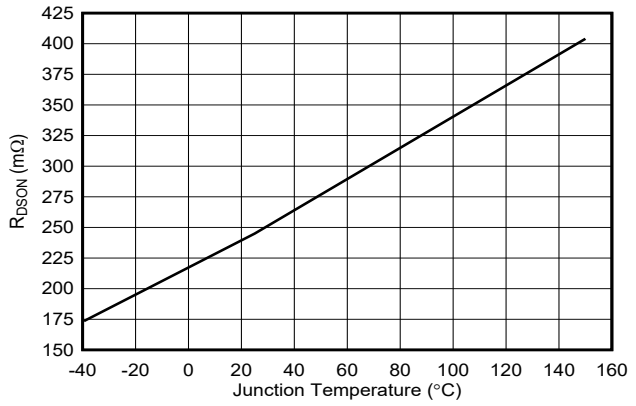


图 7-6. MOSFETs On-State Resistance Versus Temperature

7.6 Typical Characteristics (continued)

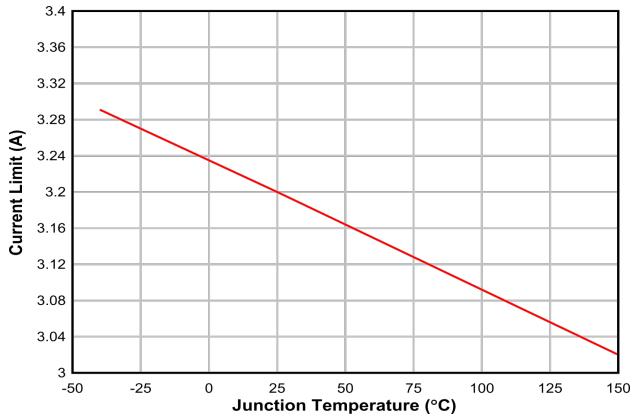


图 7-7. Peak Current Limit Versus Temperature

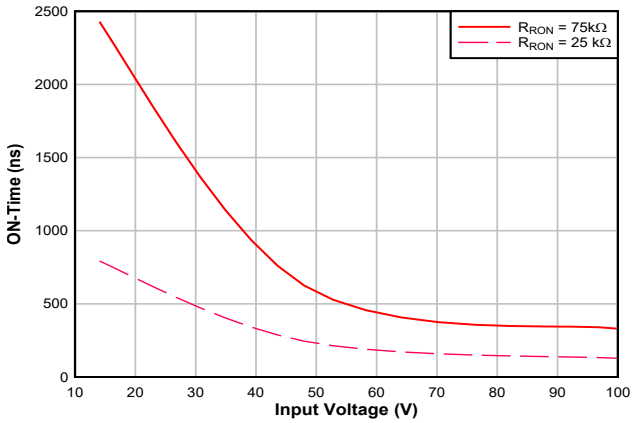


图 7-8. COT On Time Versus V_{IN}

8 Detailed Description

8.1 Overview

The LM5012-Q1 is an easy-to-use, ultra-low I_Q constant on-time (COT) non-synchronous step-down buck regulator. With an integrated high-side power MOSFET, the LM5012-Q1 is a low-cost, highly efficient buck converter that operates from a wide input voltage of 6 V to 100 V, delivering up to 2.5-A DC load current. The LM5012-Q1 is available in an 8-pin SO PowerPAD integrated circuit package with 1.27-mm pin pitch for adequate spacing in high-voltage applications. This constant on-time (COT) converter is ideal for low-noise, high-current, and fast load transient requirements, operating with a adaptive on-time switching pulse. Over the input voltage range, input voltage feedforward is used to achieve a quasi-fixed switching frequency. A controllable on time as low as 50 ns permits high step-down ratios and a minimum forced off time of 50 ns provides extremely high duty cycles, allowing V_{IN} to drop close to V_{OUT} before frequency foldback occurs. At light loads, the device transitions into an ultra-low I_Q mode to maintain high efficiency and prevents draining battery cells connected to the input when the system is in standby. The LM5012-Q1 implements a peak current limit detection circuit to ensure robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count.

The LM5012-Q1 incorporates additional features for comprehensive system requirements:

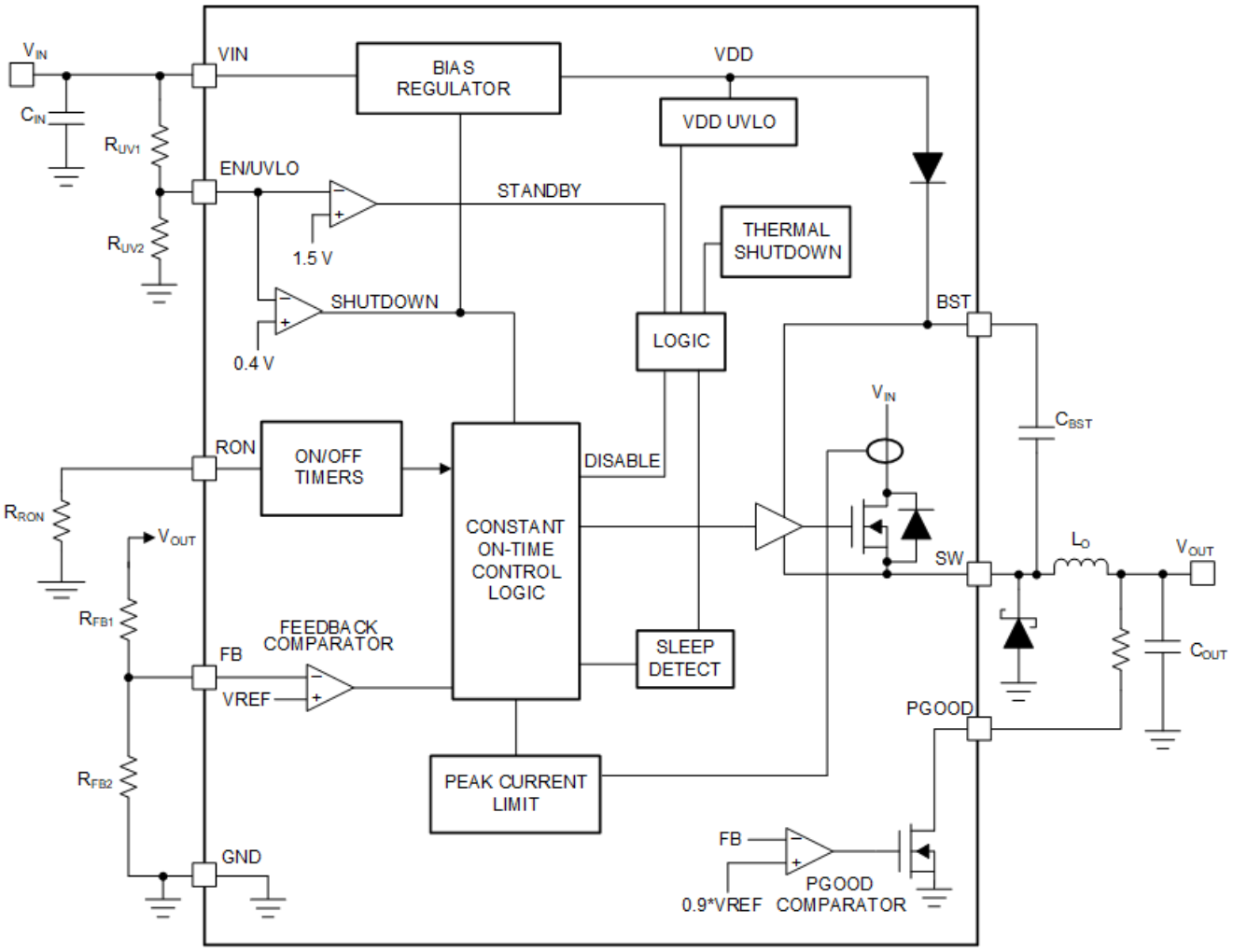
- Power-rail sequencing and fault reporting
- Internally-fixed soft start
- Open-drain power good
- Monotonic start-up into prebiased loads
- Precision enable for programmable line undervoltage lockout (UVLO)
- Smart cycle-by-cycle current limit for optimal inductor sizing
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The LM5012-Q1 supports a wide range of end-equipment systems requiring a regulated output from a high input supply where the transient voltage deviates from the DC level. The following are examples of such end equipment systems:

- 48-V automotive systems
- High cell-count battery-pack systems
- Hybrid, electric, and powertrain systems
- Inverter and motor control

The pin arrangement is designed for a simple layout requiring only a few external components.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Architecture

The LM5012 step-down switching converter employs a constant on-time (COT) control scheme. The COT control scheme sets a fixed on time, t_{ON}, of the high-side FET using a timing resistor (R_{ON}). t_{ON} is adjusted as V_{IN} changes and is inversely proportional to the input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After t_{ON} expires, the high-side FET remains off until the feedback pin is equal or below the 1.2-V reference voltage. To maintain stability, the feedback comparator requires a minimal ripple voltage that is in-phase with the inductor current during the off time. Furthermore, this change in feedback voltage during the off time must be large enough to dominate any noise present at the feedback node. The minimum recommended feedback ripple voltage is 20 mV. See 表 8-1 for different types of ripple injection schemes that ensure stability over the full input voltage range.

During a rapid start-up or a positive load step, the regulator operates with minimum off times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady-state operation, the off time automatically adjusts itself to produce the SW-pin duty cycle required for output voltage regulation to maintain a fixed switching frequency. In CCM, the switching frequency, F_{SW}, is programmed by the R_{RON} resistor. Use 方程式 1 to calculate the switching frequency.

$$F_{SW}(kHz) = \frac{V_{OUT}(V) \cdot 2500}{R_{RON}(k\Omega)} \quad (1)$$

表 8-1. Ripple Generation Methods

Type 1	Type 2	Type 3
Lowest Cost	Reduced Ripple	Minimum Ripple
$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$	$R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}}$ $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$	$C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ $R_A C_A \leq \frac{(V_{IN\text{-}nom} - V_{OUT}) \cdot t_{ON\,(@V_{IN\text{-}nom})}}{20mV}$ $C_B \geq \frac{t_{TR\text{-}settling}}{3 \cdot R_{FB1}}$

表 8-1 presents three different methods for generating appropriate voltage ripple at the feedback node. Type-1 ripple generation method uses a single resistor, R_{ESR}, in series with the output capacitor. The generated voltage ripple has two components: capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance, R_{ESR}. The capacitive ripple component is out-of-phase with the inductor current and does not decrease monotonically during the off time. The resistive ripple component is in-phase with the inductor current and decreases monotonically during the off time. The resistive ripple must exceed the capacitive ripple at V_{OUT} for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession followed by a long off time. The lowest cost bill of materials (BOM) define the value of the series resistance R_{ESR} to ensure sufficient in-phase ripple at the feedback node.

Type-2 ripple generation uses a C_{FF} capacitor in addition to the series resistor. As the output voltage ripple is directly AC-coupled by C_{FF} to the feedback node, the R_{ESR} and ultimately the output voltage ripple, are reduced by a factor of V_{OUT} / V_{FB1}.

Type-3 ripple generation uses an RC network consisting of R_A and C_A, and the switch node voltage to generate a triangular ramp that is in-phase with the inductor current. This triangular wave is the AC-coupled into the feedback node with capacitor C_B. Because this circuit does not use output voltage ripple, it is suited for applications where low output voltage ripple is critical. The *Selecting an Ideal Ripple Generation Network for Your COT Buck Converter* application report provides additional details on this topic.

备注

For all methods specified, 12 mV is the minimum FB ripple voltage. 20 mV is calculated as a conservative figure. For wide-V_{IN} ranges, calculating for 20 mV can be insufficient to achieve 12-mV FB ripple at minimum input voltage. Careful evaluation should be done to ensure the minimum ripple requirement is fulfilled, or the design can be faced with large output ripple, irregular switching at the application minimum output voltage.

8.3.2 Internal VCC Regulator and Bootstrap Capacitor

The LM5012-Q1 contains an internal linear regulator that is powered from VIN with a nominal output of 5 V, eliminating the need for an external capacitor to stabilize the linear regulator. The internal VCC regulator supplies current to internal circuit blocks including the non-synchronous FET driver and logic circuits. The input pin (VIN) can be connected directly to line voltages up to 100 V. As the power MOSFET has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. It is required to select a high-quality ceramic bootstrap capacitor with an effective value of 2.2-nF, 50-V X7R as specified in the *Absolute Maximum Ratings*. VCC does not have current limit protection, so selecting a higher value capacitance stresses the internal VCC regulator and can damage the device. A lower capacitance than required is not sufficient to drive the internal gate of the power MOSFET. An internal diode connects from the VCC regulator to the BST pin to replenish the charge in the high-side gate drive bootstrap capacitor when the SW voltage is low.

8.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.2-V reference. The LM5012-Q1 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF}. A resistor divider programs the ratio from output voltage, V_{OUT}, to FB.

For a target V_{OUT} setpoint, use 方程式 2 to calculate R_{FB2} based on the selected R_{FB1}.

$$R_{FB2} = \frac{1.2\,V}{V_{OUT} - 1.2\,V} \cdot R_{FB1} \tag{2}$$

TI recommends selecting R_{FB1} in the range of 100 kΩ to 1 MΩ for most applications. A larger R_{FB1} consumes less DC current, which is mandatory if light-load efficiency is critical. R_{FB1} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. Make sure to route the feedback trace away from the noisy area of the PCB and minimize the feedback node size. Route the feedback trace away from the noisy areas of the PCB and minimize the feedback node size. FB resistors, type 3 ripple injection resistors, or both must be kept close to the device pin.

8.3.4 Internal Soft Start

The LM5012-Q1 employs an internal soft-start control ramp that allows the output voltage to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. The soft-start feature produces a controlled, monotonic output voltage start-up. The soft-start time is internally set to 3.5 ms.

8.3.5 On-Time Generator

The on time of the LM5012-Q1 high-side FET is determined by the R_{RON} resistor and is inversely proportional to the input voltage, V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Use 方程式 3 to calculate the on time.

$$t_{ON}\,(\mu s) = \frac{R_{RON}\,(k\Omega)}{V_{IN}\,(V) \cdot 2.5} \tag{3}$$

Use 方程式 4 to determine the R_{RON} resistor to set a specific switching frequency in CCM.

$$R_{RON}\,(k\Omega) = \frac{V_{OUT}\,(V) \cdot 2500}{F_{SW}\,(kHz)} \tag{4}$$

Select R_{RON} for a minimum on time (at maximum V_{IN}) greater than 50 ns for proper operation. In addition to this minimum on time, the maximum frequency for this device is limited to 1 MHz.

8.3.6 Current Limit

The LM5012-Q1 manages overcurrent conditions with cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold (3.2 A). There is a 100-ns leading-edge blanking time following the high-side MOSFET turn-on transition to eliminate false tripping off the current limit comparator. To protect the converter from potential current runaway conditions, the LM5012-Q1 includes a t_{OFF} timer that is proportional to V_{IN} and V_{OUT} that is enabled if a 3.2-A peak current limit is detected. As shown in 图 8-1, if the peak current in the high-side MOSFET exceeds 3.2 A (typical), the present cycle is immediately terminated regardless of the programmed on time (t_{ON}), the high-side MOSFET is turned off and the t_{OFF} timer is activated. This action allows the peak inductor current to fall from 3.2-A peak to an acceptable value to ensure no excessive current in the power stage. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 3.2 A to ensure proper short-circuit and heavy-load protection of the LM5012-Q1. This innovative current limit

scheme enables ultra-low duty-cycle operation, permitting large step-down voltage conversions while ensuring robust protection of the converter.

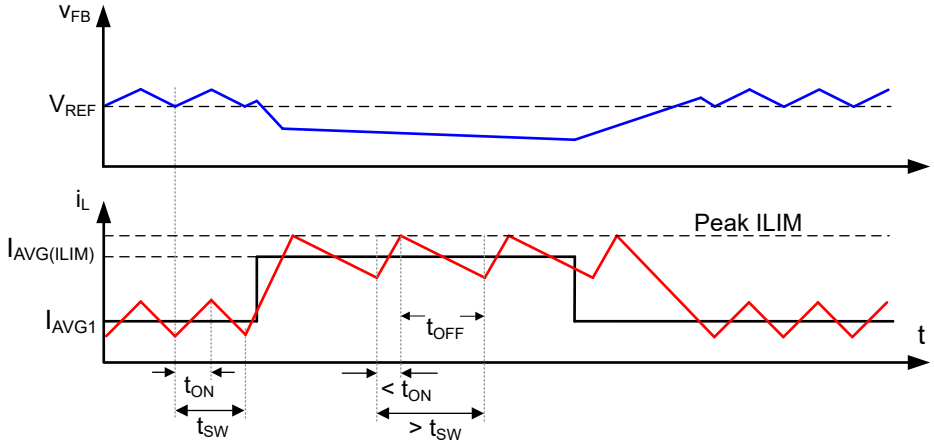


图 8-1. Current Limit Timing Diagram

8.3.7 N-Channel Buck Switch and Driver

The LM5012-Q1 integrates an N-channel buck switch and an associated floating high-side gate driver. The gate-driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage bootstrap diode. A high-quality 2.2-nF, 50-V X7R ceramic capacitor connected between the BST and SW pins provides the voltage to the high-side driver during the buck switch on time. During the off time, the SW pin is pulled down to approximately 0 V, and the bootstrap capacitor charges from the internal VCC through the internal bootstrap diode. The minimum off timer, set to 50 ns (typical), ensures a minimum time each cycle to recharge the bootstrap capacitor. When the on time is less than 300 ns, the minimum off timer is forced to 250 ns to ensure that the BST capacitor is charged in a single cycle. This is vital during wake-up from sleep mode when the BST capacitor is most likely discharged.

8.3.8 Schottky Diode Selection

A Schottky diode is required for all LM5012-Q1 applications to re-circulate the energy in the output inductor when the high-side MOSFET is off. The reverse breakdown rating of the diode must be greater than the maximum V_{IN} plus a 25% safety margin, as specified in 节 9. The current rating of the diode must exceed the maximum DC output current and support the peak current limit (IPEAK current limit) for the best reliability. In this case, the diode carries the maximum load current.

8.3.9 Enable/Undervoltage Lockout (EN/UVLO)

The LM5012-Q1 contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 1.1 V (typical), the converter is in a low-current shutdown mode and the input quiescent current (I_Q) is dropped down to 3 µA. When the voltage is greater than 1.1 V but less than 1.5 V (typical), the converter is in standby mode. In standby mode, the internal bias regulator is active while the control circuit is disabled. When the voltage exceeds the rising threshold of 1.5 V (typical), normal operation begins. Install a resistor divider from VIN to GND to set the minimum operating voltage of the regulator. Use 方程式 5 and 方程式 6 to calculate the input UVLO turn-on and turn-off voltages, respectively.

$$V_{IN(on)} = 1.5\,V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (5)$$

$$V_{IN(off)} = 1.4\,V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (6)$$

TI recommends selecting R_{UV1} in the range of no more than 1 MΩ for most applications. A larger R_{UV1} consumes less DC current, which is mandatory if light-load efficiency is critical. If input UVLO is not required, the power-supply designer can either drive EN/UVLO as an enable input driven by a logic signal or connect it directly to VIN. If EN/UVLO is directly connected to VIN, the regulator begins switching as soon as the internal bias rails are active.

8.3.10 Power Good (PGOOD)

The LM5012-Q1 provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 14 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. When the FB voltage exceeds 95% of the internal reference, V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 90% of V_{REF}, an internal 8-Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

8.3.11 Thermal Protection

The LM5012-Q1 includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 175°C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The LM5012-Q1 initiates a restart sequence when the junction temperature falls to 165°C, based on a typical thermal shutdown hysteresis of 10°C. This is a non-latching protection, so the device cycles into and out of thermal shutdown if the fault persists.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

EN/UVLO provides ON and OFF control for the LM5012-Q1. When $V_{EN/UVLO}$ is below approximately 1.1 V, the device is in shutdown mode. Both the internal linear regulator and the switching regulator are off. The quiescent current in shutdown mode drops to 3 µA at V_{IN} = 24 V. The LM5012-Q1 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below the UV threshold, the regulator remains off.

8.4.2 Standby Mode

The LM5012-Q1 enters standby mode during light or no-load on the output. The LM5012-Q1 enters standby mode to prevent draining the input power supply. All internal controller circuits are turned off to reduce the current consumption. The quiescent current in standby mode is 25 µA (typical).

8.4.3 Active Mode

The LM5012-Q1 is in active mode when $V_{EN/UVLO}$ is above the precision enable threshold and the internal bias rail is above its UV threshold. In COT active mode, the LM5012-Q1 is in one of three modes depending on the load current:

- CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
- The LM5012-Q1 enters discontinuous conduction mode when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation.
- Current limit CCM with peak current limit protection when an overcurrent condition is applied at the output

8.4.4 Sleep Mode

During discontinuous conduction mode, the load current is lower than half of the peak-to-peak inductor current ripple and the switching frequency decreases when the load is further decreased in pulse skipping mode. A switching pulse is set when V_{FB} drops below 1.2 V.

As the frequency of operation decreases and V_{FB} remains above 1.2 V (V_{REF}) with the output capacitor sourcing the load current for greater than 15 µs, the converter enters an ultra-low I_Q sleep mode to prevent draining the input power supply. The input quiescent current (I_Q) required by the LM5012-Q1 decreases to 10 µA in sleep mode, improving the light-load efficiency of the regulator. In this mode, all internal controller circuits are turned off to ensure very low current consumption by the device. Such low I_Q renders the LM5012-Q1 as the best option to extend operating lifetime for off-battery applications. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference, V_{REF}, and the converter transitions out of sleep mode into active mode. There is a 9-µs wake-up delay from sleep to active states.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LM5012-Q1 requires only a few external components to step down from a wide range of supply voltages to a fixed output voltage. Several features are integrated to meet system design requirements, including the following:

- Precision enable
- Input voltage UVLO
- Internal soft start
- Programmable switching frequency
- A PGOOD indicator

To expedite the process of designing with LM5012-Q1, a LM5012-Q1 design calculator is available on the product folder under the *Design tools & simulation* section. This calculator is complemented by an evaluation module for order, PSPICE models, as well as TI's WEBENCH® Power Designer.

9.2 Typical Application

图 9-1 shows the schematic for 48-V to 12-V conversion.

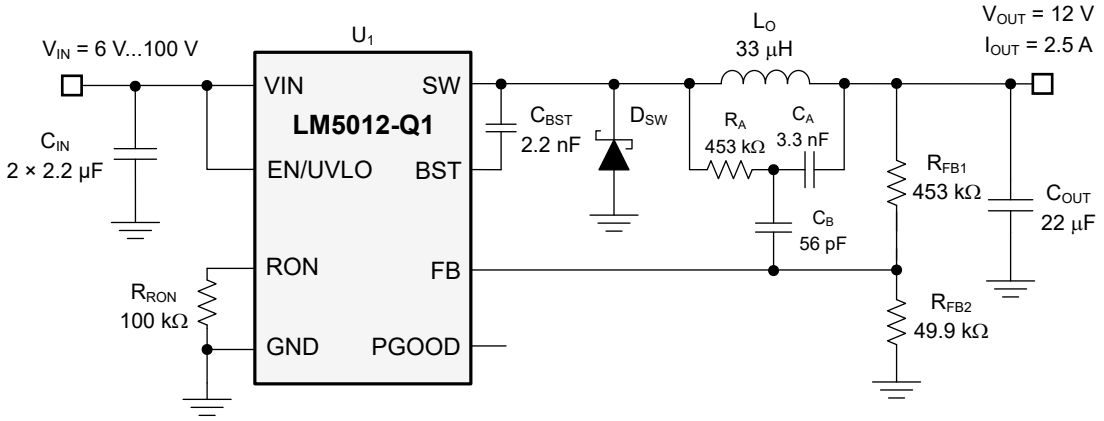


图 9-1. Typical Application, $V_{IN(nom)}$ = 48 V, V_{OUT} = 12 V, $I_{OUT(max)}$ = 2.5 A, $F_{SW(nom)}$ = 300 kHz

备注

This and subsequent design examples are provided herein to showcase the LM5012-Q1 converter in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See the *Power Supply Recommendations* for more details.

9.2.1 Design Requirements

The target full-load efficiency is 92% based on a nominal input voltage of 48 V and an output voltage of 12 V. The required input voltage range is 15 V to 100 V. The switching frequency is set by resistor R_{ON} at 300 kHz. The output voltage soft-start time is 3.5 ms. Refer to *Detailed Design Procedure* for more details on component selection.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5012-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Switching Frequency (R_{RON})

The switching frequency of the LM5012-Q1 is set by the on-time programming resistor placed at R_{RON}. As shown by 方程式 7, a standard 100-kΩ, 1% resistor sets the switching frequency at 300 kHz.

$$R_{RON}(k\Omega) = \frac{V_{OUT}(V) \cdot 2500}{F_{SW}(kHz)} \tag{7}$$

Note that at very low duty cycles, the 50-ns minimum controllable on time of the high-side MOSFET, $t_{ON(min)}$, limits the maximum switching frequency. In CCM, $t_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. Use 方程式 8 to calculate the minimum controllable duty cycle.

$$D_{MIN} = t_{ON(min)} \cdot F_{SW} \tag{8}$$

Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size, and efficiency. Use 方程式 9 to calculate the maximum supply voltage for a given $t_{ON(min)}$ before switching frequency reduction occurs.

$$V_{IN(max)} = \frac{V_{OUT}}{t_{ON(min)} \cdot F_{SW}} \tag{9}$$

9.2.2.3 Buck Inductor (L_O)

Use 方程式 10 and 方程式 11 to calculate the inductor ripple current (assuming CCM operation) and peak inductor current, respectively.

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L_O} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{10}$$

$$I_{L(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \tag{11}$$

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the rated load current at nominal input voltage. Use 方程式 12 to calculate the inductance.

$$L_O = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \quad (12)$$

For applications in which the device must support input transients exceeding 72 V, TI advises to select the inductor to be at least 22 µH. This action ensures that excessive current rise does not occur in the power stage due to the large inductor current slew that can occur during an output short-circuit condition.

Choosing a 33-µH inductor in this design results in 909-mA peak-to-peak ripple current at a nominal input voltage of 48 V, equivalent to 36% of the 2.5-A rated load current. For designs that must operate up to the maximum input voltage at the full-rated load current of 2.5 A, the inductance must increase to ensure current limit (I_{PEAK} current limit) is not hit.

Check the inductor data sheet to make sure the saturation current of the inductor is well above the current limit setting of the LM5012-Q1. TI recommends that the saturation current be greater than 4.5 A. Ferrite-core inductors have relatively lower core losses and are preferred at high switching frequencies, but exhibit a hard saturation characteristic — the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, and reduced efficiency, in turn compromising reliability. Note that inductor saturation current levels generally decrease as the core temperature increases.

9.2.2.4 Output Capacitor (C_{OUT})

Select a ceramic output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that is generated from the triangular inductor current ripple flowing into and out of the capacitor. Select an output capacitance using 方程式 13 to limit the voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \cdot V_{OUT(ripple)}} \quad (13)$$

Substituting $\Delta I_{L(nom)}$ of 909-mA gives C_{OUT} greater than 7 µF. Considering the voltage coefficients of ceramic capacitors, a 22-µF, 25-V rated capacitor with X7R dielectric is selected.

9.2.2.5 Input Capacitor (C_{IN})

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck power stage at every switching cycle. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5012-Q1. The input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform.

Along with the ESR-related ripple component, use 方程式 14 to calculate the peak-to-peak ripple voltage amplitude.

$$V_{IN(ripple)} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (14)$$

Use 方程式 15 to calculate the input capacitance required for a load current, based on an input voltage ripple specification (ΔVIN).

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot \left(V_{IN(ripple)} - I_{OUT} \cdot R_{ESR}\right)} \quad (15)$$

The recommended high-frequency input capacitance is 4.4 µF or higher. Ensure the input capacitor is a high-quality X7S or X7R ceramic capacitor with sufficient voltage rating for C_{IN}. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating preferably twice the maximum input voltage. Additionally, some bulk capacitance can required for large input loop inductance or long wire harnesses used in the system. This capacitor provides parallel damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics. See the *Power Supply Recommendations* for more detail.

9.2.2.6 Type 3 Ripple Network

A Type 3 ripple generation network uses an RC filter consisting of R_A and C_A across SW and V_{OUT} to generate a triangular ramp that is in-phase with the inductor current. This triangular ramp is then AC-coupled into the feedback node using capacitor C_B as shown in 图 9-1. Type 3 ripple injection is suited for applications where low output voltage ripple is crucial.

Use 方程式 16 and 方程式 17 to calculate R_A and C_A to provide the required ripple amplitude at the FB pin.

$$C_A \geq \frac{10}{F_{SW} \cdot \left(R_{FB1} \| R_{FB2}\right)} \tag{16}$$

For the feedback resistors R_{FBT} = 453 kΩ and R_{FBB} = 49.9 kΩ values shown in 图 9-1, 方程式 16 dictates a minimum C_A of 742 pF. In this design, a 3300-pF capacitance is chosen. This is done to keep R_A within practical limits between 100 kΩ and 1 MΩ when using 方程式 17.

$$R_a \times C_a \leq \frac{\left(V_{IN(nom)} - V_{OUT}\right) \times t_{ON(nom)}}{20mV} \tag{17}$$

Based on C_A set at 3.3 nF, R_A is calculated to be 453 kΩ to provide a 20-mV ripple voltage at FB. The general recommendation for a Type 3 network is to calculate R_A and C_A to get 20 mV of ripple at typical operating conditions. A smaller R_A can be required to operate below nominal 48-V input.

备注

12 mV of FB ripple or more must be ensured at the minimum input voltage of the design to ensure stability.

While the amplitude of the generated ripple does not affect the output voltage ripple, it impacts the output regulation as it reflects as a DC error of approximately half the amplitude of the generated ripple. For example, a converter circuit with Type 3 network that generates a 40-mV ripple voltage at the feedback node has approximately 10-mV worse load regulation scaled up through the FB divider to V_{OUT} than the same circuit that generates a 20-mV ripple at FB. Use 方程式 18 to calculate the coupling capacitance, C_B.

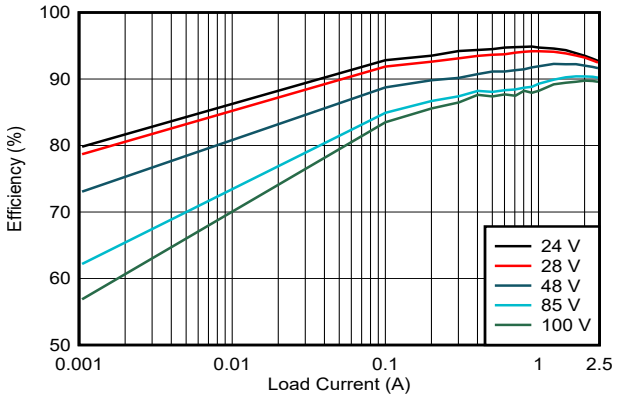
$$C_B \geq \frac{t_{TR\text{-}settling}}{3 \cdot R_{FB1}} \tag{18}$$

where

- $t_{TR\text{-}settling}$ is the desired load transient response settling time.

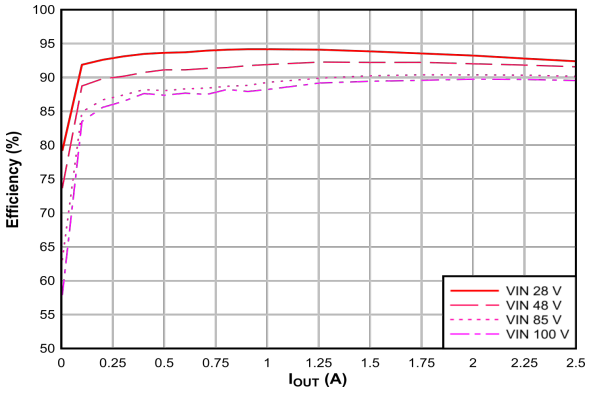
C_B calculates to 56 pF based on a 75-µs settling time. This value avoids excessive coupling capacitor discharge by the feedback resistors during sleep intervals when operating at light loads. To avoid capacitance fall-off with DC bias, use a C0G or NP0 dielectric capacitor for C_B.

9.2.3 Application Curves



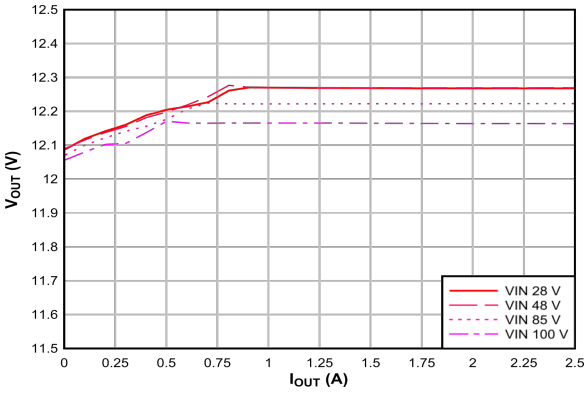
V_{OUT} = 12 V R_{ON} = 102 kΩ L_O = 22 µH

图 9-2. Conversion Efficiency (Log Scale)



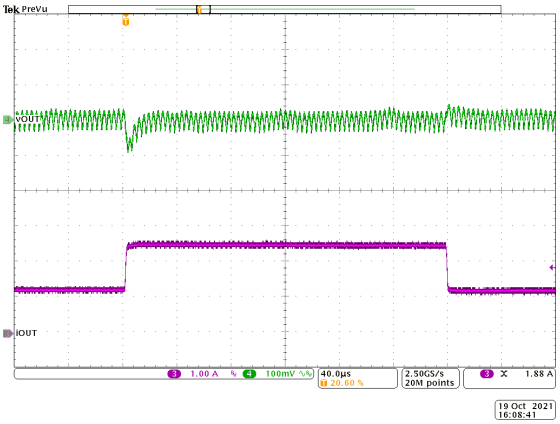
V_{OUT} = 12 V R_{ON} = 102 kΩ L_O = 22 µH

图 9-3. Conversion Efficiency (Linear Scale)



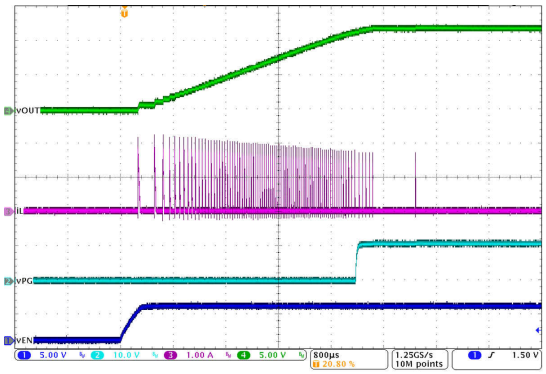
V_{OUT} = 12 V R_{ON} = 102 kΩ L_O = 22 µH

图 9-4. Load and Line Regulation Performance



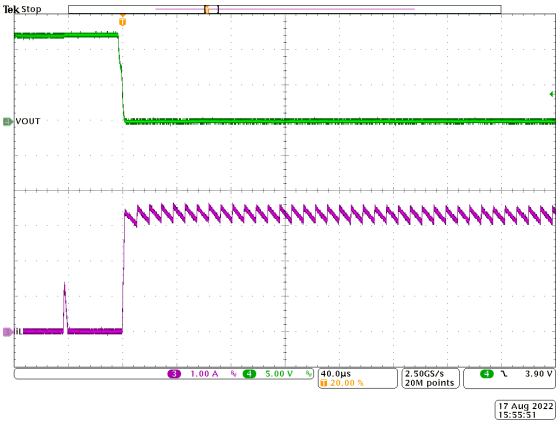
V_{IN} = 48 V V_{OUT} = 12 V I_{OUT} = 1.0-A to 2.5-A (Rise/fall time = 1A/uS)

图 9-5. Load Step Response



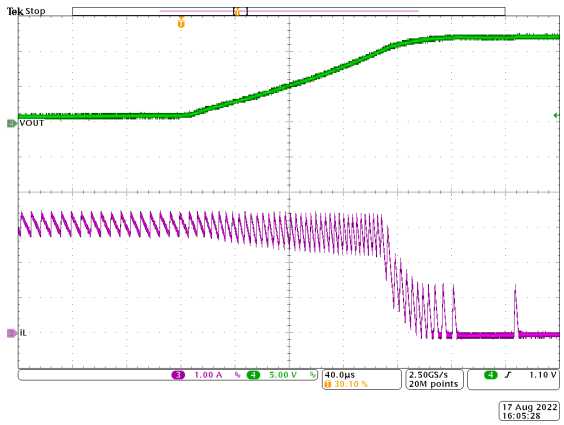
V_{IN} = 48 V V_{OUT} = 12 V I_{OUT} = 0 A

图 9-6. No-Load Start-Up with EN/UVLO



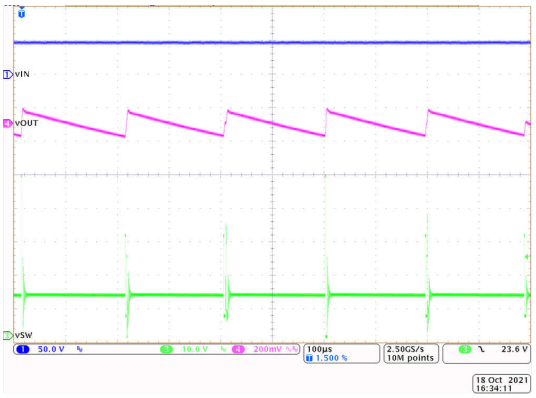
V_{IN} = 48 V V_{OUT} 12 V Load = 0 A to Short

图 9-7. Short Circuit Applied



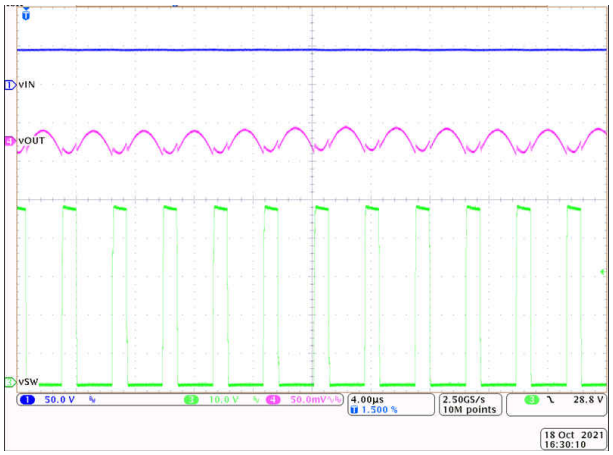
V_{IN} = 48 V V_{OUT} 12 V Load = 0 A to Short

图 9-8. Short-Circuit Recovery



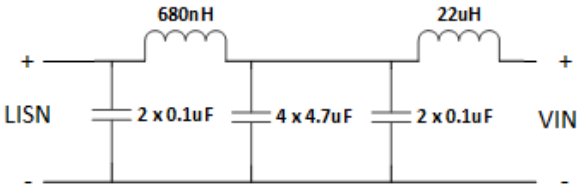
V_{IN} = 48 V V_{OUT} 12 V I_{OUT} = 200 mA

图 9-9. Light-Load Switching



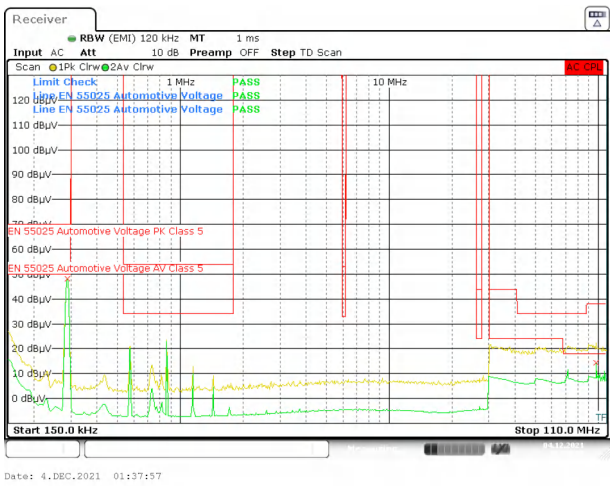
V_{IN} = 48 V V_{OUT} = 12 V I_{OUT} = 2.5 A

图 9-10. Full-Load Switching



Filter used for EMC scan. Additionally, the regulator was housed in an enclosed shield.

图 9-11. Suggested EMC Filter for CISPR 25 Class 5 Compliance



V_{IN} = 48 V V_{OUT} = 12 V I_{OUT} = 3.5 A (LM5013-Q1)

图 9-12. CISPR 25 Class 5 Conducted Emissions Plot, 150 kHz to 110 MHz

9.3 Power Supply Recommendations

The LM5012-Q1 buck converter is designed to operate from a wide input voltage range between 6 V and 100 V. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use 方程式 19 to estimate the average input current.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{19}$$

where

- η is the efficiency.

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the converter is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset, in addition to potential stability issues. The circuit can be damped with a "parallel damping network." For example, a 22-µF damping capacitor in series with a 1.4-Ω resistor connected to the VIN node creates a parallel damped network, providing sufficient damping for a 8.2-µH input filter inductor and 4.4-µF ceramic input capacitance. Damping is not only needed for an input EMC filter, but also when the application usees a power harness which can present a large input loop inductance. For example, two cables (one for VIN and one for GND), each one meter (approximately three feet) long with approximately 1-mm diameter (18 AWG), placed 1 cm (approximately 0.4 inch) apart, forms a rectangular loop resulting in about 1.2 µH of inductance. The *Input Filter Design for Switching Power Supplies Application Report* provides more detail on this topic.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters Application Report* provides helpful suggestions when designing an input filter for any switching regulator.

9.4 Layout

9.4.1 Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

- To help eliminate these problems, bypass the VIN pin to GND with a low-ESR ceramic bypass capacitor with a high-quality dielectric. Place C_{IN} as close as possible to the LM5012-Q1 VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the GND pin and GND PAD.
- Minimize the loop area formed by the input capacitor connections to the VIN and GND pins.
- Locate the inductor and Schottky diode close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
- Place the Schottky diode anode terminal in close proximity to the input capacitor ground/return.
- Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
- Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
- Place a single-point ground connection to the plane. Route the ground connections for the feedback, soft start, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

- Minimize trace length to the FB pin. Place both feedback resistors, R_{FB1} and R_{FB2}, close to the FB pin. Place C_{FF} (if needed) directly in parallel with R_{FB1}. If output setpoint accuracy at the load is important, connect the V_{OUT} sense at the load. Route the V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a grounded shielding layer.
- The RON pin is sensitive to noise. Thus, locate the R_{RON} resistor as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RON to GND must not exceed 20 pF.
- Provide adequate heat sinking for the LM5012-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, these thermal vias must also be connected to inner layer heat-spreading ground planes.
- Reference 节 9.4.2.

9.4.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimizing radiated EMI is to identify the pulsing current path and minimize the area of that path.

图 9-13 denotes the critical switching loop of the buck converter power stage in terms of EMI. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor, the integrated MOSFET of the LM5012-Q1, and Schottky diode. It becomes mandatory to reduce the parasitic inductance of this loop by minimizing the effective loop area.

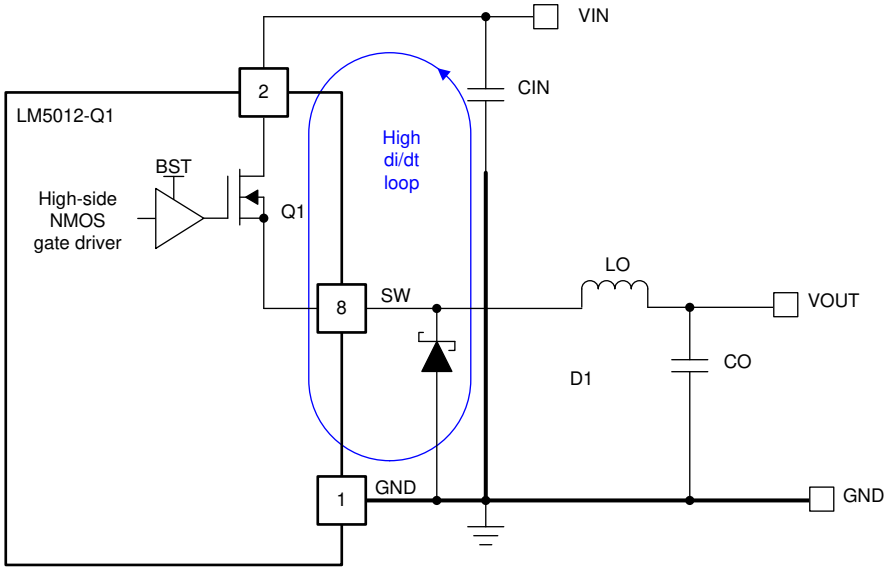


图 9-13. DC/DC Buck Converter With Power Stage Circuit Switching Loop

The input capacitor provides the primary path for the high di/dt components of the current of the high-side MOSFET. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. In addition, the cathode of the Schottky diode must be placed closely to the SW pin of the device, while its anode is kept closely to the GND pin.

Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the return terminal of the capacitor to the GND pin and exposed PAD of the LM5012-Q1.

9.4.1.2 Feedback Resistors

Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the

input to the feedback comparator, and as such, is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor, and V_{IN} to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances greater than 100 kΩ are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node, and V_{IN} so there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources.

9.4.2 Layout Example

图 9-14 shows an example layout for the PCB top layer of a 2-layer board with essential components placed on the top side.

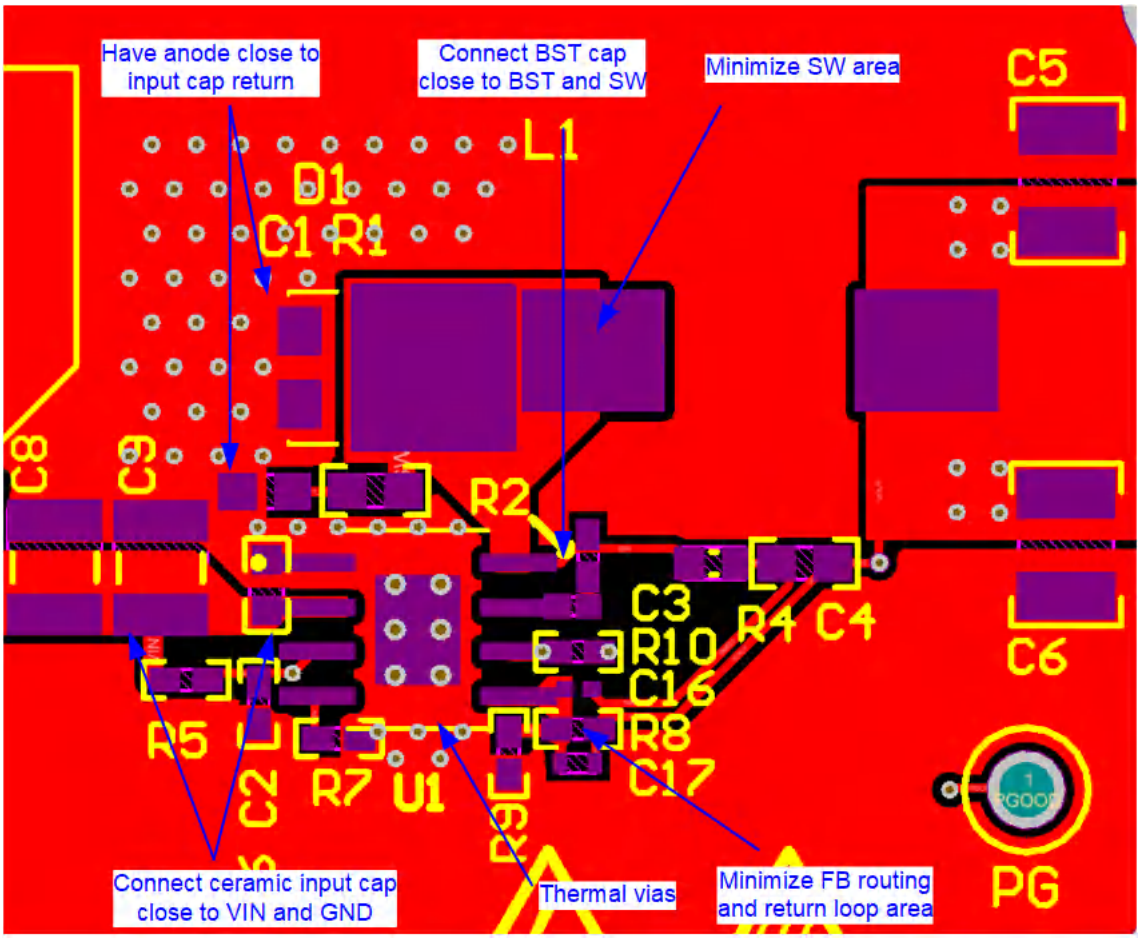


图 9-14. LM5012-Q1 Layout Example

9.4.2.1 Thermal Considerations

As with any power conversion device, the LM5012-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the application
- PCB layout

The maximum internal die temperature for the LM5012-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 方程式 20 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the *Thermal*

Information is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. The value of $R_{\theta JA(EVM)}$ is applicable to the LM5168PEVM and is given for reference only. See the *Semiconductor and IC Package Thermal Metrics Application Report* for more information and the resources given at the end of this section.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (20)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The LM5012-Q1 features a die attach paddle, or "thermal pad" (EP), to provide a place to solder down to the PCB heat-sinking copper. This provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. Typical examples of can be found in 图 9-15. The copper area given in the graph is for each layer. The top and bottom layers are 2-oz copper each, while the inner layers are 1 oz. Remember that the data given in the graph is for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

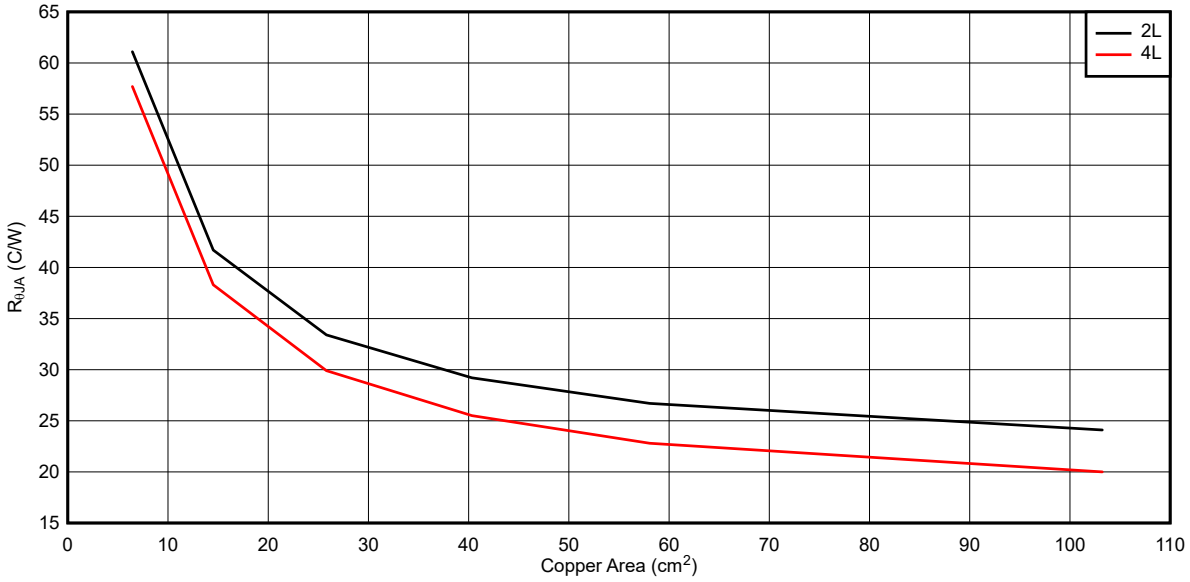


图 9-15. Typical $R_{\Theta JA}$ vs Copper Area

To continue with the design example, assume that the user has an ambient temperature of 70°C and wishes to estimate the required area to keep the device junction temperature below 125°C, at full load. From the curves in Conversion Efficiency (Linear Scale). Typical $R_{\Theta JA}$ vs Copper Area, an efficiency of about 92% was found at an input voltage of 48 V with an output of 12 V with a 1.75-A load. The efficiency is somewhat less at high junction temperature, so an efficiency of approximately 90% is assumed. This gives a total loss of about 2.3 W. Subtracting out the conduction loss alone for the inductor and catch diode, the user arrives at a devise

dissipation of 1.54 W. With this information, the user can calculate the required $R_{\Theta JA}$ of about 30°C/W. Based on 图 9-15, the required copper area is about 40 cm^2, for a two-layer PCB.

The engineer’ s best judgment is to be used if using a lossy inductor, diode, or both in the application, as their large loss can contribute to localized heating of the component, as well, the nearby regulator. As an example, biasing the Schottky diode (D_{SW} with 1.3-A continuous current (average current for 1.75-A load current) results in approximately 10°C rise in the case temperature of the regulator. This should be "buffered" for in the ambient temperature used in the previous calculation. For more details on the these calculations, please see the *PCB Thermal Design Tips for Automotive DC/DC Converters Application Note.*

The following resource can be used as a guide to optimal thermal PCB design and estimating $R_{\Theta JA}$ for a given application environment:

- LM5013 Thermal Optimization and Example PCB design
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *AN-2020 Thermal Design By Insight, Not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Using New Thermal Metrics Application Report*
- *PCB Thermal Design Tips for Automotive DC/DC Converters Application Report*

10 Device and Documentation Support

10.1 Device Support

10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

10.1.2 Development Support

- *LM5012 Quickstart Calculator*
- *LM5012-Q1 Simulation Models*
- *TI Reference Design Library*
- Technical Articles:
  - *Use a Low-quiescent-current Switcher for High-voltage Conversion*
  - *Powering Smart Sensor Transmitters in Industrial Applications*
  - *Industrial Strength Design – Part 1*
  - *Trends in Building Automation: Predictive Maintenance*
  - *Trends in Building Automation: Connected Sensors for User Comfort*

10.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5012-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LM5012/3/4/3/4-Q1EVM-041 EVM User's Guide*
- Texas Instruments, *Selecting an Ideal Ripple Generation Network for Your COT Buck Converter Application Report*
- Texas Instruments, *Valuing Wide V_{IN}, Low-EMI Synchronous Buck Circuits for Cost-Effective, Demanding Applications White Paper*
- Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies White Paper*
- Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies White Paper*
- Texas Instruments, *24-V AC Power Stage with Wide V_{IN} Converter and Battery Gauge for Smart Thermostat Design Guide*
- Texas Instruments, *Accurate Gauging and 50- μA Standby Current, 13S, 48-V Li-ion Battery Pack Reference Design Guide*
- Texas Instruments, *AN-2162: Simple Success with Conducted EMI from DC/DC Converters Application Report*
- Texas Instruments, *Powering Drones with a Wide V_{IN} DC/DC Converter Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5012QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	LM5012	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

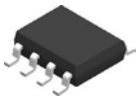
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5012-Q1 :

- Catalog : LM5012

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

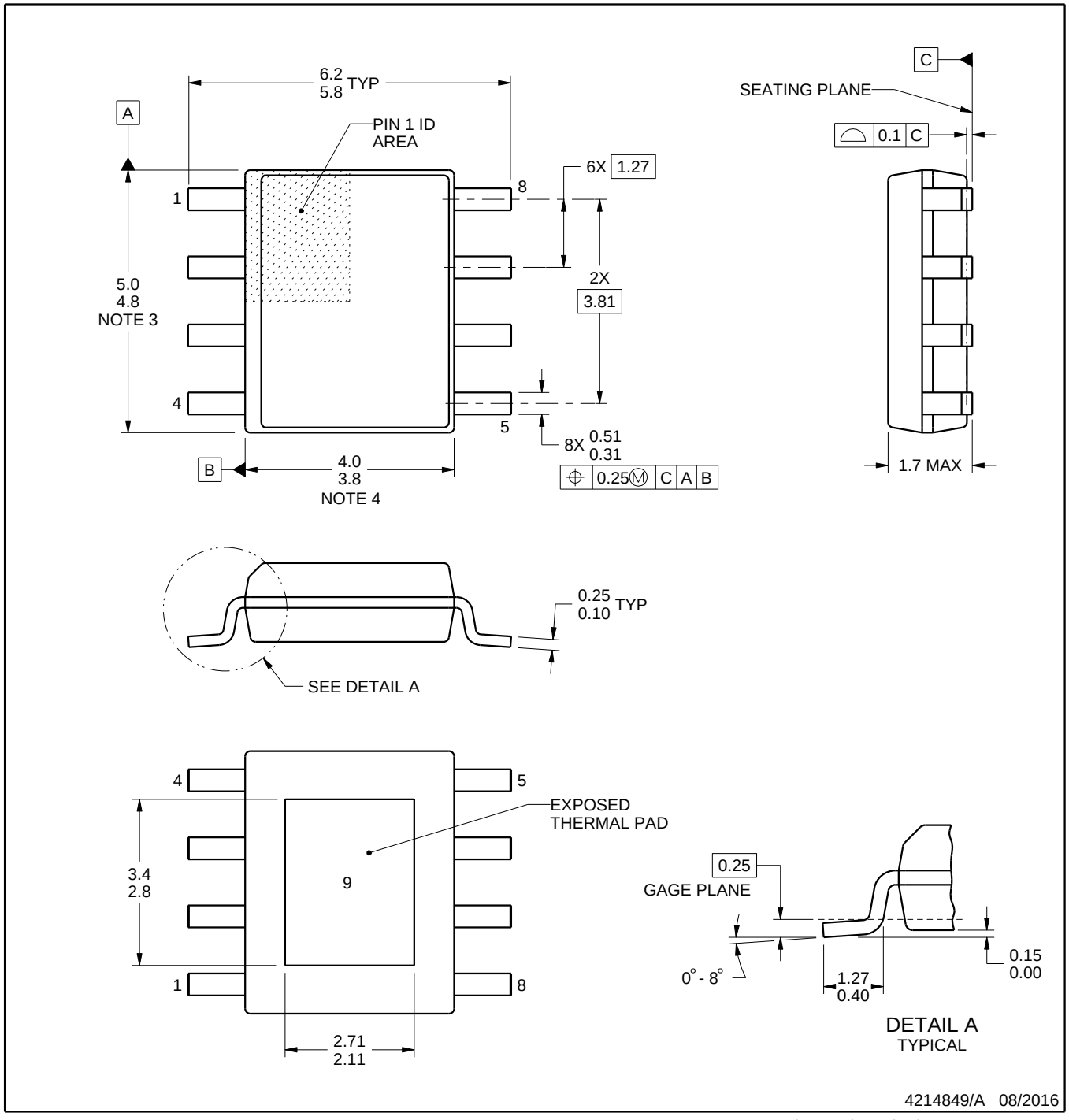


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

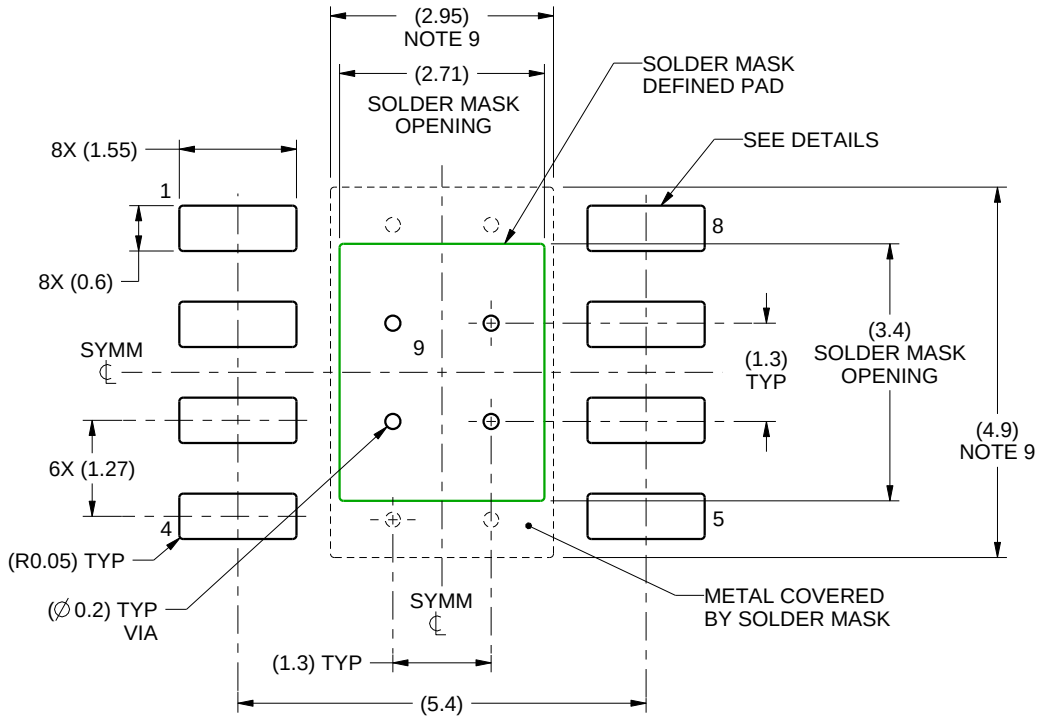
PLASTIC SMALL OUTLINE



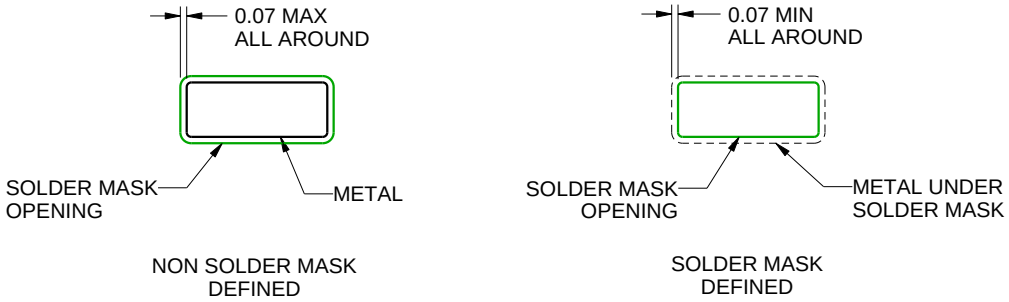
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

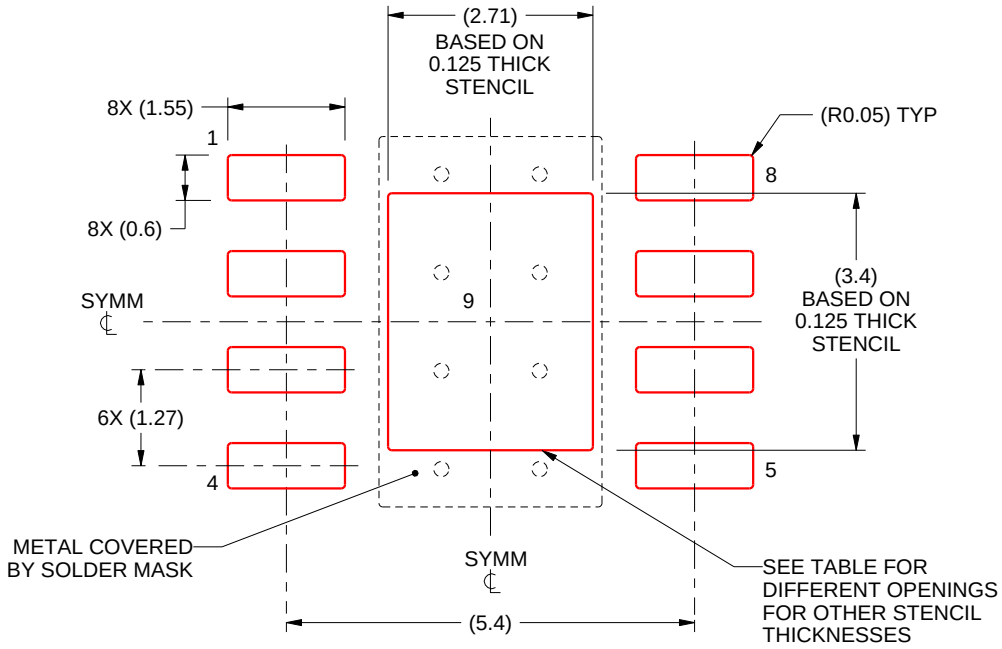
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

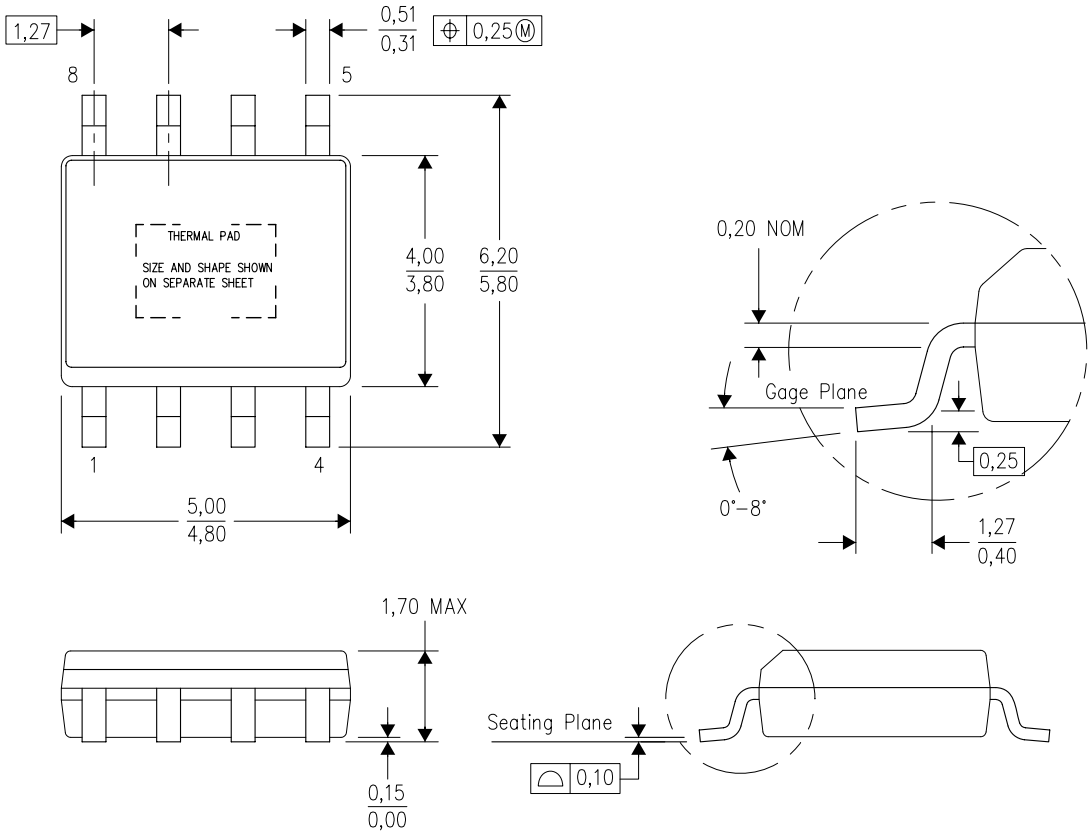
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

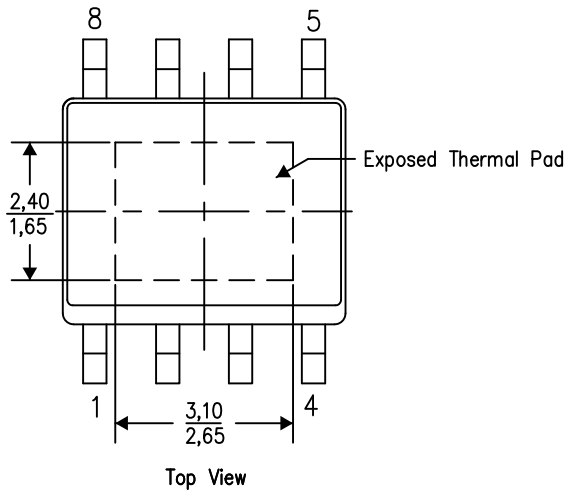
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



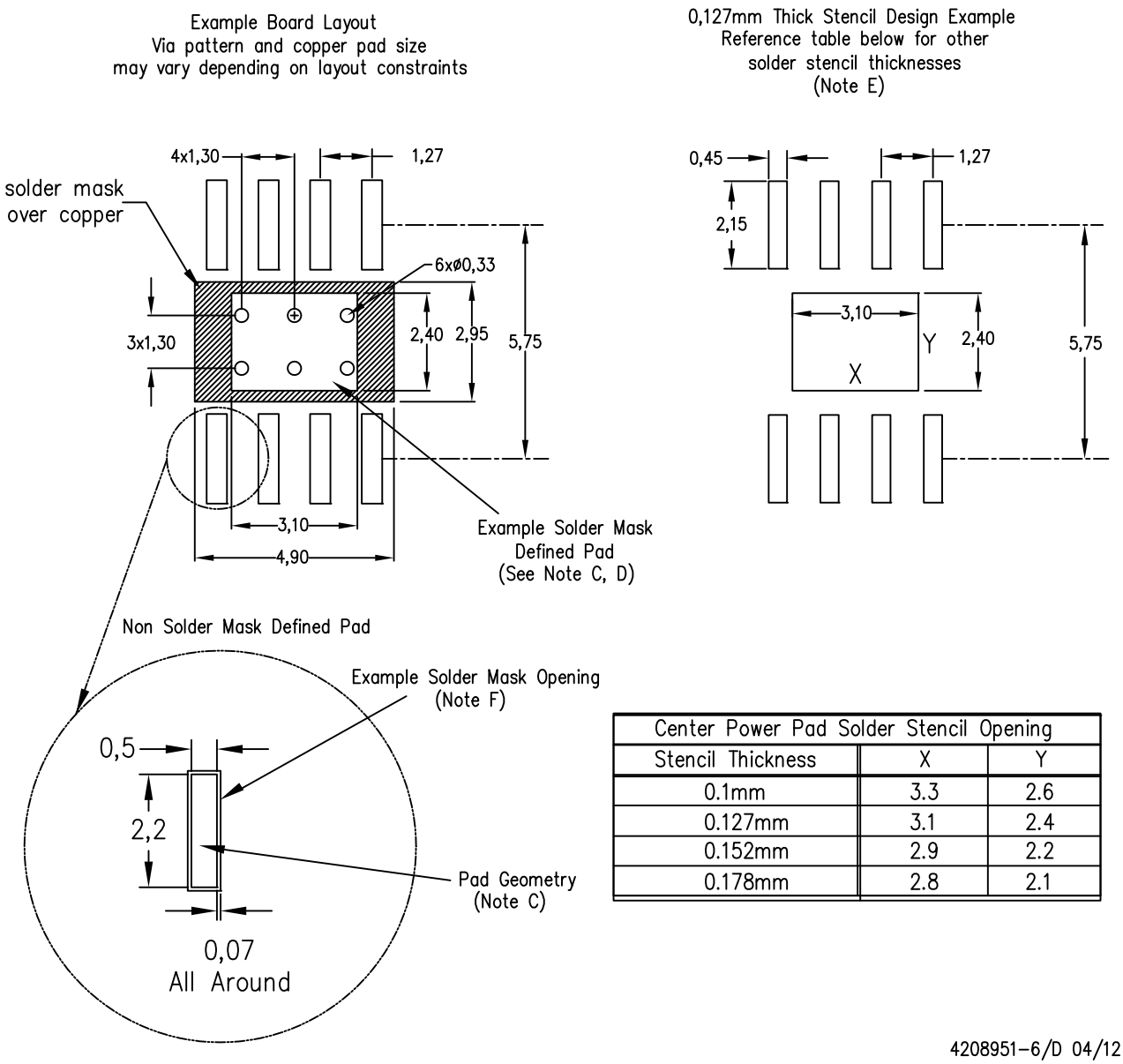
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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