LM4992 Boomer® Audio Power Amplifier Series 420mW Stereo Cell Phone Audio Amplifier

Check for Samples: LM4992, LM4992SDBD

FEATURES

- **Available in Space-Saving WSON Package**
- **Ultra Low Current Shutdown Mode**
- **BTL Output Can Drive Capacitive Loads**
- **Improved Click and Pop Circuitry Eliminates Noise During Turn-On and Turn-Off Transitions**
- **2.2 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 217Hz & 1KHz: 64 dB (1KHz)**
- **Stereo Output Power at 5.0V, 1% THD, 8Ω: 1.07 W (typ)**
- **Stereo Output Power at 3.3V, 1% THD, 8Ω: 420 mW (typ)**
- **Shutdown Current, V_{dd} = 3.3V: 0.2 µA (typ)**

DESCRIPTION

The LM4992 is a stereo audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt, per channel, of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

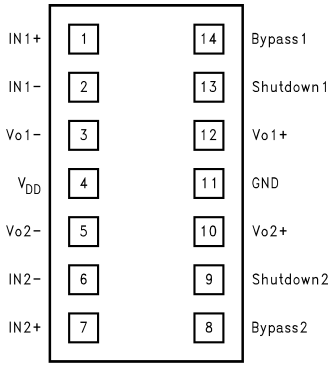
Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4992 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4992 features independent shutdown control for each channel and a low-power consumption shutdown mode, which is achieved by driving both shutdown pins with logic low. Additionally, the LM4992 features an internal thermal shutdown protection mechanism.

The LM4992 contains advanced click and pop circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The LM4992 is unity-gain stable and can be configured by external gain-setting resistors.

Connection Diagram



14 Pin WSON (Top View)
See Package Number NHK0014A

TYPICAL APPLICATION

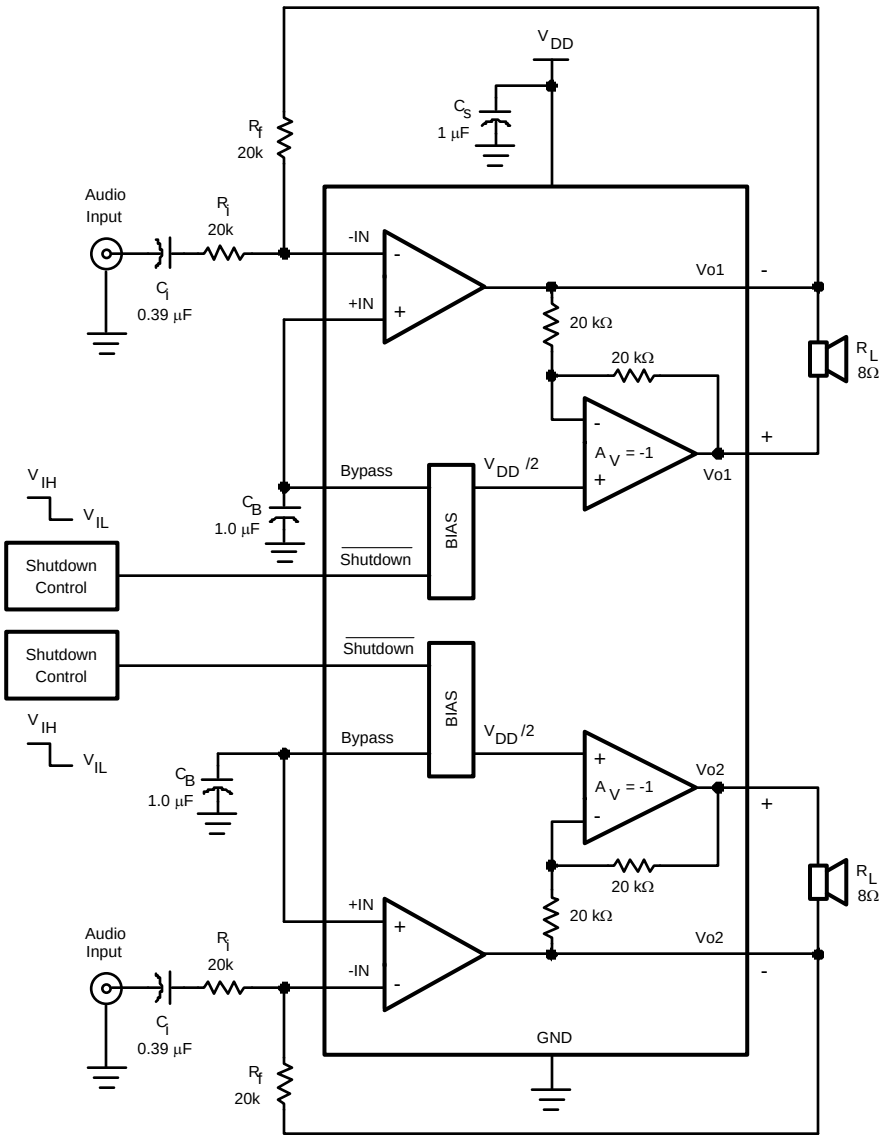


Figure 1. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (3)		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation (4) (5)		Internally Limited
ESD Susceptibility (6)		2000V
ESD Susceptibility (7)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (WSON)	103°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) If the product is in Shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the device will be protected. If the device is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operation life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

(5) Maximum power dissipation in the device (P_{DMAX}) occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation (1) shown in the APPLICATION INFORMATION section. It may also be obtained from the power dissipation graphs.

(6) Human body model, 100pF discharged through a 1.5kΩ resistor.

(7) Machine Model, 220pF–240pF discharged through all pins.

OPERATING RATINGS

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		2.2V ≤ V_{DD} ≤ 5.5V

ELECTRICAL CHARACTERISTICS V_{DD} = 5V(1) (2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4992		Units (Limits)
			Typical (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	6	14	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	7	18	mA (max)
I_{SD}	Shutdown Current	V_{SD} = V_{GND}	1.4	3	µA (max)
V_{SDIH}	Shutdown Voltage Input High		1.5		V
V_{SDIL}	Shutdown Voltage Input Low		1.3		V
V_{OS}	Output Offset Voltage		7	30	mV (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz, per channel	1.07	0.9	W (min)
T_{WU}	Wake-up time		100		ms
THD+N	Total Harmonic Distortion+Noise	P_o = 0.5 Wrms; f = 1kHz	0.15		%
Xtalk	Crosstalk		80		dB
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	60 (f = 217Hz) 64 (f = 1kHz)	55	dB (min)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS V_{DD} = 3.3V(1) (2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4992		Units (Limits)
			Typical (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	4	12	mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	5	15	mA (max)
I_{SD}	Shutdown Current	V_{SD} = V_{GND}	0.2	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High		1.2		V
V_{SDIL}	Shutdown Voltage Input Low		1.0		V
V_{OS}	Output Offset Voltage		7	30	mV (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz, per channel	420		mW (min)
T_{WU}	Wake-up time		75		ms
THD+N	Total Harmonic Distortion+Noise	P_o = 0.25 Wrms; f = 1kHz	0.1		%
Xtalk	Crosstalk		80		dB
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	65 (f = 217Hz) 70 (f = 1kHz)	55	dB (min)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS V_{DD} = 2.6V (1) (2)

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4992		Units (Limits)
			Typical (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, No Load	4.0		mA (max)
		V_{IN} = 0V, I_o = 0A, 8Ω Load	6.0		mA (max)
I_{SD}	Shutdown Current	V_{SD} = V_{GND}	0.02	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High		1.2		V
V_{SDIL}	Shutdown Voltage Input Low		1.0		V
V_{OS}	Output Offset Voltage		5	30	mV (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz, per channel	240		mW (min)
T_{WU}	Wake-up time		70		ms
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15 Wrms; f = 1kHz	0.1		%
Xtalk	Crosstalk		80		dB
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p Input terminated with 10Ω	51 (f = 217Hz) 51 (f = 1kHz)		dB (min)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

External Components Description

(Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at f_C= 1/(2π R_iC_i).
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at f_c = 1/(2π R_iC_i). Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

TYPICAL PERFORMANCE CHARACTERISTICs

THD+N vs Frequency at V_{DD} = 5V, 8Ω R_L, and PWR = 500mW, per channel

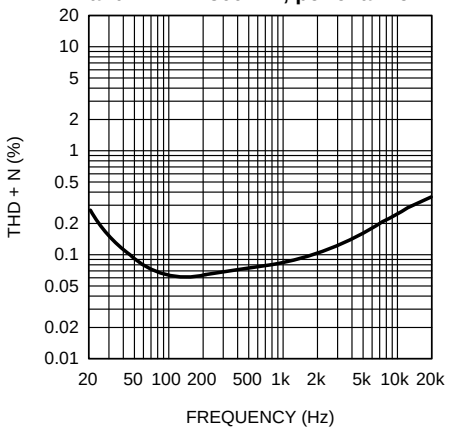


Figure 2.

THD+N vs Frequency at V_{DD} = 3.3V, 8Ω R_L, and PWR = 250mW, per channel

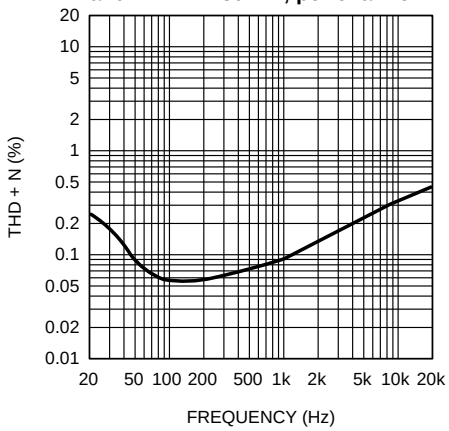


Figure 3.

THD+N vs Frequency at V_{DD} = 2.6V, 8Ω R_L, and PWR = 150mW, per channel

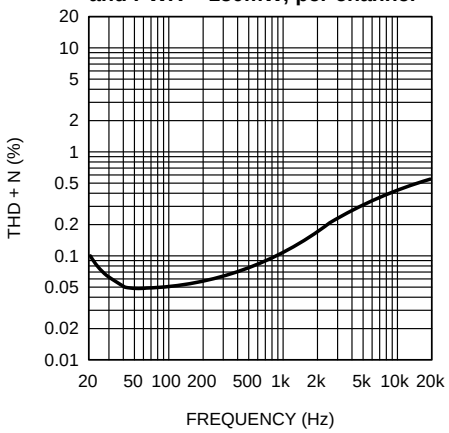


Figure 4.

THD+N vs Power Out at V_{DD} = 5V, 8Ω R_L, 1kHz, per channel

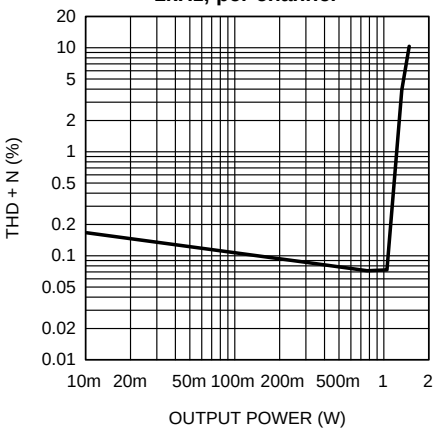


Figure 5.

THD+N vs Power Out at V_{DD} = 3.3V, 8Ω R_L, 1kHz, per channel

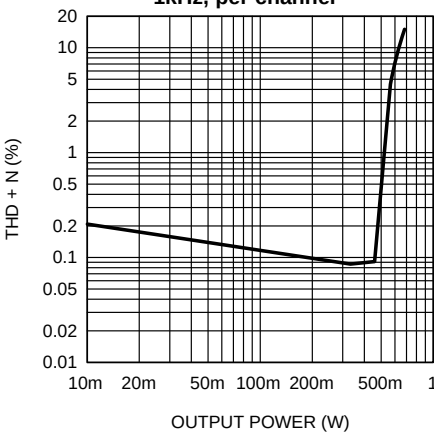


Figure 6.

THD+N vs Power Out at V_{DD} = 2.6V, 8Ω R_L, 1kHz, per channel

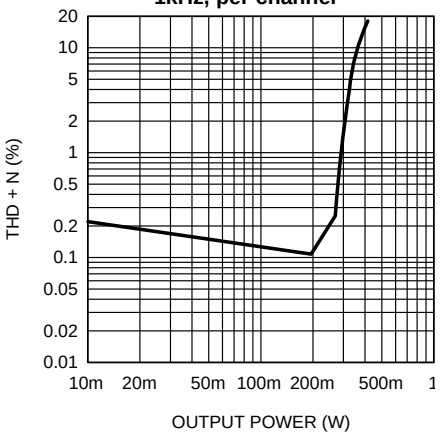


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICs (continued)

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 5V, 8Ω R_L

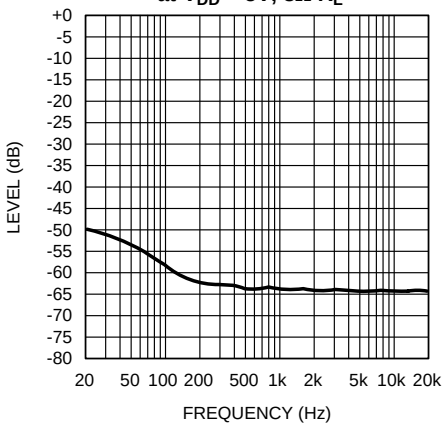


Figure 8. Input terminated with 10Ω

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 5V, 8Ω R_L

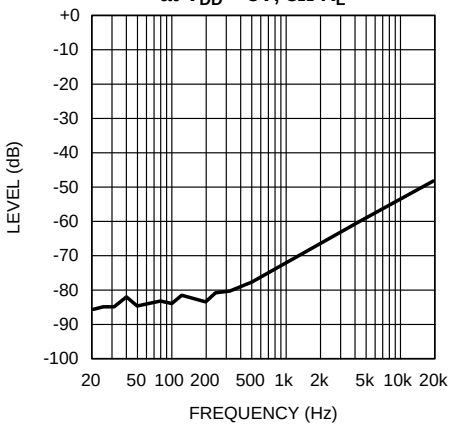


Figure 9. Input Floating

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 3.3V, 8Ω R_L

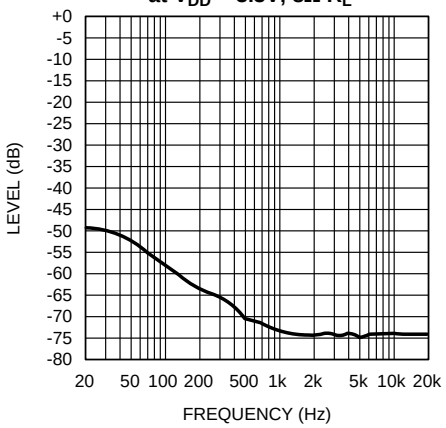


Figure 10. Input Floating

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 3.3V, 8Ω R_L

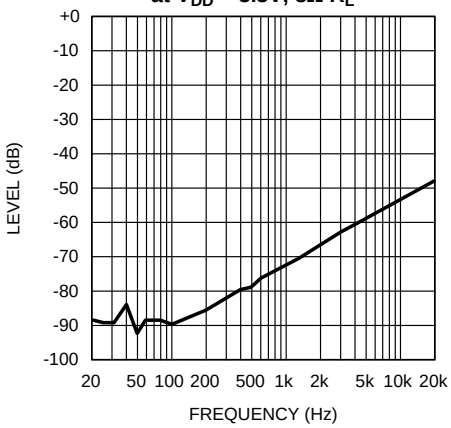


Figure 11. Input Floating

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 2.6V, 8Ω R_L

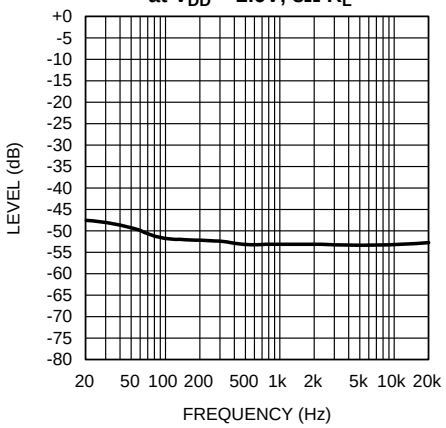


Figure 12. Input terminated with 10Ω

Power Supply Rejection Ratio (PSRR) vs Frequency at V_{DD} = 2.6V, 8Ω R_L

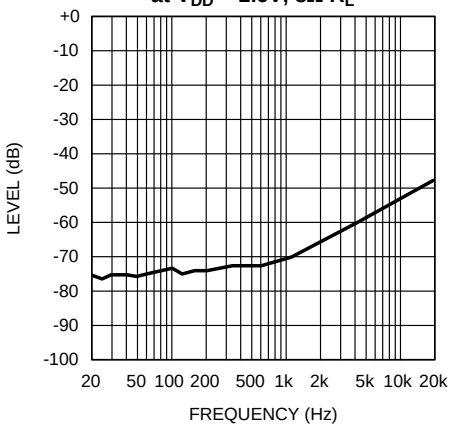


Figure 13. Input Floating

TYPICAL PERFORMANCE CHARACTERISTICs (continued)

Open Loop Frequency Response, 5V

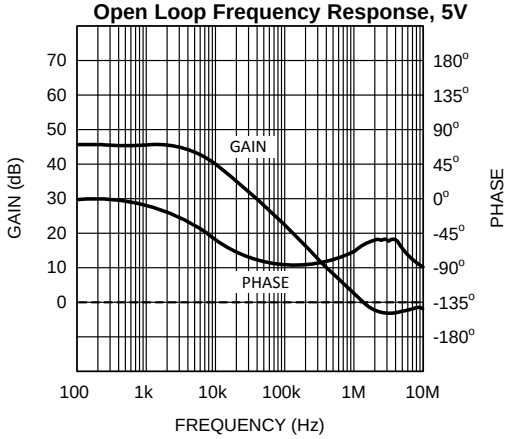


Figure 14.

Open Loop Frequency Response, 3.3V

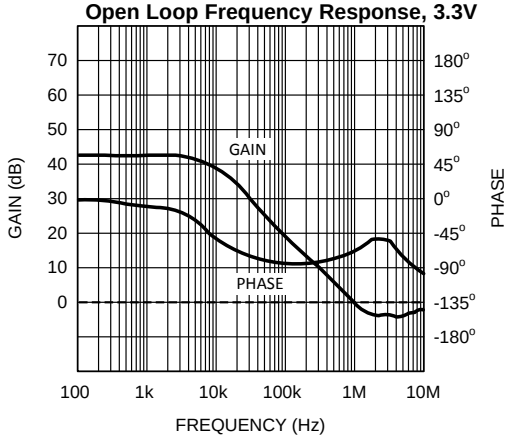


Figure 15.

Open Loop Frequency Response, 2.6V

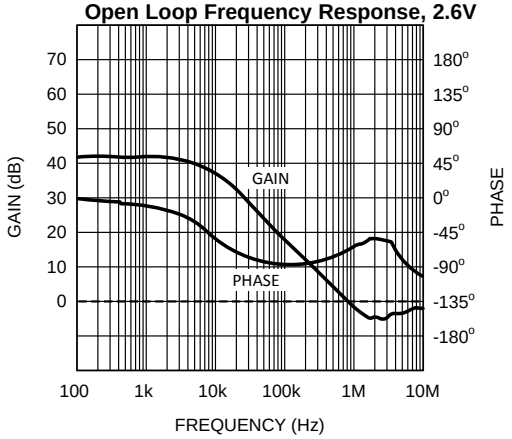


Figure 16.

Noise Floor, 5V, 8Ω
80kHz Bandwidth, Input to GND

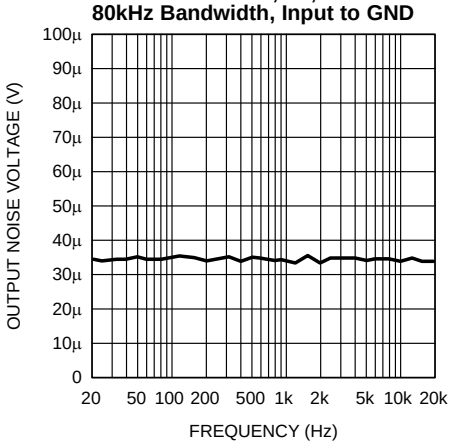


Figure 17.

Crosstalk vs Frequency
5V, 8Ω, P_{OUT} = 1W

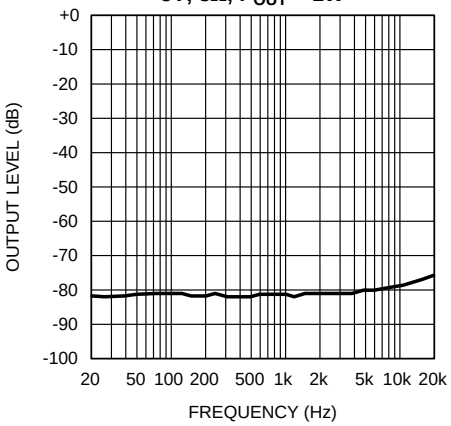


Figure 18.

Crosstalk vs Frequency
3.3V, 8Ω, P_{OUT} = 400mW

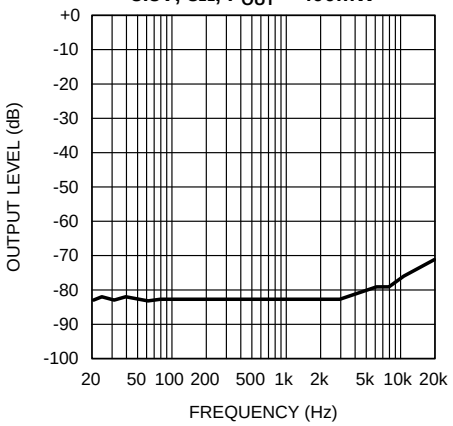


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICs (continued)

Crosstalk vs Frequency
2.6V, 8Ω, P_{OUT} = 200mW

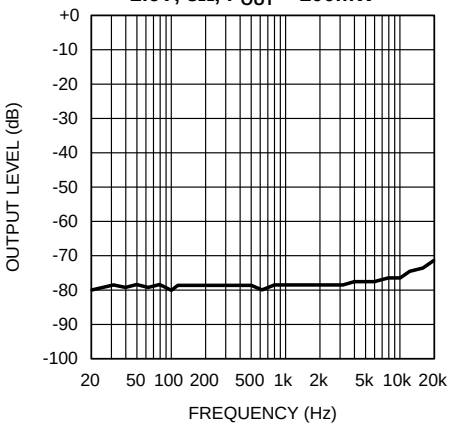


Figure 20.

Power Dissipation vs Output Power, 5V, 8Ω, per channel

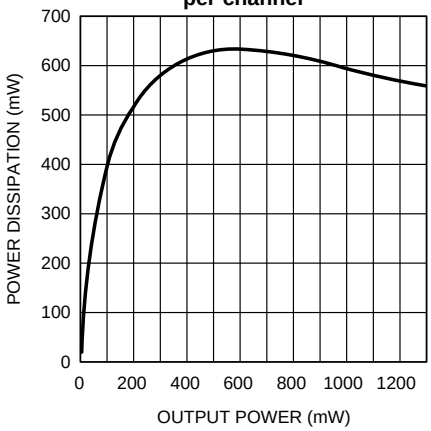


Figure 21.

Power Dissipation vs Output Power, 3.3V, 8Ω, per channel

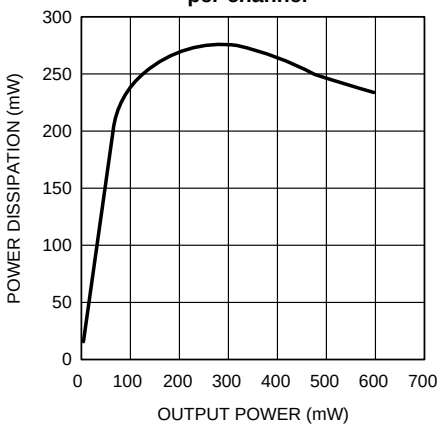


Figure 22.

Power Dissipation vs Output Power, 2.6V, 8Ω, per channel

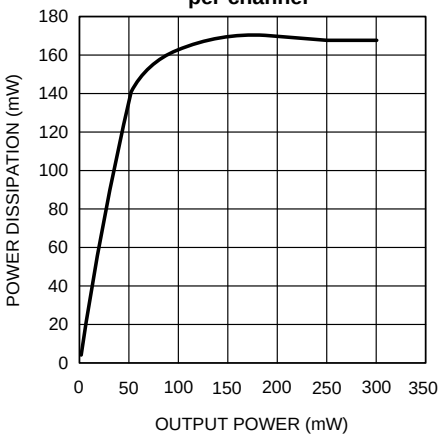


Figure 23.

Shutdown Hysteresis Voltage 5V

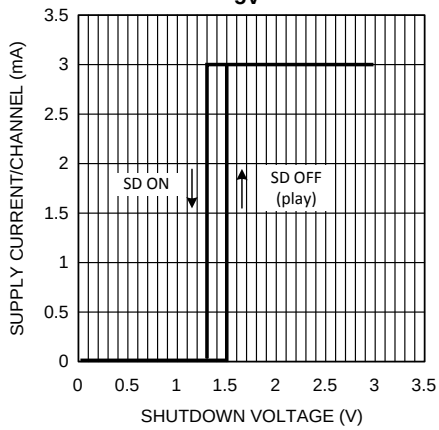


Figure 24.

Shutdown Hysteresis Voltage 3.3V

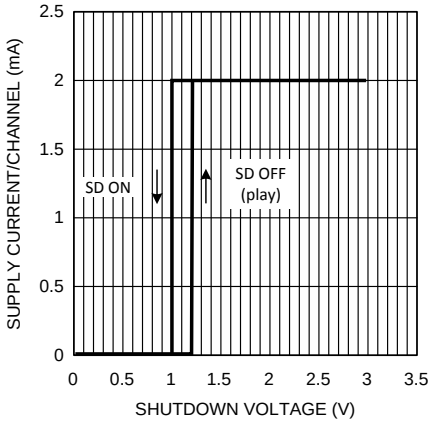


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICs (continued)

Shutdown Hysteresis Voltage 2.6V

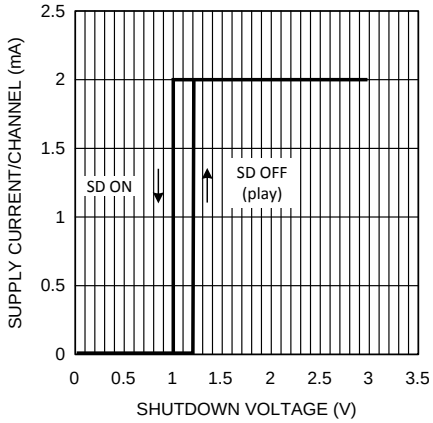


Figure 26.

Output Power vs Supply Voltage, 8Ω

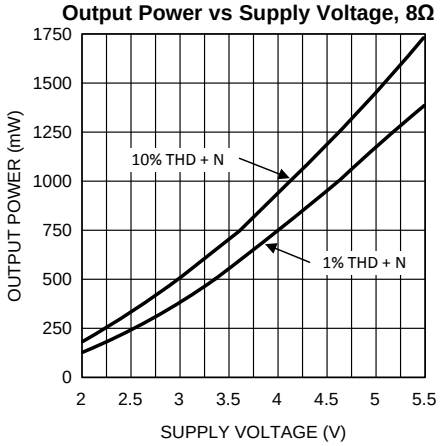


Figure 27.

Frequency Response vs Input Capacitor Size

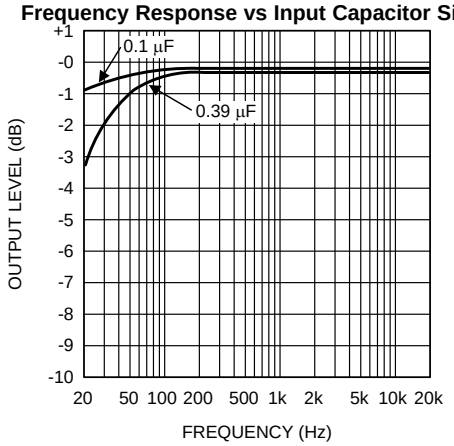


Figure 28.

Wakeup Time vs Supply Voltage

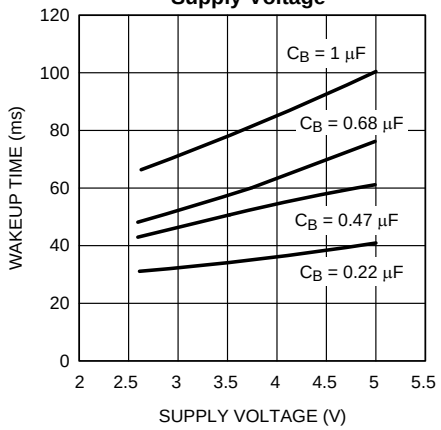


Figure 29.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4992 has two internal operational amplifiers per channel. The first amplifier's gain is externally configurable , while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4992, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The maximum internal power dissipation per channel is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation (2).

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} is a function of P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA}, resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the LM4992. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4992 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the TYPICAL PERFORMANCE CHARACTERISTICs curves for power dissipation information for different output powers and output loading.

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4992's exposed-DAP (die attach paddle) packages (NHK) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.07W dissipation per channel in an 8Ω load at ≤ 1% THD+N. This power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4992's performance and activate unwanted, though necessary, thermal shutdown protection.

The LM4992SD must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4992. The selection of a bypass capacitor, C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4992 contains shutdown circuitry that is used to independently turn off each channel's bias circuitry. This shutdown feature turns a given channel off when logic low is placed on the corresponding shutdown pin. By switching a particular shutdown pin to GND, the LM4992 supply current draw due to that channel will be minimized in idle mode. Idle current is measured with the shutdown pin connected to GND. The trigger point for shutdown is shown as a typical value in the Shutdown Hysteresis Voltage graphs in the TYPICAL PERFORMANCE CHARACTERISTICs section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.2µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor. This scheme ensures that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4992 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4992 is unity-gain stable which gives the designer maximum system flexibility. The LM4992 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4992 turns on. The slower the LM4992's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the TYPICAL PERFORMANCE CHARACTERISTICs section, the supply rail can be easily found.

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4992 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation (3).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

$$R_f/R_i = A_{VD}/2 \quad (4)$$

From Equation (3), the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20 kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

$$f_L = 100\ Hz/5 = 20\ Hz \quad (5)$$

$$f_H = 20\ kHz * 5 = 100\ kHz \quad (6)$$

As stated in the PROPER SELECTION OF EXTERNAL COMPONENTS section, R_i in conjunction with C_i create a highpass filter.

$$C_i \geq 1/(2\pi * 20\ k\Omega * 20\ Hz) = 0.397\ \mu F;\ use\ 0.39\ \mu F \quad (7)$$

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100 kHz, the resulting GBWP = 300kHz which is much smaller than the LM4992 GBWP of 1.5MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4992 can still be used without running into bandwidth limitations.

The LM4992 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in SCHEMATIC DRAWING to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing High Frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

SCHEMATIC DRAWING

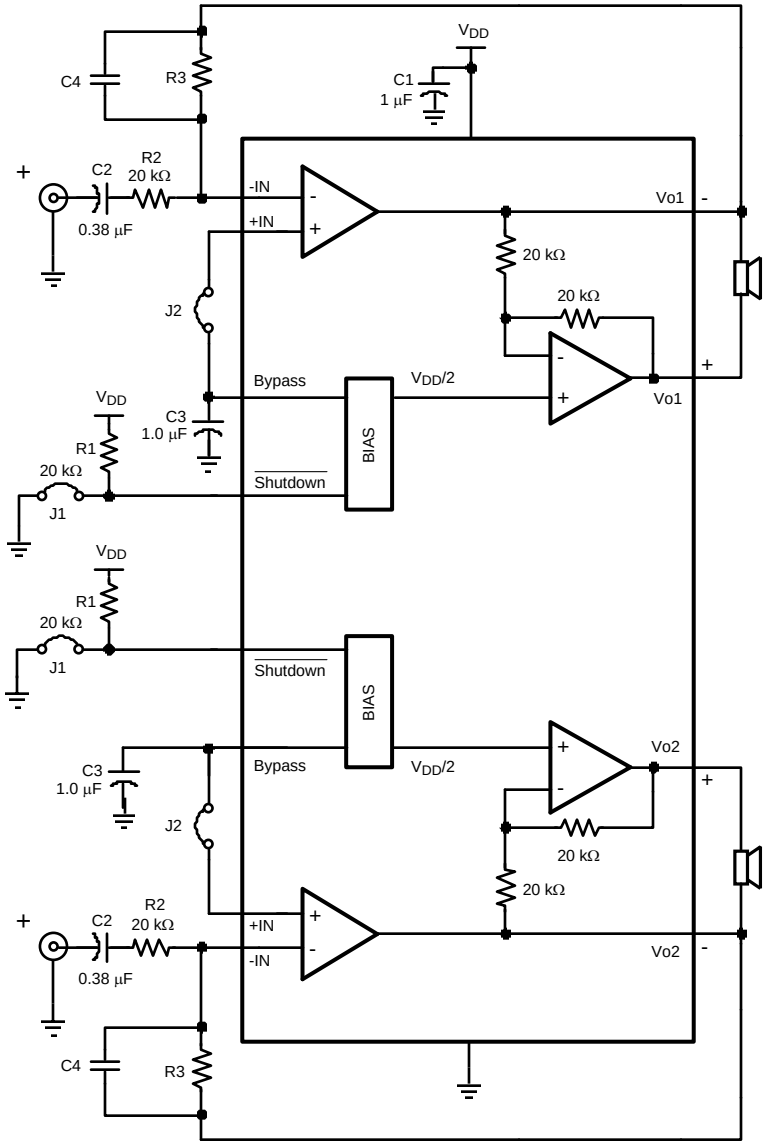


Figure 30. Higher Gain Schematic Drawing

Demonstration Board Layout

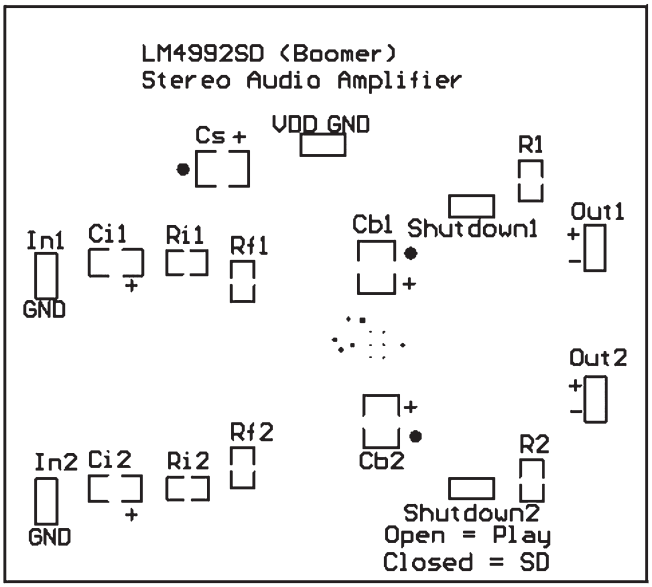


Figure 31. Recommended WSON Board Layout: Top Overlay

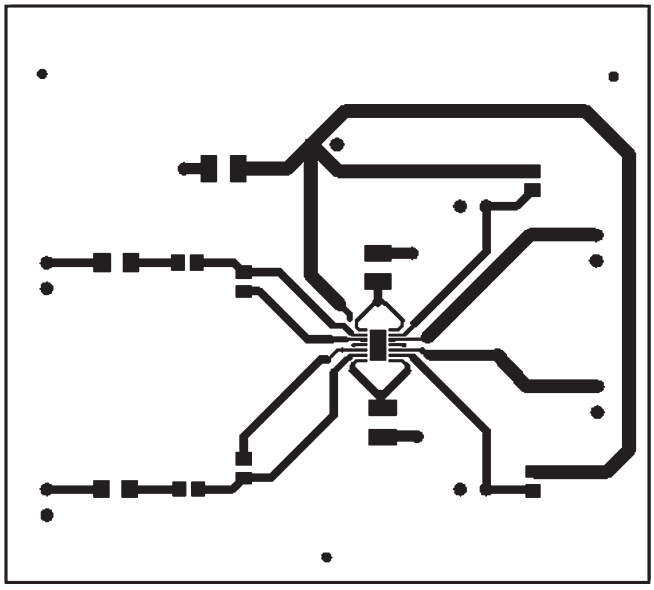


Figure 32. Recommended WSON Board Layout: Top Layer

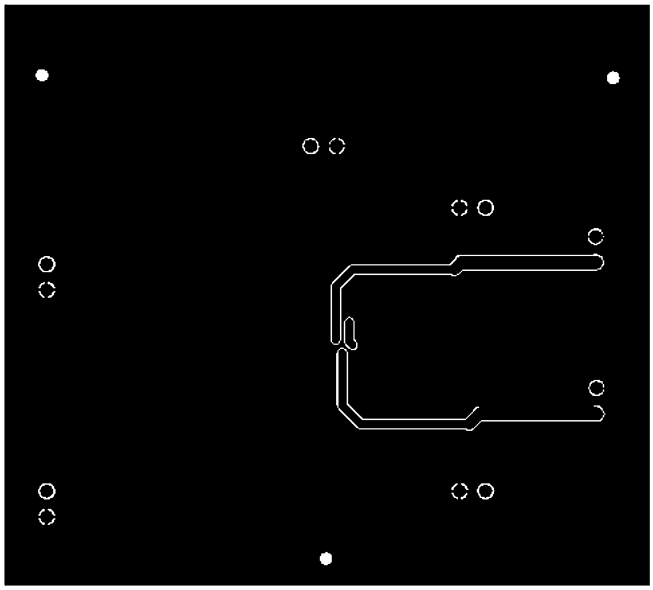


Figure 33. Recommended WSON Board Layout: Bottom Layer

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4992SD/NOPB	Active	Production	WSON (NHK) | 14	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L4992

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

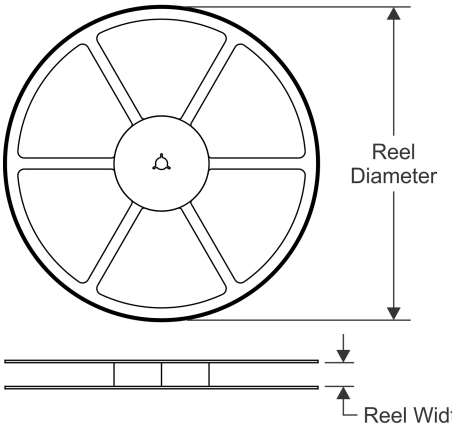
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

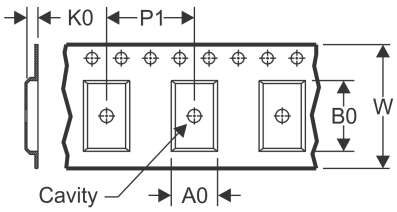
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

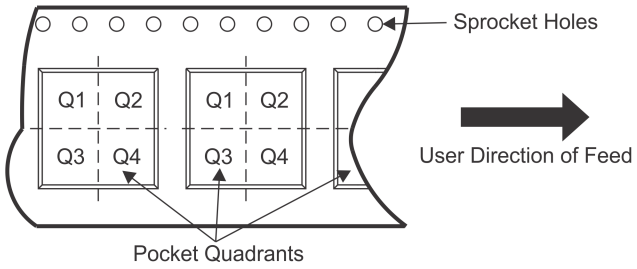


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

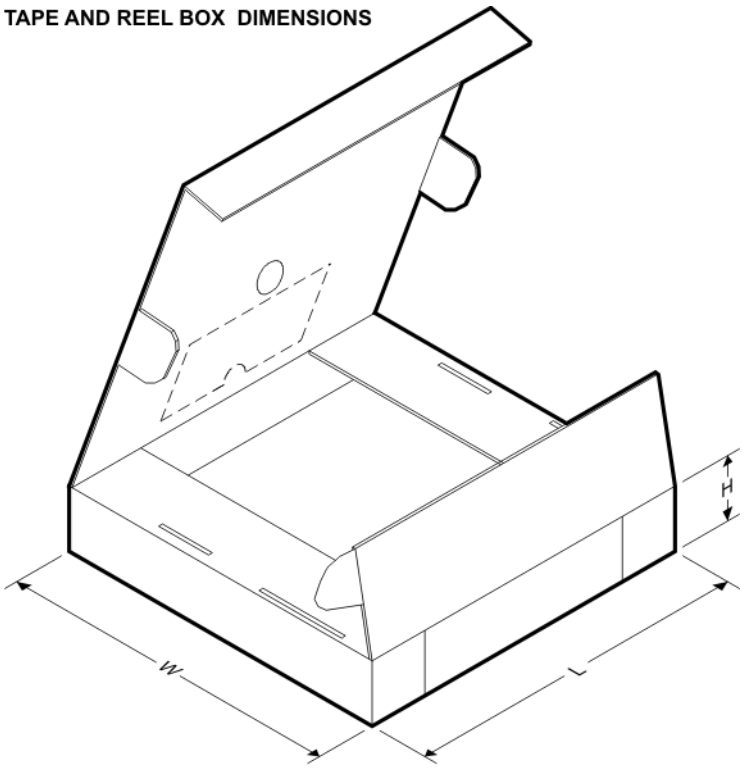
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4992SD/NOPB	WSON	NHK	14	1000	178.0	12.4	3.3	4.3	1.0	8.0	12.0	Q1

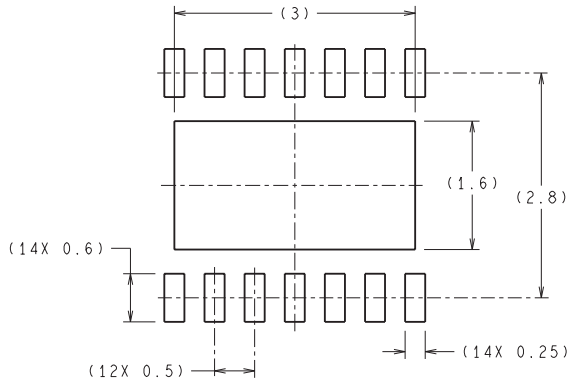
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

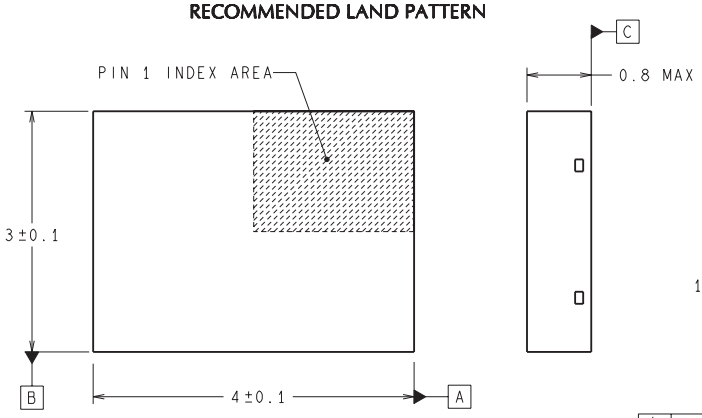
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4992SD/NOPB	WSON	NHK	14	1000	208.0	191.0	35.0

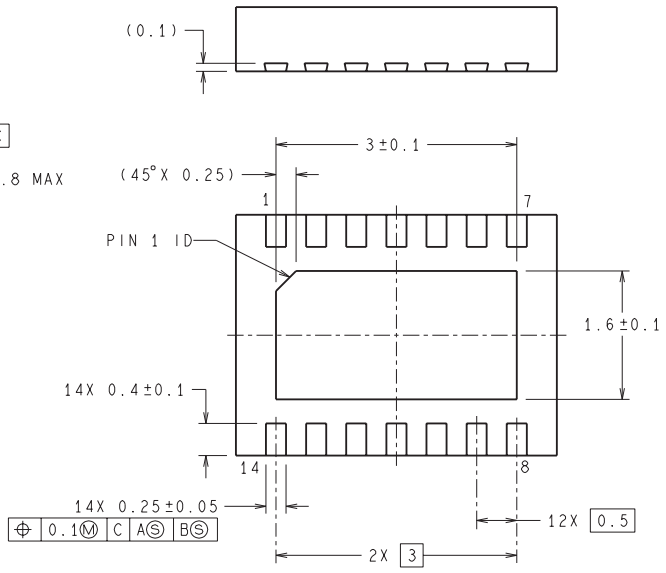
NHK0014A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA14A (Rev A)

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