用于 LED 照明的相位调光，初级侧电源调节功率因数校正 (PFC) 反激转换控制器

查询样品: LM3447

特性

- 集成型相位角度解码
  - 可以同时兼容前斩波和后斩波
  - 超过 **50:1** 的调光范围
- 总谐波失真较低的功率因数校正
- 使用输入电压前馈技术实现的初级侧控制
- 带有改进线路调节的输入功率调节机制
- **LED** 的恒定功率运行用来补偿温度和使用寿命范围内的前馈电压变化
- 定频不连续电感模式运行
- 谷底开关操作以实现高效率和低电磁干扰 **(EMI)**
- 高效三端双向交流开关 **(TRIAC)** 保持电流管理
- 用于 **LED** 保护的热折返功能
- **LED** 开电路和短路保护

应用范围

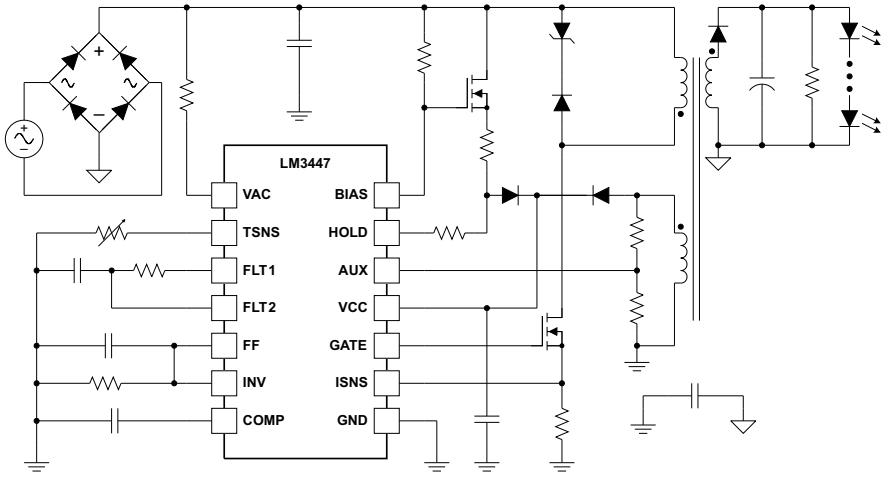
- 亮度可调节 **A19**，**R20**，**PAR30/38 LED** 灯
- 嵌入式 **LED** 射灯和吊灯
- 工业用和商用固态照明

说明

LM3447 是一款多用途功率因数校正 (PFC) 控制器，此控制器设计用于满足与切相调光器兼容的住宅和商用 LED 灯驱动器性能需求。 此器件集成有一个相位解码电路和一个可调保持电流电路来提供顺畅且无闪光的亮度调节操作。 基于输入电压前馈的私有初级侧控制技术被用于调节取自 LED 驱动器的输入功率并且实现宽输入电压范围上的线路调节功能。 执行谷底开关操作可大大减少开关损失和 EMI。 根据一个单外部负温度系数 (NTC) 热敏电阻器上感测到的温度，一个内部热折返电路可保护 LED 不受过热损坏。 额外的特性还包括 LED 开电路和短路保护、逐周期场效应管 (FET) 过流保护、使用一个内部 812ms 故障定时器的突发模式故障操作和内部热关断。

LM3447 是亮度可调、隔离式单级 LED 灯驱动器应用的理想选择，在此类应用中，简单性、低组件数量和较小的解决方案尺寸是首要的。 目前，此器件采用薄型小外形尺寸 (TSSOP) 14 引脚封装。

典型应用图



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

TEMPERATURE RANGE (T_J)	PACKAGE(2)	PINS	PACKAGE DRAWING	ORDERABLE DEVICE NUMBER	TRANSPORT MEDIA	QUANTITY
–40°C to 125°C	TSSOP	14	MTC14	LM3447MT	Tube	94
				LM3447MTE	Tape and Reel	250
				LM3447MTX	Tape and Reel	2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	VCC(2)	–0.3	22	V
Input voltage range	HOLD(3)	–0.3	22	V
	VAC(4)	–0.3	6	V
	TSNS, FLT1, FLT2, FF, INV, COMP, ISNS, AUX	–0.3	6	V
Output voltage range	GATE(2) (Pulse < 20ns)	–1.5	19	V
Continuous input current	I_{BIAS}(4)		10	mA
Junction temperature	T_J(5)		165	°C
Storage temperature range(5)	T_{STG}	–65	150	°C
Lead temperature	Soldering, 10s		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VCC is internally limited to approximately 18.9V. See ELECTRICAL CHARACTERISTICS table.
(3) HOLD current is limited by the internal power dissipation of the device.
(4) Voltage on VAC and BIAS is internally clamped. The clamp level varies with operating conditions. In normal use, VAC and BIAS are current fed with the voltage internally limited.
(5) Maximum junction temperature is internally limited.

PACKAGE DISSIPATION RATINGS(1) (2)

PACKAGE	θ_{JA}, THERMAL IMPEDANCE JUNCTION TO AMBIENT,NO AIRFLOW (°C/W)	T_A = 25°C POWER RATING (mW)	T_A = 70°C POWER RATING (mW)	T_A = 85°C POWER RATING (mW)
TSSOP–14 (MTC)	155(1)	645(3)	355(3)	258(3)

(1) Tested per JEDEC EIA/JESD51-1. Thermal resistance is a function of board construction and layout. Air flow reduces thermal resistance. This number is included only as a general guideline; see TI document (SPRA953) device Package Thermal Metrics.
(2) Thermal resistance to the circuit board is lower. Measured with standard single-sided PCB construction. Board temperature, TB, measured approximately 1 cm from the lead to board interface. This number is provided only as a general guideline.
(3) Maximum junction temperature, T_J, equal to 125°C

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC}	Input Voltage	7.5	14	17.5	V
I_{BIAS}	BIAS current from a high impedance source			500	µA
I_{VAC}	VAC current from a high impedance source			500	µA
T_J	Operating junction temperature	–40	25	125	°C

(1) For specified performance limits and associated test conditions, see the Electrical Characteristics table.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MAX	UNIT
Human Body Model (HBM)	2	kV
Field Induced Charged Device Model (FICDM)	750	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified –40°C < T_J = T_A < 125°C, VCC = 14V, V_{TSNS} = 1.75V, V_{FLT2} = 1.75V, V_{AUX} = 0.5V, V_{INV} = 0V, I_{VAC} = 100µA, I_{BIAS} = 100µA, C_{VCC} = 10µF, C_{COMP} = 0.047µF, R_{HLD} = 10kΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VCC)						
$VCC_{(UVLO)}$	Rising threshold		9.5	10.5	11.5	V
	Falling threshold		6.8	7.5	8.3	V
	Hysteresis			3		V
$VCC_{(OVP)}$	Rising threshold		17.7	18.89	20.1	V
	Falling threshold		17.5	18.72	19.9	V
	Hysteresis			175		mV
I_{VCC}	Startup current	VCC = 6.7V, V_{INV} = 0 V		180		µA
	Standby current	V_{INV} = 1.75V, V_{AUX} = 1 V		1.6		mA
	Switching current	C_{GATE} = 1 nF		3.3		mA
INPUT VOLTAGE FEEDFORWARD and ANGLE DETECTION (VAC, FF)						
$VAC_{(CLAMP)}$	VAC clamp voltage			1.24		V
$I_{VAC(ANGLE)}$	Dimmer angle detect threshold	Sweep I_{VAC}		66		µA
$I_{VAC(HOLD)}$	HOLD FET turn-on threshold	Sweep I_{VAC}, V_{FLT2} = 0 V		95		µA
I_{FF}	Feedforward source current	V_{GATE} = VCC, I_{VAC} = 100 µA		10		µA
DIMMING DECODER CIRCUIT (FLT1, FLT2)						
$FLT1_{(HIGH)}$	FLT1 voltage high	FLT1 open	1.67	1.75	1.83	V
$FLT2_{(MIN)}$	Minimum dimming decode voltage	V_{FLT2} falling	263	290	315	mV
$G_{(DECODE)}$	Decode gain, VINV/VFLT2			0.877		
$FLT2_{HOLD(EN)}$	HOLD circuit enable threshold	V_{FLT2} falling		1		V
$FLT2_{HOLD(DIS)}$	HOLD circuit disable threshold	V_{FLT2} rising		1.2		V
HOLD CIRCUIT (HOLD)						
$R_{DS(ON)}$	HOLD MOSFET on-resistance	I_{VAC} = 50 µA, V_{FLT2} = 1 V		24		Ω
PRE-REGULATOR GATE BIAS CIRCUIT (BIAS)						
$BIAS_{(HIGH)}$	BIAS high voltage clamp	VCC < $VCC_{(UVLO)}$	16.1	17.7	19.3	V
BIAS(LOW)	BIAS low voltage clamp	VCC > $VCC_{(UVLO)}$	12.3	13.5	14.7	V

ELECTRICAL CHARACTERISTICS (continued)

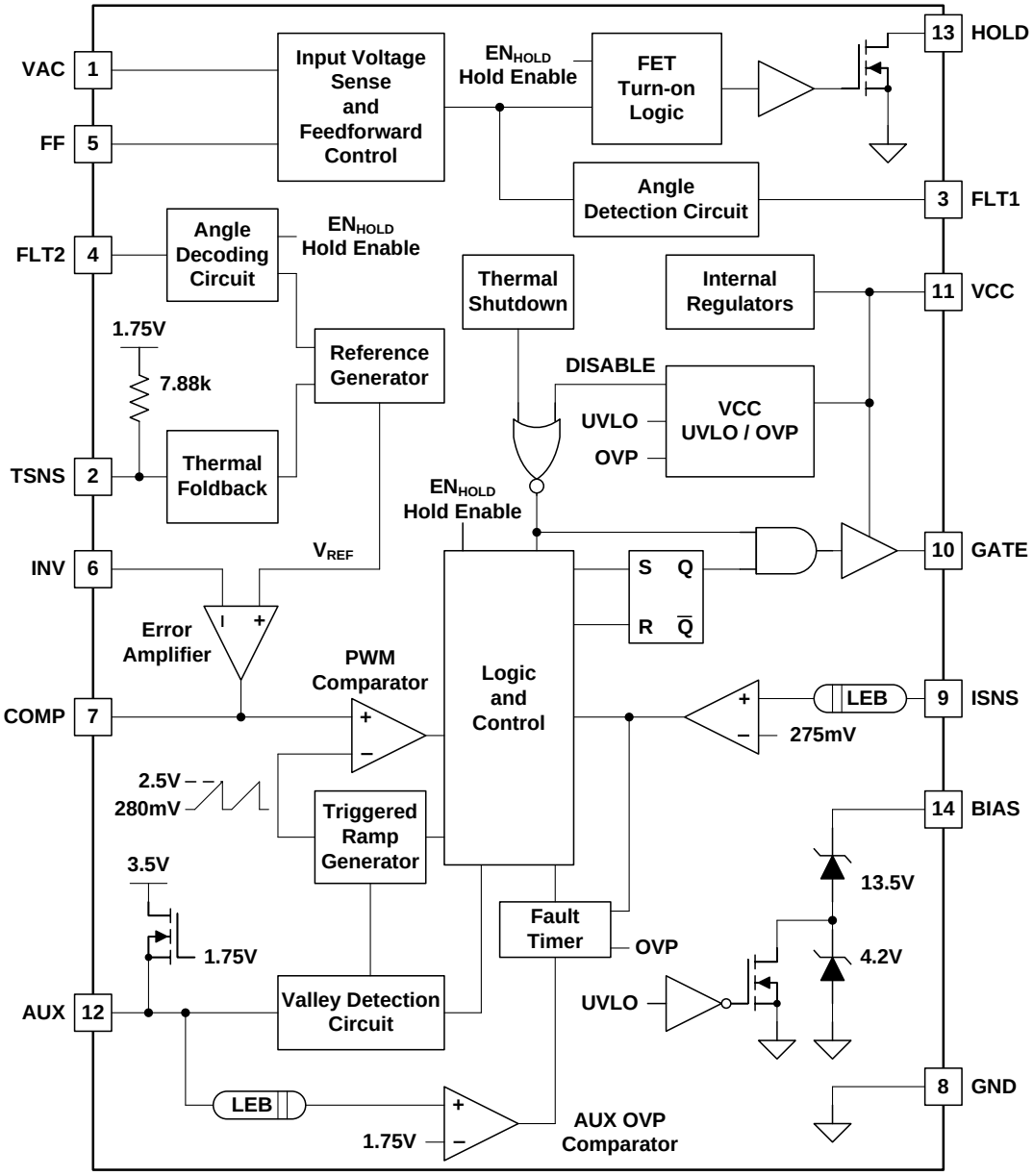
Unless otherwise specified –40°C < T_J = T_A < 125°C, VCC = 14V, V_{TSNS} = 1.75V, V_{FLT2} = 1.75V, V_{AUX} = 0.5V, V_{INV} = 0V, I_{VAC} = 100µA, I_{BIAS} = 100µA, C_{VCC} = 10µF, C_{COMP} = 0.047µF, R_{HLD} = 10kΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE COMPARATOR (ISNS)						
$I_{SNS(TH)}$	Current limit threshold		239	275	305	mV
$R_{ISNS(LEB)}$	ISNS pull down impedance			1.13		kΩ
$t_{ISNS(LEB)}$	Leading edge blanking time			170		ns
ERROR AMPLIFIER (INV, COMP)						
V_{REF}	Reference voltage	V_{FLT2} = 1.5 V, V_{TSNS} = 1.75 V	0.95	1	1.05	V
$I_{INV(BIAS)}$	Input bias current	V_{INV} = V_{REF}		45		nA
G_M	Transconductance	V_{COMP} = V_{REF}		100		µmho
I_{COMP}	Current source capacity	V_{INV} = 0 V		77	104	µA
	Current sink capacity	V_{INV} = 2V	50	77		µA
COMP(LOW)	Minimum PWM ramp voltage	I_{VAC} = 110 µA, V_{INV} = 1 V		280		mV
$D_{(MAX)}$	Maximum duty cycle	I_{VAC} = 110 µA, V_{INV} = 0 V			76.5%	
VALLEY DETECT CIRCUIT (AUX)						
$AUX_{(OVP)}$	Overvoltage protection	V_{AUX} rising	1.67	1.75	1.83	V
$t_{AUX(LEB)}$	AUX leading edge blanking			1.84		µs
$I_{AUX(SOURCE)}$	AUX source current	V_{AUX} = –0.3 V		207		µA
$t_{AUX(TO)}$	Valley detect timeout	V_{AUX} = 1 V		4		µs
PWM OSCILLATOR AND FAULT TIMER						
t_{OSC}	Oscillator period		13.9	14.5	15.1	µs
t_{FAULT}	Fault timer			812		ms
THERMAL FOLDBACK (TSNS)						
$T_{SNS(OC)}$	Open circuit voltage		1.67	1.75	1.83	V
$T_{SNS(TH)}$	Thermal foldback threshold	V_{TSNS} falling	0.955	1	1.045	V
R_{TSNS} (1)	Internal pull-up resistor	T_J = 25°C	7.09	7.88	8.67	kΩ
THERMAL SHUTDOWN						
$T_{SD(TH)}$ (2)	Thermal shutdown temperature			165		°C
$T_{SD(HYS)}$ (2)	Thermal shutdown hysteresis			25		°C

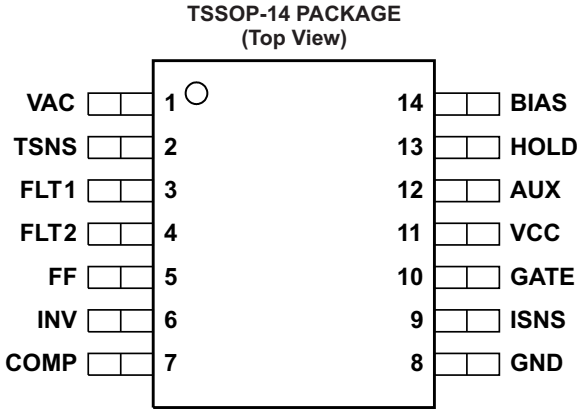
(1) Resistance varies with junction temperature and has typical temperature coefficient of 25ppm/°C.
(2) Device performance at or near thermal shutdown temperature is not specified or assured.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN FUNCTIONS

NO.	NAME	I/O	DESCRIPTION
1	VAC	I	The current at this pin sets the input power level during normal operation. Connect through a resistor to rectified input line voltage.
2	TSNS	I	To implement thermal foldback, connect this pin to an external negative temperature coefficient (NTC) resistor.
3	FLT1	O	This pin is the output of angle sense comparator. Connect a series resistor from this pin to a capacitor to ground to establish the low pass filter bandwidth.
4	FLT2	I	Connect this pin to the output of low pass filter from FLT1 pin to enable dimming. This pin is an input to the internal dim decoder circuitry. For non-dimming applications connect this pin to TSNS.
5	FF	O	Connect a parallel resistor and capacitor from this pin to ground to filter twice the line frequency ripple. This is the output of the input voltage feedforward circuitry.
6	INV	I	This pin is the input of the internal Gm error amplifier. To implement primary side power regulation, connect this to the FF. To implement secondary side current regulation, connect this pin to the output of opto-isolator circuit.
7	COMP	I/O	Output of the Gm error amplifier. Connect a capacitor to ground set desired integral loop compensation bandwidth.
8	GND		Ground return
9	ISNS	I	Connect to the source of the switching MOSEFT and a resistor ground to sense transistor current. Overcurrent protection is engaged when the voltage exceeds 275mV threshold.
10	GATE	O	This output provides the gate drive for the power switching MOSEFT.
11	VCC		This is the input to the internal pre-regulator. Connect a bypass capacitor to ground. This pin enables and disables general functions of the LM3447 using the UVLO feature. Device enters overvoltage protection mode when the voltage is >18.9V.
12	AUX	I	This pin is used to sense the auxiliary winding voltage and perform valley switching operation. Overvoltage protection is engaged when the voltage exceeds the threshold of 1.75V during off time.
13	HOLD		Connect to a holding resistor from the drain of the pre-regulator to this pin. The pin draws current during the zero crossings of the rectified input line voltage.
14	BIAS		Connect to external pre-regulator transistor to enable startup. When VCC is below UVLO threshold the pin is clamped to 17.7V. After VCC crosses UVLO threshold the pin is clamped to 13.5V.

TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C, V_{VCC} = 14 V, V_{TSNS} = 1.75V, V_{FLT2} = 1.75V, V_{AUX} = 0.5V, V_{INV} = 0V, I_{VAC} = 100 µA, I_{BIAS} = 100µA, C_{VCC} = 10 µF, C_{COMP} = 0.047 µF

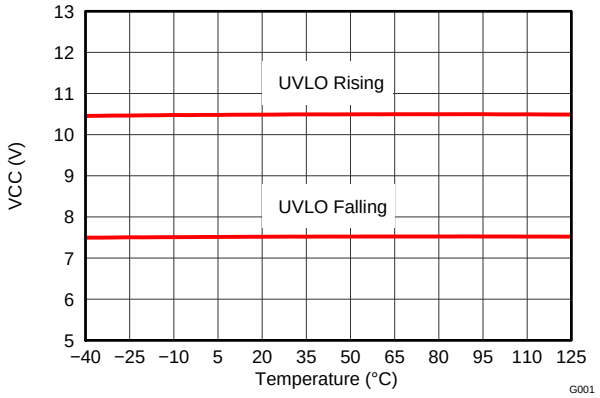


Figure 1. VCC UVLO vs. Junction Temperature

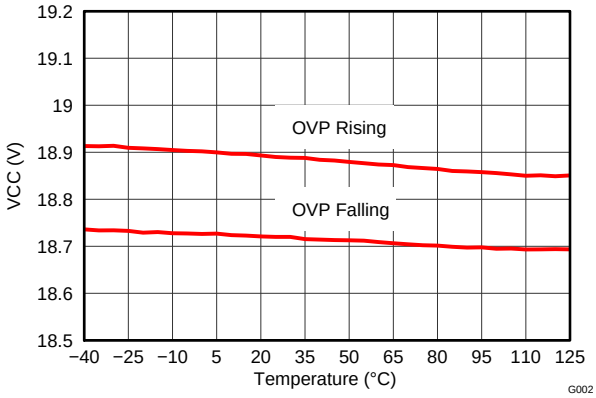


Figure 2. VCC OVP vs. Junction Temperature

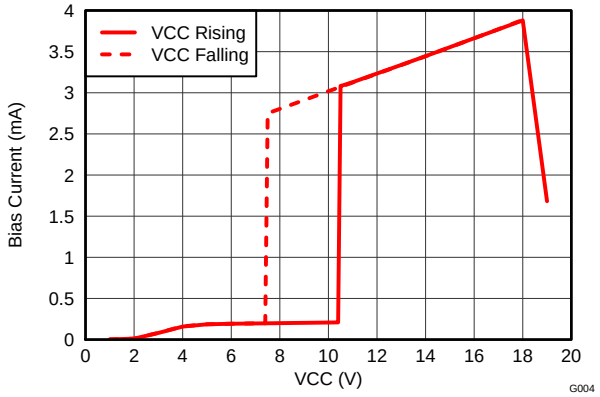


Figure 3. Operational IVCC vs. VCC Voltage

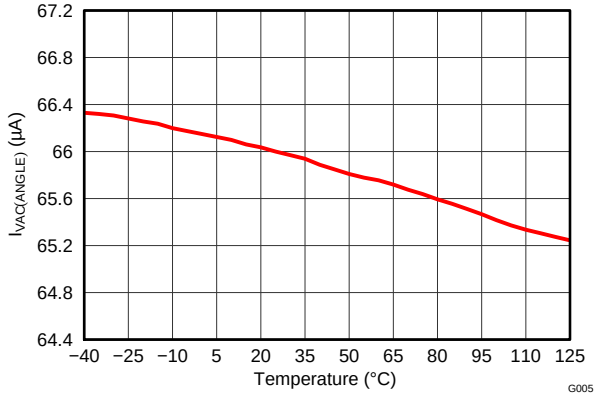


Figure 4. Dimmer Angle Detect Threshold Current vs. Junction Temperature

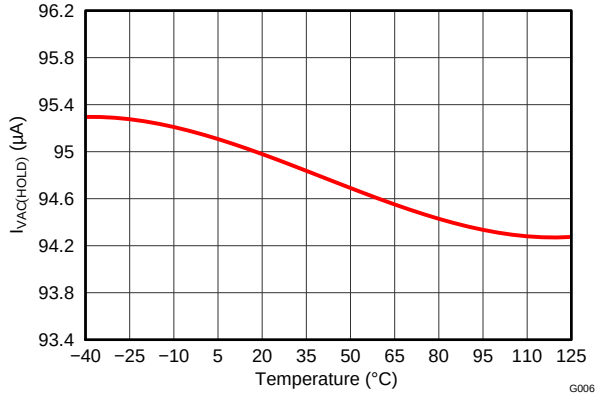


Figure 5. Hold MOSFET Turn-on Threshold Current vs. Junction Temperature

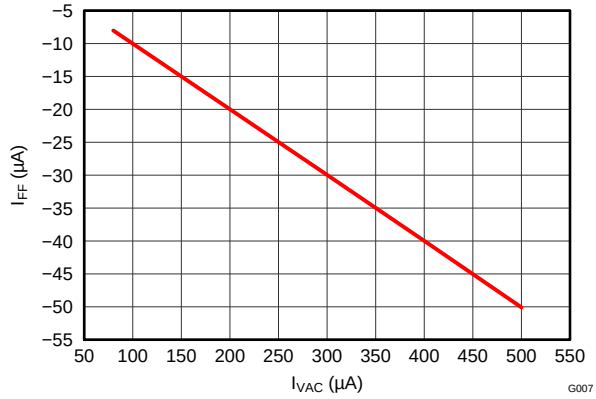


Figure 6. Feedforward Source Current (I_{FF}) vs. VAC Current (I_{VAC})

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C, V_{VCC} = 14 V, V_{TSNS} = 1.75V, V_{FLT2} = 1.75V, V_{AUX} = 0.5V, V_{INV} = 0V, I_{VAC} = 100 µA, I_{BIAS} = 100µA, C_{VCC} = 10 µF, C_{COMP} = 0.047 µF

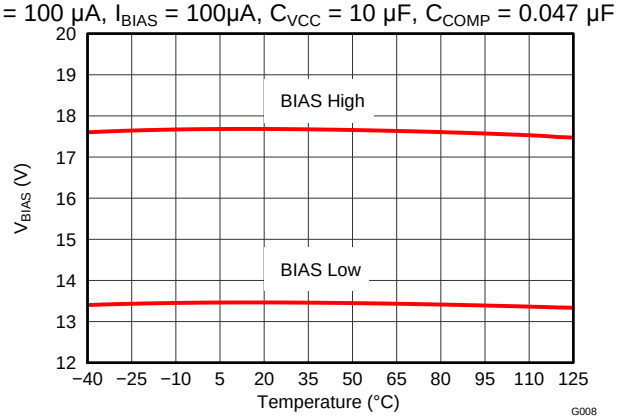


Figure 7. BIAS Clamp Voltage vs. Junction Temperature

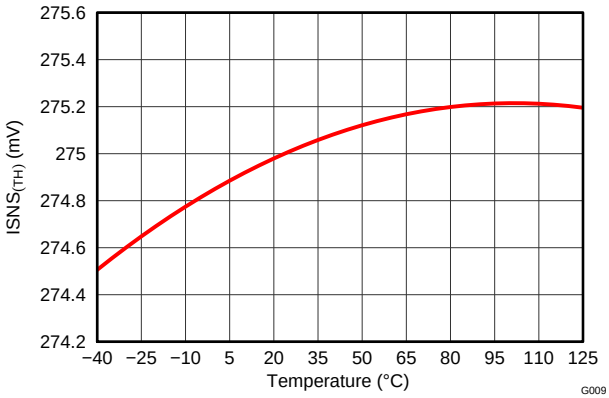


Figure 8. Current Limit Threshold vs. Junction Temperature

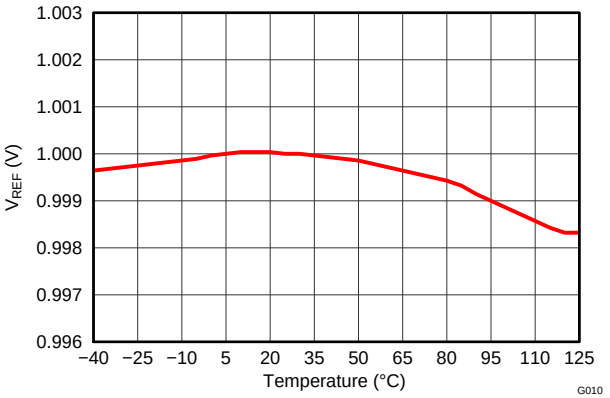


Figure 9. VREF vs. Junction Temperature

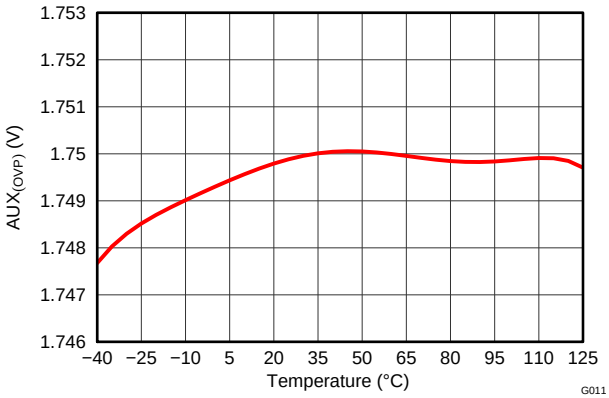


Figure 10. AUX OVP vs. Junction Temperature

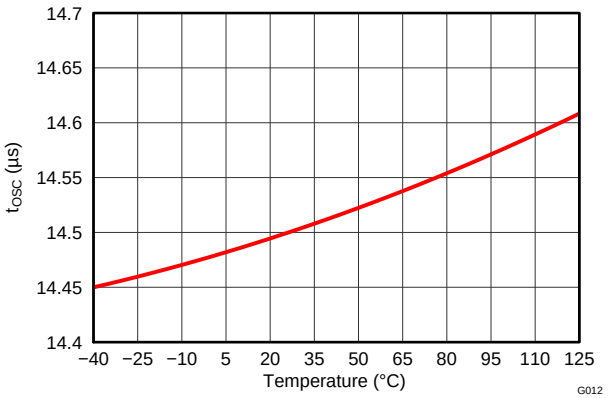


Figure 11. Oscillator Period vs. Junction Temperature

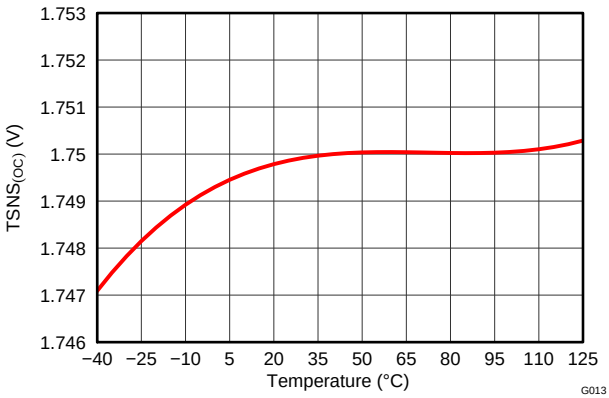


Figure 12. TSNS Open Circuit Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C, V_{VCC} = 14 V, V_{TSNS} = 1.75V, V_{FLT2} = 1.75V, V_{AUX} = 0.5V, V_{INV} = 0V, I_{VAC} = 100 µA, I_{BIAS} = 100µA, C_{VCC} = 10 µF, C_{COMP} = 0.047 µF

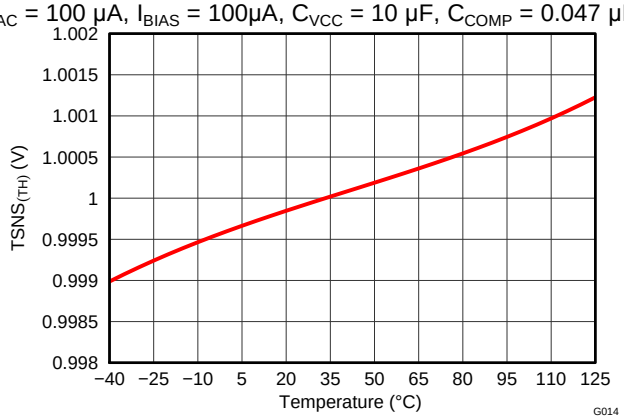


Figure 13. Thermal Foldback Thershold vs. Junction Temperature

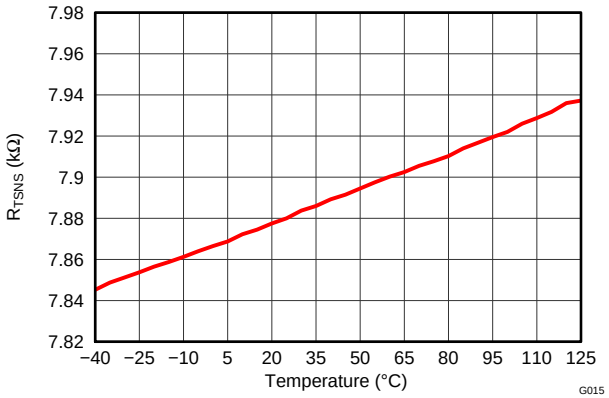


Figure 14. TSNS Internal Pull-up Resistor vs. Junction Temperature

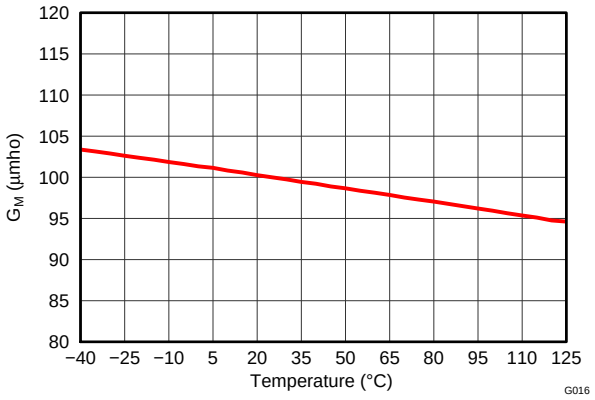


Figure 15. G_M vs. Junction Temperature

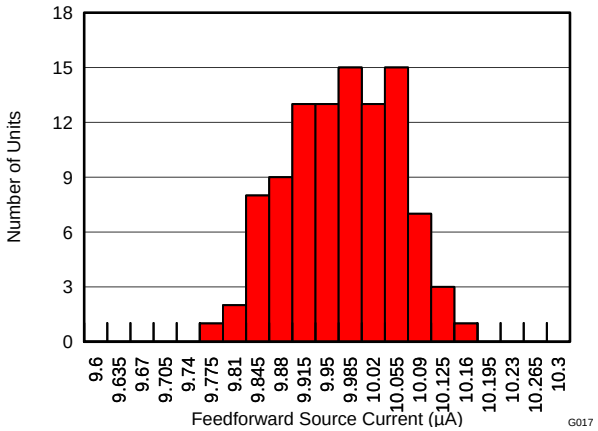


Figure 16. Feedforward Source Current (I_{FF}) Variation (I_{VAC}=100µA, Temperautre = 25°C)

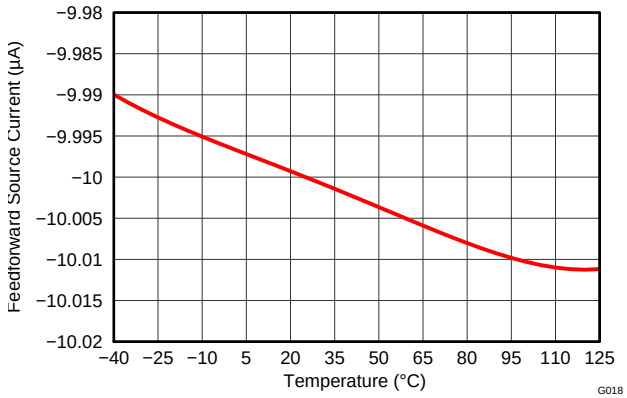


Figure 17. Feedforward Source Current (I_{FF}) vs. Junction Temperature

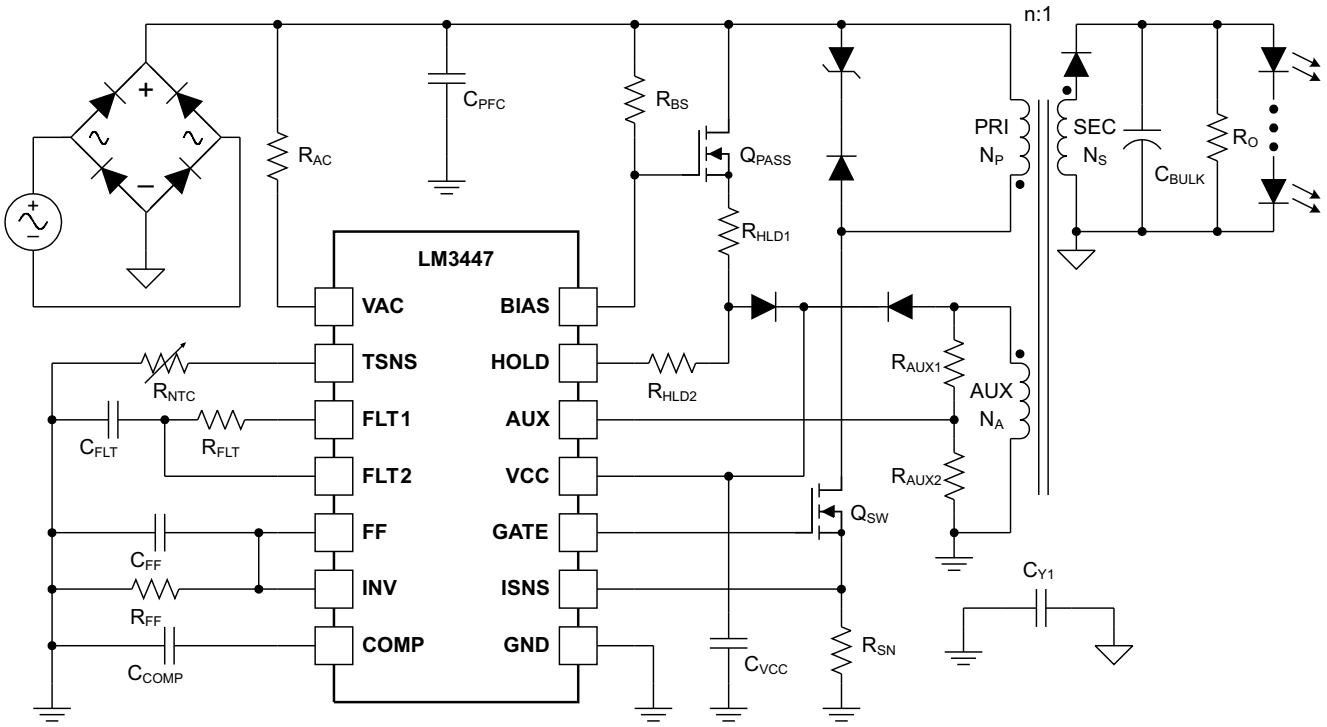


Figure 18. Typical Primary Side Power Regulated Flyback LED Driver

APPLICATION INFORMATION

DESCRIPTION

LM3447 is an AC-DC power factor correction (PFC) controller for phase-cut dimmer compatible LED lighting applications. The device incorporates an innovative primary side input power regulation technique for controlling the LED light output over a wide input AC voltage and ambient temperature range. Operating LEDs with constant power allows the controller to compensates for the LED forward voltage variations caused by temperature modulation and LED aging. This also provides improved lamp lumen output maintenance and higher luminous efficacy.

Smooth, flicker free LED dimming is performed by varying the power regulation set-point based on the dimmer phase angle. The device includes internal angle detection and decoding circuitry to accurately interpret the phase angle from a forward phase (leading edge) and reverse phase (trailing edge) based dimmers Power factor correction (PFC) with low input current total harmonic distortion (THD) is maintained by forcing discontinuous conduction mode (DCM) using a trimmed internal oscillator and valley detect circuitry.

These features, along with LED open circuit and short circuit protection, LED thermal foldback and cycle-by-cycle FET overcurrent protection, make the LM3447 an ideal device for implementing a compact single stage isolated Flyback AC-DC LED driver for 5–30W power output range. In addition, it is also possible to configure LM3447 with minor modifications to control SEPIC and Cúk based dimmable AC-DC PFC LED drivers. In this datasheet, a discussion of the LM3447 functionality is presented using a typical Flyback LED driver circuit, as shown in Figure 18.

VCC BIAS SUPPLY AND START-UP

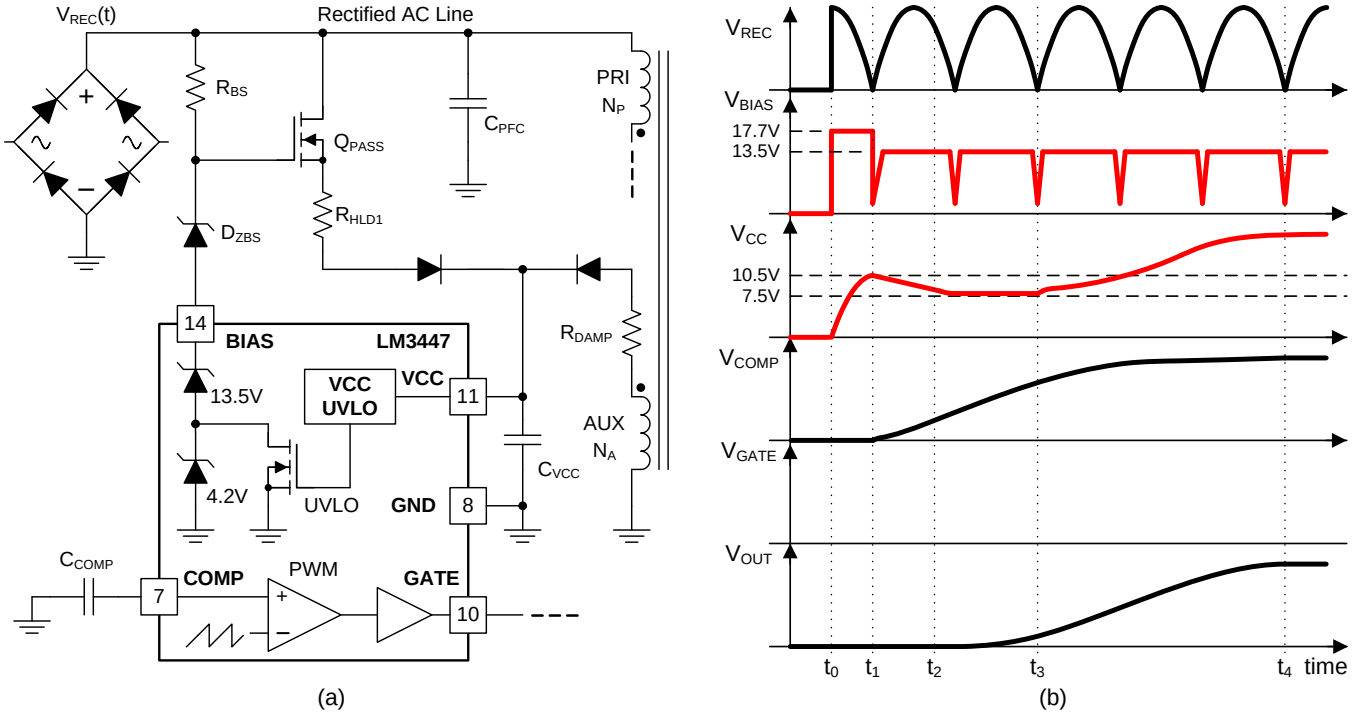


Figure 19. (a) Bias Circuit and (b) Typical Startup Waveforms

The LM3447 is designed to achieve instant turn-on using an external linear regulator circuit, shown in Figure 19 (a). The start-up sequence is internally controlled by the BIAS voltage and VCC undervoltage lockout (UVLO) circuit and is illustrated in Figure 19 (b). The BIAS input is a low current voltage clamp circuit that provides a reference to the linear pass transistor, Q_{PASS}. The clamp circuit current is set by connecting resistor, R_{BS}, between the input rectified AC voltage, V_{REC} and BIAS. When power is applied, the BIAS voltage set to 17.7V and the capacitor, C_{VCC} is rapidly charged by transistor Q_{PASS}. Resistor R_{HLD1} is used to limit the maximum allowable current, based on the safe operating area (SOA) rating of the transistor. The LM3447 starts operating when VCC exceeds the UVLO rising threshold of 10.5V, after which the BIAS voltage is reduced to 13.5V. The GATE drive output is enabled when the COMP voltage exceeds the minimum internal PWM ramp threshold of 280mV. As the output voltage, V_{OUT}, increases, the bootstrap circuit based on an auxiliary winding of the transformer is energized and begins delivering power to the device. At any time, if VCC falls below 7.5V the device enters a UVLO state forcing BIAS to step back to 17.7V to initiate a new start-up sequence. The switching of BIAS voltage between two thresholds, 17.7V to 13.5V, is performed in association with a large VCC UVLO hysteresis of 3V to allow for a larger variation in auxiliary output voltage.

The key waveforms illustrating the bias circuit operation and start-up sequence under dimming are shown in Figure 20. The impact of phase-cut dimming on BIAS, V_{OUT} and VCC behavior is highlighted. The chopping of the input voltage by an external dimmer causes the output voltage, V_{OUT}, to vary along with LED current. As VCC voltage tracks the output voltage, V_{OUT}, it too fluctuates based on the dimming command. At low dimming levels, UVLO is engaged as VCC falls below 7.5V and the BIAS switches to 17.7V, initiating a start-up sequence. The BIAS behavior interacts with the external dimmer circuit, causing the device to enter into a re-start condition, where VCC fluctuates between UVLO high and low thresholds. With this mode of operation, the LM3447 is capable of providing quick response to any changes in the dimming command. In the case where the external dimmer is switched off, VCC is discharged and all of the device operation is ceased. A new start-up cycle is initiated, when the dimmer is switched on and the device responds in the manner illustrated in Figure 19 (b).

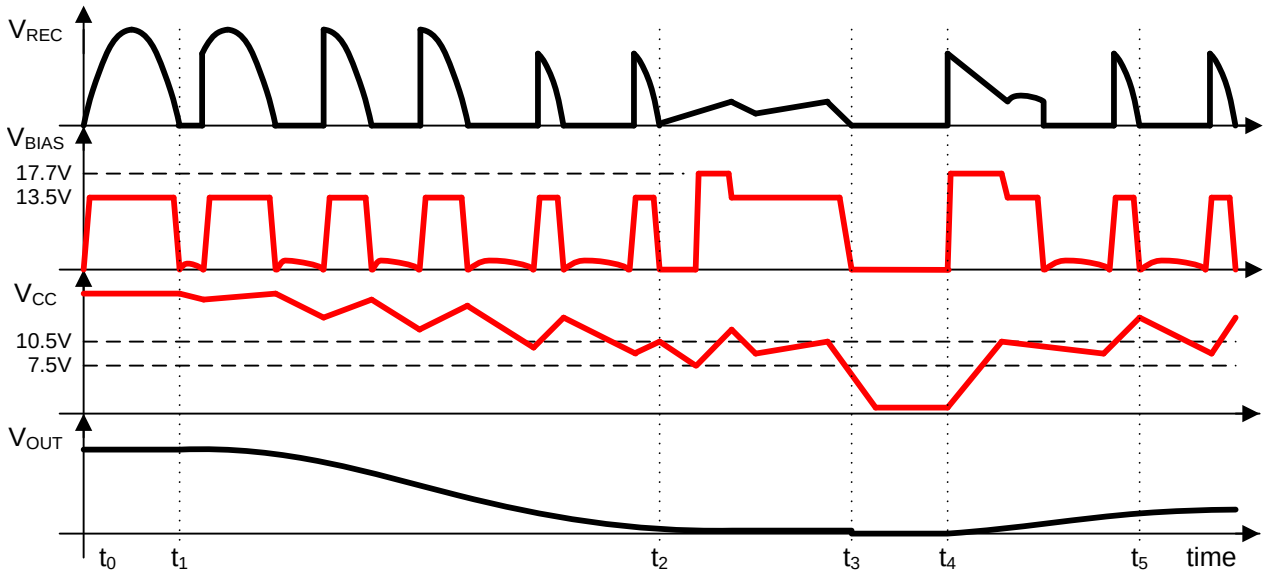


Figure 20. Typical Waveforms and Start-up Sequence Under Dimming Conditions

The value of capacitor C_{VCC} is critical design parameter as it determines VCC ripple voltage during dimming operation. A X7R ceramic capacitor with value ranging from 22µF to 47µF and 25V voltage rating is recommended for C_{VCC} as trade-off between size and performance in space constraint applications. At low dimming levels, large VCC voltage ripple and Q_{PASS} threshold voltage variations can intefere with smooth dimming performance. An external zener doide, D_{ZBS}, can be placed in series with BIAS to boost VCC voltage and eliminate any observable dimming discontinuities. A low power zener diode (200mW) with reverse breakdown voltage ranging from 1.8V to 4.5V is recommended for most dimming application.

VCC OVERVOLTAGE PROTECTION

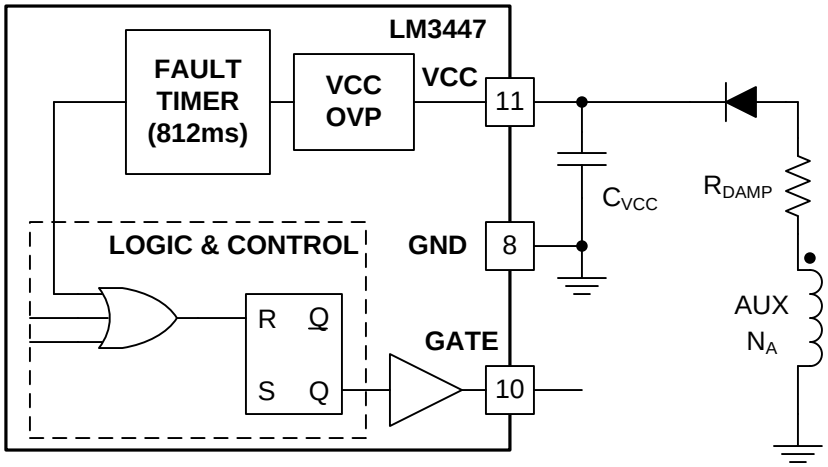
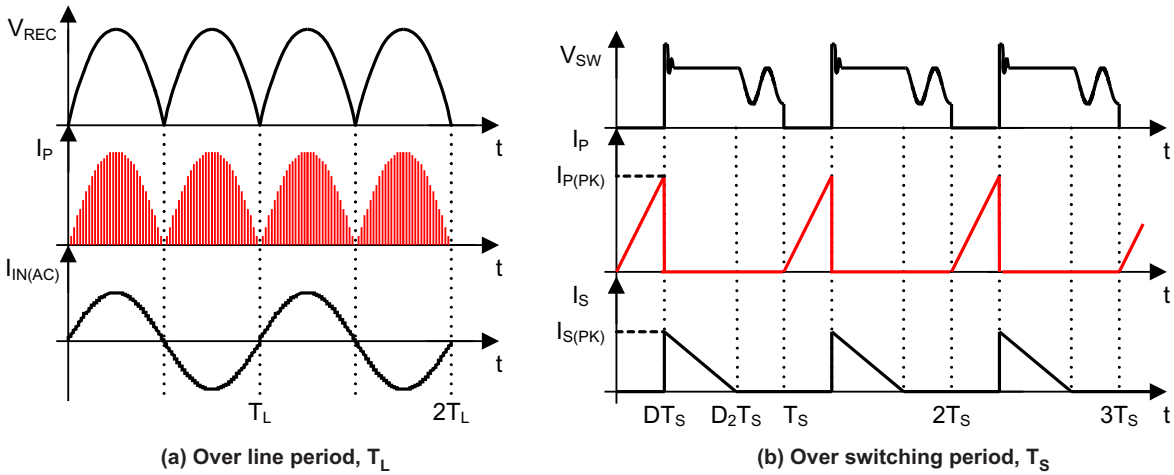


Figure 21. VCC Overvoltage Protection Circuit

The LM3447 has a built-in overvoltage protection (OVP) mode to protect VCC from exceeding its ABS MAX rating under fault conditions. The VCC voltage is monitored by a comparator with a rising threshold of 18.9V and 175mV of hysteresis. Upon detecting an overvoltage condition, GATE is pulled low for duration of 812ms, determined by the internal fault timer. On clearance of the fault, the timer is disabled and normal device operation resumes. An optional damping resistor, R_{DAMP} in series with the auxiliary winding can be used to prevent transformer leakage current from peak charging C_{VCC} and false triggering the OVP circuit. Based on the magnitude of leakage inductance a resistor of 10Ω to 47Ω should provide proper damping.

POWER FACTOR CORRECTION



(a) Over line period, T_L (b) Over switching period, T_S

Figure 22. DCM Flyback PFC Waveforms

Power factor correction is performed by operating the Flyback converter in discontinuous conduction mode (DCM). In this mode, the peak primary current, $I_{P(PK)}$ is given by

$$I_{P(PK)} = \frac{v_{REC}(t)}{L_M} DT_S = \frac{\|v_{in}(t)\|}{L_M} DT_S, \text{ for} \tag{1}$$

$$v_{in}(t) = V_{IN(PK)} \sin\left(\frac{2\pi}{T_L} t\right), \tag{2}$$

where $v_{IN}(t)$ is the input voltage, $v_{REC} = \|v_{in}\|$ is the rectified input voltage, L_M is the transformer magnetizing inductance referred to the primary winding, D is the duty cycle, T_S is the switching period and T_L is the line period. For a fixed switching frequency controller, if duty cycle D, is held constant over a line cycle, then the peak primary current, $I_{P(PK)}$, varies in proportion to input voltage, $v_{IN}(t)$, as shown in Figure 22 (a). The resulting input current, I_{IN}, is obtained by averaging the area under primary current, I_P, shown in Figure 22 (b),

$$i_{in}(t) = \text{Average}\left(I_P\right)\Big|_{T_S} = \frac{1}{2}\frac{v_{in}(t)}{L_M} D^2 T_S, \tag{3}$$

is sinusoidal and in-phase with input voltage, $v_{IN}(t)$. As a result, the DCM Flyback converter behaves much like a resistor and exhibits a power factor close to unity.

The input power, $P_{IN(AVG)}$ drawn by the Flyback PFC is derived by averaging the product of input voltage, $v_{in}(t)$ and input current, $i_{in}(t)$, over half line cycle $T_L/2$,

$$P_{IN(AVG)} = \frac{2}{T_L}\int_0^{T_L/2} v_{in}(t) \times i_{in}(t)dt = \frac{2}{T_L}\int_0^{T_L/2} \frac{1}{2}\frac{V_{IN(PK)}^2 D^2 T_S}{L_M} \sin^2\left(\frac{2\pi}{T_L} t\right)dt; \tag{4}$$

$$P_{IN(AVG)} = \frac{1}{4}\frac{V_{IN(PK)}^2 D^2 T_S}{L_M} = \frac{V_{IN(RMS)}^2}{\left(\frac{2L_M}{D^2 T_S}\right)} = \frac{V_{IN(RMS)}^2}{R_e}; \; R_e = \frac{2L_M}{D^2 T_S}, \tag{5}$$

The low frequency behavior of the DCM Flyback is defined by an effective resistance, R_e. The expression for average input power is given by Equation 5 and is based on R_e and the input RMS voltage $V_{IN(RMS)}$. For a single stage Flyback PFC driver, the output power, P_{OUT}, delivered to the LED load is a function of the converter efficiency, η_{FLY}, and is given by

$$P_{OUT} = \eta_{FLY} P_{IN}. \tag{6}$$

The average LED current through the string with forward voltage drop $V_{LED} = V_{OUT}$ is

$$I_{LED(AVG)} = \frac{P_{OUT(AVG)}}{V_{OUT}} = \eta_{FLY}\frac{P_{IN(AVG)}}{V_{OUT}} = \eta_{FLY}\frac{V_{IN(RMS)}^2}{V_{OUT}R_e}, \quad (7)$$

The LED current will have a ripple component varying at twice line frequency due to the PFC operation. The magnitude of the ripple component is based on the energy storage capacitor connected in parallel with the LED string at the output of Flyback PFC. In typical application, a low voltage aluminum electrolytic bulk capacitor is used as an energy storage device and is connected across the LED string to limit the ripple current within an acceptable range.

INPUT POWER REGULATION AND INPUT VOLTAGE FEEDFORWARD CONTROL

Using the LM3447, it is possible to regulate the LED current by implementing a control scheme using the duty cycle, D, as the control variable. The duty cycle is generated using an internal GM error-amplifier and a fixed frequency, triggered ramp generator, as shown in Figure 23. This technique should not be confused with other current mode control schemes where switch current, I_{SW}, is used for control.

With the LM3447, LED current can be directly controlled using a series sense resistor and a conventional closed-loop feedback control scheme. Typically, for systems that need galvanic isolation between primary and secondary sides of the transformer, feedback control is complicated and expensive as it requires an additional signal processing amplifier and an opto-isolator. For improved luminous efficacy and simplicity, the LM3447 incorporates an innovative primary side input power regulation scheme based on input voltage feedforward control techniques. By commanding input power, the DCM Flyback PFC output is matched with the LED load characteristics to achieve indirect control of LED string current. The feedforward loop, consisting of input voltage sensing circuitry, the G_M error amplifier and PWM comparator, is able to reject any input voltage disturbance by adjusting the duty cycle, thus achieving tight line regulation.

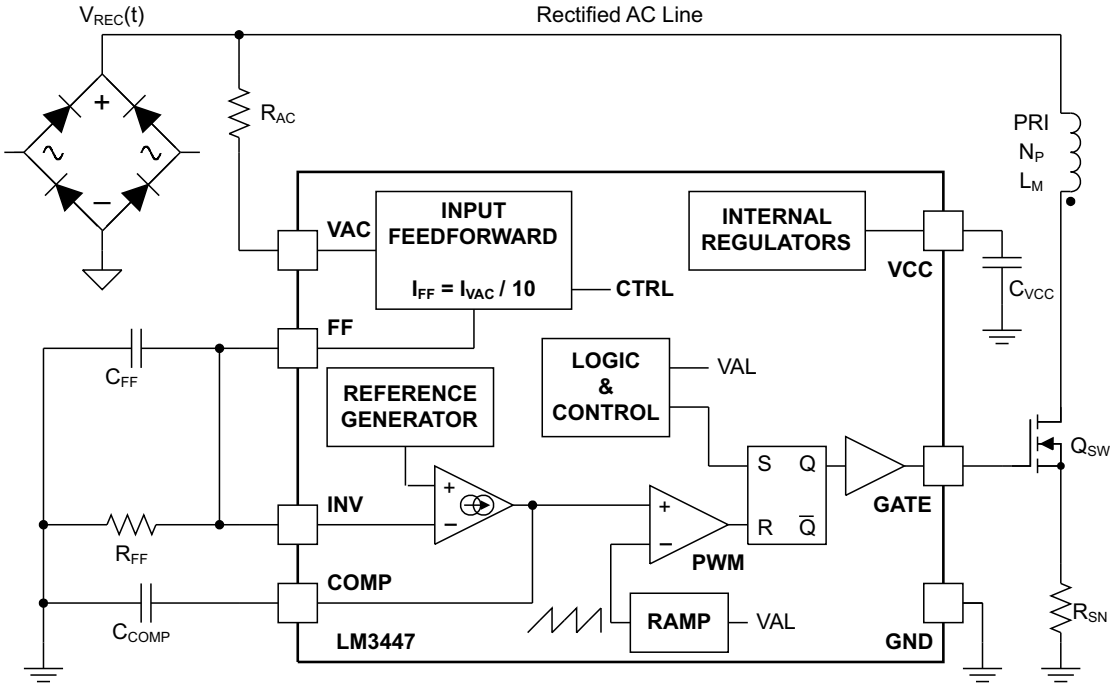


Figure 23. Feedforward Control Circuit

The reference power level, P_{IN}, for the LM3447, is set choosing resistors, R_{FF} and R_{AC}, based on the magnetizing inductance, L_M, the internal reference voltage, V_{REF}, the switching frequency, f_S and the feedforward gain, G_{FF}, such that

$$\frac{R_{FF}}{R_{AC}} = \frac{\pi}{4}\frac{G_{FF}V_{REF}}{\sqrt{L_M P_{IN} f_S}} \quad (8)$$

The feedforward gain, $G_{FF} = I_{VAC}/I_{FF} = 10$ and internal reference voltage $V_{REF} = 1$ V.

For the above relationship to be valid and for PFC, it is necessary to ensure that the energy in the magnetizing inductor, L_M, is reset every switching cycle and the power stage operates in DCM for the reference power level, P_{IN}, over the entire range of input voltages. Based on this constraint, the transformer magnetizing inductor should be chosen as

$$L_M \le \frac{V_{REF}}{4P_{IN} f_S \left(\frac{1}{nV_{OUT}} + \frac{1}{V_{REC(PK,MIN)}} \right)^2}, \quad (9)$$

where n is the transformer primary to secondary turns-ratio, $V_{OUT} = V_{LED}$ is the LED string voltage and $V_{REC(PK,MIN)}$ is the minimum peak rectified input voltage. For the LM3447 internal circuit implementation, shown in Figure 23, the reference voltage, V_{REF} = 1V and the feedforward gain, G_{FF} = 10. To ensure a robust design and to reject manufacturing variations, a margin of 2% to 10% should be provided when designing the transformer for magnetizing inductance calculated using Equation 9.

A small capacitor, C_{FF} is connected in parallel with the resistor R_{FF}, to create a low pass filter that can attenuate twice the line frequency component from the sensed input voltage. It is recommended to set the filter pole frequency between 10–12Hz to provide 20dB attenuation, such that

$$C_{FF} \ge \frac{1}{2\pi(10\ Hz - 12\ Hz)R_{FF}}, \quad (10)$$

Slow integral compensation is achieved by placing a compensation capacitor C_{COMP} at the output of the G_M amplifier. A capacitor value ranging from 4.7µF to 10µF is recommended to achieve a low bandwidth loop of 1Hz to 10Hz, based on the power level and transient response.

AUX CIRCUIT AND VALLEY DETECT

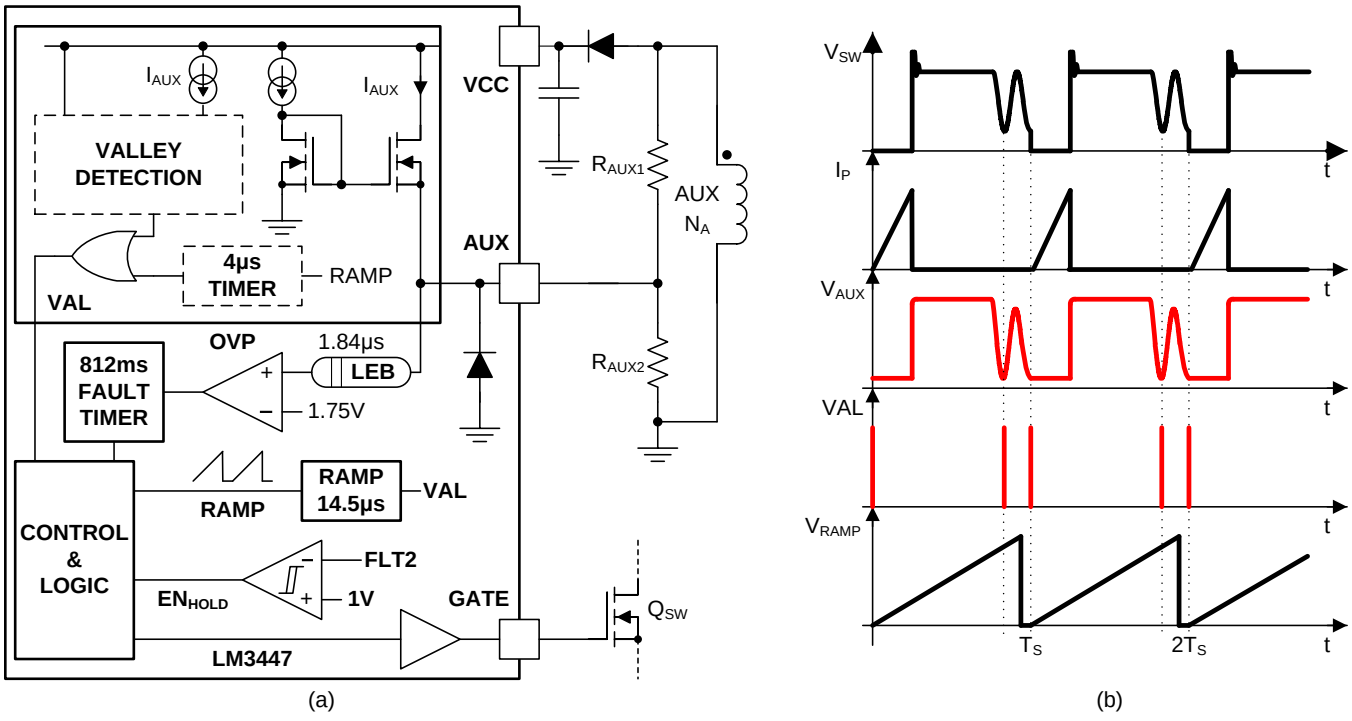


Figure 24. (a) AUX Circuit; (b) Valley Switching Waveforms

Valley switching is implemented by connecting the transformer auxiliary winding to the AUX input of LM3447 through a resistor divider network, R_{AUX1} and R_{AUX2}, as shown in Figure 24 (a). The valley level is detected by monitoring the current sourced out of the AUX pin when the voltage at the auxiliary winding of the transformer is negative with respect to the GND node. The voltage at this node is clamped at approximately 100mV by the internal circuitry to protect the device during negative voltage excursions of the auxiliary winding. The waveforms in Figure 24(b) illustrate the sequence of events that have to occur for the LM3447 to initiate a new switching cycle.

An internal 14.5µs timer is started at the same time as the switching FET (Q_{SW}) is turned on. This 14.5µs timer, set by the internal ramp rise time, is used to set the maximum frequency. After this timer expires the switching FET (QSW) is allowed to turn back on if a valley is detected (VAL) or the 4µs ($t_{AUX(TO)}$) catch timer expires. The catch timer starts immediately after the Ramp signal drops and sets the lowest operating frequency.

The particular valley (1^{st}, 2^{nd} …) in the ringing waveform, where the switch is enabled is a function of the input voltage and varies over the half line cycle. As a result, the AUX circuit shows increased sensitivity where the valley detect signal, VAL, overlaps the Ramp period. Here, the switching point is observed to randomly jump between two adjacent valleys, causing a discrete change in the switching period. Such perturbations in switching frequency cause the switching ripple component of the input current to increase and interfere with phase dimming performance. Therefore, valley switching is disabled and hard switching operation with fixed Ramp period is initiated on detection of external phase dimmers, as shown in Figure 25. The valley switching operation is controlled by the FLT2 input. The operation is disabled when the VFLT2 falls below 1V and is enabled again when it rises above 1.2V. A 200mV hysteresis is provided for noise immunity.

A second function of AUX pin is to program the output overvoltage protection or open-LED detection feature. The output voltage is monitored by sampling the voltage at the auxiliary winding. The voltage is sampled after a fixed delay of 1.84µs, from the falling edge of the GATE drive signal. The leading edge blanking circuit helps reject the voltage transients caused by the leakage energy of the transformer thus preventing false tripping of OVP. The fault condition is detected when the AUX voltage exceeds the internal threshold, $V_{AUX(OVP)}$ (1.75V). In the case of an overvoltage fault, the switch is turned off for 812ms before attempting to restart the circuit. During this fault period, the compensation capacitor (C_{COMP}) is discharged, and the control loop is disabled. When the fault is cleared, the 812ms fault timer is disengaged and the control loop is activated to resume normal operation.

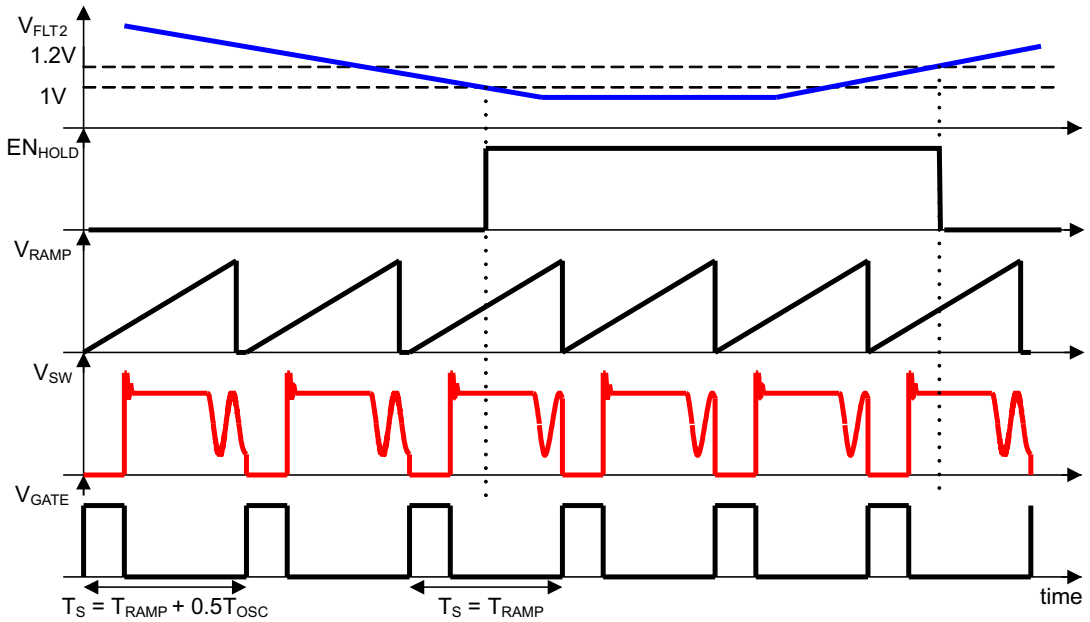


Figure 25. Waveforms Illustrating Valley Switching Enable and Disable Sequence

The sizing of resistor R_{AUX1} and R_{AUX2} govern the AUX circuit behavior. Resistor R_{AUX1} is also used to limit the maximum source current from the AUX pin to 200µA and is based on the maximum input voltage and the transformer primary to auxiliary turns-ratio;

$$R_{AUX1} = \frac{N_A}{N_P} \frac{V_{REC(PK,MAX)}}{200 \times 10^{-6}}, \quad (11)$$

Resistor R_{AUX2} is then selected to set the desired output overvoltage threshold, $V_{OUT(OVP)}$ based on the secondary to auxiliary turns-ratio

$$R_{AUX2} = \left(\frac{1.75}{\frac{N_A}{N_S} V_{OUT(OVP)} - 1.75} \right) R_{AUX1}, \quad (12)$$

It is necessary to select the transformer's secondary to auxiliary turns-ratio (N_A/N_S) to ensure that $V_{AUX(OVP)}$ is tripped before $VCC_{(OVP)}$.

CURRENT SENSE AND OVERCURRENT PROTECTION

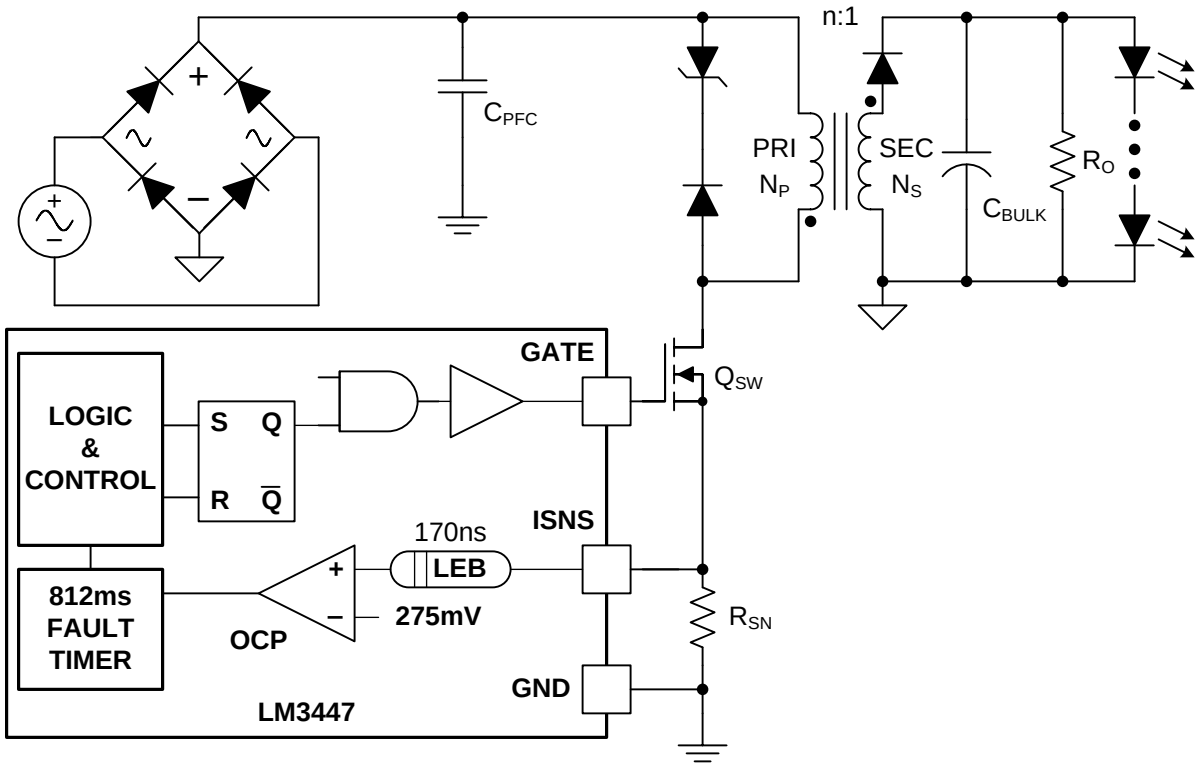


Figure 26. Current Sense Circuit

The LM3447 provides switch overcurrent and LED short circuit protection by sensing the current through the switching transistor, Q_{SW} via a series connected sense resistor, R_{SN}, as shown in Figure 26. At the beginning of each switching cycle, the Leading Edge Blanking (LEB) circuit pulls the ISNS input low for approximately 170ns. This prevents false tripping of the protection circuit due to voltage spikes caused by switch turn on transients. The cycle-by-cycle current limit is realized by comparing the sensed voltage at ISNS with the internal 275mV overcurrent protection threshold. When the sense voltage exceeds 275mV, the switch is immediately turned off for a duration of 812ms, set by the fault timer and the COMP capacitor, C_{COMP} is discharged. Under fault conditions, the LM3447 enters a hiccup mode, attempting to restart the circuit after a duration of 812ms. Upon clearance of the fault, normal operation resumes.

The overcurrent limit is set by selecting the sense resistor, R_{SN}. It is typical to limit the switch current to two times the maximum peak primary current, $I_{P(PK,MAX)}$, where

$$I_{P(PK,MAX)} = 2\sqrt{\frac{P_{IN} T_S}{L_M}}, \quad (13)$$

and

$$R_{SN} = \frac{275 \times 10^{-3}}{2I_{P(PK,MAX)}} \quad (14)$$

For R_{SN} It is recommended to use a film type SMD resistor, with power rating greater than P_{SN} and with low ESL.

ANGLE DETECT CIRCUIT

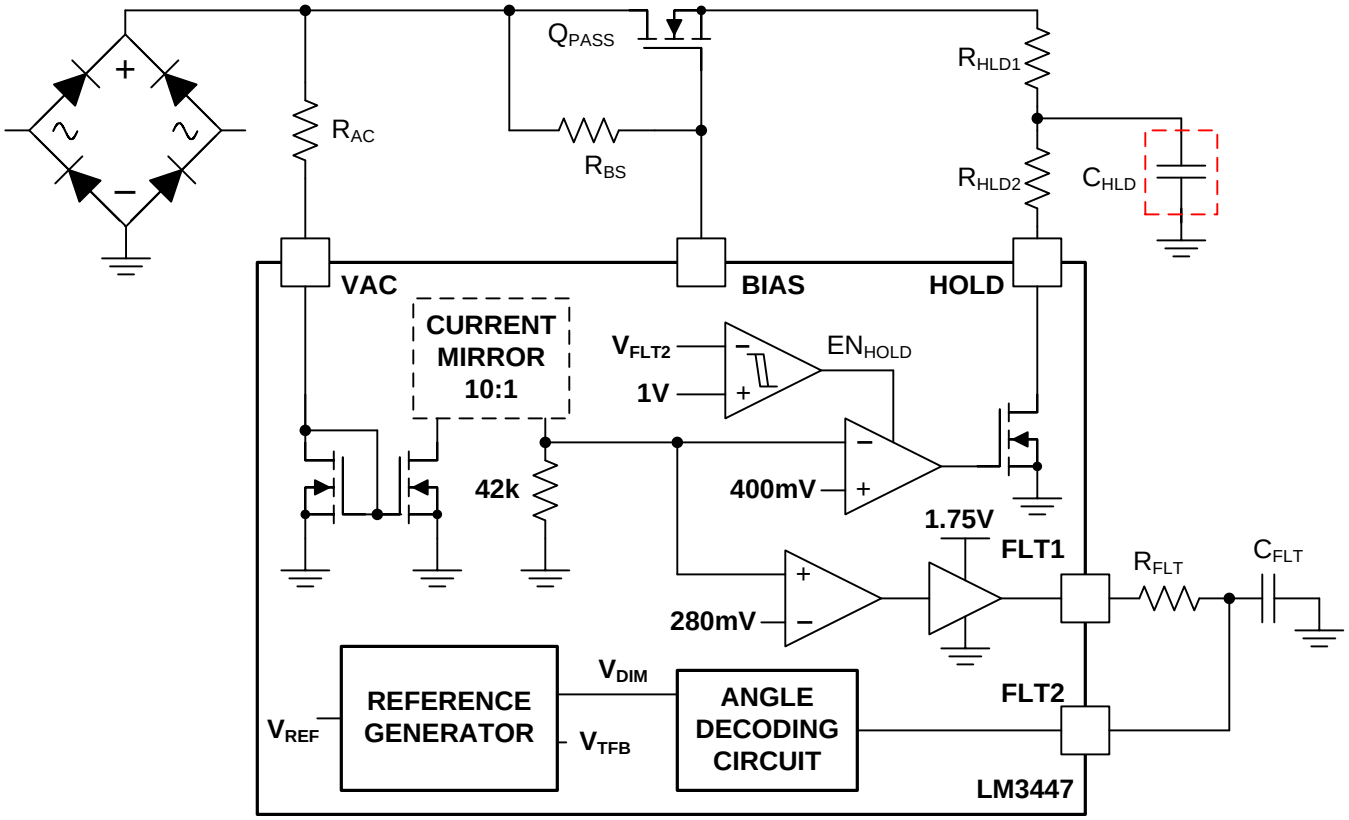


Figure 27. Phase Angle Detection and HOLD Current Circuit

The LM3447 uses the input voltage, V_{REC}, to detect the conduction phase angle. Figure 27 shows the LM3447 angle detect circuit, where the input voltage, V_{REC}, is scaled by the current mirror circuits and re-generated across an internal 42kΩ resistor. This replica of the input voltage is compared with internal 280mV reference to obtain the conduction information. The resulting PWM signal, with its on-time proportional to the conduction period, is buffered and supplied through the FLT1 pin, as shown in Figure 28. To match the external phase dimmer characteristics with the LM3447 decoding circuit and prevent EMI filter capacitors from interfering with dimming operation, it is necessary to select an angle detection threshold, $V_{ADET(TH)}$. This threshold can then be programmed using the resistor, R_{AC}, such that

$$R_{AC} = \frac{V_{ADET}}{I_{VAC(ANGLE)}} = \frac{V_{ADET}}{66 \times 10^{-6}}. \quad (15)$$

For best results, set $V_{ADET(TH)}$ as follows:

- 25V to 40V for 120V systems
- 50V to 80V for 230V systems

Resistor R_{AC} should also limit the VAC current under worst case operating conditions. The value of R_{AC} should be optimized to meet both angle detect, V_{ADET}, and VAC current, I_{VAC} constraints.

HOLD CURRENT CIRCUIT

The LM3447 incorporates an efficient hold current circuit to enhance compatibility with TRIAC based leading edge dimmers. Holding current from an external dimmer is drawn before the Flyback PFC circuit through the pass transistor, Q_{PASS} and limited by resistors R_{HLD1} and R_{HLD2}, as shown in Figure 27. It should be noted that the additional current drawn has no effect on the rectified input voltage and therefore does not interfere with the input power regulation control scheme.

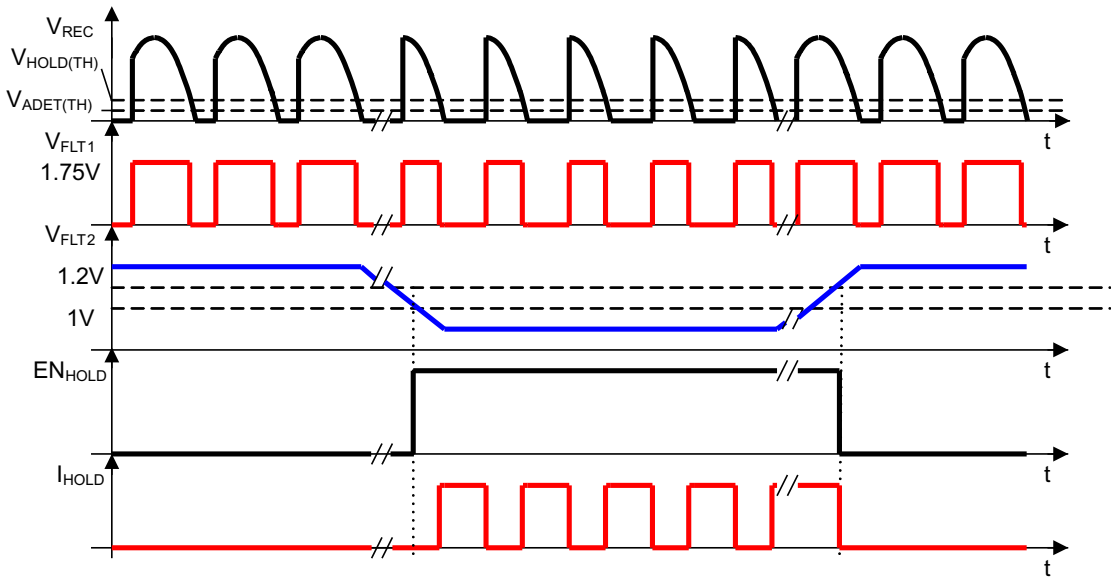


Figure 28. Angle Detection Circuit and Hold Current Circuit Operation

To provide high efficiency, the hold circuit is enabled only when the presence of an external dimmer is detected based on the FLT2 input. The EN_{HOLD} signal is asserted and hold operation is permitted when V_{FLT2} falls below 1V. The hold operation is halted when V_{FLT2} rises above 1.2V. During dimming, the hold current is drawn during the interval when rectified input voltage is below the $V_{HOLD(TH)}$, based on the external resistor R_{AC}. The FET turn-on is controlled by an internal comparator with a reference of 400mV (higher than angle detect reference), such that hold current is always asserted before angle detect threshold $V_{ADET(TH)}$. The hold circuit operation is summarized in Figure 28. The hold trun-on threshold, $V_{HOLD(TH)}$ is given by

$$V_{HOLD(TH)} = R_{AC} I_{VAC(HOLD)} = 95 \times 10^{-6} R_{AC}. \quad (16)$$

The hold current is based on the BIAS voltage and set by the sum of resistors R_{HLD1} and R_{HLD2},

$$I_{HOLD} = \frac{13.5 - V_{GS(PASS)}}{(R_{HLD1} + R_{HLD2})}. \quad (17)$$

In selecting the hold current level, it is critical to consider its impact on the average power dissipation and the operating junction temperature of pass transistor, Q_{PASS} under worst case operating conditions. The current should be limited to a safe value based on the pass transistor specifications or the ABS MAX rating of LM3447 (70mA). For best performance, it is recommended to set the hold current magnitude between 5mA and 20mA. A capacitor, C_{HLD} of 2.2µF to 10µF, from R_{HLD2} to GND is connected to limit the rate of change of input current (di_{in}/dt) caused by the step insertion of holding current. This prevents TRIAC based dimmers from misfiring at low dimming level.

ANGLE DECODING CIRCUIT AND DIMMING

The LM3447 incorporates a linear decoding circuit that translates the sensed conduction angle into an internal dimming command, V_{DIM}. The conduction angle information, represented by the PWM signal at FLT1 output, is processed by an external low pass filter consisting of resistor, R_{FLT} and capacitor, C_{FLT}, which attenuates the twice line frequency component from the signal. The resulting analog signal at FLT2 is converted into the dimming command by a linear analog processing circuit. The piecewise linear relationship between the FLT2 input and the dimming command is shown graphically in Figure 29.

The dimming command, V_{DIM} is

- held constant at 1V for V_{FLT2} ranging from 1.75V to 1.45V (conduction angle 180° to 150°)
- linearly varied with gain of 0.877 for V_{FLT2} ranging from 1.45V to 280mV (conduction angle 150° to 30°)
- saturated at 13mV for V_{FLT2} lower than 280mV (conduction angle less than 30°)

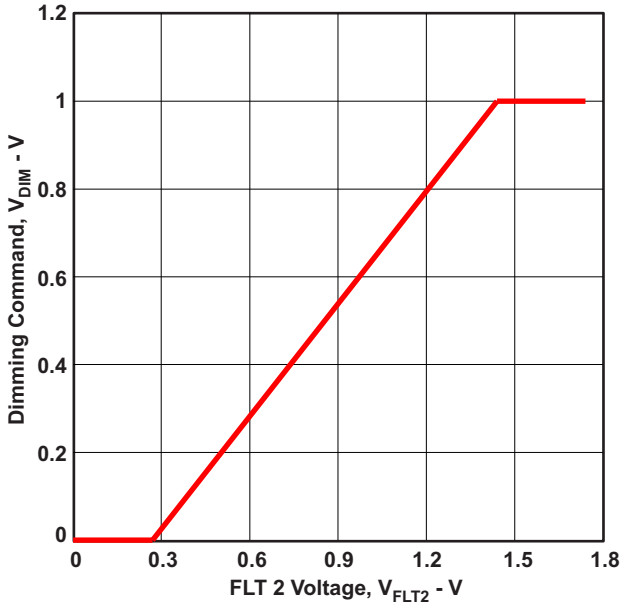


Figure 29. Relationship Between V_{FLT2} and V_{DIM}

The relationship implemented by the angle decoding circuit is designed to map the non-linear power behavior of external phase dimmer circuits and enhance Flyback PFC power stage compatibility.

Under normal operating conditions, the dimming command, V_{DIM} is translated into a reference voltage, V_{REF}, where $V_{REF} = V_{DIM}$. As dimming progresses, the input power commanded by the feedforward loop is modulated in accordance with V_{REF}. This causes the output power and hence the LED current to vary based on the input conduction angle. Using this feedforward control scheme and the internal angle decoding circuit of the LM3447, it is possible to achieve monotonic, smooth and flicker free dimming with a dimming ratio of more than 50:1.

THERMAL FOLDBACK CIRCUIT

Thermal protection is necessary to prevent the LEDs and other power supply components from sustaining damage when operated at elevated ambient temperatures. A thermal foldback circuit is incorporated into the LM3447 to limit the maximum operating temperature of the LEDs by scaling the output power based on the heatsink temperature. The LED temperature is sensed using an external NTC resistor, R_{NTC}, connected between the TSNS pin and GND, as shown in Figure 30(a). The thermal protection is engaged when the TSNS voltage decreases below the thermal foldback threshold voltage, $V_{TSNS(TH)}$, of 1V. The power is scaled by adjusting the reference voltage, V_{REF}, based on the thermal foldback output voltage, V_{TFB}, according to the relationship shown in Figure 30(b). The resistor value, $R_{NTC(BK)}$, at which the device enters thermal protection is fixed by the internal 7.88kΩ pull-up resistor and the TSNS reference voltage, $V_{TSNS(REF)}$ and is given by

$$R_{NTC} = \frac{7.88\ k\Omega}{V_{TSNS(REF)} - V_{TSNS(TH)}} = 10.5\ k\Omega \tag{18}$$

The temperature break-point, T_{BK} and rate-of-change (slope) are governed by the non-linear characteristics of the NTC resistor, R_{NTC}, given by its β-value. To achieve a break-point temperature, T_{BK}, the NTC resistor, R_{NTC} should selected as

$$R_{NTC(T_o)} = \frac{R_{NTC(BK)}}{\exp\left[\beta\left(\frac{1}{T_{BK}} - \frac{1}{T_o}\right)\right]}. \tag{19}$$

where, T_o is the room temperature in Kelvin, and $R_{NTC(To)}$ is the NTC value at room temperature. A temperature break-point ranging from 70°C (343K) to 90°C (363K) can be achieved by selecting an NTC resistance ranging from 100kΩ to 220kΩ and β-value of 3500K to 4500K.

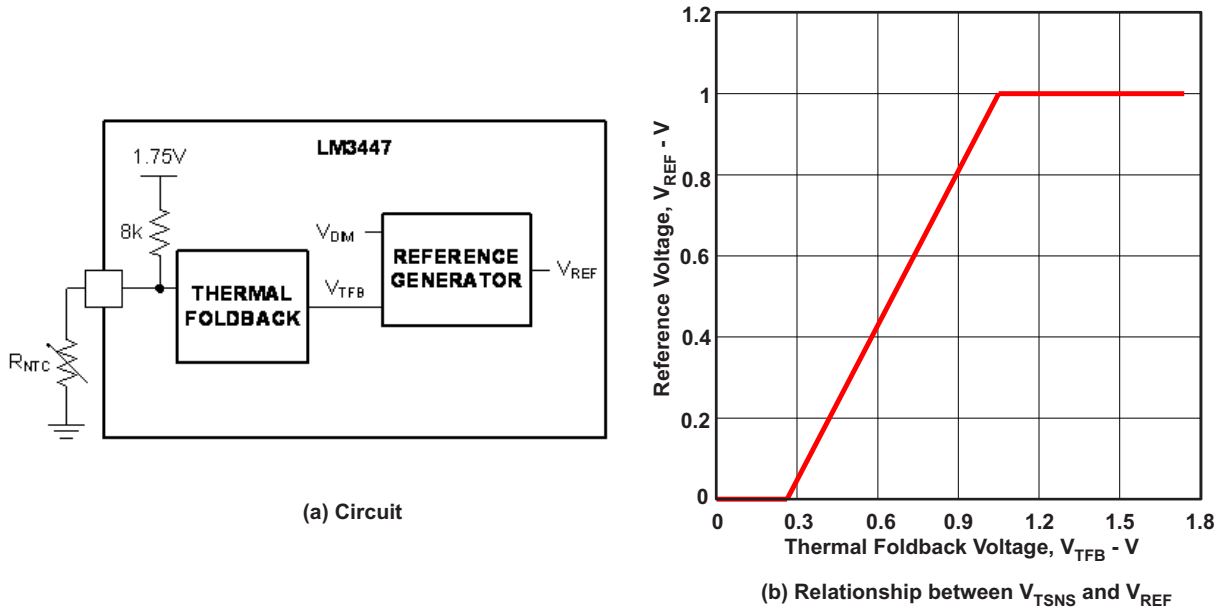


Figure 30. Thermal Foldback

The precedence between the thermal foldback input, V_{TFB} and the dimming input, V_{DIM}, is decided by the reference generator circuit. This allows dimming operation to be performed when thermal protection is engaged. Dimming operation is allowed when the input power demanded by the decoder circuit, V_{DIM}, is lower than the maximum power limit set by the thermal protection circuit, V_{TFB}. This feature provides optimal lamp utilization under adverse operating conditions.

OUTPUT BULK CAPACITOR

The output bulk capacitor, C_{BULK}, is required to store energy during the input voltage zero crossing interval and limit twice the line frequency ripple component flowing through the LEDs. The value of output capacitor is given by

$$C_{BULK} \geq \frac{P_{IN}}{2\pi f_L R_{LED} V_{OUT} I_{LED(RIP)}}, \quad (20)$$

where, R_{LED} is the dynamic resistance of LED string, $I_{LED(RIP)}$ is the average to peak LED ripple current and f_L is line frequency. In typical applications, the solution size becomes a limiting factor and dictates the maximum dimensions of the bulk capacitor. When selecting an electrolytic capacitor, manufacturer recommended de-rating factors should be applied based on the worst case capacitor ripple current, output voltage and operating temperature to achieve the desired operating lifetime.

It is essential to provide a minimum load at the output of the PFC to discharge the capacitor after the power is switched off or during LED open circuit failures. A 20kΩ resistor, R_O, is recommended for best performance.

DESIGN PROCEDURE(1)(2)

STEP	VARIABLE	DESCRIPTION
1	P_{IN}	$P_{IN} = \frac{V_{OUT} I_{LED}}{\eta_{FLY}}$ where $V_{OUT} = V_{LED}$ = Typical LED string voltage, I_{LED} is the average LED current, $\eta_{TOT} = \eta_{EMI} \times \eta_{FLY}$, η_{TOT} is the LED driver efficiency, η_{EMI} is the EMI input filter efficiency and η_{FLY} is the Flyback PFC efficiency.
2	D_{MAX}	$0.4 < D_{MAX} < 0.5$ where DMAX is the maximum allowable Flyback PFC duty cycle
3	n:1	$n = \frac{D_{MAX}}{1 - D_{MAX}} \frac{V_{REC(PK,MIN)}}{V_{OUT}}$, $V_{SW} = nV_{OUT} + V_{REC(PK,MAX)} + V_{OS}$ and V_{SW} < Maximum FET (Q1) breakdown voltage. where n is the transformer turns-ratio, $V_{REC(PK,MIN)}$ is the minimum peak rectified input voltage, $V_{REC(PK,MAX)}$ is the maximum peak rectified input voltage, $V_{IN(RMS,MIN)}$ is the minimum input RMS voltage, $V_{IN(RMS,MAX)}$ is the maximum input RMS voltage, V_{SW} is the switch drain to source voltage, V_{OS} is the overshoot voltage because of leakage inductance.
4	L_M	$L_M \leq \frac{V_{REF}}{4P_{IN} f_S \left(\frac{1}{nV_{OUT}} + \frac{1}{V_{REC(PK,MIN)}} \right)^2}$, where V_{REF} is the internal reference voltage; V_{REF} = 1V, f_S is the fixed switching frequency; f_S = 70 kHz.
5	$I_{P(PK,MAX)}$	$I_{P(PK,MAX)} = 2\sqrt{\frac{P_{IN} T_S}{L_M}}$, where T_S is the switching period, $T_S = 1/f_S$
8	N_P, N_A, N_S	Transformer Design • Core geometry (EE, PQ, RM) • Bobbin (UL Class B or Class F) L_M is the magnetizing inductance referred to primary side n:1 = N_P:N_S, primary to secondary winding turns-ratio $N_A = \frac{VCC}{V_{OUT}} N_S$, where N_A is the auxiliary winding turns $B_{MAX} < 0.3T$, where B_{MAX} is the maximum operating flux density corresponding to $I_{P(PK,MAX)}$

(1) See the Electrical Characteristics Table for all constants and measured values, unless otherwise noted.
(2) See Figure 18 for all component locations in the Design Procedure Table.

STEP	VARIABLE	DESCRIPTION
6	R_{AC}	$R_{AC} = \frac{V_{ADET}}{I_{VAC(ANGLE)}}$ where V_{ADET} is the angle detection voltage; • 25V to 40V for 120V system • 50V to 80V for 230V system $I_{VAC(ANGLE)}$ is the angle detection threshold, and $\frac{V_{REC(PK,MAX)}}{R_{AC}} \leq 500\ \mu A$
7	R_{FF}	$R_{FF} = \frac{\pi}{4} \frac{G_{FF} V_{REF}}{\sqrt{L_M P_{IN} f_S}} R_{AC}$, where G_{FF} is the gain of Feedforward circuit; G_{FF} = 10.
8	C_{FF}	$C_{FF} \leq \frac{1}{2\pi (10\ Hz - 12\ Hz) R_{FF}}$,
9	C_{COMP}	4.7µF ≤ C_{COMP} ≤ 10µF
10	Q_{PASS}, R_{HLD1}	$V_{DS(PASS)} = 1.2\ V_{REC(PK,MAX)}$, $R_{HLD1} = \frac{V_{BIAS(HIG)} - V_{GS(PASS)}}{I_{SOA(PASS)}}$, where $V_{GS(PASS)}$ is the drain to source withstand voltage of pass transistor, Q_{PASS}, $I_{SOA(PASS)}$ is the maximum current through pass transistor based on safe operating area characteristics.
11	R_{BS}	$R_{BS} = \frac{V_{REC(PK,MAX)}}{I_{BIAS}}$ where, I_{BIAS} is the BIAS current and I_{BIAS} ≤ 500 µA
12	R_{AUX1}, R_{AUX2}	$R_{AUX1} = \frac{N_A}{N_P} \frac{V_{REC(PK,MAX)}}{200 \times 10^{-6}}$, $R_{AUX2} = \left(\frac{1.75}{\frac{N_A}{N_S} V_{OUT(OVP)} - 1.75} \right) R_{AUX1}$, where, $V_{OUT(OVP)}$ is the maximum output voltage under OVP condition
13	R_{SN}	$R_{SN} = \frac{275 \times 10^{-3}}{2 I_{P(PK,MAX)}}$
14	R_{FLT}, C_{FLT}	R_{FLT} = 280 kΩ, C_{FLT} = 0.1 µF
15	R_{HOLD}	$R_{HLD2} = \frac{13.5 - V_{GS(PASS)}}{I_{HOLD}} - R_{HLD1}$ where, I_{HOLD} is the holding current drawn through the external phase dimmer circuit

STEP	VARIABLE	DESCRIPTION
16	R_{NTC}	$R_{NTC(T_o)} = \frac{R_{NTC(BK)}}{\exp\left[\beta\left(\frac{1}{T_{BK}} - \frac{1}{T_o}\right)\right]}$, where, $R_{NTC(BK)}$ = 10.5 kΩ, is the fixed break point resistance, T_{BK} is the break point temperature in Kelvin, T_O is the room temperature in Kelvin, $R_{NTC(To)}$ is the manufacturer specified NTC resistance at room temperature, β is the NTC resistor characteristics specified by the manufacturer.
17	C_{BULK}, R_O	$C_{BULK} \leq \frac{P_{IN}}{2\pi f_L R_{LED} V_{OUT} I_{LED(RIP)}}$, where, $I_{LED(RIP)}$ is the average to peak magnitude of twice the line frequency current ripple through LED, R_{LED} is the dynamic resistance of the LED string, f_L is the line frequency R_O = 20 kΩ, is the recommended bleeder resistance

REVISION HISTORY

Changes from Original (April 2012) to Revision A **Page**

- 将器件状态从：产品预览改为：生产 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3447MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L3447 MT	Samples
LM3447MTE/NOPB	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L3447 MT	Samples
LM3447MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L3447 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

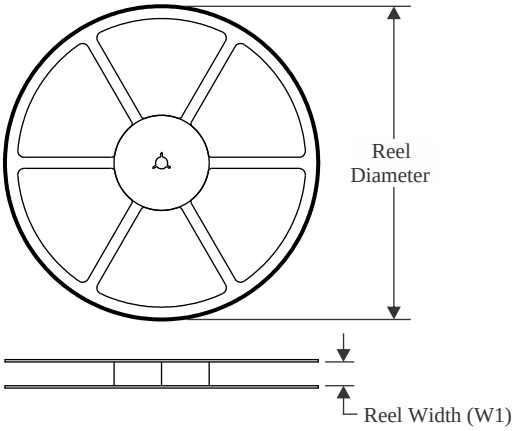
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

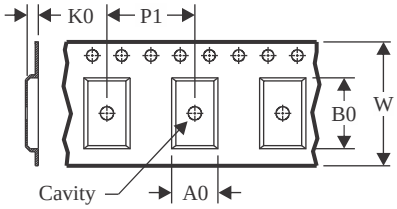
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

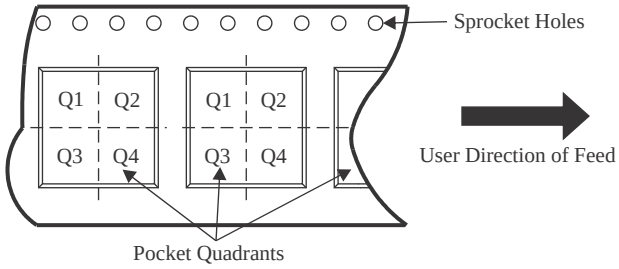


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

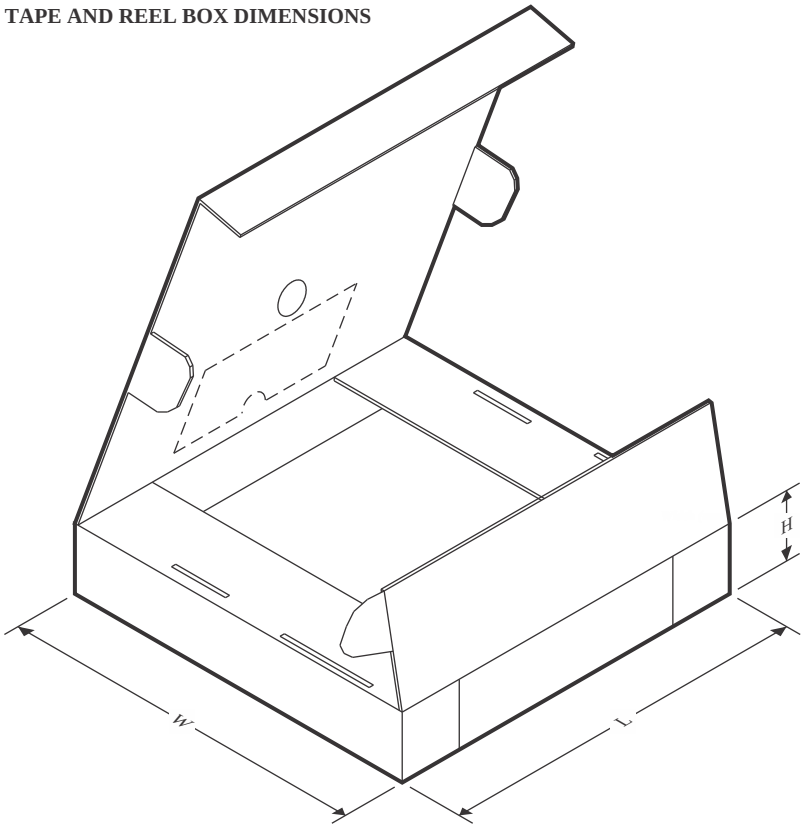
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3447MTE/NOPB	TSSOP	PW	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3447MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

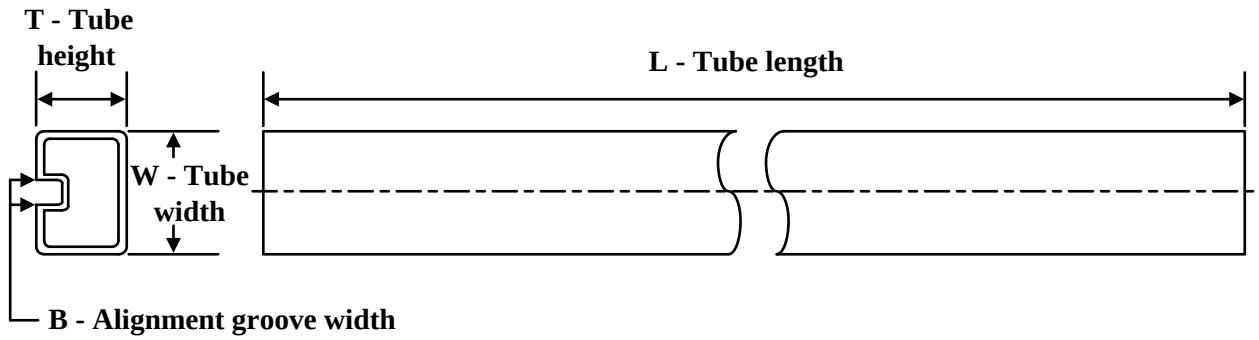
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3447MTE/NOPB	TSSOP	PW	14	250	208.0	191.0	35.0
LM3447MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

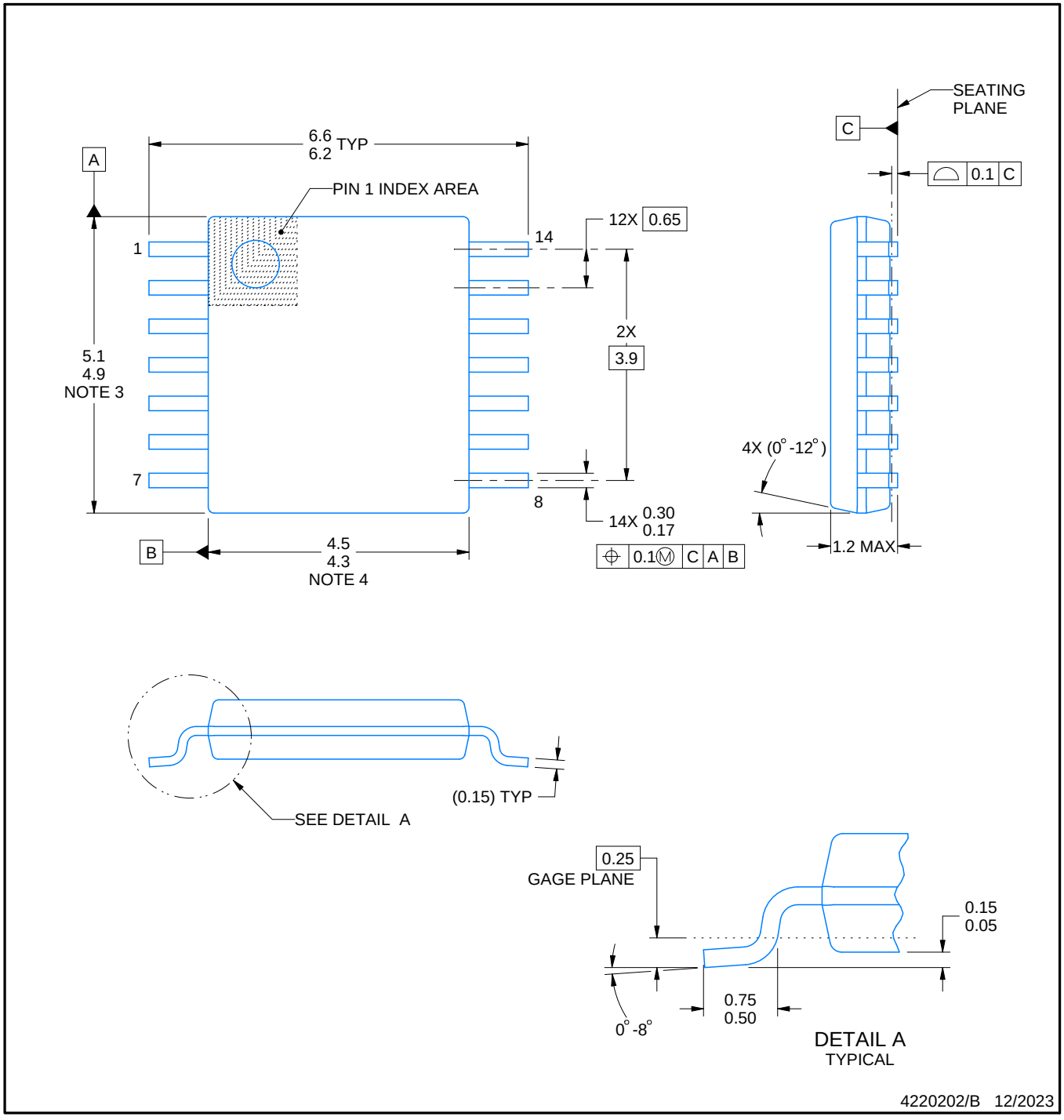
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3447MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LM3447MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

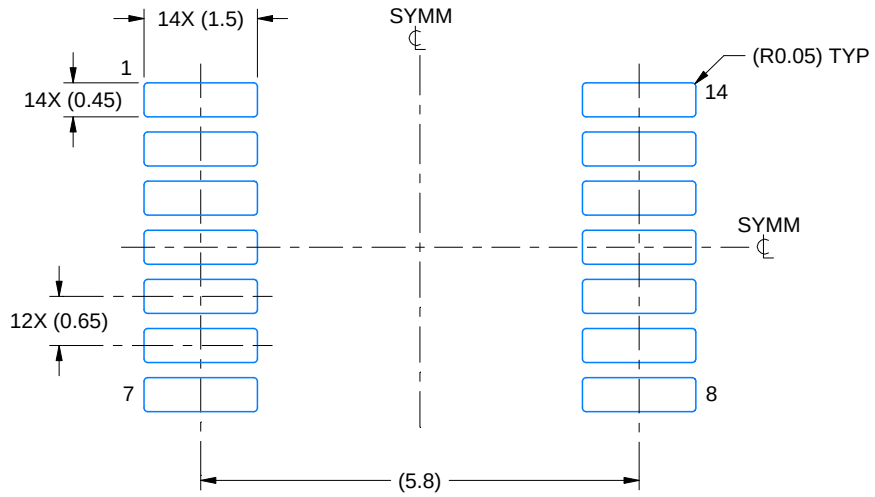
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

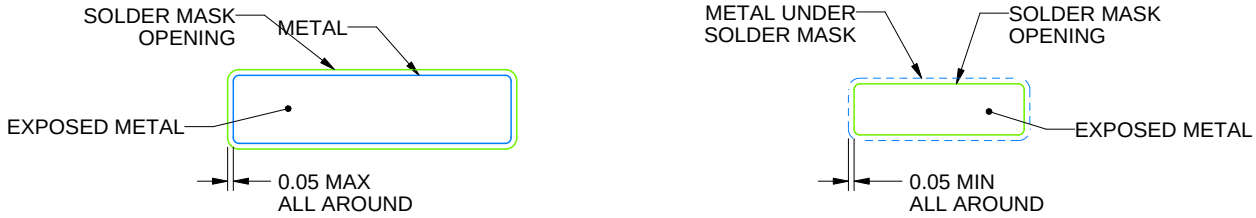


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

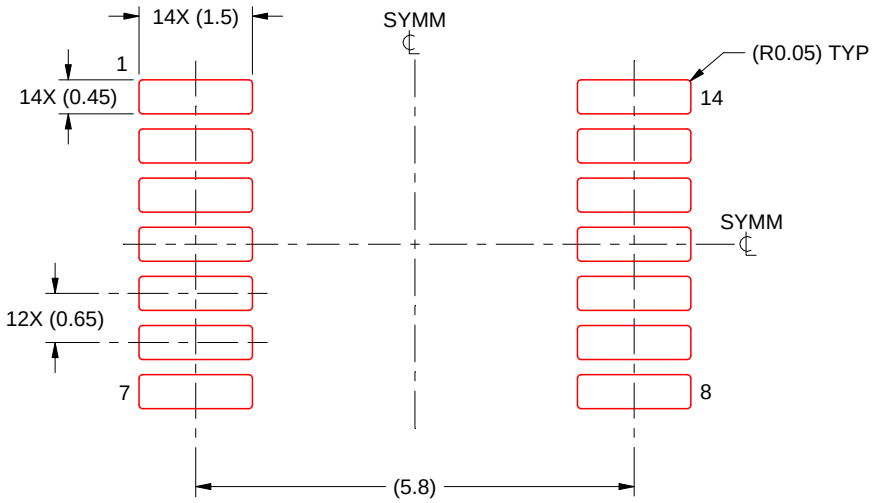


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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