LM2767 开关电容器电压转换器

1 特性

- 使输入电源电压加倍
- SOT-23 5 引脚封装
- 输出阻抗典型值 20 Ω
- 15mA 的典型转换效率为 96%

2 应用

- 手机
- 呼叫器
- PDA、整理器
- 运算放大器电源
- 接口电源
- 手持仪器

3 说明

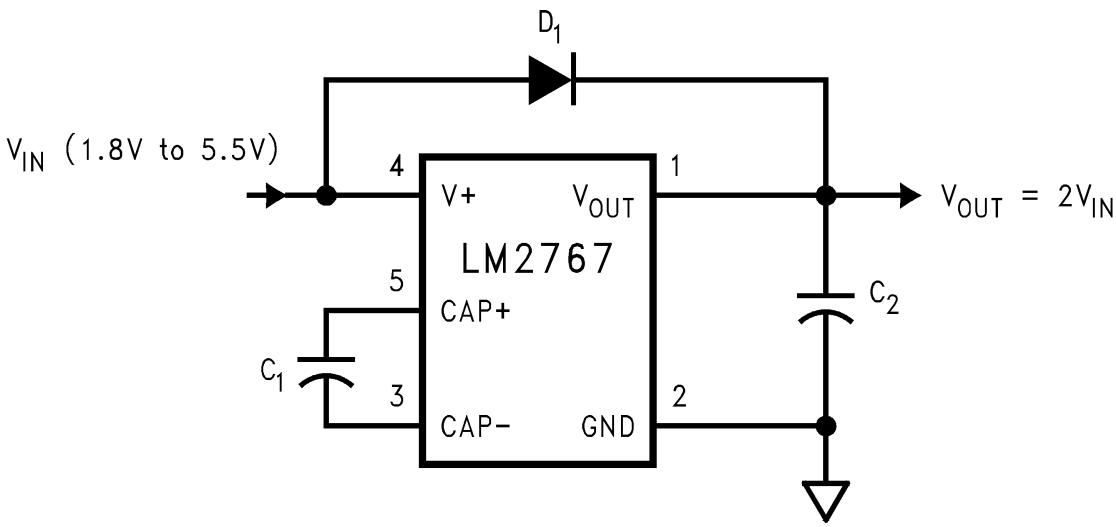
LM2767 CMOS 电荷泵电压转换器用作电压加倍器，可实现 1.8V 至 5.5V 的输入电压范围。此电路中使用了两个低成本电容器和一个二极管来提供至少 15mA 的输出电流。

LM2767 在 11kHz 的开关频率下工作，用于避免音频语音频带干扰。由于工作电流仅为 40μA（在大多数负载条件下工作效率大于 90%），LM2767 能够为电池供电系统提供出色的性能。该器件采用 5 引脚 SOT-23 封装。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM2767	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (August 2015) to Revision E (January 2022) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.......... 1
- Added additional I_L specification test condition 5

Changes from Revision C (May 2013) to Revision D (August 2015) **Page**

- 添加了*器件信息*与*引脚配置和功能*部分、“ESD 等级”表、*特性说明*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档支持*以及*机械、封装和可订购信息*部分.......... 1

5 Pin Configuration and Functions

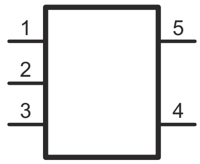


图 5-1. DBV Package 5-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	VOUT	Power	Positive voltage output.
2	GND	Ground	Power supply ground input.
3	CAP−	Power	Connect this pin to the negative terminal of the charge-pump capacitor.
4	V+	Power	Power supply positive voltage input.
5	CAP+	Power	Connect this pin to the positive terminal of the charge-pump capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or V+ to V_{OUT})		5.8	V
V_{OUT} continuous output current		30	mA
Output short-circuit duration to GND[(3)]		1	sec
Continuous power dissipation (T_A = 25°C)[(4)]		400	mW
T_{JMax} [(4)]		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) V_{OUT} may be shorted to GND for one second without damage. For temperatures above 85°C, V_{OUT} must not be shorted to GND or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Machine model (CDM), per JEDEC specification JESD22-C101[(2)]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Junction temperature	−40		100	°C
Ambient temperature	−40		85	°C
Lead temperature (soldering, 10 sec.)			240	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		LM2767 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, typical limits are for T_J = 25°C, minimum and maximum limits apply over the full operating temperature range: V+ = 5 V, C_1 = C_2 = 10 μF.[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V+	Supply voltage		1.8		5.5	V
I_Q	Supply current	No load		40	90	µA
I_L	Output current	2.5 V ⩽ V+ ⩽ 5.5 V	15			mA
		1.8 V ⩽ V+ < 2.5 V	10			mA
R_{OUT}	Output resistance[(2)]	I_L = 15 mA		20	40	Ω
f_{OSC}	Oscillator frequency	See[(3)]	8	22	50	kHz
f_{SW}	Switching frequency	See[(3)]	4	11	25	kHz
P_{EFF}	Power efficiency	R_L (5 kΩ) between GND and OUT		98%		
		I_L = 15 mA to GND		96%		
V_{OEFF}	Voltage conversion efficiency	No load		99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 10-µF, 0.3-Ω maximum ESR capacitors. Capacitors with higher ESR may increase output resistance, and reduce output voltage and efficiency.
(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in 节 9 for positive voltage doubler.
(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2 \times f_{SW}$.

6.6 Typical Characteristics

(Circuit of 图 7-1, V_{IN} = 5 V, T_A = 25°C unless otherwise specified).

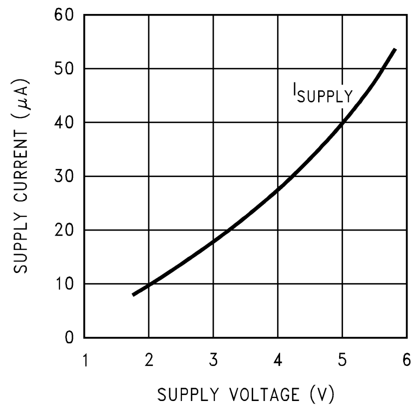


图 6-1. Supply Current vs Supply Voltage

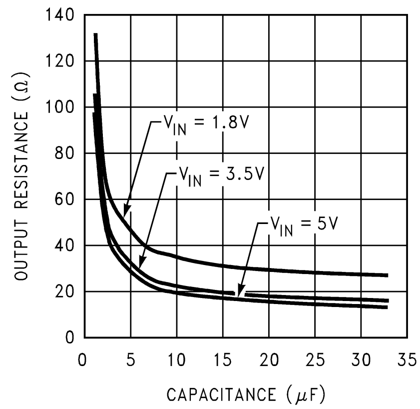


图 6-2. Output Resistance vs Capacitance

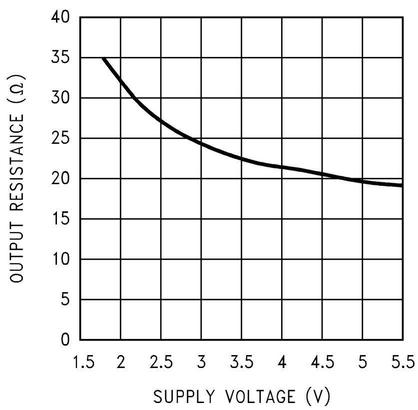


图 6-3. Output Resistance vs Supply Voltage

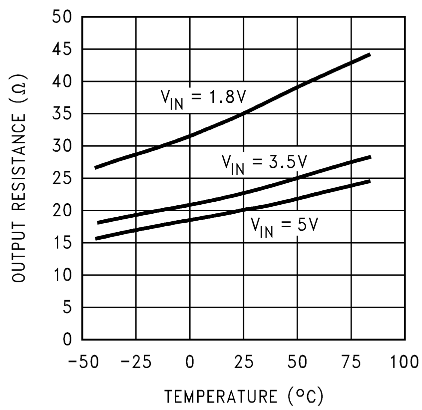


图 6-4. Output Resistance vs Temperature

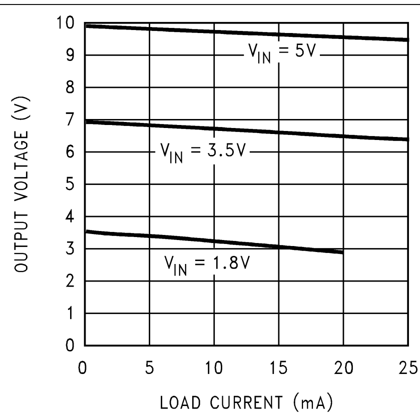


图 6-5. Output Voltage vs Load Current

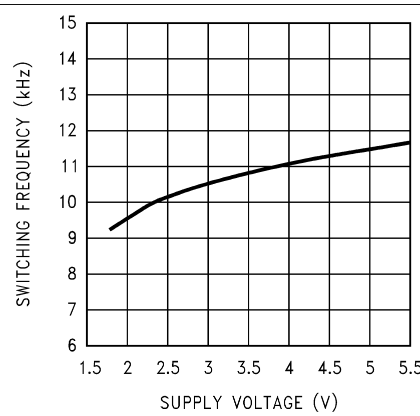


图 6-6. Switching Frequency vs Supply Voltage

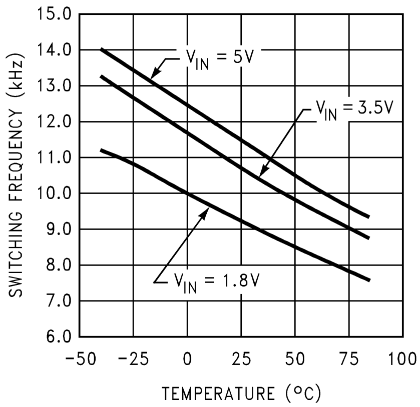


图 6-7. Switching Frequency vs Temperature

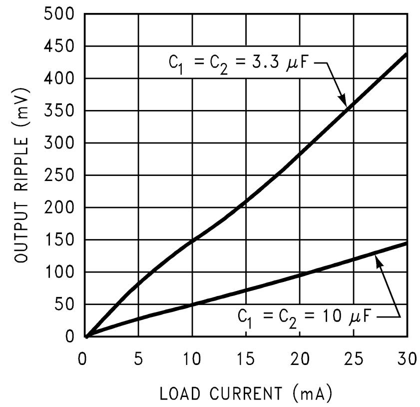


图 6-8. Output Ripple vs Load Current

7 Parameter Measurement Information

7.1 Test Circuit

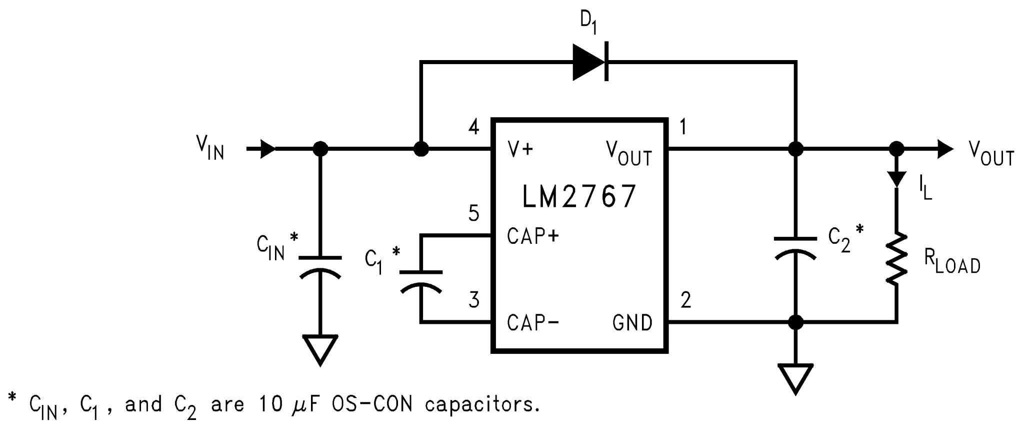


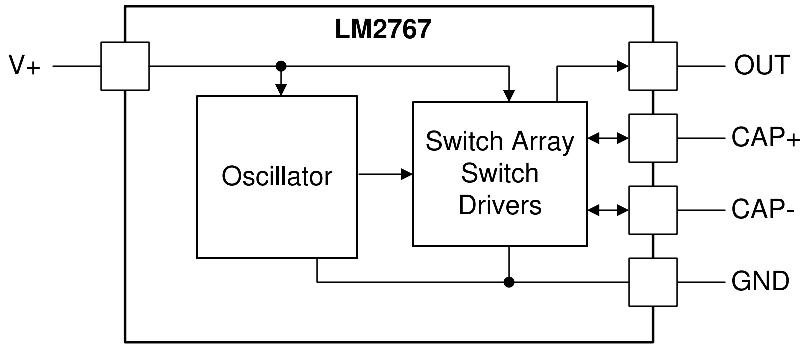
图 7-1. LM2767 Test Circuit

8 Detailed Description

8.1 Overview

The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit.

8.2 Functional Block Diagram



8.3 Feature Description

The LM2767 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. 图 9-2 illustrates the voltage conversion scheme. When S_2 and S_4 are closed, C_1 charges to the supply voltage V+. During this time interval, switches S_1 and S_3 are open. In the next time interval, S_2 and S_4 are open; at the same time, S_1 and S_3 are closed, the sum of the input voltage V+ and the voltage across C_1 gives the 2V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details are discussed in 节 9.

8.4 Device Functional Modes

The LM2767 is always enabled when power is applied to the V+ pin (1.8 V $\leqslant V_{IN} \leqslant$ 5.5 V). To disable the part, power must be removed.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LM2767 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

9.2 Typical Application

The main application of the LM2767 is to double the input voltage. The range of the input supply voltage is 1.8 V to 5.5 V.

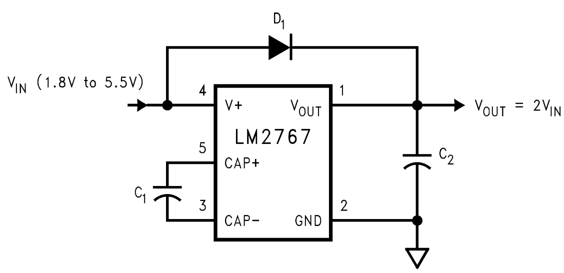


图 9-1. LM2767 Typical Application

9.2.1 Design Requirements

For typical switched-capacitor voltage converter applications, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	1.8 to 5.5 V
Output current (minimum)	15 mA
Switching frequency	11 kHz (typical)

9.2.2 Detailed Design Procedure

9.2.2.1 Positive Voltage Doubler

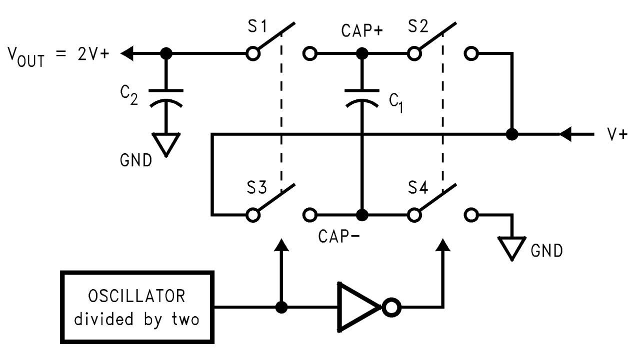


图 9-2. Voltage Doubling Principle

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+. The output resistance R_{out} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2. Because the switching current charging and discharging C_1 is approximately twice the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of R_{out} is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in 图 9-2.

The peak-to-peak output voltage ripple is determined by the oscillator frequency as well as the capacitance and ESR of the output capacitor C_2:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

High capacitance, low ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode D_1 is only needed to protect the device from turning on its own parasitic diode and potentially latching up. During start-up, D_1 also quickly charges up the output capacitor to V_{IN} minus the diode drop thereby decreasing the start-up time. Therefore, the Schottky diode D_1 must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

9.2.2.2 Capacitor Selection

As discussed in *节 9.2.2.1*, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{{I_L}^2 R_L}{{I_L}^2 R_L + {I_L}^2 R_{OUT} + I_Q(V+)} \quad (3)$$

where

- $I_Q(V+)$ is the quiescent power loss of the device; and
- ${I_L}^2 R_{out}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the allowable voltage droop (which equals I_{out} R_{out}), and the desired output voltage ripple. Low-ESR capacitors (表 9-2) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

表 9-2. Low-ESR Capacitor Manufacturers

MANUFACTURER	PHONE	WEBSITE	CAPACITOR TYPE
Nichicon Corp.	(847)-843-7500	www.nichicon.com	PL & PF series, through-hole aluminum electrolytic
AVX Corp.	(843)-448-9411	www.avxcorp.com	TPS series, surface-mount tantalum
Sprague	(207)-324-4140	www.vishay.com	593D, 594D, 595D series, surface-mount tantalum
Sanyo	(619)-661-6835	www.sanyovideo.com	OS-CON series, through-hole aluminum electrolytic
Murata	(800)-831-9172	www.murata.com	Ceramic chip capacitors
Taiyo Yuden	(800)-348-2496	www.t-yuden.com	Ceramic chip capacitors
Tokin	(408)-432-8020	www.tokin.com	Ceramic chip capacitors

9.2.2.3 Paralleling Devices

Any number of LM2767 devices can be paralleled to reduce the output resistance. Because there is no closed loop feedback, as found in regulated circuits, stable operation is assured. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{OUT} is needed as shown in 图 9-3. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT}\ \text{of each LM2767}}{\text{Number of Devices}} \quad (4)$$

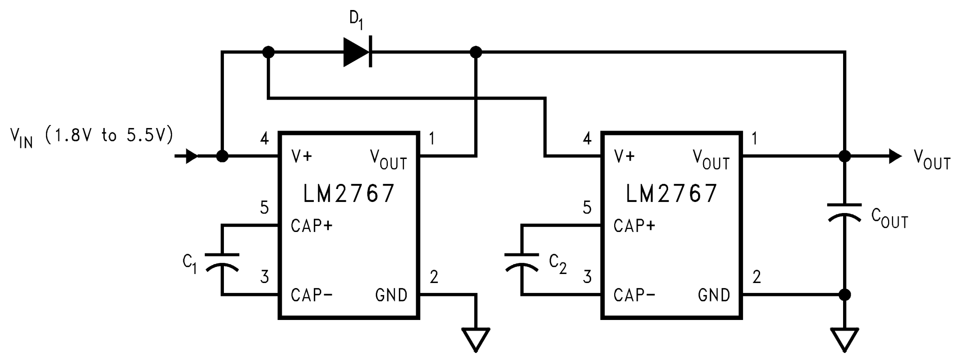


图 9-3. Lowering Output Resistance by Paralleling Devices

9.2.2.4 Cascading Devices

Cascading the several LM2767 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in 图 9-4).

The effective output resistance is equal to the weighted sum of each individual device:

$$R_{OUT} = 1.5\ R_{OUT\_1} + R_{OUT\_2} \quad (5)$$

Note that increasing the number of cascading stages is practically limited because it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

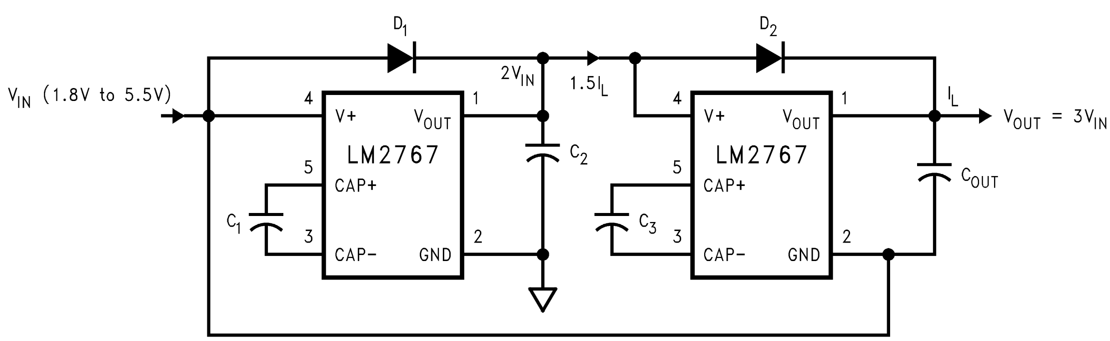


图 9-4. Increasing Output Voltage By Cascading Devices

9.2.2.5 Regulating V_{OUT}

It is possible to regulate the output of the LM2767 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in 图 9-5.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

The following conditions must be satisfied simultaneously for worst case design:

$$2V_{IN\_MIN} > V_{OUT\_MIN} + V_{DROP\_MAX}\ (LP2980) + I_{OUT\_MAX} \times R_{OUT\_MAX} \quad (6)$$

$$2V_{IN\_MAX} < V_{OUT\_MAX} + V_{DROP\_MIN}\,(LP2980) + I_{OUT\_MIN} \times R_{OUT\_MIN} \quad (7)$$

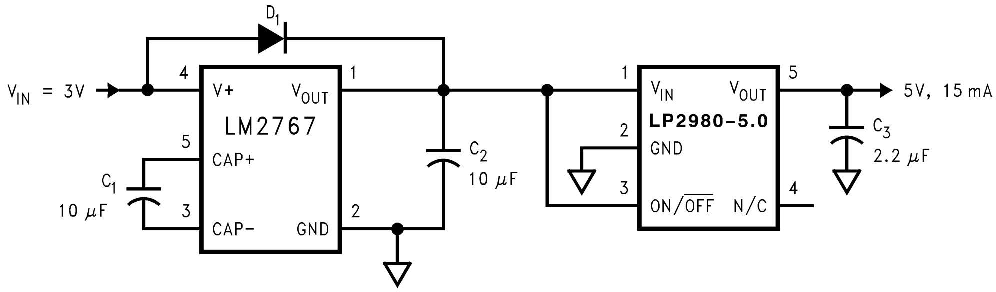


图 9-5. Generate a Regulated 5-V From 3-V Input Voltage

9.2.3 Application Curve

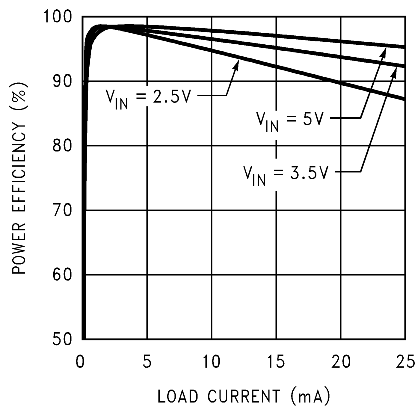


图 9-6. Efficiency vs Load Current

10 Power Supply Recommendations

The LM2767 is designed to operate from as an inverter over an input voltage supply range from 1.8 V and 5.5 V. This input supply must be well-regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

Use the following steps as a reference to ensure the device is stable across its intended operating voltage and current range.

- Place CIN on the top layer (same layer as the LM2767) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place COUT on the top layer (same layer as the LM2767) and as close as possible to the OUT and GND pin. The returns for both CIN and COUT must come together at one point, as close to the GND pin as possible. Connecting COUT through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the VOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2767 device) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP – pins.

11.2 Layout Example

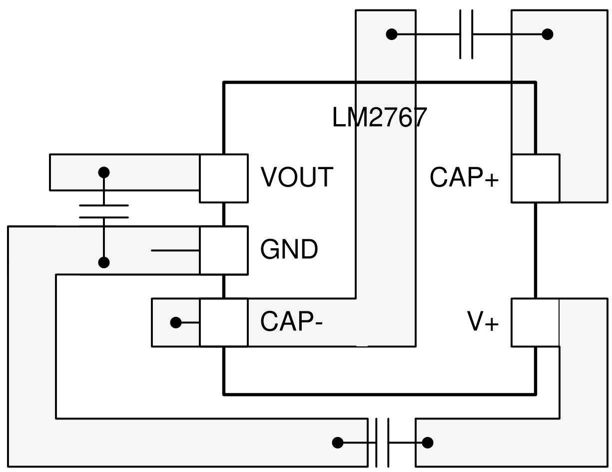


图 11-1. LM2767 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2767M5	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	No	Call TI	Level-1-260C-UNLIM	-40 to 85	S17B
LM2767M5.Z	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	No	Call TI	Level-1-260C-UNLIM	-40 to 85	S17B
LM2767M5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	S17B
LM2767M5/NOPB.Z	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	S17B
LM2767M5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	S17B
LM2767M5X/NOPB.Z	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	S17B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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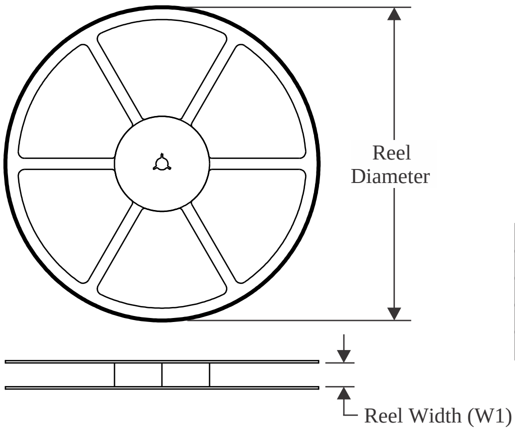
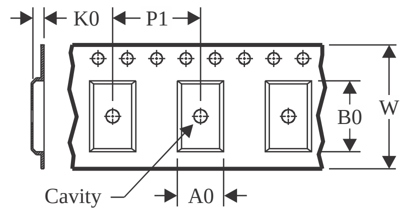
TAPE AND REEL INFORMATION

REEL DIMENSIONS

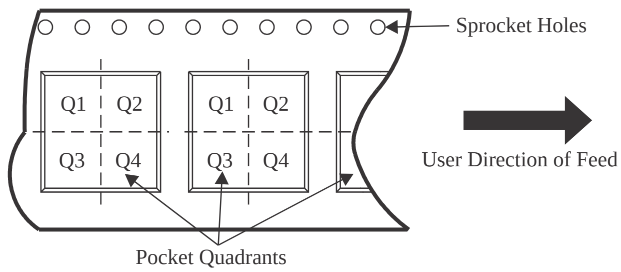


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

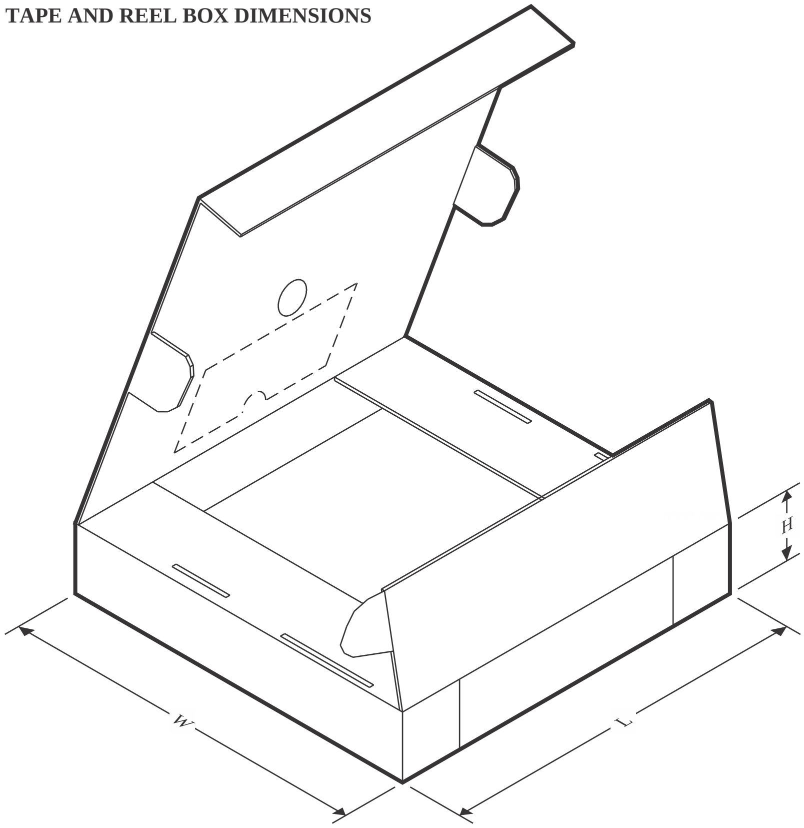
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

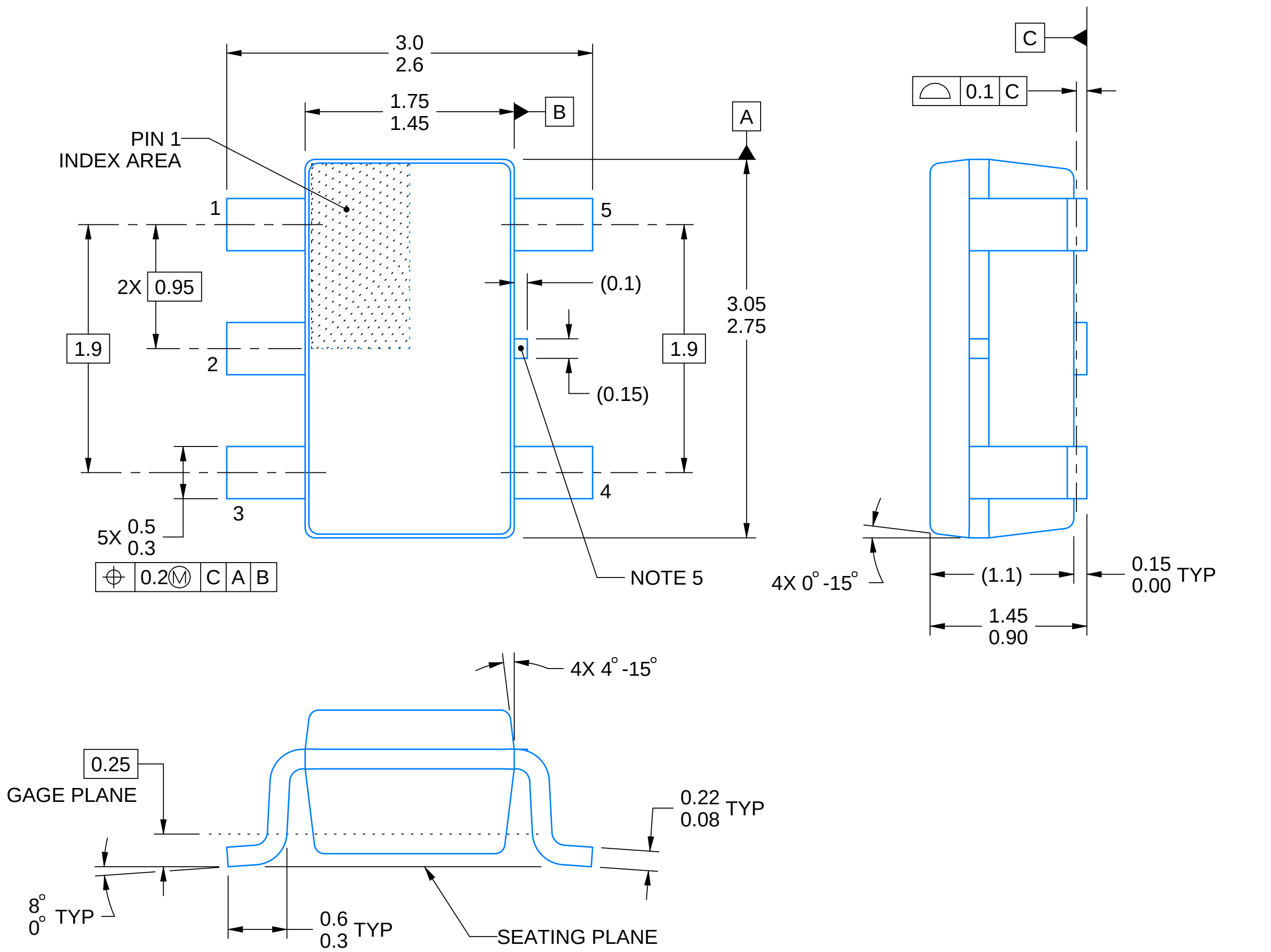
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2767M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2767M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2767M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2767M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2767M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2767M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



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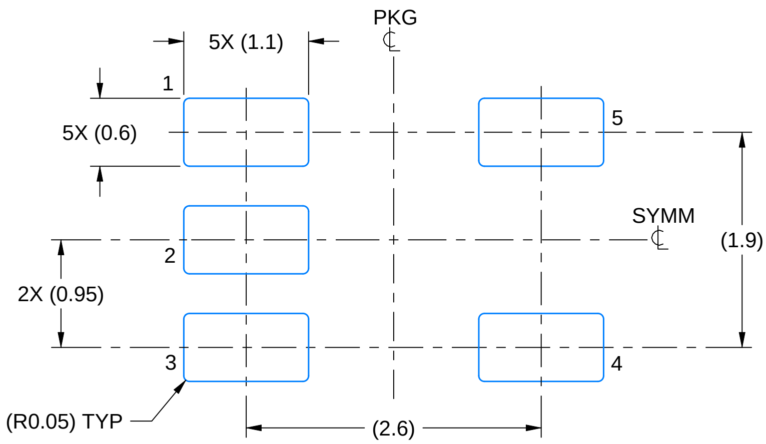
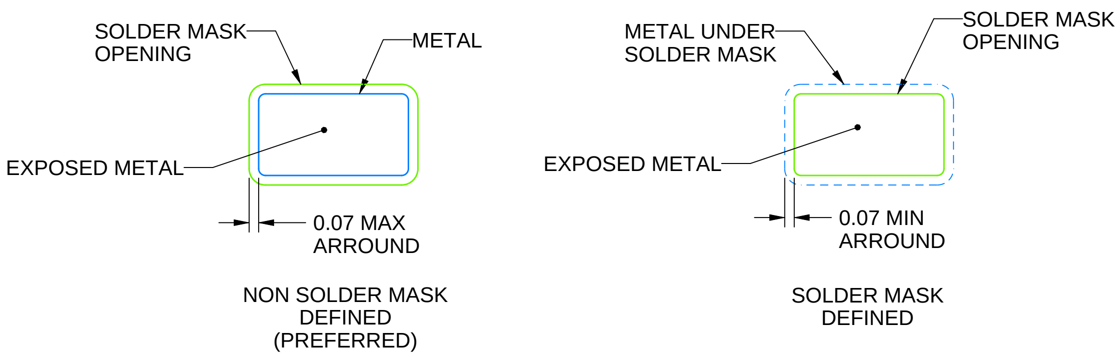
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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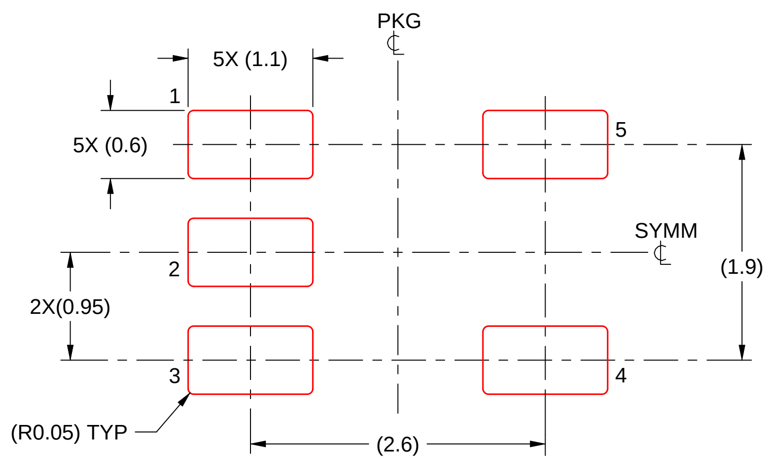
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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