LM2766 Switched Capacitor Voltage Converter

1 Features

- Doubles Input Supply Voltage
- SOT-23 6-Pin Package
- 20-Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 20 mA
- 0.1-µA Typical Shutdown Current

2 Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

3 Description

The LM2766 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode are used in this circuit to provide up to 20 mA of output current.

The LM2766 operates at 200-kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 350 µA (operating efficiency greater than 90% with most loads) and 0.1-µA typical shutdown current, the LM2766 provides ideal performance for battery-powered systems. The device is manufactured in a SOT-23 6-pin package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2766	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Voltage Doubler Application

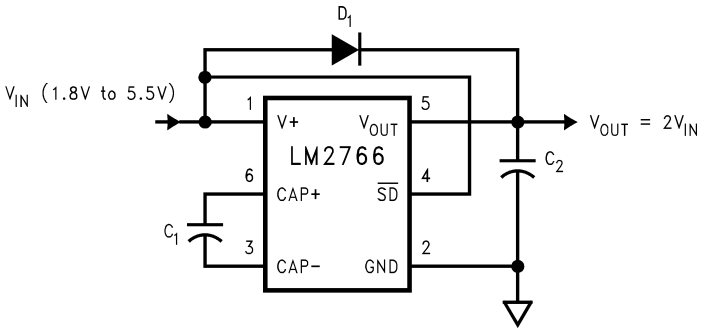


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C **Page**

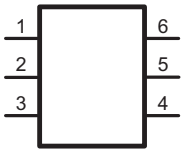
- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision A (May 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format ... 12

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V+	Power	Power supply positive voltage input.
2	GND	Ground	Power supply ground input.
3	CAP−	Power	Connect this pin to the negative terminal of the charge-pump capacitor.
4	$\overline{SD}$	Input	Shutdown control pin, tie this pin to V+ in normal operation.
5	V_{OUT}	Power	Positive voltage output.
6	CAP+	Power	Connect this pin to the positive terminal of the charge-pump capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or V+ to V_{OUT})		5.8	V
$\overline{SD}$	(GND − 0.3)	(V+ + 0.3)	V
V_{OUT} continuous output current		40	mA
Output short-circuit duration to GND[3]		1	sec
Continuous power dissipation (T_A = 25°C)[4]		600	mW
T_{JMax}[4]		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) V_{OUT} may be shorted to GND for one second without damage. For temperatures above 85°C, V_{OUT} must not be shorted to GND or device may be damaged.
(4) The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Machine model (CDM), per JEDEC specification JESD22-C101[2]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Junction temperature	−40		100	°C
Ambient temperature	−40		85	°C
Lead temperature (soldering, 10 sec.)			240	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2766 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, typical limits are for T_J = 25°C, minimum and maximum limits apply over the full operating temperature range: V+ = 5 V, $C_1 = C_2$ = 10 µF.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V+	Supply voltage		1.8		5.5	V
I_Q	Supply current	No load		350	950	µA
$I_{\overline{SD}}$	Shutdown supply current	T_J = 25°C		0.1	0.5	µA
		T_A = 85°C		0.2		
$V_{\overline{SD}}$	Shutdown pin input voltage		0.6			V
					2	
I_L	Output current	2.5 V ≤ V_{IN} ≤ 5.5 V	20			mA
		1.8 V ≤ V_{IN} ≤ 2.5 V	10			
R_{OUT}	Output resistance(2)	I_L = 15 mA		20	55	Ω
f_{OSC}	Oscillator frequency	See(3)	220	400	700	kHz
f_{SW}	Switching frequency	See(3)	110	200	350	kHz
P_{EFF}	Power efficiency	I_L = 20 mA to GND		94%		
V_{OEFF}	Voltage conversion efficiency	No load		99.96%		

(1) In the test circuit, capacitors C_1 and C_2 are 10-µF, 0.3-Ω maximum ESR capacitors. Capacitors with higher ESR may increase output resistance, and reduce output voltage and efficiency.
(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in *Application and Implementation* for positive voltage doubler.
(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2 \times f_{SW}$.

6.6 Typical Characteristics

(Circuit of *Typical Voltage Doubler Application*, V_{IN} = 5 V, T_A = 25°C unless otherwise specified)

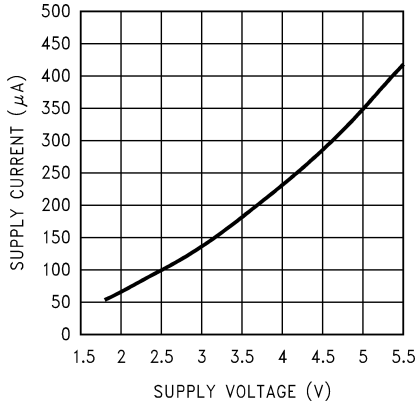


Figure 1. Supply Current vs Supply Voltage

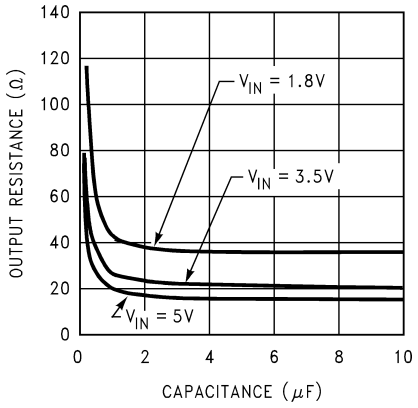


Figure 2. Output Resistance vs Capacitance

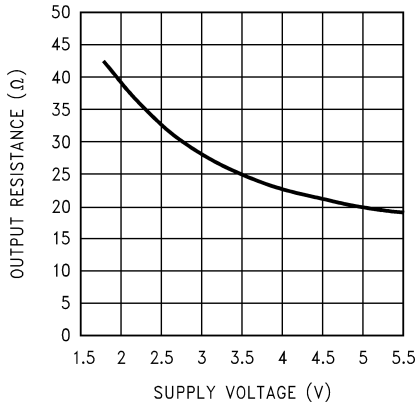


Figure 3. Output Resistance vs Supply Voltage

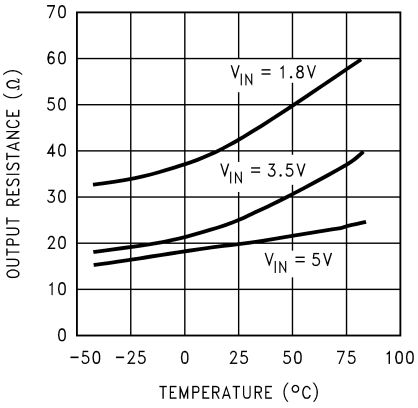


Figure 4. Output Resistance vs Temperature

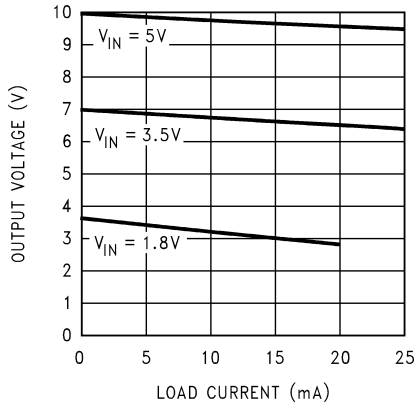


Figure 5. Output Voltage vs Load Current

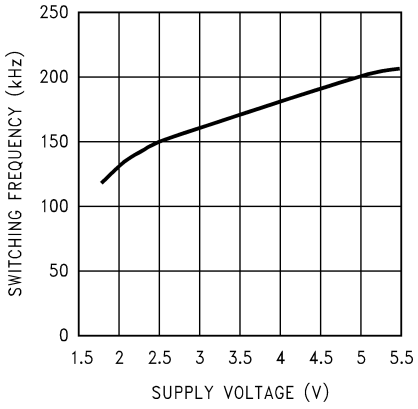


Figure 6. Switching Frequency vs Supply Voltage

Typical Characteristics (continued)

(Circuit of *Typical Voltage Doubler Application*, V_{IN} = 5 V, T_A = 25°C unless otherwise specified)

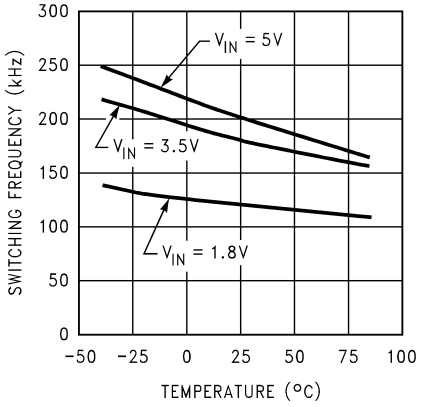


Figure 7. Switching Frequency vs Temperature

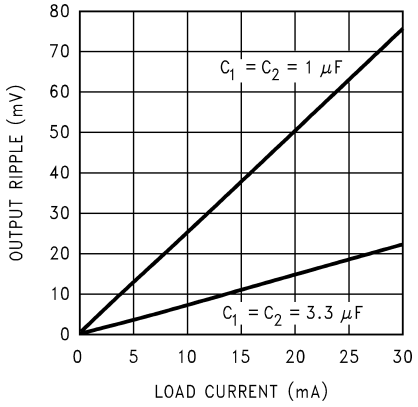
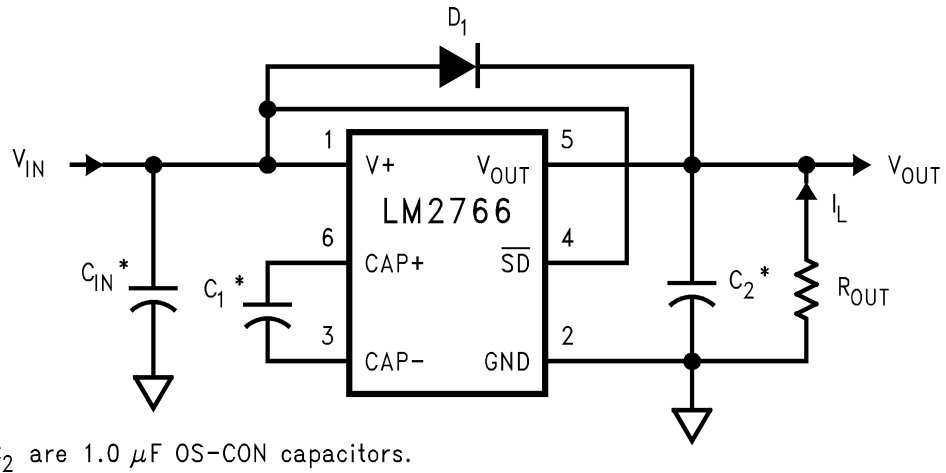


Figure 8. Output Ripple vs Load Current

7 Parameter Measurement Information

7.1 Test Circuit



* C_{IN}, C_1, and C_2 are 1.0 µF OS-CON capacitors.

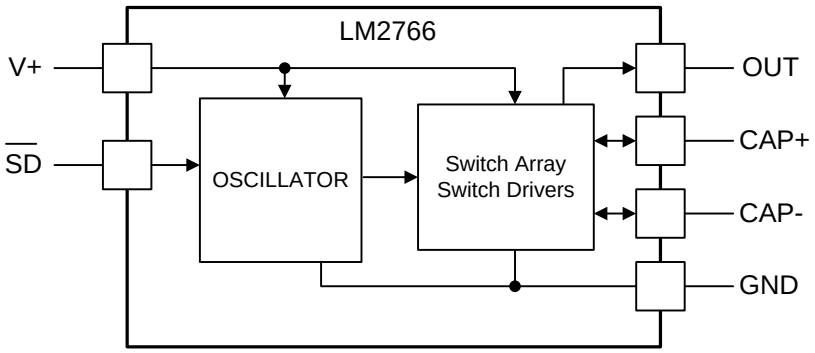
Figure 9. LM2766 Test Circuit

8 Detailed Description

8.1 Overview

The LM2766 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Test Circuit

The LM2766 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 10 illustrates the voltage conversion scheme. When S_2 and S_4 are closed, C_1 charges to the supply voltage V+. During this time interval, switches S_1 and S_3 are open. In the next time interval, S_2 and S_4 are open; at the same time, S_1 and S_3 are closed, the sum of the input voltage V+ and the voltage across C_1 gives the 2 V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance ($R_{ds(on)}$ of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. See *Application and Implementation* for further details.

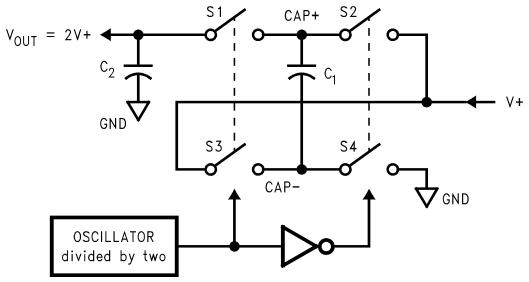


Figure 10. Voltage Doubling Principle

8.4 Device Functional Modes

8.4.1 Shutdown Mode

A shutdown ($\overline{SD}$) pin is available to disable the device and reduce the quiescent current to 0.1 µA. In normal operating mode, the $\overline{SD}$ pin is connected to V+. The device can be brought into the shutdown mode by applying to the $\overline{SD}$ pin a voltage less than 20% of the V+ pin voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2766 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

9.2 Typical Application

The main application of the LM2766 is to double the input voltage.

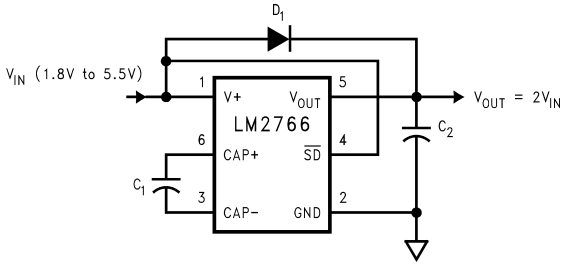


Figure 11. LM2766 Typical Application

9.2.1 Design Requirements

For typical switched-capacitor voltage converter applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	1.8 to 5.5 V
Output current (minimum), 2.5 V ≤ V_{IN} ≤ 5.5 V	20 mA
Output current (minimum), 1.8 V ≤ V_{IN} ≤ 2.5 V	10 mA
Switching frequency	200 kHz (typical)

9.2.2 Detailed Design Procedure

9.2.2.1 Positive Voltage Doubler

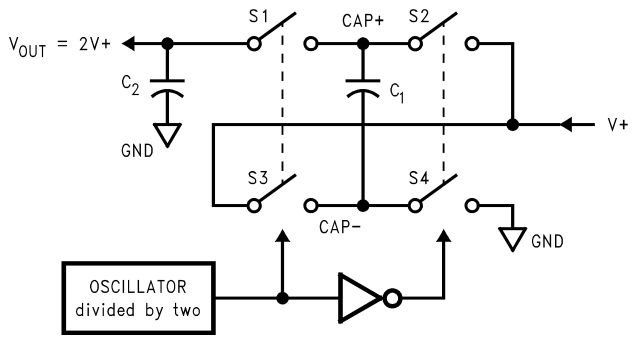


Figure 12. Voltage Doubling Principle

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+. The output resistance R_{out} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2. Because the switching current charging and discharging C_1 is approximately twice the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of R_{out} is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 12.

The peak-to-peak output voltage ripple is determined by the oscillator frequency as well as the capacitance and ESR of the output capacitor C_2:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

High capacitance, low ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode D_1 is only needed to protect the device from turning on its own parasitic diode and potentially latching up. During start-up, D_1 also quickly charges up the output capacitor to V_{IN} minus the diode drop thereby decreasing the start-up time. Therefore, the Schottky diode D_1 must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

9.2.2.2 Capacitor Selection

As discussed in *Positive Voltage Doubler*, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L{}^2 R_L}{I_L{}^2 R_L + I_L{}^2 R_{OUT} + I_Q(V+)} \quad (3)$$

where

- $I_Q(V+)$ is the quiescent power loss of the device; and
- $I_L{}^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the specifications of the dropout voltage (which equals I_{OUT} R_{OUT}), the output voltage ripple, and the converter efficiency. Low ESR capacitors (Table 2) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

Table 2. Low ESR Capacitor Manufacturers

MANUFACTURER	WEBSITE	CAPACITOR TYPE
Nichicon Corp.	www.nichicon.com	PL & PF series, through-hole aluminum electrolytic
AVX Corp.	www.avxcorp.com	TPS series, surface-mount tantalum
Sprague	www.vishay.com	593D, 594D, 595D series, surface-mount tantalum
Sanyo	www.sanyovideo.com	OS-CON series, through-hole aluminum electrolytic
Murata	www.murata.com	Ceramic chip capacitors
Taiyo Yuden	www.t-yuden.com	Ceramic chip capacitors
Tokin	www.tokin.com	Ceramic chip capacitors

9.2.2.3 Paralleling Devices

Any number of LM2766 devices can be paralleled to reduce the output resistance. Because there is no closed loop feedback, as found in regulated circuits, stable operation is assured. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{OUT} is needed as shown in Figure 13. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT} \text{ of each LM2766}}{\text{Number of Devices}} \quad (4)$$

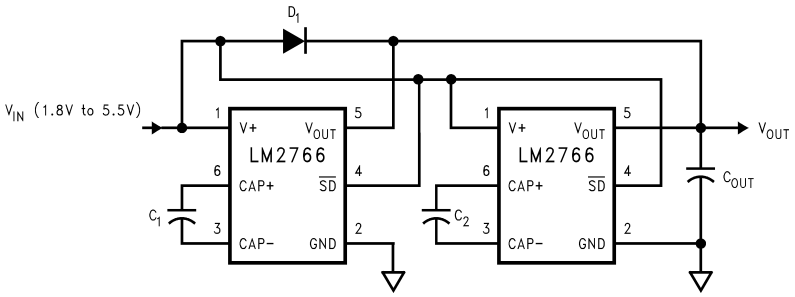


Figure 13. Lowering Output Resistance By Paralleling Devices

9.2.2.4 Cascading Devices

Cascading the several LM2766 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in Figure 14).

The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = 1.5R_{out\_1} + R_{out\_2} \quad (5)$$

Note that increasing the number of cascading stages is practically limited because it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

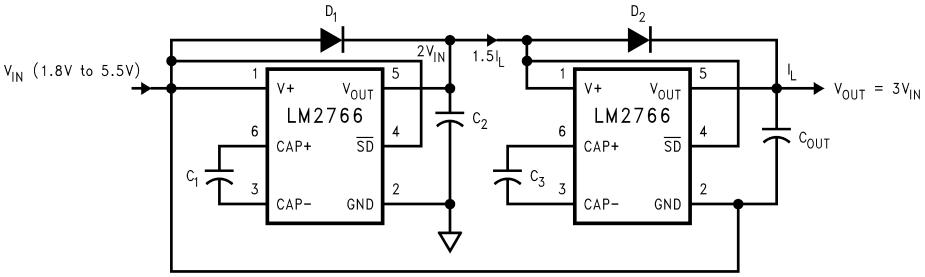


Figure 14. Increasing Output Voltage By Cascading Devices

9.2.2.5 Regulating V_{OUT}

It is possible to regulate the output of the LM2766 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 15.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

The following conditions must be satisfied simultaneously for worst case design:

$$2V_{in\_min} > V_{out\_min} + V_{drop\_max} \text{ (LP2980)} + I_{out\_max} \times R_{out\_max} \text{ (LM2766)} \quad (6)$$

$$2V_{in\_max} < V_{out\_max} + V_{drop\_min} \text{ (LP2980)} + I_{out\_min} \times R_{out\_min} \text{ (LM2766)} \quad (7)$$

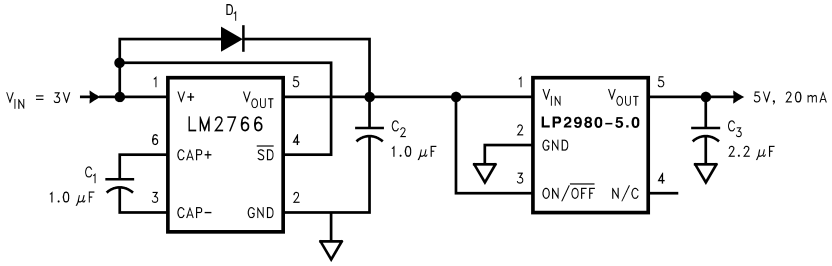


Figure 15. Generate a Regulated 5-V From 3-V Input Voltage

9.2.3 Application Curve

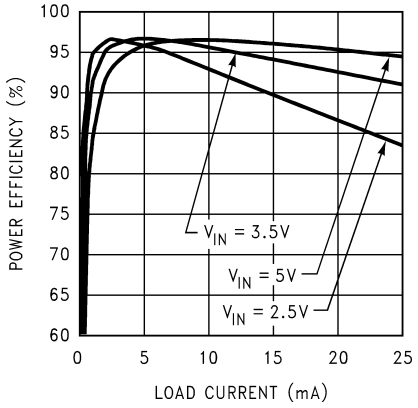


Figure 16. Efficiency vs Load Current

10 Power Supply Recommendations

The LM2766 is designed to operate from as an inverter over an input voltage supply range from 1.8 V and 5.5 V. This input supply must be well-regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2766 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

- Place C_{IN} on the top layer (same layer as the LM2766) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place C_{OUT} on the top layer (same layer as the LM2766) and as close as possible to the OUT and GND pin. The returns for both C_{IN} and C_{OUT} must come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2766 device) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example

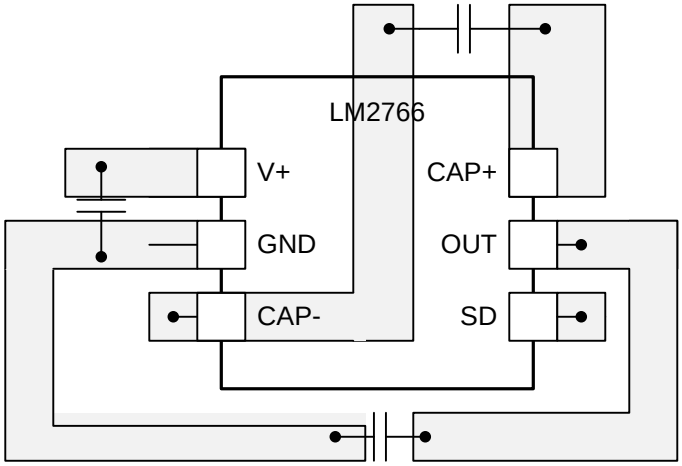


Figure 17. LM2766 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2766M6/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	S16B	Samples
LM2766M6X/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	S16B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

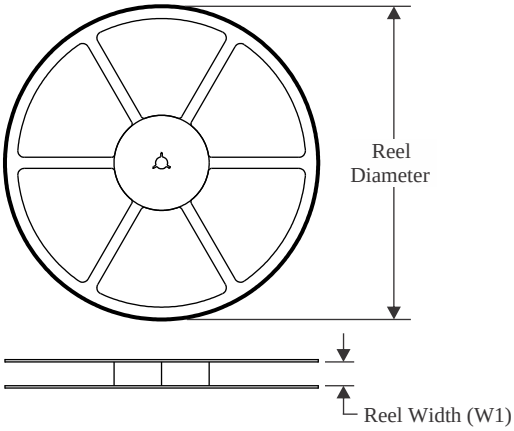
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

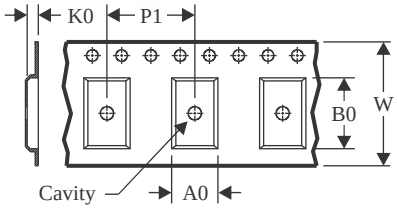
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

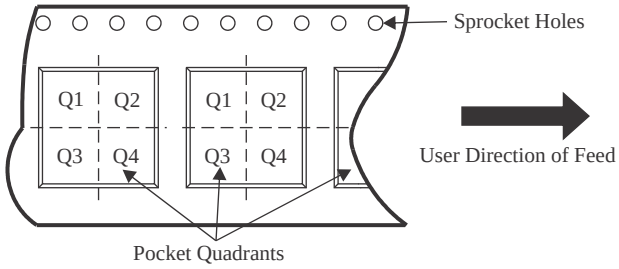


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

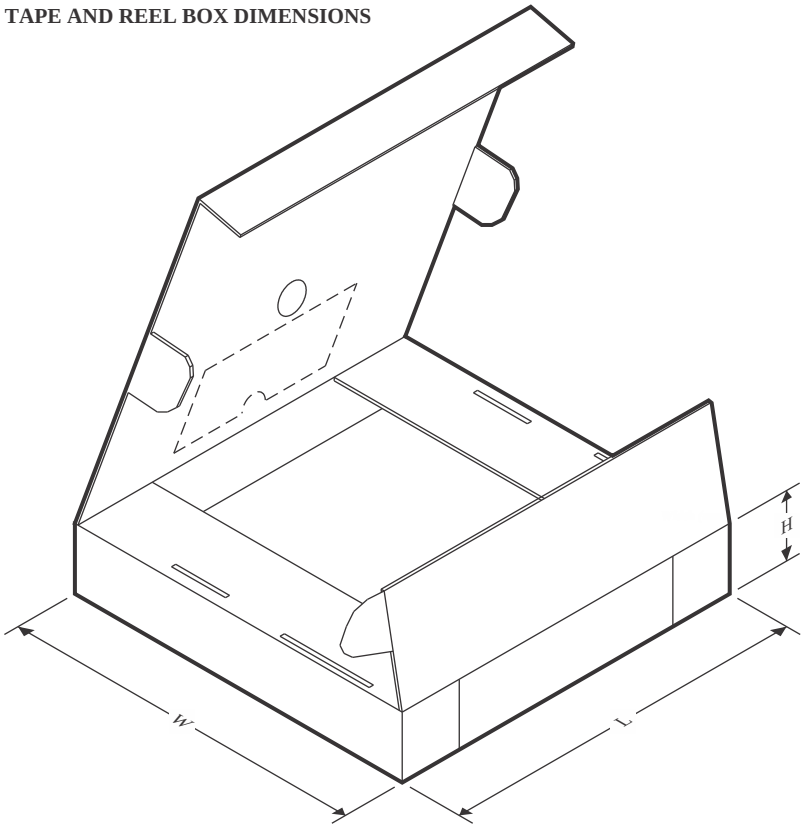
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2766M6/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2766M6X/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

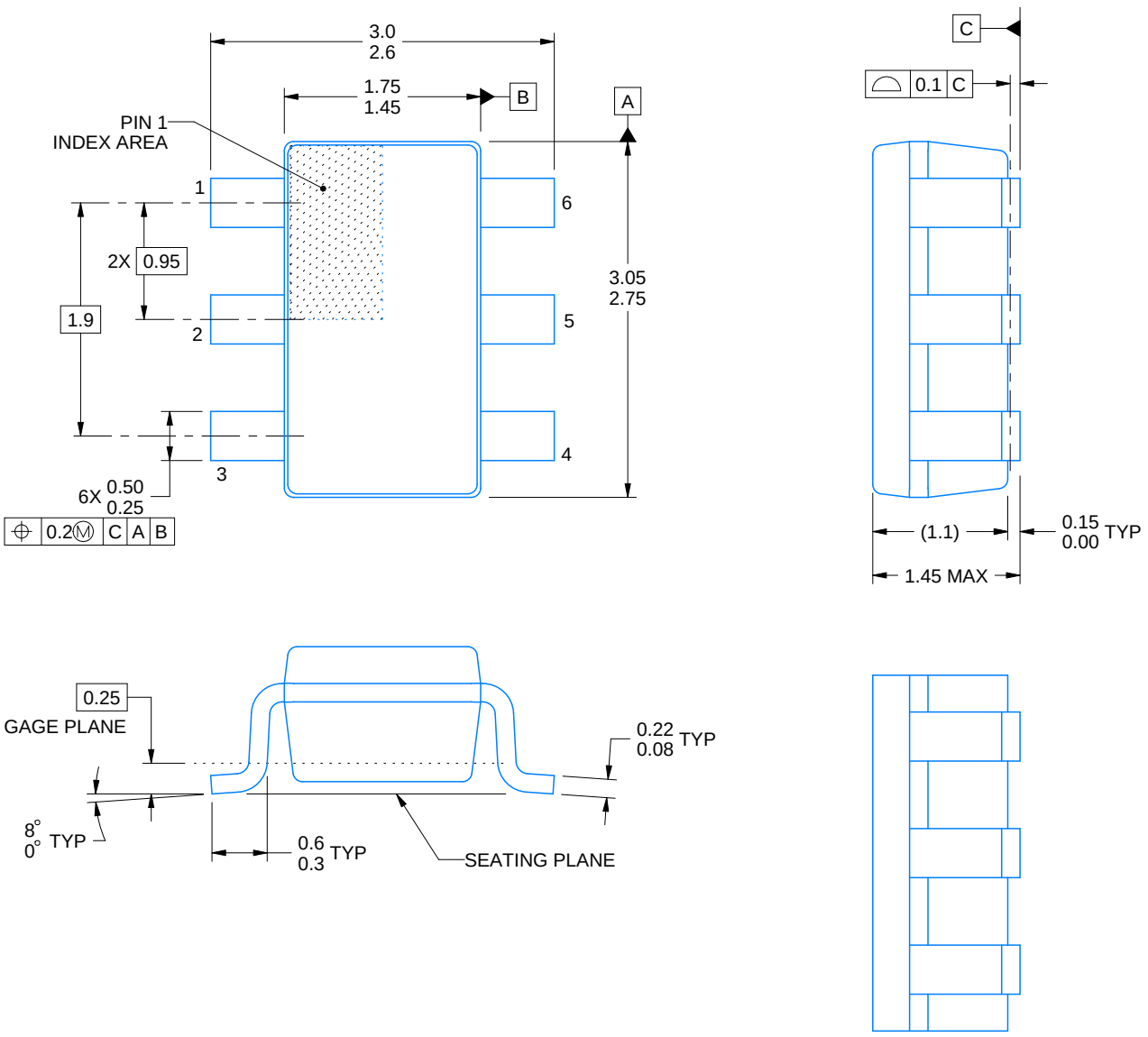
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2766M6/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM2766M6X/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

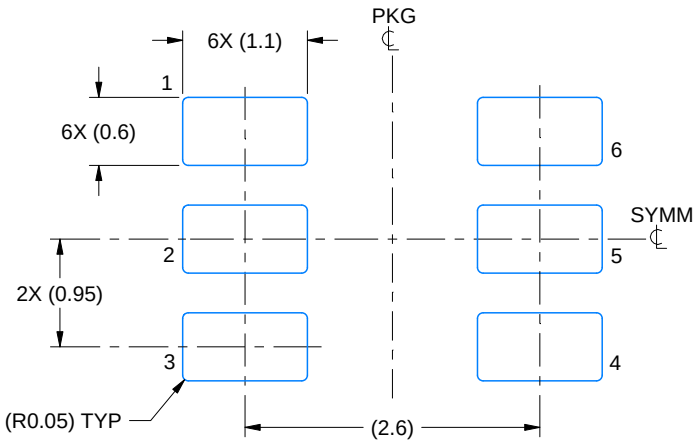


ALTERNATIVE PACKAGE SINGULATION VIEW

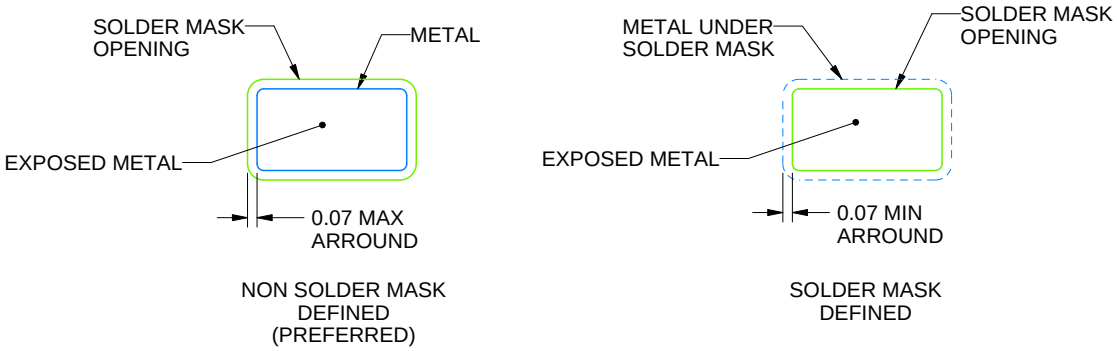
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

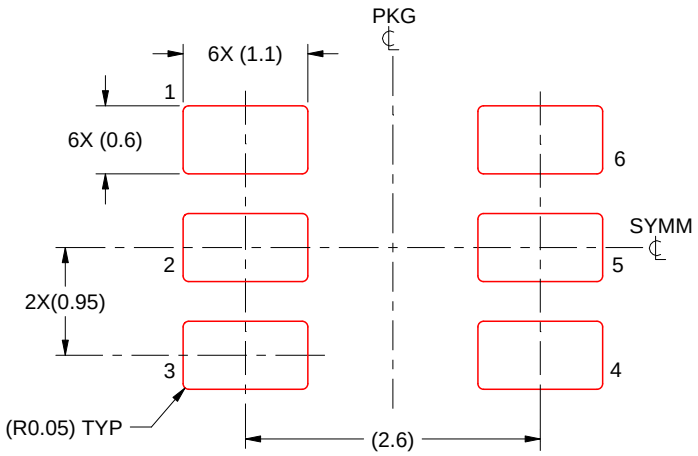


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265