LM27213 Single Phase Hysteretic Buck Controller

Check for Samples: LM27213

FEATURES

- **Ideal Load and Line Transient Responses**
- **5V to 30V Input Range**
- **On-Chip Gate Drive**
- **Convenient CLK_EN# Signal**
- **Input Under-Voltage Lockout**
- **High Light-Load Efficiency**
- **Adjustable Analog Soft Start**
- **Peak Current Limit**
- **Over-Voltage Protection**
- **Error Correction for Good Static Accuracy**
- **±1% DAC Accuracy Over Temperature**
- **Interfaces with the LM2647 System Supply**
- **Available in TSSOP or WQFN Packages**

APPLICATIONS

- **Core Voltage Supply for Low Power Processors**
- **Low Voltage High Current Buck Regulators**

Benefits

- **Single Chip Core Power Solution**
- **Minimum Output Capacitance Required**
- **Low Cost, Compact Design**

DESCRIPTION

The LM27213 is a single-phase synchronous buck regulator controller designed to fully support a portable microprocessor. On-chip gate drive makes for a compact, single chip solution. Output currents in excess of 25 Amps are possible.

The IC employs a current mode hysteretic control mechanism. Inductor current is sensed through a low value sense resistor.

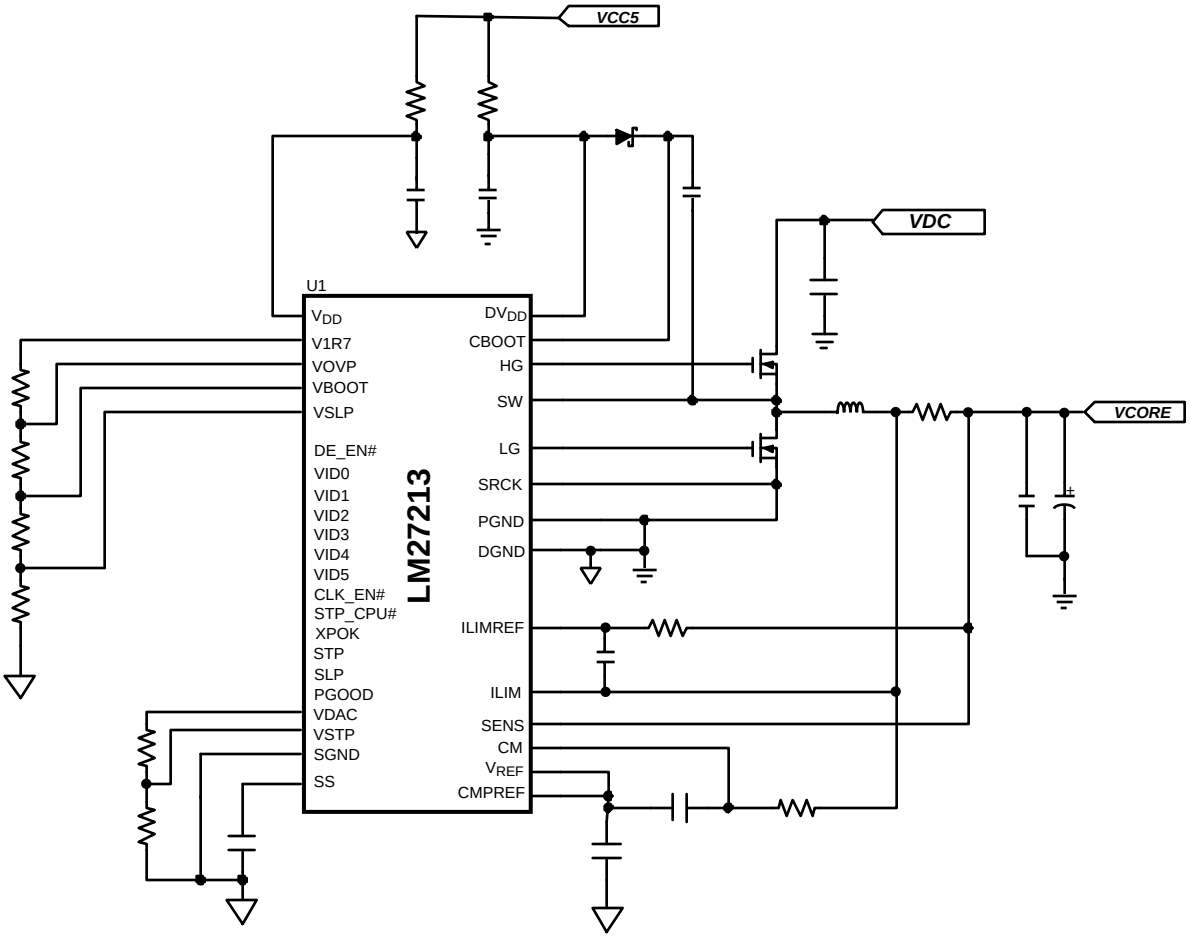
The LM27213 will operate over an input voltage range of 5V to 30V. The output voltage is programmed through 6 Voltage Identification (VID) pins and ranges from 0.700V to 1.708V in 64 steps.

Since the error in the output voltage directly sets the inductor current, the dynamic response to a large, fast load transient is close to a square wave. This is optimal for mode transition requirements. Also, due to the intrinsic input voltage feedforward characteristic of hysteretic control, the line transient response is excellent as well.

The IC provides cycle-by-cycle peak current limit, over-voltage protection, and a power good signal. The LM27213 fully supports the Stop CPU and Sleep modes offered by some processors. When enabled, the IC enters a power-saving “diode emulator” mode which helps prolong battery runtime for portable systems.

The LM27213 also has a soft start feature for the external adjustment of soft start speed.

Typical Application



Connection Diagram

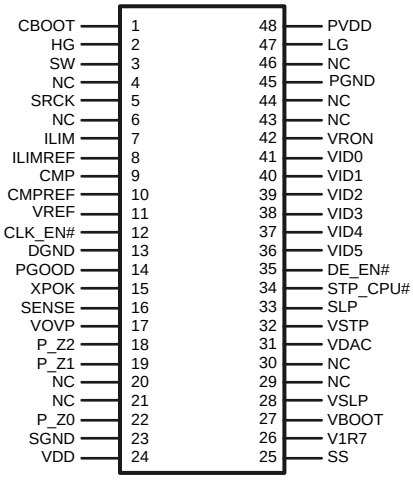


Figure 1. Top View
48-Lead TSSOP
See DGG Package

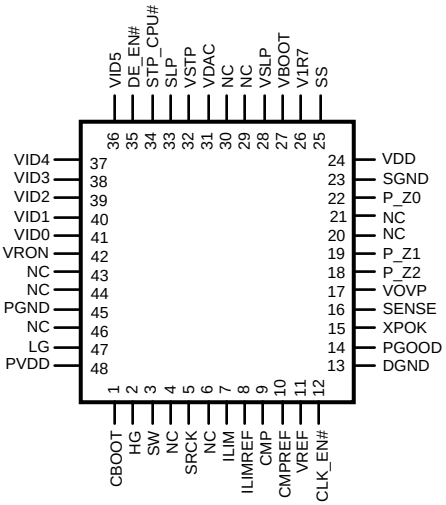


Figure 2. Top View
48-Lead WQFN
See RHS0048A Package

PIN DESCRIPTIONS (TSSOP/LLP)

Pin	Name	Description
1	CBOOT	Connection for the high-side drive bootstrap capacitor
2	HG	High-side FET gate drive output
3	SW	Connect to switch node (drain of bottom power FET) to detect inductor current reversal. Also serves as the return path for the high-side FET gate drive currents
4	NC	No connect
5	SRCK	Source Kelvin. Connect directly to source of low-side FET to detect negative inductor current
6	NC	No connect
7	ILIM	Over-current sense. Voltage between this pin and the regulator output is the voltage across the current sense resistor
8	ILIMREF	Current limit reference. Voltage between this pin and the regulator output sets the inductor current limit level
9	CMP	Current sense. Voltage between this pin and the regulator output sets the cycle by cycle inductor current
10	CMPREF	Inductor current reference. Voltage between this pin and the regulator output programs the inductor current
11	VREF	Desired regulator output voltage under no load
12	CLK_EN#	Signal to start clock chip PLL locking. A low level indicates that the core supply is now stable and the CPU can begin clocking
13	DGND	Digital ground
14	PGOOD	Power good flag. Open-drain output. Logic high when output voltage enters the power good window and XPOK is asserted. Masked during transitions
15	XPOK	Input that tells the LM27213 that the supply voltage for the Memory Controller Hub is up. The LM27213 will regulate the output voltage to VBOOT until XPOK transitions to a high state. PGOOD is forced low as long as this pin is low
16	SENSE	Regulator output voltage sense. Connect directly to output
17	VOVP	Over-voltage protection level. Connect this pin to the desired reference voltage to set the trigger level for over-voltage protection
18	P_Z2	Factory reference trim, do not connect. This pin must float
19	P_Z1	Factory reference trim, do not connect. This pin must float
20	NC	No connect
21	NC	No connect
22	P_Z0	Factory reference trim, do not connect. This pin must float
23	SGND	Signal Ground
24	VDD	Chip power supply
25	SS	Soft start, soft shutdown and slew rate control. Connect a capacitor between this pin and ground to control the soft start and soft shutdown speed. The value of the capacitor will also define the slew rate of the dynamic VID transitions
26	VIR7	1.7V reference voltage
27	VBOOT	Initial output voltage desired after soft start completes. Connect this pin to the desired reference level
28	VSLP	Desired Voltage in Sleep Mode. Connect this pin to the desired reference level
29	NC	No connect
30	NC	No connect
31	VDAC	Buffered Digital-to-Analog converter output
32	VSTP	Desired output voltage in Stop CPU mode. Connect this pin to the desired reference level
33	SLP	When this pin is logic high, VREF voltage is equal to that on the VSLP pin
34	STP_CPU#	When this pin is logic low, VREF voltage is equal to that on the VSTP pin
35	DE_EN#	Power saving mode trigger signal. Enables diode emulation
36	VID5	6th and most significant bit to program the output voltage
37	VID4	5th bit to program the output voltage
38	VID3	4th bit to program the output voltage
39	VID2	3rd bit to program the output voltage

PIN DESCRIPTIONS (TSSOP/LLP) (continued)

Pin	Name	Description
40	VID1	2nd bit to program the output voltage
41	VID0	First and least significant bit to program the output voltage
42	VR_ON	Chip enable input
43	NC	No connect
44	NC	No connect
45	PGND	Power Ground. Connect to ground plane
46	NC	Power ground connection
47	LG	Low-side FET gate drive output
48	PVDD	Power input for the gate drives

VID						Voltage (V)	VID						Voltage (V)
5	4	3	2	1	0		5	4	3	2	1	0	
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VDD, DVDD XPOK, VR_ON, DE_EN#, VOVP, VBOOT, VID0 to VID5, STP_CPU#, SLP, VSLP, VSTP, SENSE, CMP1, CMP2, CMPREF, ILIM1, ILIM2, ILIMREF	-0.3V to 7V
PGOOD	-0.3V to 6V
SW to GND (3)	-2V to 30V
CBOOT to SW	-0.3V to 8V
Power Dissipation TSSOP, TA = 25°C, (4)	1.56W
WQFN, TA = 25°C, (4)	4.9W
Junction Temperature	+150°C
Functional Temp. Range	-20°C to +110°C
ESD Rating (5)	2kV
Storage Temp Range	-65°C to +150°C
Soldering Dwell Time, Temperature Wave Infrared Vapor Phase	 4sec, 260°C 10sec, 240°C 75sec, 219°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For ensured performance limits and associated test conditions, see the Electrical Characteristics table. Functional temperature range is the range within which the device performs its intended functions, but not necessarily meeting the limits specified in the Electrical Characteristic table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The SW pin can have -2V to -0.5 volts applied for a maximum duty cycle of 10% with a minimum frequency of 1Hz. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30 Volts.
(4) The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{JMAX} - T_A) / \theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The TSSOP rating of 1.56W results from using 150°C, 25°C, and 80°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. The θ_{JA} of 90°C/W represents the worst-case condition with no heat sinking of the 48-Pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation should be de-rated by 12.5mW per °C above 25°C ambient. The SQA rating of 5.2W results from using 150°C, 25°C, and 24.2°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. The Absolute Maximum power dissipation should be de-rated by 41mW per °C above 25°C ambient. The LM27213 actively limits its junction temperature to about 150°C.
(5) For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Operating Ratings (1)

VDD	4.75V to 6V
Junction Temperature	-5°C to +110°C
Ambient Temperature	-5°C to +105°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For ensured performance limits and associated test conditions, see the Electrical Characteristics table. Functional temperature range is the range within which the device performs its intended functions, but not necessarily meeting the limits specified in the Electrical Characteristic table.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in **bold face type** apply over a junction temperature range of -5°C to +110°C. Unless otherwise specified, VDD = 5V, SGND = DGND = PGND = SRCK = 0V, unless otherwise stated. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Chip Supply						
I_{sd}	VDD Shutdown Current	VR_ON = 0V, VDD = 6V		1	**10**	µA
I_q	VDD Normal Operating Current	VR_ON = 3.3V		3	**4.2**	mA

(1) All limits are specified at room temperature (standard face type) and at temperature extremes (bold face type). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those in **bold face type** apply over a junction temperature range of -5°C to +110°C. Unless otherwise specified, VDD = 5V, SGND = DGND = PGND = SRCK = 0V, unless otherwise stated. (1)

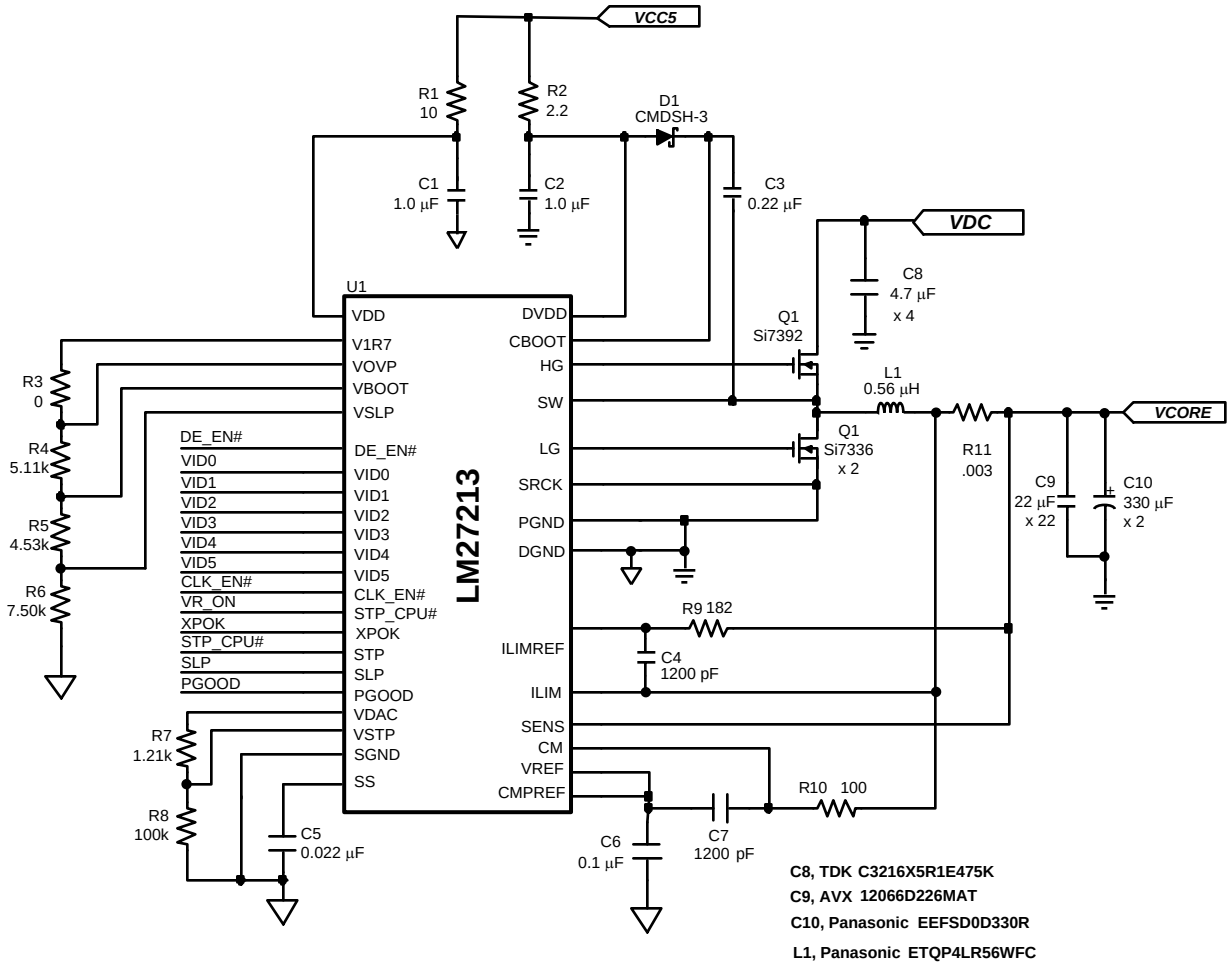
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	UVLO Threshold	VDD = V5A = V5B, rising from 0V	**4**	4.3	**4.5**	V
	UVLO Hysteresis	VDD = V5A = V5B falling from UVLO Threshold	**0.2**	0.66		V
Logic						
V_{LH}	VR_ON, STP_CPU#, XPOK and SLP Input Logic High	VR_ON, STP_CPU#, XPOK or SLP rising from 0V	**2.31**	1.9		V
V_{LL}	VR_ON, STP_CPU#, XPOK and SLP Input Logic Low	VR_ON, STP_CPU#, XPOK or SLP falling from 3.3V		1.43	**0.99**	V
	CLK_EN# Sink Current	CLK_EN# = 0.1V and asserted	**2.5**	7		mA
Power Good						
V_{PGH}	Power Good Upper Threshold As A Percentage of VREF	SENSE voltage rising from 0V	**108**	114	**119**	%
V_{PGL}	Power Good Lower Threshold As A Percentage of VREF	SENSE voltage falling from above VREF	**85**	88	**91**	%
	Hysteresis			5		%
t_{dpgood}	Power Good Delay			3		µs
I_{pgood}	PGOOD Sink Current	PGOOD = 0.1V and asserted	**2.5**	7		mA
Output Voltage Slew Rate Control						
$I_{ss(on)}$	Soft Start Current	SS = 0V	**16**	22	**32**	µA
$I_{ss(off)}$	Soft Shutdown Current		**33**	45	**57**	µA
$I_{ss(slew)}$	VID and Mode Change Slew Rate Control Current		**255**	337	**415**	µA
DAC and References						
VID_{LH}	VID Pins Input Logic High		**0.63**	0.56		V
VID_{LL}	VID Pins Input Logic Low			0.48	**0.315**	V
V_{dac}	DAC Accuracy	Measured at VREF pin				%
		DAC codes from 0.7V to 0.828V	**-1.3**		**1.3**	
		DAC codes from 0.844V to 1.004V	**-1.1**		**1.1**	
		DAC codes from 1.020V to 1.196V	**-0.9**		**0.9**	
		DAC codes from 1.212V to 1.356V	**-1**		**1**	
		DAC codes from 1.372V to 1.500V	**-1.1**		**1.1**	
		DAC codes from 1.516V to 1.708V	**-1.3**		**1.3**	
V1R7	V1R7 Accuracy	17kΩ from V1R7 to GND	**-1.674**	1.708	**1.742**	V
	VSTP Offset	VSTP = 1.398V, Measured at VREF pin	**-5**		**5**	mV
	VBOOT Offset	VBOOT = 1.00V, Measured at VREF pin	**-5**		**5**	mV
	VSLP Offset	VSLP = 0.748V, Measured at VREF pin	**-5**		**5**	mV
I_{VREF}	VREF Driving Capability	source		1.3		mA
		sink		12.6		mA
I_{VDAC}	VDAC Driving Capability	source		1.3		mA
		sink		13.4		mA
I_{V1R7}	V1R7 Driving Capability	source	**90**	549		µA
Error Comparator						
I_{BEC}	Error Comparator Input Bias Current (Sourcing)	CMP = 1.436V.	**12**	21	**33**	µA
V_{OSEC}	Error Comparator Input Offset Voltage	CMPREF = 1.436V.	**-3**		**3**	mV
I_{HYST}	Hysteresis Current (bi-directional)	R_{hys} = 17kW	**38**	50	**68**	µA
		R_{hys} = 170kW		5		µA

Electrical Characteristics (continued)

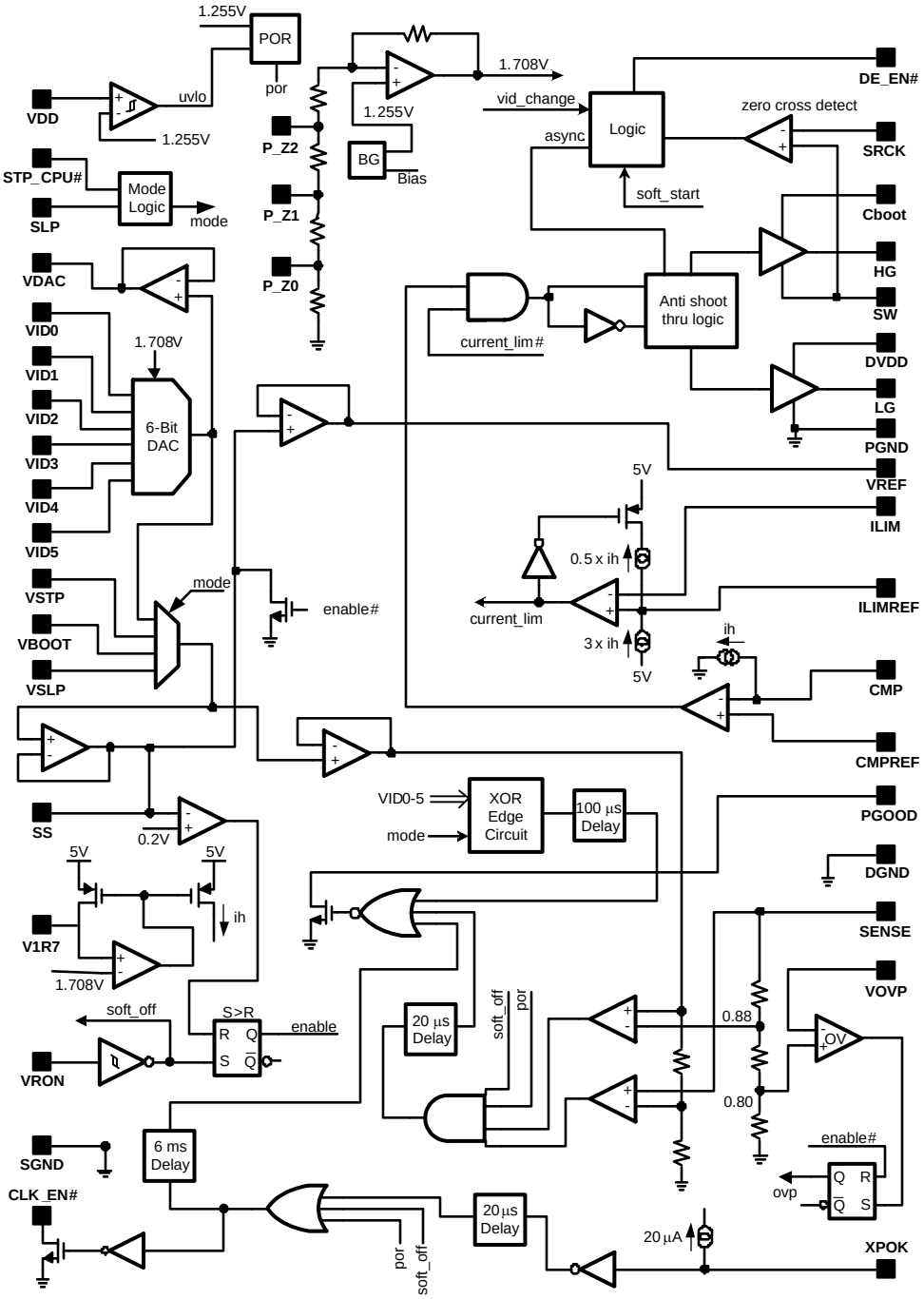
Specifications with standard typeface are for T_J = 25°C, and those in **bold face type** apply over a junction temperature range of -5°C to +110°C. Unless otherwise specified, VDD = 5V, SGND = DGND = PGND = SRCK = 0V, unless otherwise stated. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Limit						
I_{BCLC}	Current Limit Comparator Input Bias Current		**9**	21	**35**	µA
V_{OSCLC}	Current Limit Comparator Input Offset Voltage	ILIMREF = 1.436V.	**-2**		**2**	mV
	Current Limit Setting Current	R_{hys} = 17kW, ILIMREF < ILIMx	**280**	337	**395**	µA
		R_{hys} = 17kW, ILIMREF > ILIMx		250		µA
		R_{hys} = 170kW, ILIMREF < ILIMx		30		µA
Time Delays						
t_{BOOT}	VBOOT Voltage Holdup Time	From assertion of XPOK to assertion of CLK_EN#.	**10**	17	**30**	µs
t_{CPU_PWRGD}	Power Good Mask For Initial VID Voltage Settling	From assertion of CLK_EN# to assertion of PGOOD.	**3**	5	**9**	ms
t_{MASK}	Power Good Mask For VID Changes		**100**	129	**179**	µs
t_{dPG}	Power Good De-assertion Delay Upon Shutdown	Delay From VR_ON de-assertion to PGOOD de-assertion		60		ns
Over-voltage Protection						
V_{TRIP}	SENSE Voltage As A Percentage of VOVP	VOVP = V1R7	**109**	125	**139**	%
System						
$DE\_EN\#_{LH}$	DE_EN# Input Logic High		**0.63**	0.56		V
$DE\_EN\#_{LL}$	DE_EN# Input Logic Low			0.47	**0.315**	V
$I_{DE\_EN\#}$	DE_EN# Pin Leakage Current	DE_EN# = 7.5V		6	**100**	µA
V_{SDT}	Soft Shutdown Finish Threshold	Low-side driver enabled after shutdown		0.3		V
Drivers						
$I_{qdriver}$	Driver Quiescent current	High drive = low, Low drive = high $V_{CBOOT} = V_{DVDD}$ = 5V		14	100	µA
	Top Driver pull-up current	V_{DVdd} = 5V, Load = 0.1Ω		3		A
	Top Drive pull-up Rds_on	$I_{CBOOT} = I_{HG}$ = 0.7A		1.2		Ω
	Top Drive pull-down current	V_{DVdd} = 5V, Load = 0.1Ω		-3.2		A
	Top Drive pull-down Rds_on	$I_{sw} = I_{HG}$ = 0.7A		0.6		Ω
T_{RISEHG}	Top drive rise time	C_{load} = 3.3nF, (10% to 90%)		17		ns
t_{FALLHG}	Top drive fall time	C_{load} = 3.3nF, (10% to 90%)		12		ns
	Bottom driver pull-up current	V_{DVdd} = 5V, Load = 0.1Ω		3.2		A
	Bottom Drive pull-up Rds_on	$I_{CBOOT} = I_{IG}$ = 0.7A		2.9		Ω
	Bottom Drive pull-down currrent	V_{DVdd} = 5V, Load = 0.1Ω		3.2		A
	Bottom Drive pull-down Rds_on	$I_{sw} = I_{IG}$ = 0.7A		0.6		Ω
T_{RISELG}	Bottom Drive rise time	C_{load} = 3.3nF, (10% to 90%)		17		ns
T_{FALLLG}	Bottom Drive fall time	C_{load} = 3.3nF, (10% to 90%)		14		ns
T_{DLY}	Prop delay, CMP to top driver	CMP rising above CMPREF (20mV overdrive) to HG dropping to VSW + 0.9 V_{DVdd}, C_{load} = 3.3nF		89		ns

Typical Application

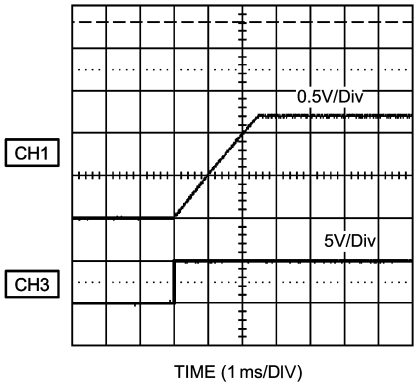


Block Diagram



Typical Performance Characteristics

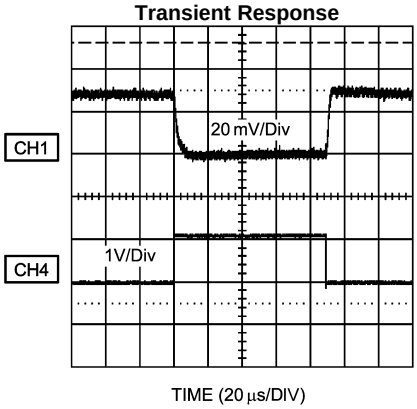
Turn-On Waveforms



Ch1: V_{OUT}
Ch3: VRON, V_{IN} = 13V, I_{OUT} = 0

Figure 3.

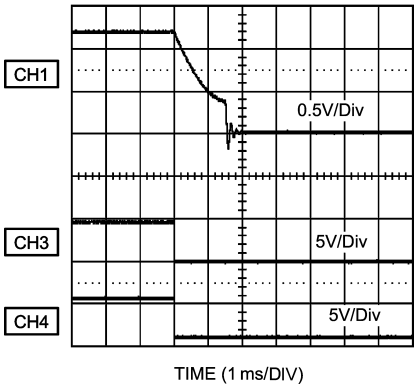
Transient Response



3.5A to 12A load step
Cursor lines are spec limits
Ch1: V_{OUT}
Ch4: I_{OUT}, 8A/div

Figure 4.

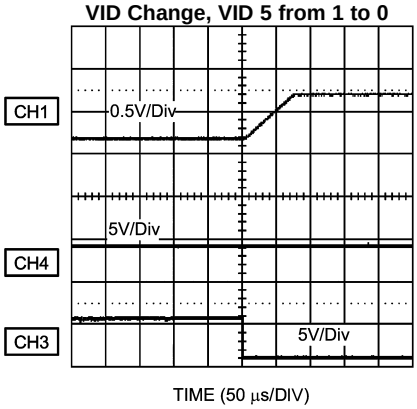
Turn-Off Waveforms



Ch1: V_{OUT}
Ch 3: VRON
Ch 4: PGOOD

Figure 5.

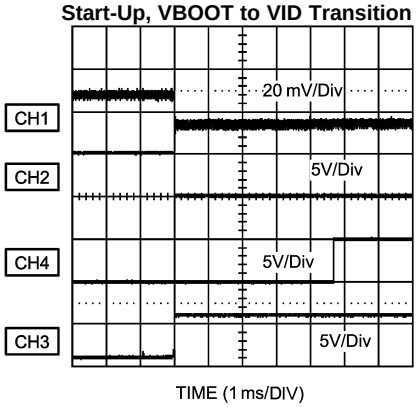
VID Change, VID 5 from 1 to 0



Ch1: V_{OUT}
Ch 3: VID5
Ch 4: PGOOD

Figure 6.

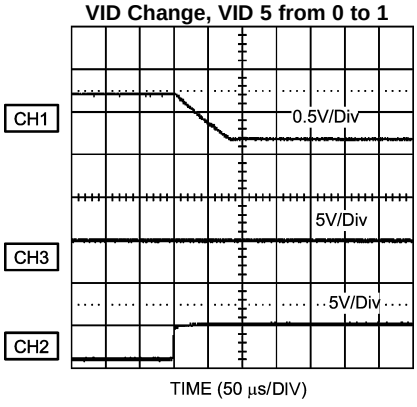
Start-Up, VBOOT to VID Transition



Ch1: V_{OUT}
Ch2: CLK_EN#
Ch 3: XPOK
Ch 4: PGOOD

Figure 7.

VID Change, VID 5 from 0 to 1

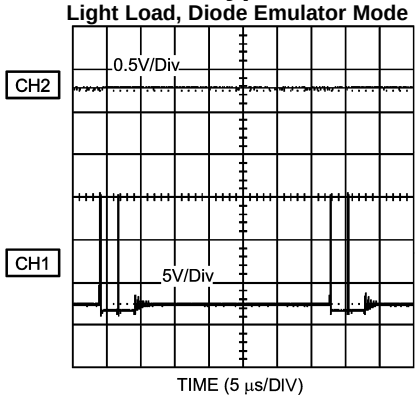


Ch1: V_{OUT}
Ch2: VID5
Ch 3: PGOOD

Figure 8.

Typical Performance Characteristics (continued)

Light Load, Diode Emulator Mode



Ch1: Switch Node
Ch2: VID5
Ch 3: V_{OUT}

Figure 9.

LM29213 Typical Efficiency

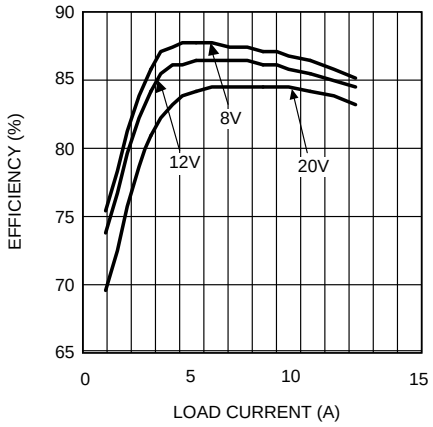


Figure 10.

ILIMREF Bias vs V_{IN} at 25°C

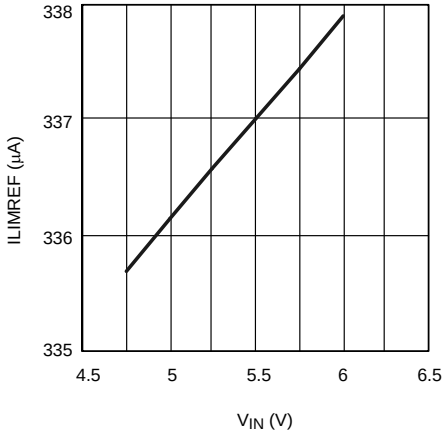


Figure 11.

Hysteresis Current vs V_{IN} at 25°C

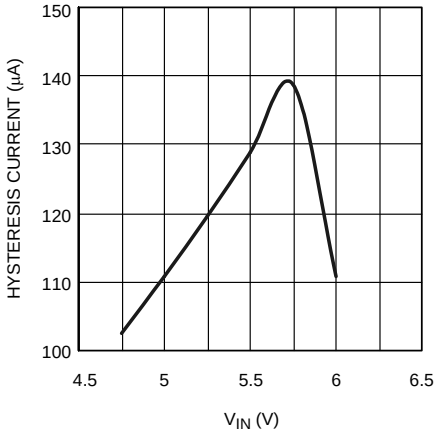


Figure 12.

ILIM vs Temperature

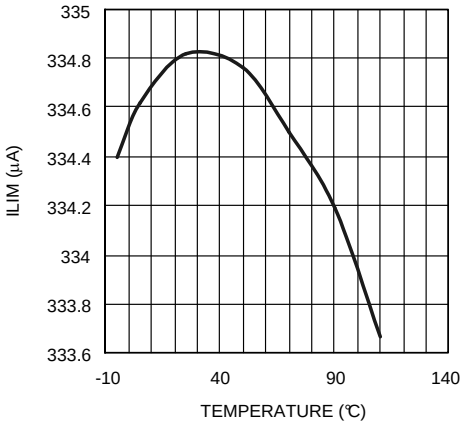


Figure 13.

Hysteresis Current vs Temperature

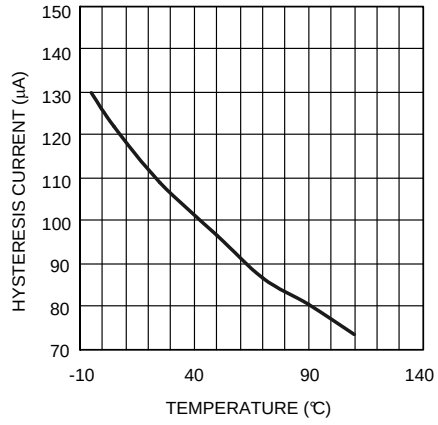


Figure 14.

Typical Performance Characteristics (continued)

DAC 100100 (1.32V) vs Temperature

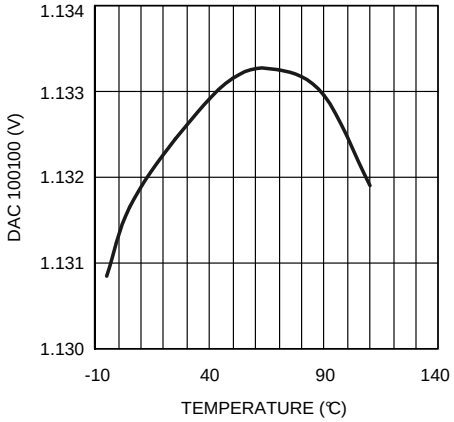


Figure 15.

UVLO Rising Threshold vs Temperature

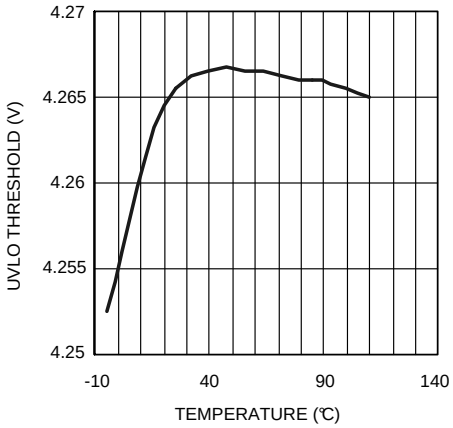


Figure 16.

DAC 100100 vs V_{IN}

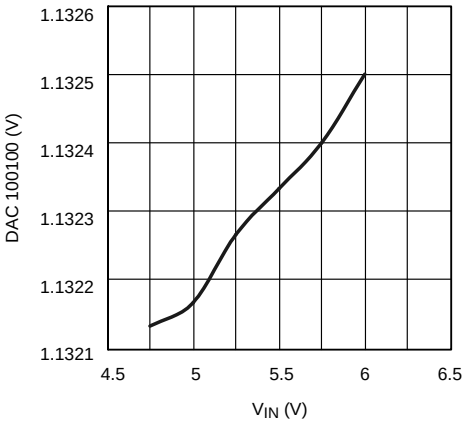


Figure 17.

UVLO Falling Threshold vs Temperature

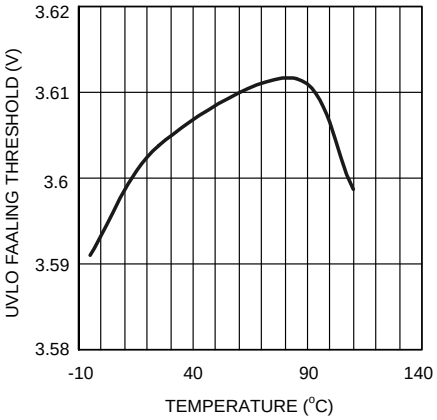


Figure 18.

APPLICATIONS INFORMATION

The LM27213 is a single phase current-mode hysteretic controller intended for controlling a power supply for a low voltage CPU core. It is capable of currents up to approximately 25A with conventional surface mount power devices. Hysteretic control assures the fastest possible transient response and a nearly ideal voltage positioning droop response.

THEORY OF OPERATION

The LM27213 controls the inductor ripple current on a cycle by cycle basis. Several reference voltages are available depending on the mode of operation selected. There is an internal DAC that gets programmed via 6 VID (Voltage Identification) bits. In addition, there are several inputs that allow separate references to be selected in various "sleep modes". An internal MUX selects the reference to be used by the control loop. A softstart function controls the rate at which the selected reference is allowed to ramp up at turn on. There is a cycle by cycle current limit loop as well as over voltage protection.

CONTROL LOOP OPERATION

The main regulator loop is a current mode hysteretic design that maintains control over the buck inductor's peak-peak ripple current. A small hysteresis current is forced to flow through resistor RH which is connected between the CMP pin and the left side of the current sense resistor. When the high-side switch is on, this current flows into the pin forcing CMP below CMPREF. As the inductor current increases, the voltage at CMP rises. The error comparator turns off the high-side switch and turns on the low-side switch when the inductor current exceeds the demand. When the high-side switch turns off the hysteresis current is reversed and current is sourced from the CMP pin. The error comparator now allows the inductor current to decay until the new threshold is crossed. Refer to Figure 19 below. The hysteresis current actually consists of four components. The main hysteresis source is programmed by the current out of the V1R7 reference pin. The total divider resistance on this pin controls the magnitude of this current which is mirrored and sent to the CMP pin. This source will only be active when the high-side switch is on. In addition, there's a small correction current that varies as a function of duty factor. Its magnitude is approximately 74µA*DF, where DF is the duty factor. At typical operating duty factors, it will be around 7µA and in the same direction as the main hysteresis current. This current will flow at all times. The tail current from the current sense comparator also needs to be accounted for. This 16µA flows from the CMP pin when PWM is high, and from the CMPREF pin when PWM is low. Its direction is opposite that of the hysteresis current source and so subtracts from the total hysteresis current. The final contribution to the hysteresis current is the 50uA that is sourced continuously and serves as the "off" hysteresis. It is recommended that approximately 100µA be programmed through the V1R7 pin. At this level the "on" and "off" currents are approximately symmetrical around zero.

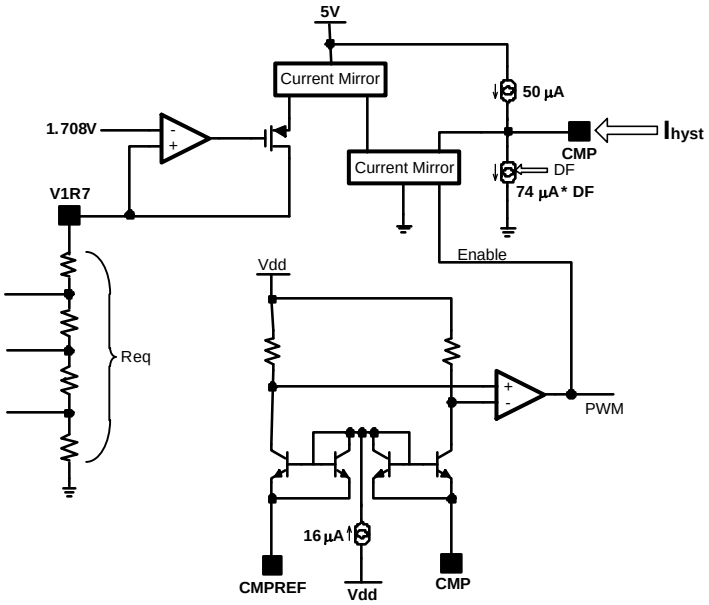


Figure 19.

The current through the V1R7 pin is simply 1.708V divided by Req. Therefore the effective divider resistance should be approximately 17kΩ. The hysteresis current when the high-side switch is on (assuming a roughly 10% duty factor) is 100µA +7µA -16µA - 50µA = 41µA. When the high-side switch is off Ihyst is only 7µA -50µA = -43µA. It is the difference between these two levels that controls the pk-pk inductor current or:

$$\Delta I_{hyst} = I_{V1R7} - 16\mu A \quad (1)$$

Note that the correction current (74µA *DF) does not appear in this equation. It serves only to move the output voltage slightly as a function of duty factor to correct for offsets that are inherent in the topology.

Figure 20 shows a higher level picture of the control loop. The reference that the CMP voltage is compared to is the voltage at the CMPREF pin. Assume that the CMPREF pin is simply tied to a fixed reference voltage (R2 open). The control loop would force the peak voltage at point A minus the hysteresis voltage to equal the reference level. Since the on and off hysteresis currents are symmetrical around zero, the average voltage at point A is therefore equal to the reference voltage. There will be a voltage droop as a function of load (load line) equal to the value of Rsense, the current sense resistor. Adding resistors R1 and R2 allows this load line slope to be increased without raising the value of the sense resistor. The voltage across R2 will equal the voltage across the sense resistor, Rs. So, if R1 = R2 the load line will be twice Rs. Algebraically,

$$LL = R_s \times (1+R1/R2) \quad (2)$$

When the high-side switch has been turned off, the 16µA comparator input bias current now flows out of the CMPREF pin through the parallel combination of R1 and R2. This results in a small increase in the reference voltage (about 1mV with typical values) and will reduce the size of the hysteresis band by an equal amount.

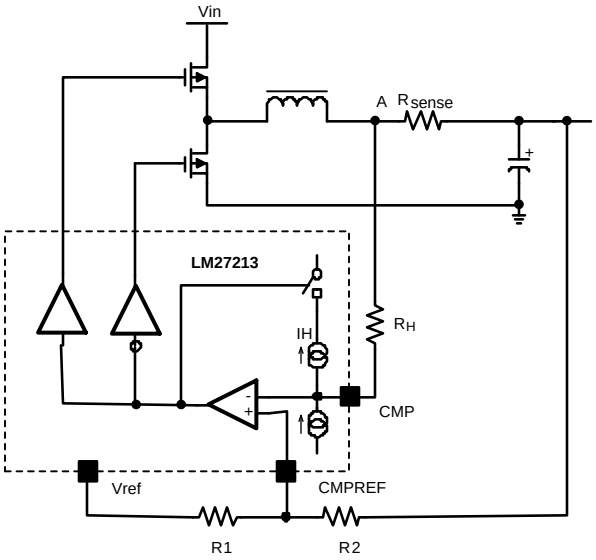


Figure 20.

Figure 21 below shows the theoretical waveform that is to be expected at the CMP pin. Zero output ripple voltage is assumed. In reality these signals ride on top of the regulator's output ripple and may be very hard to discern. There's a small delay time from the instant the voltage on the CMP pin crosses the voltage on CMPREF. This delay will result in the inductor peak current overshooting the hysteresis setting. For high step-down ratios the inductor current down-slope will be much more shallow than the up-slope. Therefore, the undershoot magnitude will be less than the overshoot magnitude. As a result of these delays the actual hysteresis will be somewhat greater than programmed.

The actual wave shapes will be very dependant on the type of output capacitor selected. The resistive component of electrolytic type capacitors (ESR) will serve to provide a significant amount of instantaneous feedforward due to the current flow through the capacitors. By contrast, if an all ceramic output capacitor decoupling network is employed, the current flow through the capacitor is integrated over time, and current information is phase shifted. This tends to alter the regulator's behavior somewhat. In particular, the operating frequency will be very hard to predict since decoupling parasitics play a significant part in shaping the waveforms at the CMP pin. As such, it is generally simplest to choose the final value for the hysteresis resistor empirically.

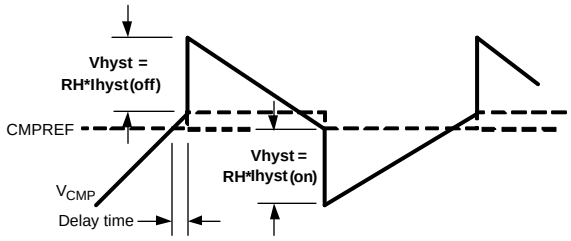


Figure 21.

The approximate operating frequency is:

$$F_{SW} = R_S \times (V_O - V_{IN}) \frac{V_O}{[\Delta I_{hys} \times R_{hys} \times L \times (2 \times V_O - V_{IN})]} \quad (3)$$

where

- R_s is the value of the current sense resistor in Ohms
- L is the inductor value in µH
- ΔI_{hyst} is the hysteresis current in Amps
- R_{hys} is the value of the hysteresis resistor in Ohms

This equation is greatly simplified and fails to account for the effects of output ripple, comparator delay times etc. There are far too many subtle variables involved in this topology to be able to make very accurate operating frequency estimates. This equation should provide a ballpark starting point with the final value of the hysteresis resistor arrived at empirically. At high frequency the delays through the comparator and driver will be the dominant factor in determining the operating frequency.

CURRENT LIMITING

Current limit is achieved by comparing the instantaneous voltage across the current sense resistor with the voltage developed across the current limit threshold resistor, R13 in the typical application circuit. If the controller sees this threshold exceeded, the current switching cycle is terminated and the hysteresis current dropped in half. The voltage across the current limit set point resistor is determined by the value of the resistor and the magnitude of the current through the ILIMREF pin. This current is nominally three times the current drawn through the V1R7 reference pin. When current limit is reached, this current is reduced to 250% of the V1R7 current. Be sure to use the full load DC current plus ½ the pk-pk inductor ripple current when determining the required current sense threshold.

POWER GOOD

The output voltage is sensed at the Sense pin (16) and monitored by a window comparator with thresholds set to nominally 88% and 112% of the selected output voltage set point. As long as V_{core} remains within the window, the power good signal will be logic high. This output is an open drain device and requires an external pull up. At power up, the LM27213 will wait approximately 5ms after XPOK is asserted before releasing PGOOD. If the output voltage is then within the ±12% window, the flag will be asserted.

OVER-VOLTAGE PROTECTION

The sense pin is also used to provide the input to the over-voltage protection circuitry. If at any time the output is determined to be more than a nominal 120% of the voltage set on the VOVP pin (17), the high-side FET is turned off and the low-side FET is turned on. The soft start capacitor will also be discharged. This state is latched. In order to initiate a restart, remove and restore power to the controller or toggle the VRON pin.

SOFT START

When VRON is enabled the regulator begins a normal start sequence that actively controls the rise of output voltage. An internal 20µA current source supplies current through the Soft Start pin (25) that charges the soft start capacitor. The output voltage is forced to track this voltage up. The result is a linear output voltage rise. The capacitor value required is simply 20µA divided by the desired slew rate. For an output voltage rate of rise of 1V/ms, the capacitor should be about 20nF.

SOFT STOP

When VRON is deasserted, the LM27213 starts to discharge the soft start capacitor with an internal 45µA current sink. V_{core} is forced to follow the resulting linear ramp voltage on the soft start capacitor downward. When V_{core} reaches approximately 300mV the high-side FET is disabled and the low-side FET is turned on to quickly discharge the output to zero and hold it there. This forces a controlled turn off slew rate that eliminates the possibility of the output voltage ringing significantly below ground. It can also be helpful in the sequencing of multiple supply rails.

STARTUP SEQUENCING

At initial power up the LM27213 targets a voltage equal to V_{boot}. This is the voltage level set at the VBOOT pin (27) by a resistor divider that is powered by the V1R7 reference output (pin 26). This divider also has taps for the OVP threshold and deeper sleep voltage set point. The regulator's output will remain at V_{boot} until a time T_{boot} after the XPOK flag clears. T_{boot} is nominally 20µs. After the T_{boot} time expires CLK_EN# will be asserted and the output will transition to the voltage selected by the VID bits. Power good will be enabled nominally 5ms after CLK_EN# is asserted.

DYNAMIC VID TRANSITIONS

Upon detecting a VID or mode change the LM27213 masks the power good comparator for a period of approximately 130µs. During the blanking interval the power good output is forced high while the output voltage is in slew to the newly selected level. The slew rate is determined by the soft start capacitor value. The charge/discharge current driving the soft start capacitor will be 350µA typically. The programmed slew rate is therefore 350µA divided by the soft start pin capacitance.

STOP CPU MODE

If the STP_CPU# pin (34) is asserted with SLP de-asserted the VREF pin voltage will be forced to the voltage on the VSTP pin (32). The output will slew at a rate determined as above to the new value. The PGOOD mask is in effect for 130µs.

SLEEP MODE

To enable sleep mode both STP_CPU# and SLP need to be asserted. The VREF pin voltage will transition to the voltage on the VSLP pin with a slew rate as discussed under ynamic VID transitions and the PGOOD mask is activated for 130µs.

POWER SAVING MODE

The LM27213 allows for high efficiency operation at very low power levels by employing a diode emulator mode. This can be activated in either deep sleep or deeper sleep modes only. Assert the DE_EN# pin while in a sleep mode to activate this function. When operating at low power the LM27213 detects inductor current reversal with a zero cross detector connected to the drain of the low-side FET. The voltage at this node is normally below ground when the low side FET is on but will become positive when the inductor current reverses. When the inductor current reversal is detected the low side switch is turned off and essentially becomes a nearly ideal diode. Due to the hysteretic control mode, the regulator operating frequency will be greatly reduced at light loads. High-side switch on-time will not change significantly compared to normal operation, but the off times will extend greatly. Care must be taken to connect the SRCK (Source Kelvin, pin 5) close to the low-side switch source connection, as this is the reference input to the zero cross detector.

Component Selection

There are numerous tradeoffs to be made in settling on a final set of component choices and as a result the process tends to be somewhat iterative. There's always more than one combination of parts that will work in a given application.

We will start with a few rule of thumb assumptions and then adjust as required to find a combination that meets the specification requirements and is cost effective. Some of the choices can be thought of as somewhat philosophical.

Let's start the design by choosing an inductor and then develop the remainder of the design around that choice.

INDUCTOR SELECTION

A good place to start is by choosing an appropriate buck inductor. A decent rule of thumb is to allow the worst case, peak to peak ripple current to be on the order of 40% to 50% of the full load output current. So, for a design of 12A at full load, the ripple current should be in the range of 4.8A to 6A. Larger or smaller ripple currents may well be acceptable but there are tradeoffs associated with these choices. As inductor value increases, there is a corresponding need to increase the amount of output capacitance to handle load transients. Conversely, as inductance is reduced, the RMS switch currents tend to rise and therefore efficiency suffers slightly while dynamic performance is improved.

The worst case ripple current will occur at the combination of maximum input and output voltage. Let's assume an output voltage of 1.180V and a maximum input of 16V. This will assume operation on a wall adapter while battery voltage may be only 12V maximum. Another assumption that must be made is the intended operating frequency. Again there exists a tradeoff between dynamic performance and efficiency. The "sweet spot" at the time of this writing is roughly in the range of 300kHz to 400kHz. That will in all likelihood shift positive in time as FET technology improves. The hysteretic architecture also varies the operating frequency as a function of input voltage with the regulator tending to run a bit slower at high input voltages. Let's assume a 300kHz frequency at high input line. Also, since the efficiency is of somewhat less of a concern when operating from a wall adapter we'll design for the high end of the ripple current range under this condition. The ripple current will be lower when operating from a battery since the input voltage will be lower and the switching frequency will be somewhat higher. With all that settled let's calculate a value for L.

$$L = (V_{IN}-V_O)V_O/(\Delta I \times V_{IN} \times f_{SW})$$

where

- L is the inductor value
- V_{in} is the input voltage
- V_o is the output voltage
- ΔI is the ripple current
- f_{sw} is the switching frequency (4)

So,

$$L = (16V-1.18V)1.18V/(6A \times 16V \times 300kHz)$$

where

- L = 0.60 µH (5)

If the switching frequency is pushed up a bit the inductor value may be reduced accordingly. In general for a 12A, low voltage CPU, a value between 0.56 µH and 0.7 µH works out well. The inductor chosen should be capable of handling the full load current continuously. It must not hard saturate under fault conditions. The saturation specifications for most inductors indicate when the inductance has fallen off by a given percentage. This percentage will vary by manufacturer and is not standardized. As such, it's best to look at the published curves of inductance vs. DC current. If the inductor maintains more than 1/3 of it's specified no load inductance under short circuit conditions, it will probably work just fine. There will also most likely be an RMS current rating for the inductor as well. This relates to the heating to be expected at the rated DC current. In most processor applications it's safe to assume the average DC current for thermal analysis purposes will be approximately 80% of the specified maximum load current. The inductor should be specified for at least this value of continuous current.

OUTPUT CAPACITOR SELECTION

Once an inductor value is chosen it's time to look at the output capacitors. There are several possible basic approaches to take with regards to output de-coupling. It's possible to use ceramic capacitors exclusively. This will require a rather large number of small case size capacitors. It is also possible to use primarily aluminum-polymer type devices for the bulk decoupling with a relatively small number of ceramic capacitors for high frequency bypassing. The third approach is something that's more a combination of the two approaches, using a moderate number of ceramic capacitor and a couple of large bulk caps. The design criteria will be slightly different with the various approaches.

The controlling factor in a CPU core voltage regulator is generally the load-off transient. When the processor load drops dramatically, all the energy stored in the inductor will get transferred into the output capacitors. The energy stored in an inductor is L x I^2/2 while the energy stored in a capacitor is C x V^2/2. So:

$$C_{min} = L(I_{max}^2 - I_{min}^2)/(V_{max2}-V_{init}^2)$$

where

- C_{min} is the minimum capacitance required to meet the specified voltage limits
- L is the inductor value
- I_{max} is the peak inductor current at the time the load step occurs
- I_{min} is the load current after the transient has settled
- V_{max} is the maximum allowed output voltage at the low load condition
- V_{init} is the initial output voltage at the time of the load step (6)

It's recommended that the current used for I_{max} be equal to the full load output current plus ½ the estimated pk-pk ripple current

From the example being examined earlier, if we assume a 12A full load, a 0.56µH inductor, an initial voltage of 1.144V, a minimum current of 3.5A and a maximum voltage of 1.197V, the minimum allowable output capacitance is calculated as:

Since ripple current is approximately 6A,

$$I_{max} = 12A + 3A = 15A \quad (7)$$

$$C_{min} = 0.56\mu H(15A^2 - 3.5A^2)/1.197V^2\text{-}1.144V^2) = 960\mu F \quad (8)$$

This calculation assumes perfect capacitors (ESR = 0) and is a reasonable assumption for an all ceramic solution only. More capacitance will be required if aluminum-poly type capacitors are used due to their higher ESR. However, that will generally not be a problem since they tend to have large capacitance values. If using 22 µF, 1206 case ceramic capacitors, this design would require approximately 44 capacitors distributed around the processor. Only capacitors with either X5R or X7R dielectrics should be considered. Lower cost devices have voltage and temperature coefficients that make them unusable in these applications. Using a small number of physically large ceramic capacitors is not recommended since the lead inductance will be excessive. They tend not to provide adequate high frequency bypassing.

A reasonable way to reduce the capacitor count is through the addition of several aluminum-poly type capacitors. A typical example may be the Panasonic SP series. A 330µF, 2.5V device is available with an ESR of only 5mΩ. Adding a pair of these will permit reducing the number of ceramic capacitors considerably.

A reasonable estimate of the soar voltage when the load is suddenly reduced when using primarily alminum-poly type capacitors can be obtained from the following equation:

$$V(T) = \left[\frac{1}{C}\left(I_0 \text{ x } T - \frac{1}{2} \text{ x } m \text{ x } T^2\right) + (I) - m \text{ x } T) \text{ x } ESR\right]$$

where

- V(T) is the instantaneous capacitor voltage increase above the initial DC voltage at the instant the load is reduced
- C is output capacitance in µF
- I_0 is the inductor current at the instant the load is decreased
- ESR is the output capacitor ESR
- m is the inductor current down slope equal to Vout/L (9)

The maxima occurs at :

$$T_{max} = \frac{I_0 - m \times ESR \times C}{m} \quad (10)$$

Simply solve for Tmax and substitute into the equation for V(T) to calculate the maximum output voltage rise. This equation accounts for the decrease in voltage across the ESR as the capacitors are being charged by the decreasing inductor current.

Using numbers from the previous example:

T_{max} = (12A-2.043A/µs*0.0025Ω*660µF)/2.043A/µs = 4.22µs

and

- V_{max} = 0.058V (11)

This is just a bit higher than the specification allows but does not account for improvements expected as a result of having a number of ceramic output capacitors on the board. The performance of combinations of capacitors is best examined using a circuit simulator as the mathematics gets unwieldy. A simple model would be an inductor connected in parallel with the output capacitors. Set the initial conditions for the peak inductor current at full load and the capacitor voltage to the lowest point on the load line. A current source in parallel with the output that is set for the minimum load current will allow the simulation of load steps that are less than 100% of full load.

A simulation of the above conditions with the addition of 10 pieces of a 22µF ceramic capacitor yields a peak excursion of 1.180V, which is well within the specified limit.

MOSFET SELECTION

The choice of power FETs is driven primarily by efficiency or thermal considerations. There are two main loss components to consider, conduction losses and switching losses. The switching losses are primarily due to parasitics in the FETs and are very hard to estimate with any degree of accuracy. The conduction losses are much easier to characterize. The switching losses in the synchronous FET are very low since it's essentially a zero voltage switched device. However, the high-side device's switching losses are usually comparable to its conduction losses. The primary contributor to high-side FET switching losses is related to the reverse recovery characteristics of the synchronous FET's body diode. During the small dead band where both FETs are off every cycle, the synchronous FET's body diode will carry the inductor current. Problems arise because the body diode exhibits a significant reverse recovery time, trr. During this time, the FET looks like a short circuit. When the high-side FET is subsequently turned on, there is a shoot through path from the input supply to ground. A larger high-side FET will tend to exhibit a larger shoot through current. Therefore, it is undesirable to oversize the high-side device. Since the synchronous FET looks like a short, the entire supply voltage is impressed across the high-side device, along with a simultaneous high current. The result is very high momentary power dissipation. The total power lost is a direct function of the switching frequency.

For a single-phase design something on the order of 1W of dissipation in the power switches is a reasonable place to start. Assume further that this will be split equally between the high and low side FETs. Since the low-side FET switches at nearly zero volts the transition losses will be very low. The high-side switch will, however, sustain large switching losses. In all likelihood they will be comparable to, or exceed, the conduction losses.

With 500mΩ allocated to the synchronous switch dissipation we can calculate the required on-resistance. Assume the hot on-resistance will be about 140% of the room temp $R_{ds(on)}$. Therefore:

$R_{ds(on)} = P_{diss}/(I^2 \times 1.4 \times (1-DF))$

where

- DF = duty factor or V_{out}/V_{in}
- P_{diss} = allowed dissipation
- I is the design thermal current (12)

As a general rule of thumb, assume the design thermal current is approximately 80% of full load current unless the specification indicates otherwise. In this case, assume a current of 9.6A. Also, duty factor should be calculated at high input line voltage. Assume 16V for our example. So the maximum on-resistance for the synchronous switch will be:

$R_{ds(on)} = 0.5W/(9.6A^2 \times 1.4 \times (1-1.15V/16V))$

- $R_{ds(on)}$ = 4.2mΩ (13)

In a similar fashion the high-side switch can be sized. Allot ½ of the total dissipation to switching losses. The on interval is now DF rather than 1-DF and low input line is assumed:

$$R_{ds(on)} = P_{diss}/(I^2 \times 1.4 \times (DF)) \quad (14)$$

$$R_{ds(on)} = 0.25W/(9.6A^2 \times 1.4 \times 1.15V/8V)$$

- $R_{ds(on)} = 13.4m\Omega$ (15)

An Si7390 high-side switch and an Si7336 low-side switch meet this requirement

If the same analysis is done assuming a 12A continuous load current the results suggest a low-side FET with an on-resistance of 2.7mΩ and a high-side FET on-resistance of 8.6mΩ.

GATE DRIVE REQUIREMENTS

The bootstrap capacitor choice is based largely on the gate charge requirements of the high-side FET. The charge stored on the bootstrap cap should be about 20X the high-side FET's gate charge. For the Si7390 the specified gate charge is 15nC max. So the bootstrap capacitor should store a minimum of 300nC at 5V. This translates to a capacitance of 0.06µF or larger. A 0.10µF or larger X5R dielectric capacitor would be a good choice. Under sizing the bootstrap capacitor will result in inadequate gate drive to the high-side switch.

INPUT CAPACITOR SELECTION

The input capacitor selection is based largely on ripple current capability. The instantaneous pulse currents drawn by the power supply must be deliv-ered by the input capacitors. This is related to the fact that the input power source, be it a battery pack or a wall adapter, will place a substantial impedance in series with the input path. As such, their ability to deliver large, fast rise time current pulses is limited. The input capacitors need to average these pulse currents and smooth the current demand placed on the source.

Ceramic capacitors offer a good combination of ripple current capability and voltage rating, however they tend to do so with relatively low capacitance values. It's also not uncommon to find wall adapters and batteries with impedances on the order of several hundred milliohms. The result is that while cycle-by-cycle current demand may be met, the input capacitor network cannot deliver enough energy to prevent significant amounts of voltage ripple when the load current is varied at a low rate. In particular, if the load varies at a frequency in the 2kHz to 4kHz range, the resulting large variation in voltage observed at the power supply input will result in noticeable audio noise being produced by the piezo electric effects that are characteristic of ceramic capacitors. There are several ways to mitigate this problem. The first is to use physically small ceramic capacitors since they tend to be less efficient noise generators. That, however, would tend to limit the amount of capacitance to an unacceptably low value. The use of aluminum-poly type capacitors such as Sanyo's Poscap series is a viable option as well. They can provide adequate levels of capacitance with very good ripple current capability. The down side of this solution is cost. Another possible approach is to use relatively large ceramic capacitors and add a relatively large aluminum electrolytic capacitor to hold up the supply voltage. The ceramics deliver the high frequency pulse currents while the bulk caps smooth the longer term variation. In general a few hundred microfarads is adequate for this purpose. As long as the AC ripple voltage impressed on the ceramic capacitors is small, on the order of a few tenths of a volt, the ceramic capacitors are not going to be excessively noisy.

For purposes of sizing the high frequency input decoupling, the RMS input ripple current must be estimated. The input ripple current will be approximately 50% of the output current at a 50% duty factor and decrease as duty factor drops. Figure 22 shows this relationship.

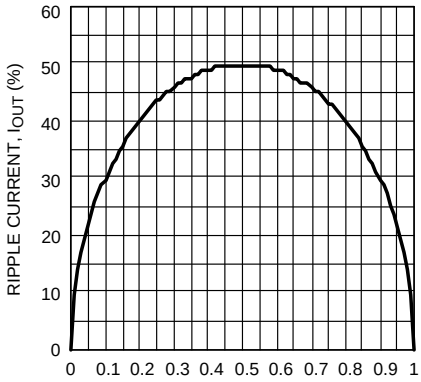


Figure 22. RMS Input Ripple Current as a Percentage of DC Output Current

So for a design that must operate at a steady state load current of 12A, with 1.4V out and 8V in, the RMS input ripple current would be about 37% of 12A or 4.4A RMS. A sufficient number of capacitors must be connected in parallel to handle this current. For capacitors rated at 1.5A each, a minimum of 3 would be required. If it's desired to add enough bulk capacitance to control the input's low frequency ripple voltage, the characteristic impedance of the input power source must be well understood.

Bypassing Considerations

The LM27213 should have its supply pin (24) well bypassed. Generally a 1µF capacitor connected between the Vdd pin and the SGND pin (23), should be adequate. It's a good idea to add a resistor of about 10Ω in series with the input source to provide some decoupling from noise on the 5V rail. The LM27213's own gate drive pulse currents can corrupt the 5V rail enough to cause problems without this filter. There also needs to be a 1µF or larger ceramic capacitor connected between the driver supply pin PVDD (48) and PGND (45). The bypass capacitors should be located very close to the pins to provide a low inductance path. This is particularly important for the PVDD bypass. This capacitor must supply all of the low-side gate drive pulse currents as well as the charging current for the high-side bootstrap capacitor. It's also a good idea to install a 0.1µF capacitor between the VREF pin (11) and SGND. In addition, there should be small filter capacitors connected between the ILIM and ILIMREF pins and the CMP and CMPREF pins. Typically, a 1200pF capacitor will prove adequate for this purpose.

Current Sense Resistor

The maximum value allowed for the current sense resistor is a value equal to the desired load line slope. Increasing beyond this value will make the load line excessively steep with no way to reduce the slope. Lower values are permissible and values as low as 1mΩ have been used successfully. The regulator will have a tendency to exhibit excessive amounts of pulse jitter if the sense resistor is too small since the current sense signal is reduced as well. One way to mitigate this problem is to add a little filtering to the load line setting resistor R2 in Figure 21. A typical time constant to shoot for is approximately 500ns. So for R2 = 100Ω, something around a 4700pF capacitor should prove helpful. If this capacitor is made too large the result will be large overshoot and undershoot in the response to load transients. See the section below on load line setting for more information about choosing these resistors.

Load Line Setting Resistors

Resistors R1, R2, and the current sense resistor (see Figure 20) are used to control the slope of the load line. In the simplest configuration R1 = 0 ohms and R2 is omitted. In this case the load line is nominally equal to the current sense resistor value. For relatively low current designs this configuration can work acceptably well. At higher current levels the DC drop across the power planes may well contribute an excessive error since the distribution path between the sense resistor and the load is effectively in series with the current sense resistor, and therefore, will steepen the load line. For designs with relatively steep load lines (3 mΩ) the power dissipation is also excessive at high currents. The solution is to lower the sense resistor value and add the R1, R2 divider to synthesize a steeper slope. The load line is calculated from:

$$LL = R_s \times (1+R1/R2) \quad (16)$$

Since the power plane resistance will increase the load line by an amount that's nearly impossible to estimate accurately, the simplest approach is to install the values calculated for the ideal, lossless power path, and run the circuit. Record the no load and full load output voltage and calculate the load line impedance.

$$LL = (V_0 - V_{full})/I_{full}$$

where

- V_0 is the no load output voltage
- V_{full} is the full load output voltage
- And I_{full} is the full load current (17)

Use this information along with the installed values of R1 and R2 to calculate the effective sense resistor value:

$$R_{se} = LL/(1+R1/R2) \quad (18)$$

Now using this value of sense resistor, recalculate a new value for R1:

$$R1 = R2(LL/R_{se} - 1) \quad (19)$$

Installing these values for R1 and R2 should yield a nearly perfect load line.

Layout Guidelines

As is true for any high-current power supply design, care needs to be taken when doing an LM27213 layout. As a general rule, it makes the most sense to start the layout by placing the power path components to connect in a logical power flow. The input ceramic capacitors should be connected as close as physically possible to the source of the low side FET and the drain of the high-side FET. The loop area enclosed by the input capacitors and FETs needs to be minimized to control ringing and optimize the switch rise and fall times. A good practice is to connect the FETs on the top side of the board with the bypass capacitors located immediately below on the back side. The capacitors' ground pads should be located directly beneath the low-side FET's source pad and a collection of vias used to hook the two together and at the same time tie to the internal ground plane. Figure on allowing one amp of load current per via if the hole diameter is less than 15 mils and two Amps per via if greater than 20 mils. More vias are almost always better than fewer.

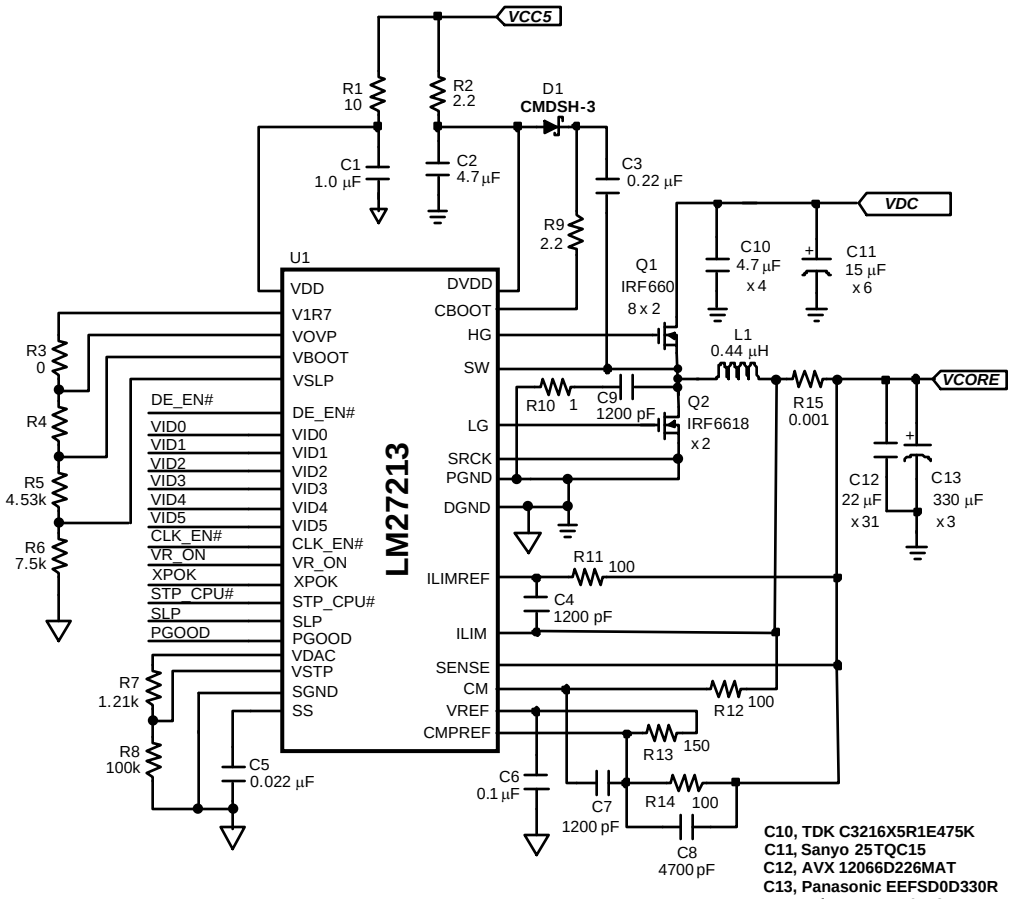
Keep the switch node connection between the two FETs and the inductor as short and wide as possible. The inductor should be located very close to the FETs. The inductor should then flow in to the sense resistor that needs to be immediately adjacent to the processor decoupling capacitors.

The LM27213 needs to be located relatively close to the FETs to minimize the gate drive lengths. Also, route the high-side gate signal (pin 2) and the SW pin (3) parallel to and very close to each other to minimize the inductance of the loop enclosed. These traces should be at least 15 mils wide. The connections to the current sense resistor must be made as Kelvin connections. Again, route these two traces in parallel if possible to minimize noise susceptibility. The sense pin (16) is best connected to the core voltage near the center of the CPU socket, but will in all likelihood work correctly if connected at the bypass capacitors located around the periphery of the CPU socket. This line is the source of output voltage information for the over voltage protection circuit and power good comparators.

Probably the most critical consideration for the controller is grounding. There are several ground-referenced pins that need to be treated quite differently. A good practice is to tie the power ground pin (45) to the main power plane with a single via. This pin is the ground connection for the gate drive and as such will carry very large pulse currents. The bypass capacitor for DVDD should connect very close to this ground connection if at all possible. DGND (13) is not particularly critical and should tie to the main ground plane as well. It only carries the return currents for the digital portions of the controller, which are not very large. The SGND pin (23) is the most critical and should also tie to the plane with a separate via close to PGND or directly to the PGND pin with a very short trace. One grounding option is to define a signal ground plane that connects to ground through this point only and resides under and around the IC. An alternative is to daisy chain a ground trace around the controller to pick up all the signal ground referenced components while maintaining only a single connection to the ground plane at the SGND pin. If doing the later and not defining signal ground as a separate net, it will not be possible to use vias to connect to other layers unless your board layout package has the ability to isolate these vias from the ground plane. Keeping the signal ground separate from the system ground plane ensures that signal ground is "quiet" relative to all internal signals in the controller. The main ground plane is usually a very noisy

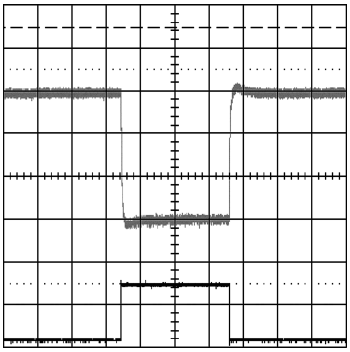
environment and not the absolute zero volt reference it tends to be thought of. Pains should be taken at every opportunity to ensure that sources of large pulse currents into the ground plane are bypassed as well as possible to minimize the disturbances to the ground plane. Under no circumstances should the controller be grounded at a point between the low-side FET source connection and the input capacitor ground connection point. This is a very noisy area.

Pin 5, SRCK, is the low-side FET source Kelvin connection and as the name implies needs to be connected directly to the low side FET source pads. This pin is used as the reference potential for the diode emulator circuit. If not connected correctly, the supply will behave erratically at light loads. The correct connection for SRCK is to tie the pin to one of the vias connecting the low-side FET source to the internal ground plane on an internal layer or the back side of the board. The trace need not be wide. A 10mil trace is adequate, as this line carries essentially no current.



27A Core Supply

The circuit above is an example of a single phase supply at much higher current. The FETs chosen lend themselves well to the use of a heatsink if desired. The transient response is quite good for a single phase below, high current design as seen from the scope photo below.



REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27213MTD/NOPB	ACTIVE	TSSOP	DGG	48	38	RoHS & Green	SN	Level-2-260C-1 YEAR	-5 to 110	27213MTD	Samples
LM27213MTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-5 to 110	27213MTD	Samples
LM27213SQ/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-5 to 110	27213SQ	Samples
LM27213SQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-5 to 110	27213SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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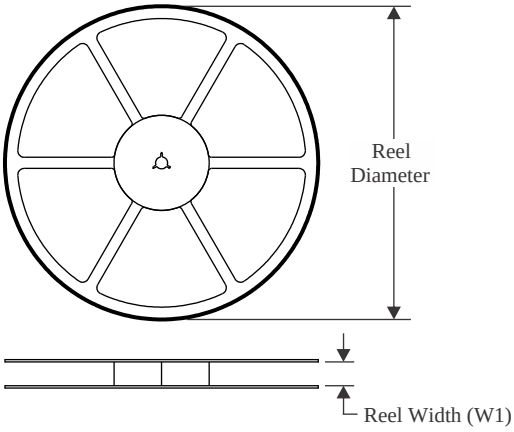
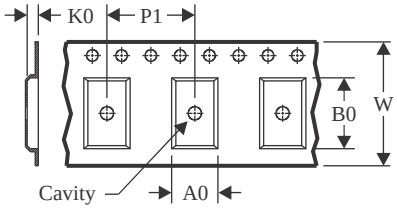
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

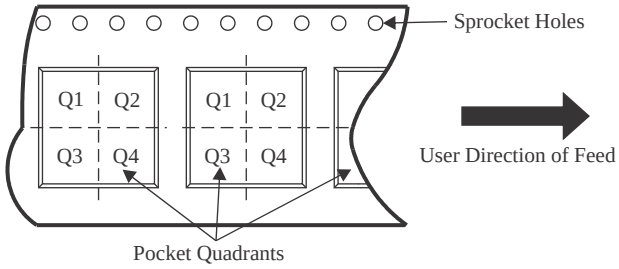


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

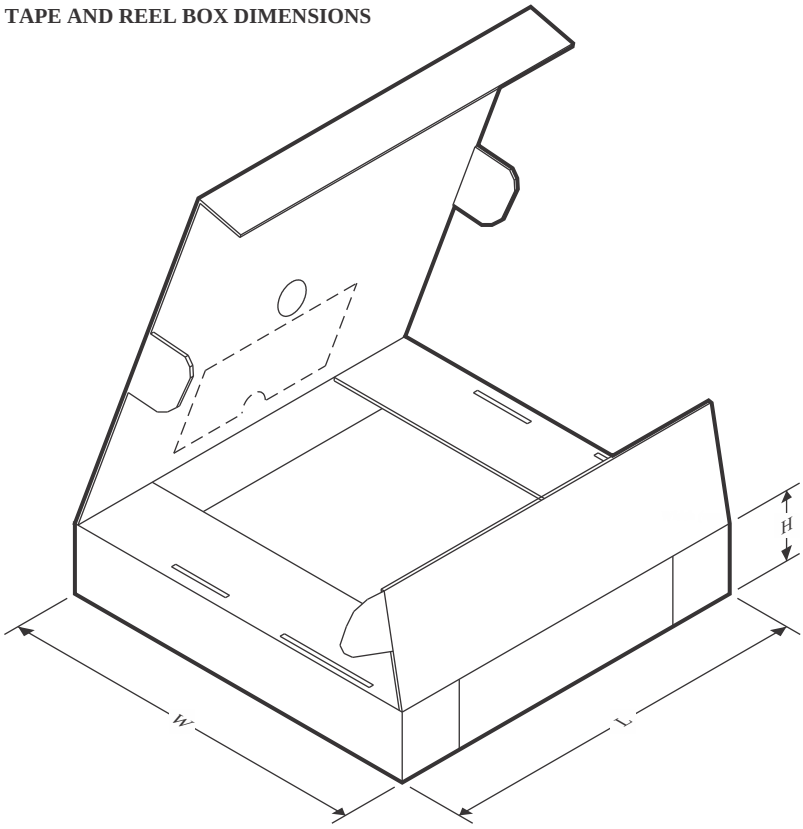
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27213MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
LM27213SQ/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LM27213SQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

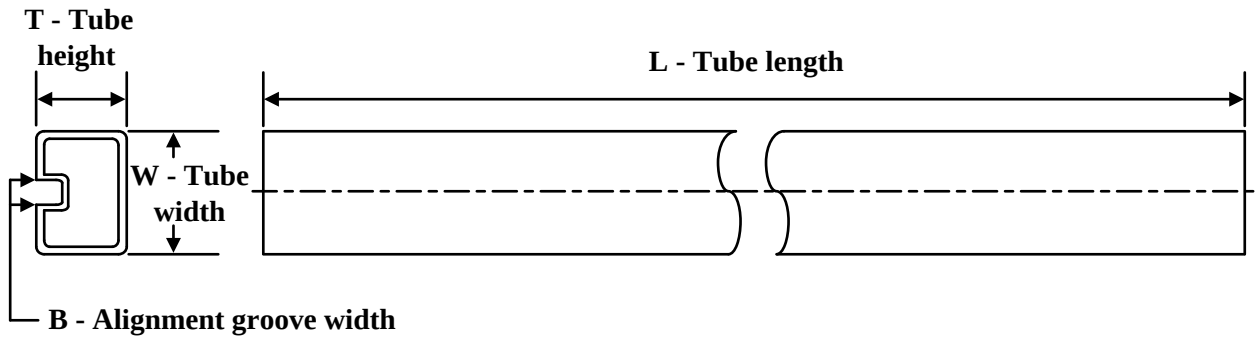
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27213MTDX/NOPB	TSSOP	DGG	48	1000	356.0	356.0	45.0
LM27213SQ/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
LM27213SQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM27213MTD/NOPB	DGG	TSSOP	48	38	495	10	2540	5.79

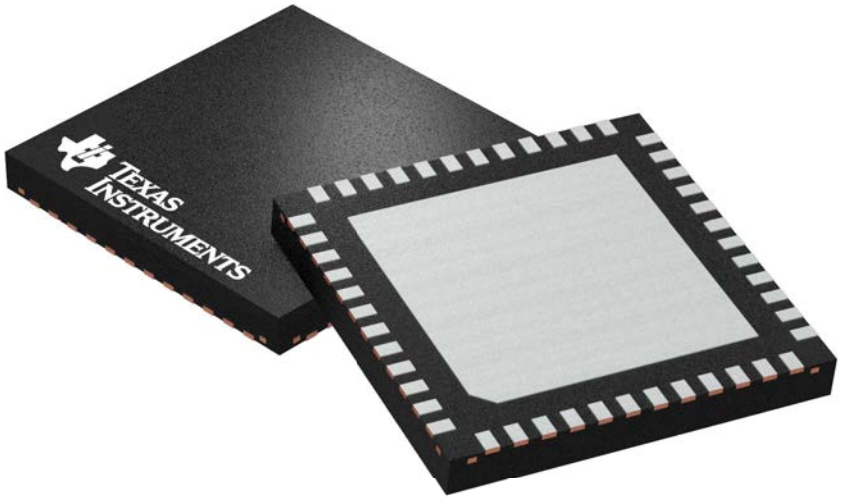
GENERIC PACKAGE VIEW

RHS 48

WQFN - 0.8 mm max height

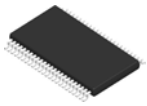
7 x 7 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205855/C

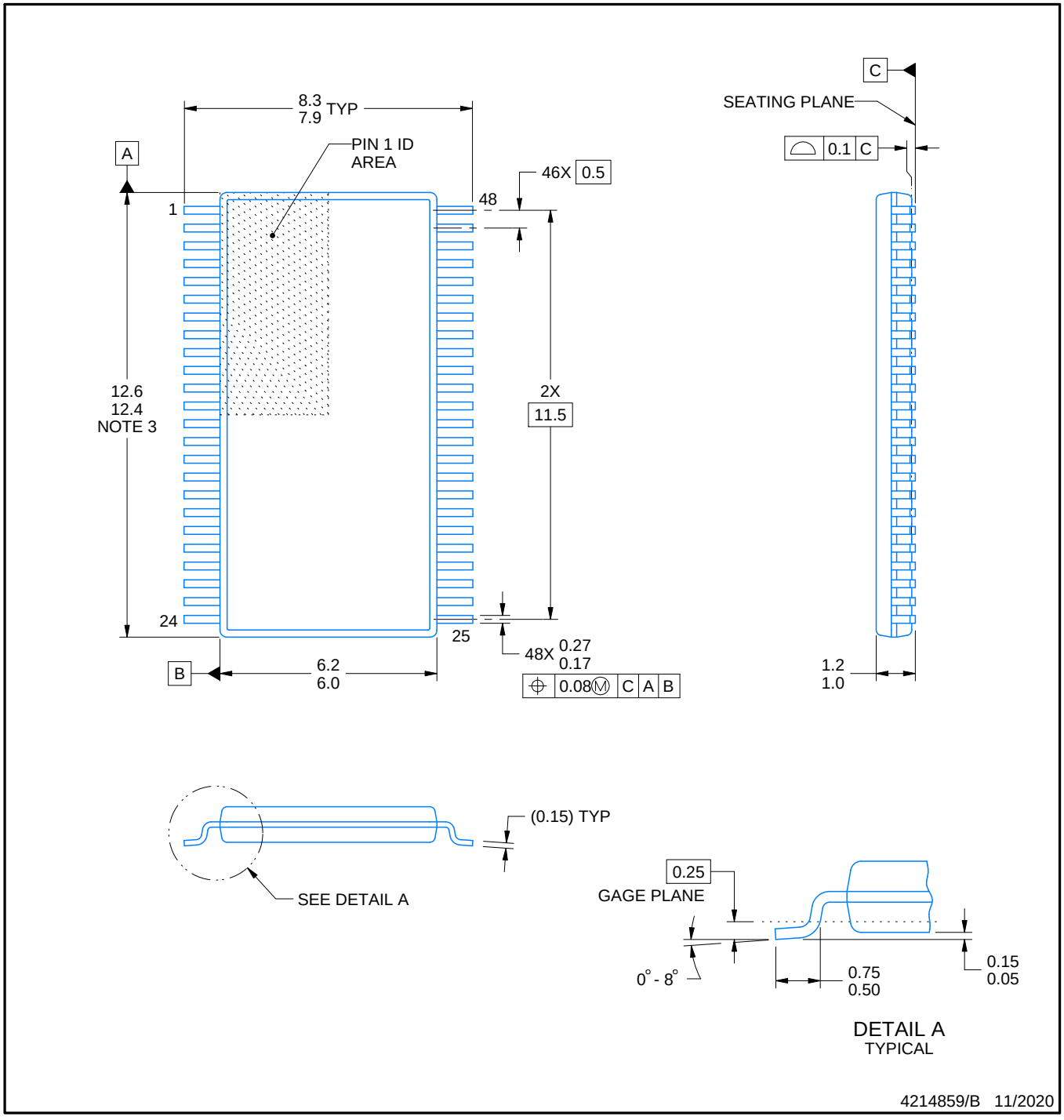


PACKAGE OUTLINE

DGG0048A

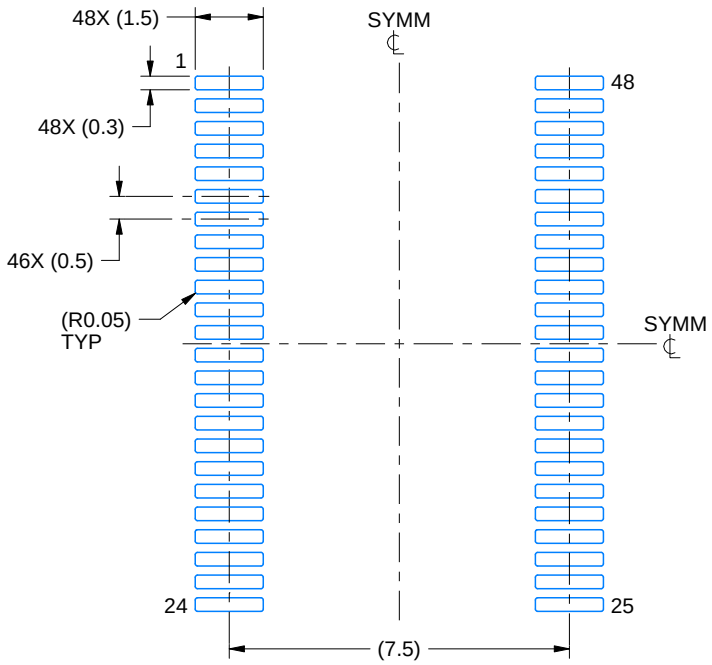
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

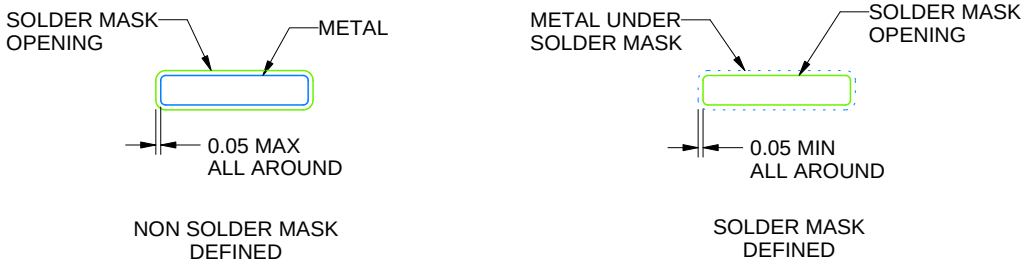


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

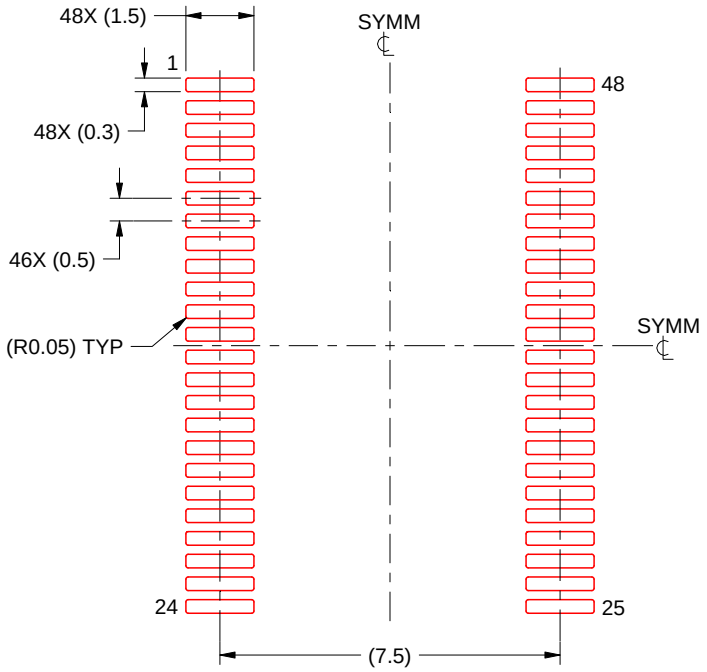


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

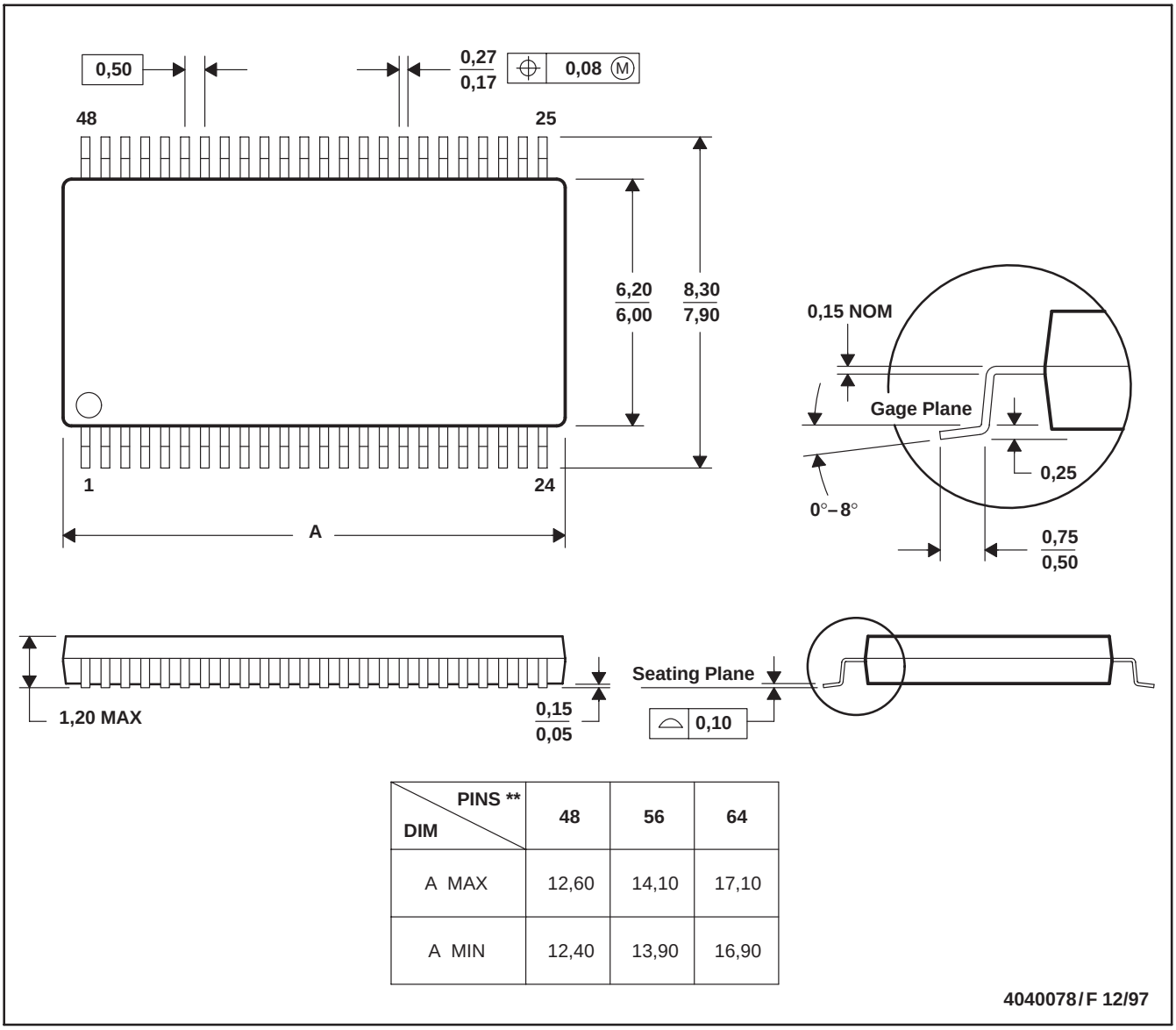
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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